TENTATIVE TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7WBL125FK

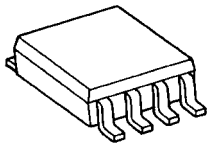
Dual Low-Voltage Bus Switch

The TC7WBL125FK is a low on-resistance, high-speed CMOS 2-bit bus switch with low voltage operation. This bus switch allows the connections or disconnections to be made with minimal propagation delay while maintaining Low power dissipation which is the feature of CMOS.

When output enable ($\overline{OE}$) is at low level, the switch is on; when at high level, the switch is off.

P-MOS and N-MOS channel block also allows that the device is suitable for analog signal transmission.

All inputs are equipped with protection circuits to protect the device from static discharge.



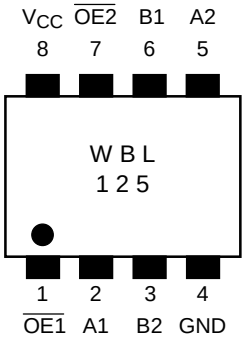
SSOP8-P-0.50A

Weight: 0.01 g (typ.)

Features

- Operating voltage: V_{CC} = 2~3.6 V
- High speed operation: t_{pd} = 0.25 ns (max) @3 V
- Ultra-low on resistance: R_{ON} = 5 Ω (typ.) @3 V
- Electro-static discharge (ESD) performance: ±200 V or more (JEITA)
  ±2000 V or more (MIL)
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power-down protection for inputs and I/O terminal.
- Package: US8

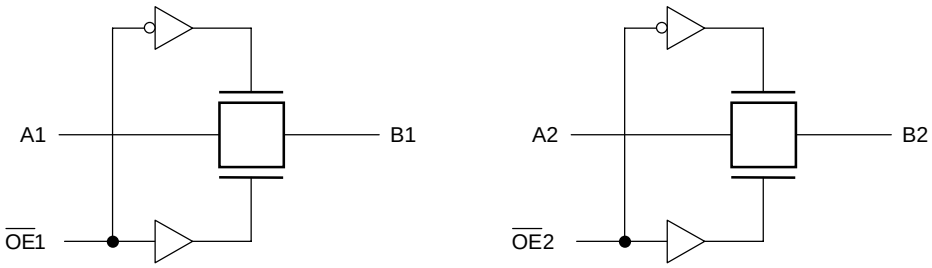
Pin Assignment (top view)



Truth Table

Inputs $\overline{OE}$	Function
L	A port = B port
H	Disconnect

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5~7.0	V
Control pin input voltage	V_{IN}	−0.5~7.0	V
Switch terminal I/O voltage	V_S	−0.5~7.0	V
Clump diode current	I_{IK}	−50	mA
Switch I/O current	I_S	128	mA
Power dissipation	P_D	200	mW
DC V_{CC}/GND current	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65~150	°C

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	2.0~3.6	V
Control pin input voltage	V_{IN}	0~5.5	V
Switch I/O voltage	V_S	0~5.5	V
Operating temperature	T_{opr}	−40~85	°C
Control pin input rise/fall time	dt/dv	0~10	ns/V

Electrical Characteristics

DC Characteristics (Ta = –40~85°C)

Characteristics		Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit
Control pin input voltage	"H" level	V_{IH}	—	2.0~3.6	0.7 × V_{CC}	—	—	V
	"L" level	V_{IL}	—	2.0~3.6	—	—	0.3 × V_{CC}	
Input leakage current		I_{IN}	V_{IN} = 0~5.5 V	2.0~3.6	—	—	±1.0	μA
Power off leakage current		I_{OFF}	A, B, $\overline{OE}$ = 0~5.5 V	0	—	—	±1.0	μA
Off-state leakage current (switch off)		I_{SZ}	A, B = 0~5.5 V, $\overline{OE}$ = V_{CC}	2.0~3.6	—	—	±1.0	μA
ON resistance (Note 3)		R_{ON}	V_{IS} = 0 V, I_{IS} = 30 mA (Note 1)	3.0	—	2	7	Ω
			V_{IS} = 3.0 V, I_{IS} = 30 mA (Note 1)	3.0	—	3	7	
			V_{IS} = 2.4 V, I_{IS} = 15 mA (Note 1)	3.0	—	5	15	
			V_{IS} = 0 V, I_{IS} = 24 mA (Note 2)	2.3	—	3	10	
			V_{IS} = 2.3 V, I_{IS} = 24 mA (Note 2)	2.3	—	4	15	
			V_{IS} = 1.7 V, I_{IS} = 15 mA (Note 2)	2.3	—	9	25	
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0	3.6	—	—	10	μA

Note 1: The typical values are at V_{CC} = 3.3 V, Ta = 25°C.

Note 2: The typical values are at V_{CC} = 2.5 V, Ta = 25°C.

Note 3: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on two (A or B) pins.

AC Characteristics (Ta = –40~85°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Propagation delay time (bus to bus)	t_{pLH} t_{pHL}	Figure 1, Figure 2 (Note 4)	3.0	—	0.25	ns
Output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 3	3.0	—	TBD	ns
			2.3	—	TBD	
Output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	3.0	—	TBD	ns
			2.3	—	TBD	

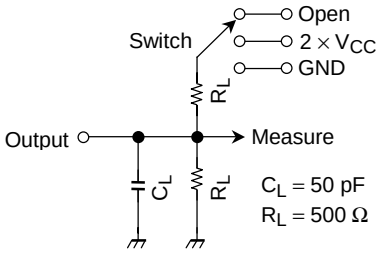
Note 4: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Control pin input capacitance	C_{IN}	(Note 5)	3.0	3	pF
Switch terminal capacitance	$C_{I/O}$	$\overline{OE}$ = V_{CC} (Note 5)	3.0	10	pF

Note 5: This item is guaranteed by design.

AC Test Circuit



Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	2 × V_{CC}
t_{pHZ}, t_{pZH}	GND

Figure 1

AC Waveform

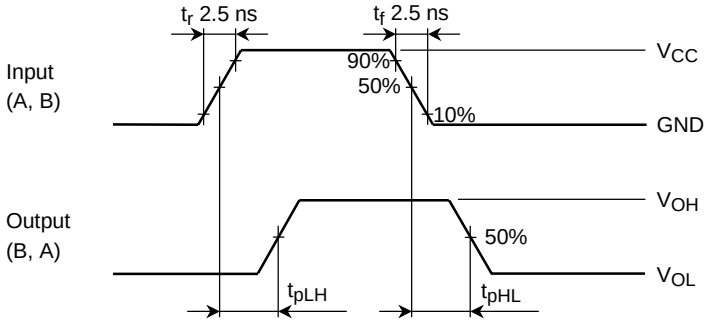


Figure 2 t_{pLH}, t_{pHL}

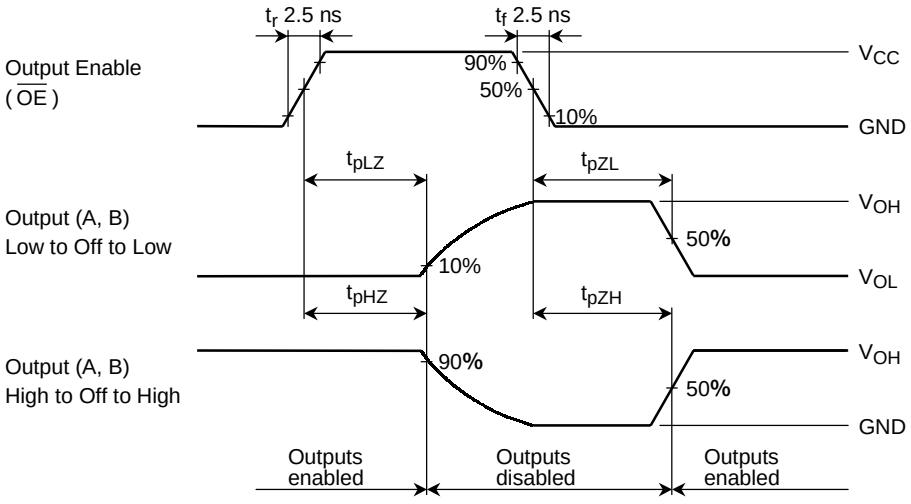
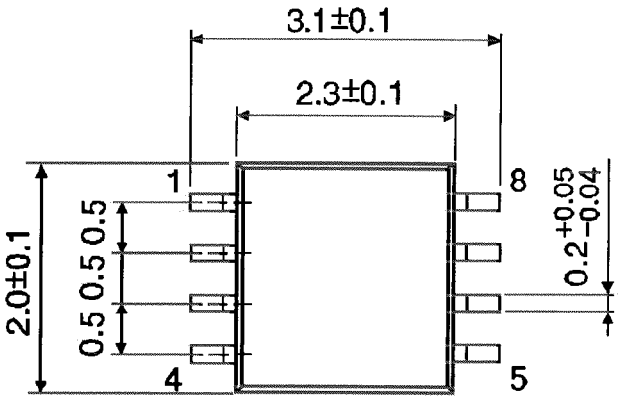
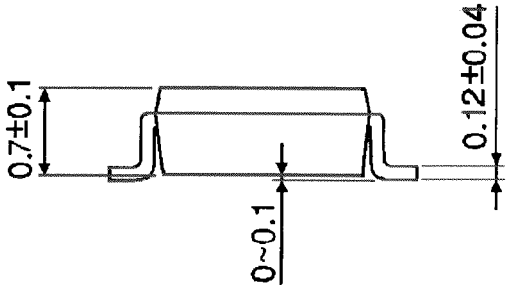


Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Package Dimensions

SSOP8-P-0.50A Unit : mm





Weight: 0.01 g (typ.)

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