

SN54LS137, SN74LS137 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

SDLS132 - JUNE 1978 - REVISED MARCH 1988

- Combines Decoder and 3-Bit Address Latch
- Incorporates 2 Enable Inputs to Simplify Cascading
- Low Power Dissipation . . . 65 mW Typ

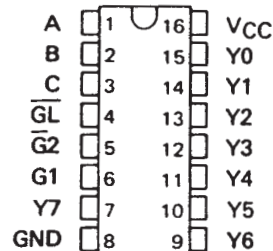
description

The 'LS137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'LS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The 'LS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

SN54LS137 . . . J OR W PACKAGE

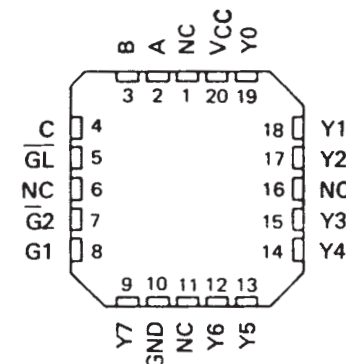
SN74LS137 . . . D OR N PACKAGE

(TOP VIEW)



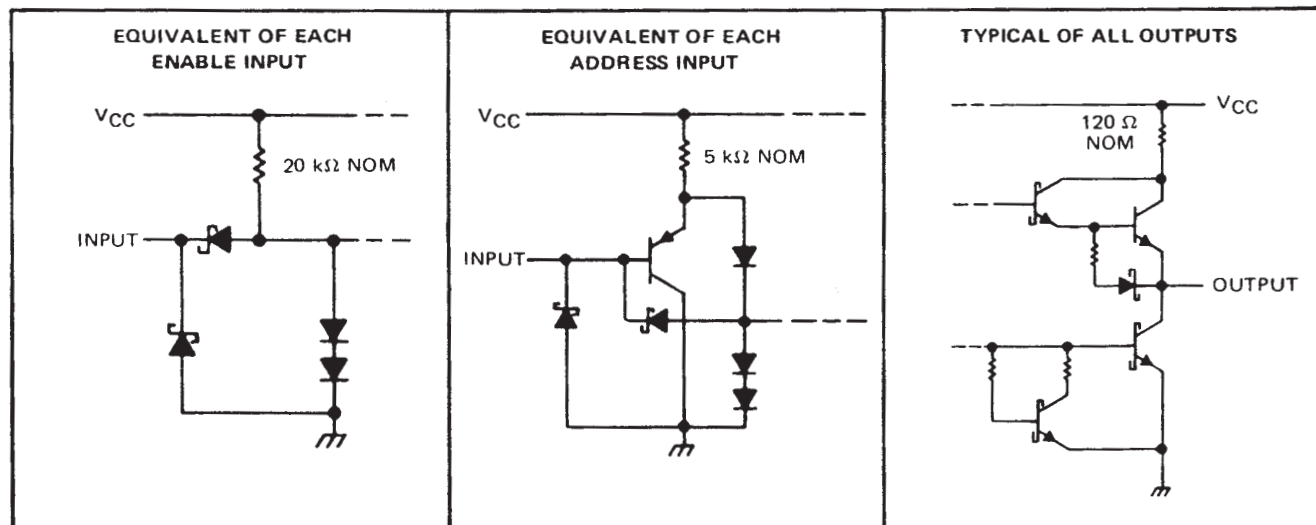
SN54LS137 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

schematics of inputs and outputs



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

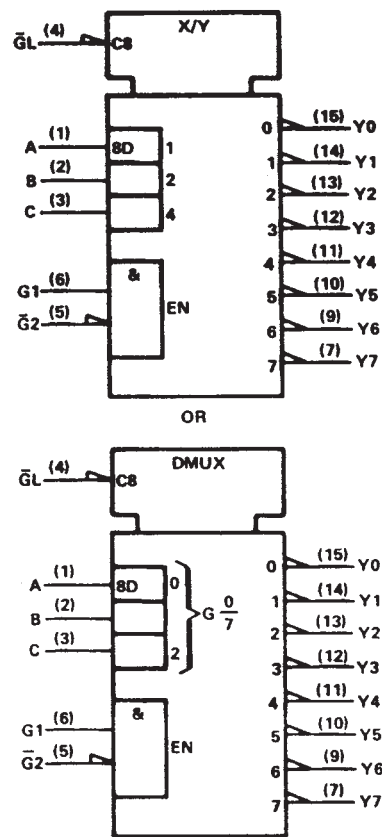
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logic symbols†



FUNCTION TABLE

INPUTS					OUTPUTS								
ENABLE			SELECT										
GL	G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

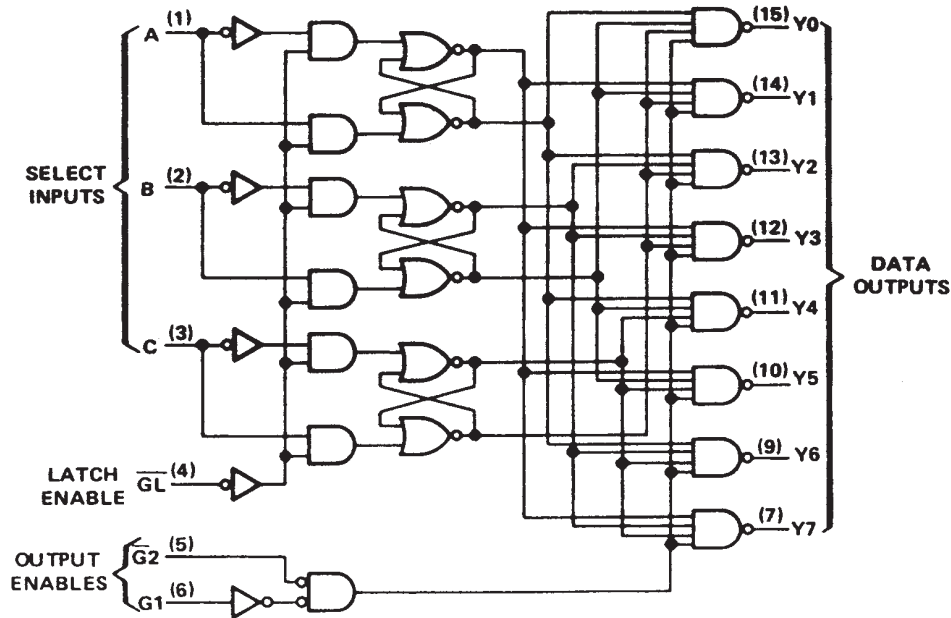
H = high level, L = low level, X = irrelevant

†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

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logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS137	-55°C to 125°C
SN74LS137	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN54LS137, SN74LS137

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

WITH ADDRESS LATCHES

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recommended operating conditions

	SN54LS137			SN74LS137			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse at $\overline{G_L}$, t_W	15			15			ns
Setup time at A, B, and C inputs, t_{su}	10			10			ns
Hold time at A, B, and C inputs, t_h	10			10			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS137		SN74LS137		UNIT
			MIN	TYP‡ MAX	MIN	TYP‡ MAX	
V _{IH} High-level input voltage			2		2		V
V _{IL} Low-level input voltage			0.7		0.8		V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = −18 mA		−1.5		−1.5		V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = −400 μA		2.5	3.5	2.7	3.5	V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 4 mA	0.25	0.4	0.25	0.4	V
		I _{OL} = 8 mA			0.35	0.5	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V		0.1		0.1		mA
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.7 V		20		20		μA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V	Enable	−0.4		−0.4		mA
		A, B, C	−0.2		−0.2		
I _{OS} Short-circuit output current §	V _{CC} = MAX		−20	−100	−20	−100	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 2		11 18		11 18		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, see note 3

PARAMETER¹	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, C	Y	2	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Note 3	11	17		ns
t_{PHL}			4		25	38		
t_{PLH}	A, B, C	Y	3		16	24		ns
t_{PHL}			3		19	29		
t_{PLH}	Enable $\overline{G_2}$	Y	2		13	21		ns
t_{PHL}			2		16	27		
t_{PLH}	Enable G1	Y	3		14	21		ns
t_{PHL}			3		18	27		
t_{PLH}	Enable $\overline{G_L}$	Y	3		18	27		ns
t_{PHL}			4		25	38		

¹ t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN54LS137J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN74LS137D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS137D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS137DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS137DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS137J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS137J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS137N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS137N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS137N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS137N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SNJ54LS137FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS137FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS137J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS137J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS137W	OBSOLETE			16		TBD	Call TI	Call TI
SNJ54LS137W	OBSOLETE			16		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



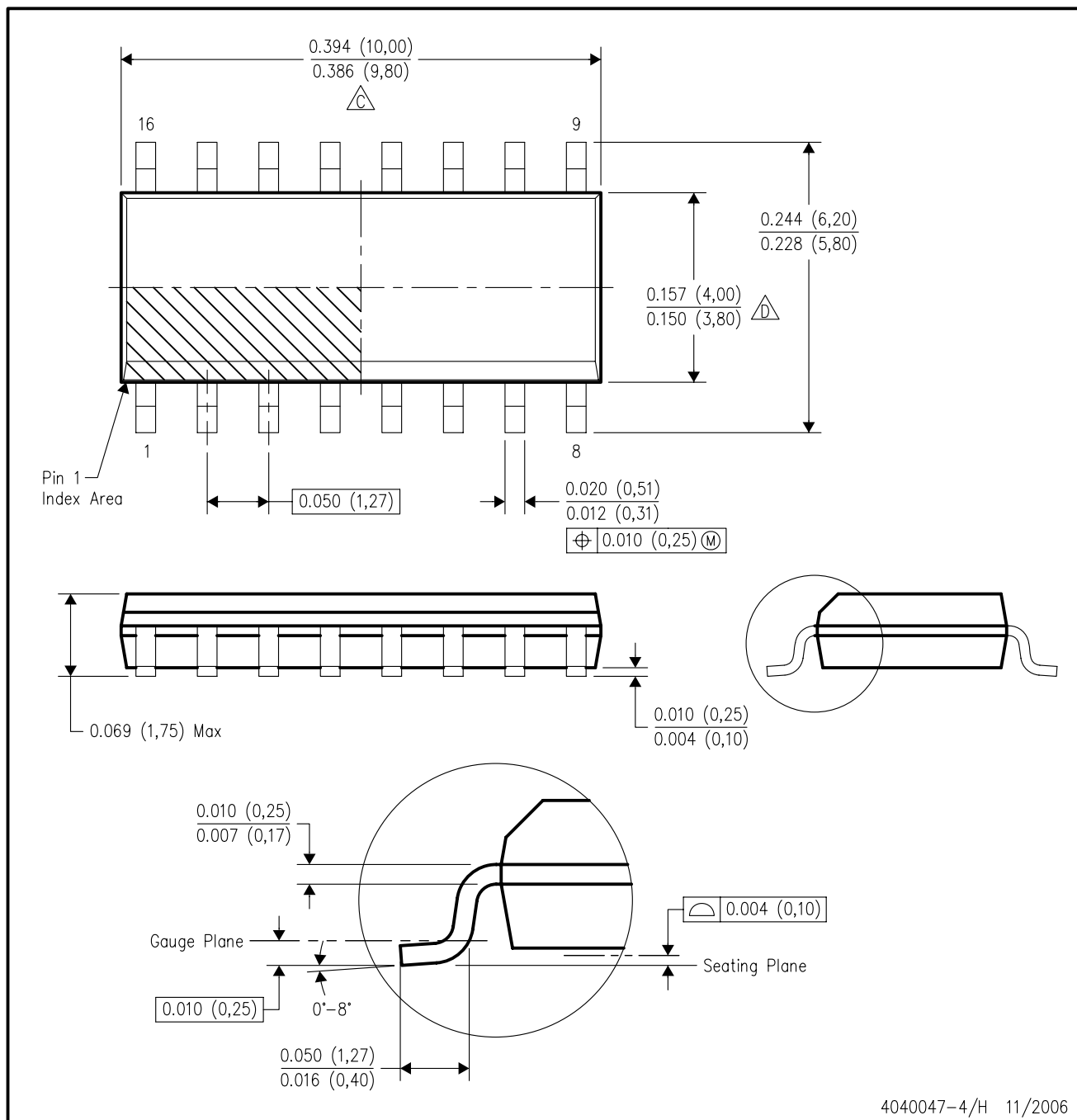
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.