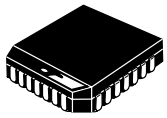
High Frequency Clock Generator

MC12439

HIGH FREQUENCY PLL CLOCK GENERATOR

The MC12439 is a general purpose synthesized clock source targeting applications that require both serial and parallel interfaces. Its internal VCO will operate over a range of frequencies from 400 to 800MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4, or 8. With the output configured to divide the VCO frequency by 1, and with a 16.66MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 16.66MHz steps.

- 50 to 800MHz Differential PECL Outputs
- ±25ps Typical Peak–to–Peak Output Jitter
- Minimal Frequency Over–Shoot
- Synthesized Architecture
- Serial 3–Wire Interface
- Parallel Interface for Power–Up
- Quartz Crystal Interface
- 28–Lead PLCC Package
- Operates from 3.3V or 5.0V Power Supply



FN SUFFIX
28–LEAD PLCC PACKAGE
CASE 776–02

Functional Description

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is sent directly to the phase detector. With a 16.66MHz crystal, this provides a reference frequency of 16.66MHz. Although this data sheet illustrates functionality only for a 16MHz and 16.66MHz crystal, any crystal in the 10–20MHz range can be used. In addition to the crystal, an LVCMOS input can also be used as the PLL reference. The reference is selected via the XTAL_SEL input pin.

The VCO within the PLL operates over a range of 400 to 800MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle.

The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated in 50Ω to V_{CC} – 2.0.

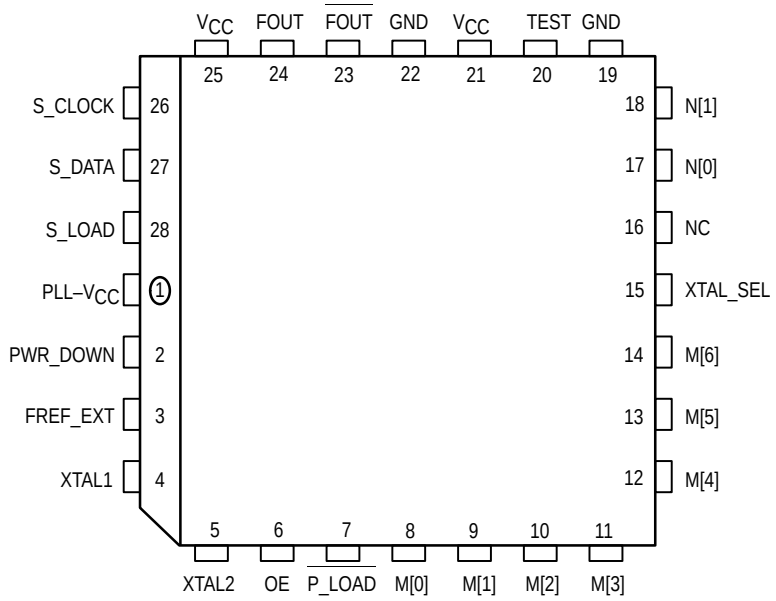
The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the P_LOAD input is held LOW until sometime after power becomes valid. On the LOW–to–HIGH transition of P_LOAD, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface centers on a twelve bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH–to–LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.

The PWR_DOWN pin, when asserted, will synchronously divide the FOUT by 16. The power down sequence is clocked by the PLL reference clock, thereby causing the frequency reduction to happen relatively slowly. Upon de–assertion of the PWR_DOWN pin, the FOUT input will step back up to its programmed frequency in four discrete increments.

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N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	1

Input	0	1
PWR_DOWN	FOUT	FOUT/16
XTAL_SEL	FREF_EXT	XTAL
OE	Disabled	Enabled

Figure 1. 28–Lead Pinout (Top View)

PIN DESCRIPTIONS

Pin Name	Type	Function
Inputs		
XTAL1, XTAL2	—	These pins form an oscillator when connected to an external series–resonant crystal.
S_LOAD	Int. Pulldown	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH–to–LOW transition of S_LOAD for proper operation.
S_DATA	Int. Pulldown	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK	Int. Pulldown	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
$\overline{\text{P_LOAD}}$	Int. Pullup	This pin loads the configuration latches with the contents of the parallel inputs .The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW–to–HIGH transition of P_LOAD for proper operation.
M[6:0]	Int. Pullup	These pins are used to configure the PLL loop divider. They are sampled on the LOW–to–HIGH transition of P_LOAD. M[6] is the MSB, M[0] is the LSB.
N[1:0]	Int. Pullup	These pins are used to configure the output divider modulus. They are sampled on the LOW–to–HIGH transition of P_LOAD.
OE	Int. Pullup	Active HIGH Output Enable.
Outputs		
F_{OUT}, $\overline{F_{OUT}}$	—	These differential positive–referenced ECL signals (PECL) are the output of the synthesizer.
TEST	—	The function of this output is determined by the serial configuration bits T[2:0].
Power		
V_{CC}	—	This is the positive supply for the chip, and is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}).
PLL_V_{CC}	—	This is the positive supply for the PLL, and should be as noise–free as possible for low–jitter operation. This supply is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}).
GND	—	These pins are the negative supply for the chip and are normally all connected to ground.
Other		
PWR_DOWN	Int. Pulldown	LVCMOS input that forces the FOUT output to synchronously reduce its frequency by a factor of 16.
FREF_EXT	Int. Pulldown	LVCMOS input which can be used as the PLL reference frequency.
XTAL_SEL	Int. Pullup	LVCMOS input that selects between the XTAL and FREF_EXT PLL reference inputs. A HIGH selects the XTAL input.

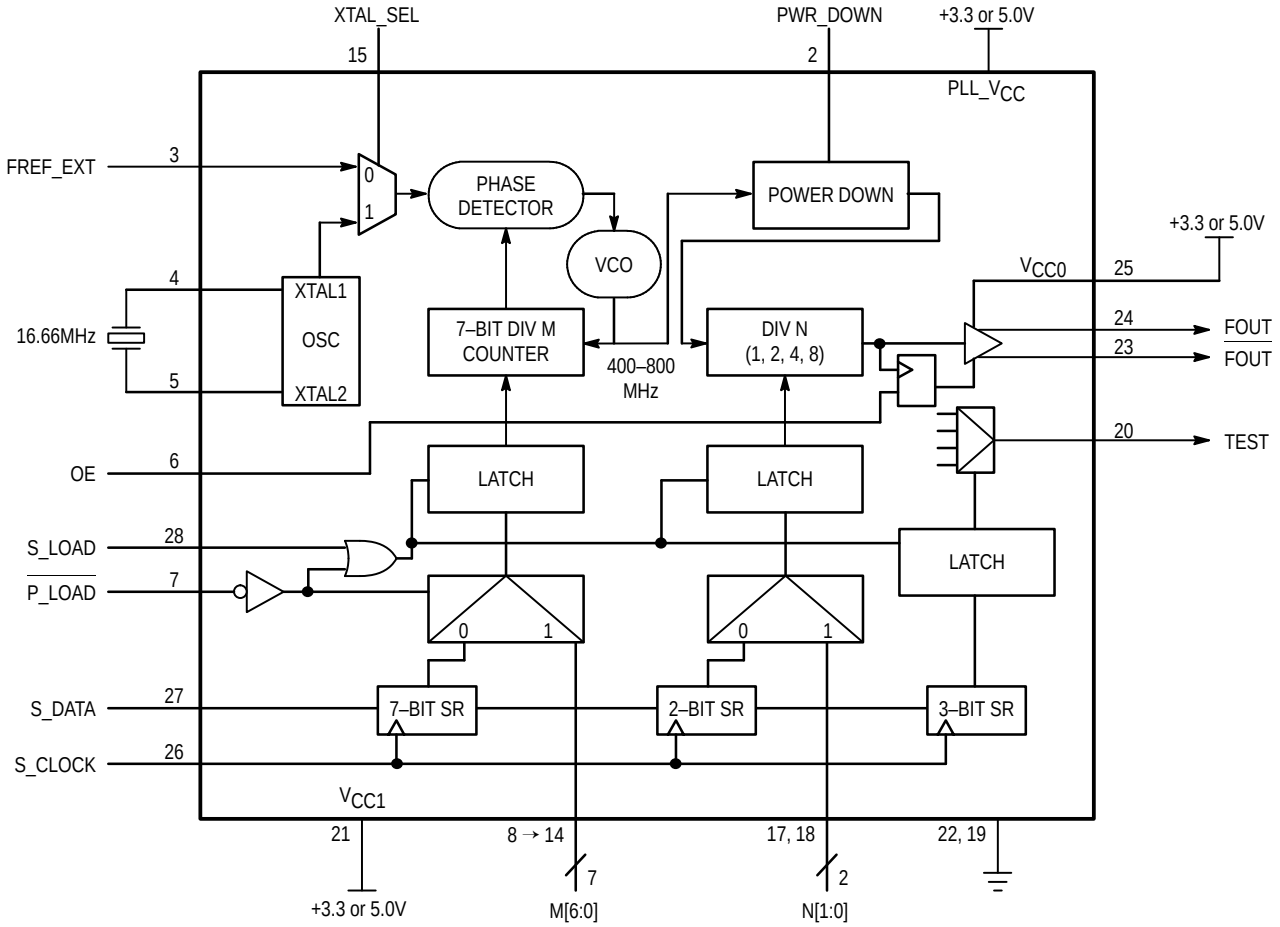


Figure 2. MC12439 Block Diagram

PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$FOUT = F_{XTAL} \times M \div N \quad (1)$$

Where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $25 \leq M \leq 50$ for a 16MHz input reference.

For input references other than 16MHz, the valid M values can be calculated from the valid VCO range of 400–800MHz.

Assuming that a 16MHz reference frequency is used the above equation reduces to:

$$FOUT = 16 \times M \div N$$

Substituting the four values for N (1, 2, 4, 8) yields:

FOUT = 16M, FOUT = 8M,
FOUT = 4M and FOUT = 2M
for 25 < M < 50

The user can identify the proper M and N values for the desired frequency from the above equations. The four output frequency ranges established by N are 400–800MHz, 200–400MHz, 100–200MHz and 50–100MHz respectively. From these ranges the user will establish the value of N required, then the value of M can be calculated based on the appropriate equation above. For example if an output frequency of 384MHz was desired the following steps would be taken to identify the appropriate M and N values. 384MHz falls within the frequency range set by an N value of 2 so N [1:0] = 00. For N = 2 FOUT = 8M and M = FOUT ÷ 8. Therefore M = 384 ÷ 8 = 48, so M[8:0] = 0110000.

For input reference frequencies other than 16MHz the set of appropriate equations can be deduced from equation 1. For computer applications another useful frequency base would be 16.666MHz. From this reference one can generate a family of output frequencies at multiples of the 33.333MHz PCI clock. As an example to generate a 533.333MHz clock

from a 16.666MHz reference the following M and N values would be used:

FOUT = 16.666 x M ÷ N

Let N = 1, M = 533.333 ÷ 16.666 = 32

The value for M falls within the constraints set for PLL stability (400÷16.666 ≤ M ≤ 800÷16.666; 24 ≤ M ≤ 48), therefore N[1:0] = 11 and M[6:0} = 0100000. If the value for M fell outside of the valid range a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW to HIGH transition will latch the information present on the M[6:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW the input latches will be transparent and any changes on the M[6:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 12 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data streeam on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M6). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. NO TAG illustrates the timing diagram for both a parallel and a serial load of the MC12439 synthesizer.

M[6:0] and N[1:0] are normally specified once at power–up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine–tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the CMOS output may not be able to toggle fast enough for some of the higher output frequencies. The T2, T1 and T0 control bits are preset to ‘000’ when P_LOAD is LOW so that the PECL FOUT outputs are as jitter–free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MC12439 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MC12439 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. NO TAG shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 250MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 250MHz as the minimum divide ratio of the N counter is 1. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

T2	T1	T0	**TEST** (Pin 20)
0	0	0	SHIFT REGISTER OUT
0	0	1	HIGH
0	1	0	FREF
0	1	1	M COUNTER OUT
1	0	0	FOUT
1	0	1	LOW
1	1	0	PLL BYPASS
1	1	1	FOUT/4

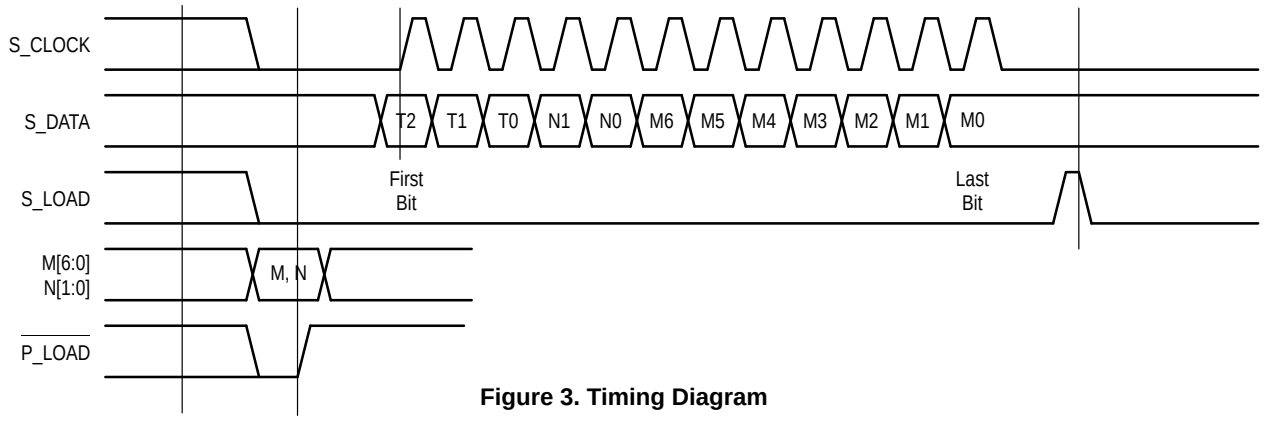
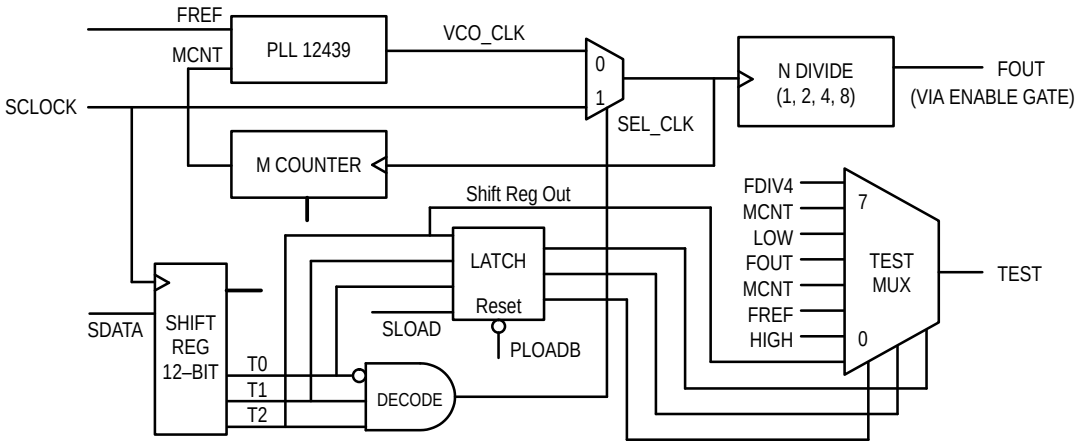


Figure 3. Timing Diagram



- T2=T1=1, T0=0: Test Mode
- SCLOCK is selected, MCNT is on TEST output, SCLOCK DIVIDE BY N is on FOUT pin

PLOADB acts as reset for test pin latch. When latch reset T2 data is shifted out TEST pin.

Figure 4. Serial Test Clock Block Diagram

DC CHARACTERISTICS (T_A = 0 to 70°C; V_{CC} = 3.3 to 5.0V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0			V	V_{CC} = 3.3 to 5.0V
V_{IL}	Input LOW Voltage			0.8	V	V_{CC} = 3.3 to 5.0V
I_{IN}	Input Current			1.0	mA	
I_{OH}	Output HIGH Current (Note 1.) (FOUT/FOUT Only)			50	mA	Continuous Current
V_{OH}	Output HIGH Voltage TEST	2.5			V	I_{OH} = –0.8mA, (Note 2.)
V_{OL}	Output LOW Voltage TEST			0.4	V	I_{OL} = 0.8mA, (Note 2.)
V_{OH}	Output HIGH Voltage FOUT / FOUT	2.27		2.47	V	V_{CC} = 3.3V (Notes 3., 4.)
V_{OL}	Output LOW Voltage FOUT / FOUT	1.49		1.68	V	V_{CC} = 3.3V (Notes 3., 4.)
I_{CC}	Power Supply Current V_{CC} / PLL_V_{CC}		90 15	110 20	mA	

1. Maximum I_{OH} spec implies the device can drive 25Ω impedance with the PECL outputs.
2. See Applications Information section for output level versus frequency information.
3. Output levels will vary 1:1 with V_{CC} variation.
4. 50Ω to V_{CC} – 2.0V pulldown.

AC CHARACTERISTICS (T_A = 0 to 70°C; V_{CC} = 3.3 to 5.0V ±5%)

Symbol	Characteristic		Min	Max	Unit	Condition
F_{MAXI}	Maximum Input Frequency	S_CLOCK Xtal Oscillator FREF_EXT	 10 10	10 20 Note 5.	MHz	
F_{MAXO}	Maximum Output Frequency	VCO (Internal) FOUT	400 50	900 800	MHz	
t_{LOCK}	Maximum PLL Lock Time		1	10	ms	
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak) (Note 6.)			±25 ±65	ps	N = 2,4,8; Note 7. N = 1; Note 7.
t_S	Setup Time	S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20 20 20		ns	
t_h	Hold Time	S_DATA to S_CLOCK M, N to P_LOAD	20 20		ns	
tpw_{MIN}	Minimum Pulse Width	S_LOAD P_LOAD	50 50		ns	Note 7.
t_r, t_f	Output Rise/Fall Time		300	800	ps	Note 7.

5. Maximum frequency on FREF_EXT is a function of the internal M counter limitations. The phase detector can handle up to 100MHz on the input, but the M counter must remain in the valid range of 25 ≤ M ≤ 50. See the programming section in this data sheet for more details.
6. See Applications Information section for additional information.
7. 50Ω to V_{CC} – 2.0V pulldown.

APPLICATIONS INFORMATION

Using the On–Board Crystal Oscillator

The MC12439 features a fully integrated on–board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MC12439 as possible to avoid any board level parasitics. To facilitate co–location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MC12439 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 1 below specifies the performance requirements of the crystals to be used with the MC12439.

Table 1. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

* See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MC12439 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MC12439 provides separate power supplies for the digital ciruitry (V_{CC}) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MC12439.

Figure 5 illustrates a typical power supply filter scheme. The MC12439 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_VCC pin of the MC12439. From the data sheet the I_{PLL_VCC} current (the current sourced through the PLL_VCC pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 5 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

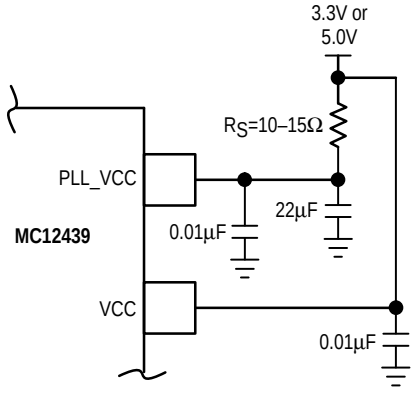


Figure 5. Power Supply Filter

A higher level of attenuation can be acheived by replacing the resistor with an appropriate valued inductor. A 1000µH choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin a low DC resistance inductor is required (less than 15Ω). Generally the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MC12439 provides sub–nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representaive board layout for the MC12439. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the 12439 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

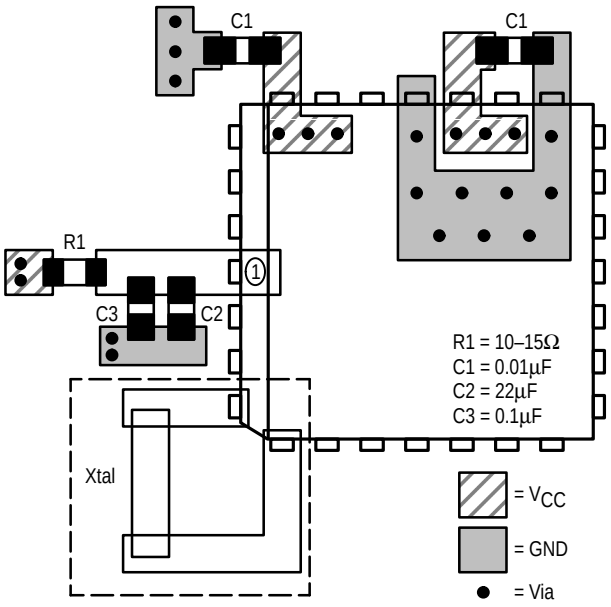


Figure 6. PCB Board Layout for MC12439

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on–board oscillator.

Although the MC12439 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Jitter Performance of the MC12439

The MC12439 exhibits long term and cycle–to–cycle jitter which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

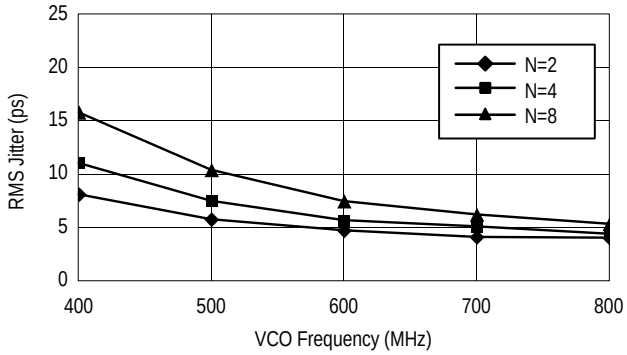


Figure 7. RMS PLL Jitter versus VCO Frequency

NO TAG illustrates the RMS jitter performance of the MC12439 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data. In addition the data represents long term period jitter, the cycle–to–cycle jitter could not be measured to the level of accuracy required with available test equipment but certainly will be smaller than the long term period jitter.

The most commonly specified jitter parameter is cycle–to–cycle jitter. Unfortunately with today's high performance measurement equipment there is no way to measure this parameter for jitter performance in the class demonstrated by the MC12439. As a result different methods are used which approximate cycle–to–cycle jitter. The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak–to–peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. The oscilloscope cannot collect adjacent pulses, rather it collects pulses from a very large sample of pulses. It is safe to assume that collecting pulse information in this mode will produce period jitter values somewhat larger than if consecutive cycles (cycle–to–cycle jitter) were measured. All of the jitter data reported on the MC12439 was collected in this manner.

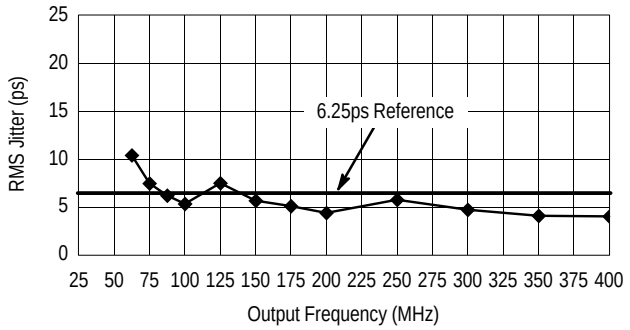


Figure 8. RMS Jitter versus Output Frequency

NO TAG shows the jitter as a function of the output frequency. For the 12439 this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ±25ps peak–to–peak long term period jitter. The graph shows that for output frequencies from 87.5 to 400MHz the jitter falls within the ±25ps peak–to–peak specification. The general trend is that as the output frequency is decreased the output edge jitter will increase.

The jitter data from NO TAG and NO TAG do not include the performance of the 12439 when the output is in the divide by 1 mode. In divide by one mode the output signal is a digitally doubled version of the VCO output. The period of the outputs of the digital doubler is dependent on the duty cycle of the VCO output. Since the VCO output duty cycle cannot be guaranteed to be always 50% the resulting 12439 output in divide by one mode will be bimodal at times. Since a bimodal distribution cannot be acurately represented with an rms value, peak–to–peak values of jitter for the divide by one mode are presented.

Figure 9 shows the peak–to–peak jitter of the 12439 output in divide by one mode as a function of output frequency. Notice that as with the other modes the jitter improves with increasing frequency. The ±65ps shown in the data sheet table represents a conservative value of jitter, especially for the higher vco, and thus output frequencies.

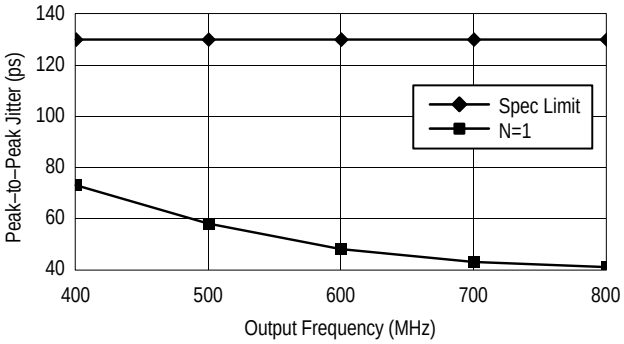


Figure 9. Peak–to–Peak Jitter versus Output Frequency

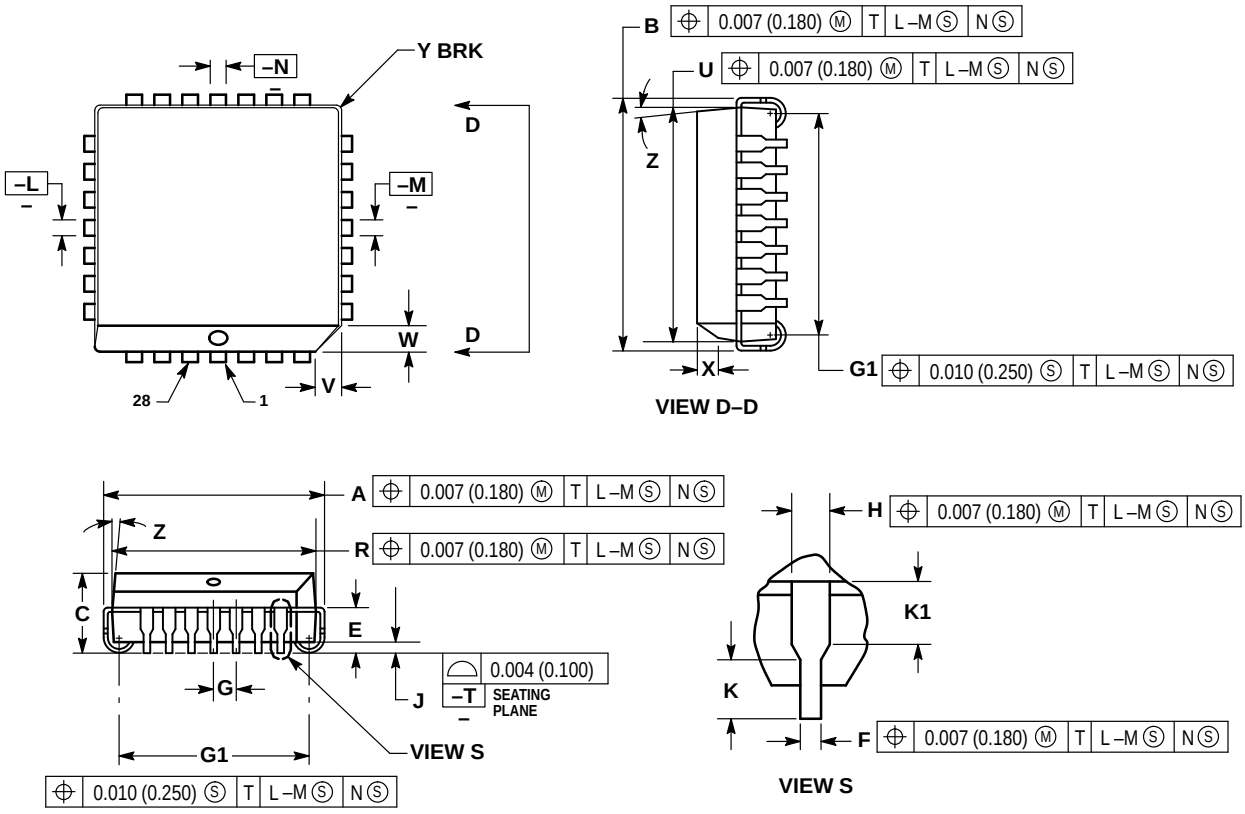
The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

Output Voltage Swing vs Frequency

In the divide by one mode the output rise and fall times will limit the peak to peak output voltage swing. For a 400MHz output the peak to peak swing of the 12439 output will be approximately 700mV. This swing will gradually degrade as the output frequency increases, at 800MHz the output swing will be reduced to approximately 500mV. For a worst case analysis it would be safe to assume that the 12439 output will always generate at least a 400mV output swing. Note that most high speed ECL receivers require only a few hundred millivolt input swings for reliable operation. As a result the output generated by the 12439 will, under all conditions, be sufficient for clocking standard ECL devices. Note that if a larger swing is desired the 12439 could drive a single gate ECLinPS Lite amplifier like the MC100LVEL16. The LVEL16 will speed up the output edge rates and produce a full swing ECL output at 800MHz.

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE D



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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