

## Description

The S494 is a monolithic integrated circuit which includes all the necessary building blocks for the design of pulse width modulate(PWM) switching power supplies, including push-pull, bridge and series configuration. The device can operate at switching frequencies between 1KHz and 300KHz and output voltage up to 40V. The S494 is specified over an operating temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

## Features

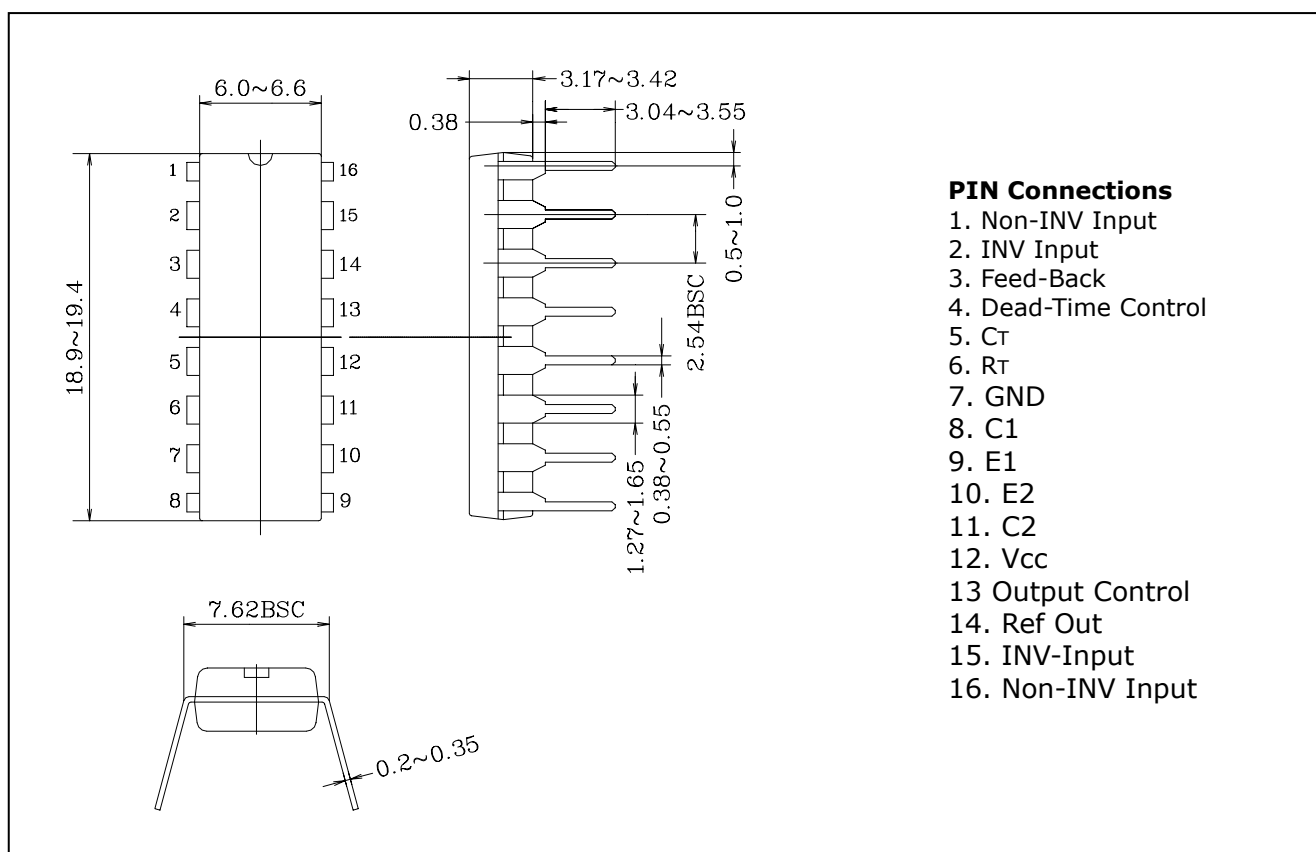
- Uncommitted output transistors capable of 200mA source or sink
- Internal protection from double pulsing of out-puts with narrow pulse widths or with supply voltages bellows specified limits
- Easily synchronized to other circuits
- Dead time control comparator
- Output control selects single-ended or push-pull operation

## Ordering Information

Type NO.	Marking	Package Code
S494P	S494P	DIP-16

## Outline Dimensions

unit : mm



**Absolute Maximum Ratings**

Ta=25°C

Characteristic	Symbol	Ratings	Unit
supply voltage	V <sub>CC</sub>	42	V
Voltage From Any Pin to Ground (except pin 8 and pin 11)	V <sub>IN</sub>	V <sub>CC</sub> +0.3	V
Output Collector Voltage	V <sub>C1</sub> , V <sub>C2</sub>	42	V
Peak Collector Current	I <sub>C1</sub> , I <sub>C2</sub>	250	mA
Power Dissipation	P <sub>D</sub>	1500	mW
Operating Temperature	T <sub>opr</sub>	-40 ~ 85	°C
Storage Temperature	T <sub>stg</sub>	-65 ~ 150	°C

**Recommended Operating Condition**

Characteristic	Symbol	Min.	Max.	Unit
supply voltage	V <sub>CC</sub>	7	40	V
Voltage on Any Pin Except Pin 8 and 11(Referenced to Ground)	V <sub>IN</sub>	-0.3	V <sub>CC</sub> +0.3	V
Output Voltage	V <sub>C1</sub> , V <sub>C2</sub>	-0.3	40	V
Output Collector Current	I <sub>C1</sub> , I <sub>C2</sub>	-	200	mA
Timing Capacitor	C <sub>t</sub>	470	-	PF
Timing Capacitor	C <sub>t</sub>	-	10	μF
Timing Resistor	R <sub>t</sub>	1.8	500	kΩ
Oscillator Frequency	f <sub>OSC</sub>	1	300	KHz

**Electrical Characteristics****Reference Section**

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Reference Voltage	V <sub>ref</sub>	I <sub>ref</sub> = 1.0mA	4.75	5.00	5.25	V
Line Regulation	V <sub>LINE</sub>	7V < V <sub>CC</sub> < 40V	-	2	25	mV
Load Regulation	V <sub>LOAD</sub>	1mA < I <sub>REF</sub> < 10mA	-	1	15	mV
Temperature Coefficient	-	0°C < Ta < 70°C	-	0.01	0.03	%/°C

**Oscillator Section**

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Oscillator Frequency	f <sub>OSC</sub>	C <sub>t</sub> =0.01 μF, R <sub>t</sub> =12 kΩ	-	10	-	kHz
Oscillator Frequency Change Over Operating Temperature Range	Δ f <sub>SOC</sub>	C <sub>t</sub> =0.01 μF, R <sub>t</sub> =12 kΩ	-	-	2	%

## Dead Time Control Section

Characteristic		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Bias Current (Pin4)		$I_{IB(DT)}$	$V_{CC} = 15V, 0V < V_4 < 5.25V$	-	-2	-10	$\mu A$
Max. Duty cycle, Each Output		$DC_{(Max)}$	$V_{CC} = 15V, Pin4 = 0V,$ Output Control Pin = Vref	43	-	45	%
Input Threshold Voltage	Zero Duty	$V_{TH}$	-	-	3	3.3	V
	Max Duty			0	-	-	

## Error Amplifier Section

Characteristic		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Offset Voltage		$V_{IOS}$	$V_3 = 2.5V$	-	2	10	mV
Input Offset Current		$I_{IOS}$	$V_3 = 2.5V$	-	25	250	nA
Input Bias Current		$I_{IB}$	$V_3 = 2.5V$	-	0.2	1	$\mu A$
Input Common Mode voltage Range		$V_{ICR}$	$7V \leq V_{CC} \leq 40V$	-0.3	-	$V_{CC}$	V
Large Signal Open Loop Voltage Range		$G_{VO}$	$0.5V \leq V_3 \leq 3.5V$	60	74	-	dB
Unity Gain Band width		$f_c$	-	-	650	-	kHz

## PWM Comparator Section (Pin3)

Characteristic		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Inhibit Threshold Voltage		$V_{THI}$	Zero duty cycle	-	4	4.5	V
Output Source Current		$I_{O^+}$	$0.5V < V_3 < 3.5V$	2	-	-	mA
Output Sink Current		$I_{O^-}$	$0.5V < V_3 < 3.5V$	-0.2	-0.6	-	mA

## Output Section

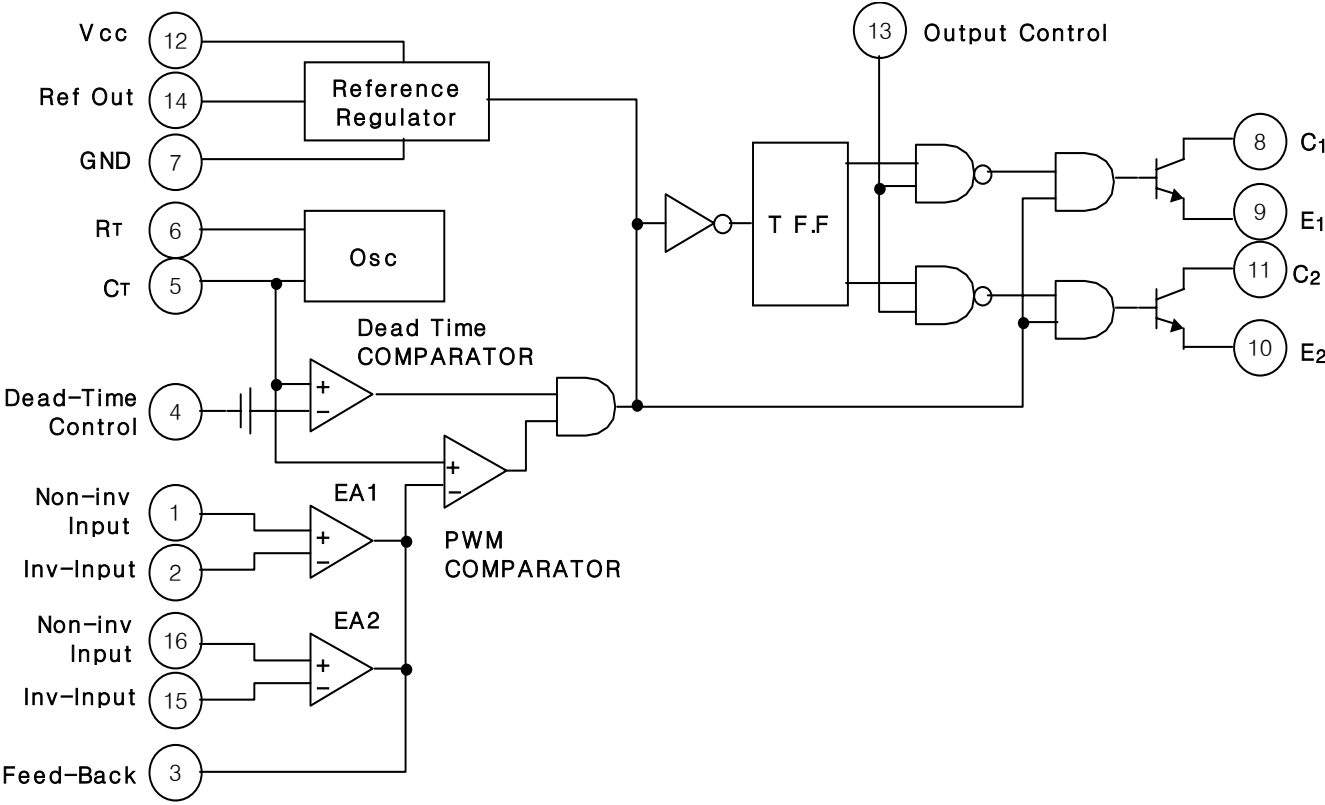
Characteristic		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Saturation Voltage	Common-Emitter	$V_{CE(SAT)}$	$V_E = 15V, I_C = 200mA$	-	1.1	1.3	V
	Emitter-Follower		$V_C = 15V, I_E = 200mA$	-	1.5	2.5	
Collector off-state Current		$I_{C(off)}$	$V_{CC} = V_C = 40V, V_E = 0$	-	2	100	$\mu A$
Emitter off-state Current		$I_{E(off)}$	$V_{CC} = V_C = 40V, V_E = 0$	-	-	-100	
Output Control(Pin 13)							
Output Control Voltage Required for single-Ended or Parallel Output Operation		$V_{OCL}$	-	-	-	0.4	V
Output Control Voltage Required for Push-pull operation		$V_{OCH}$	-	2.4	-	-	V
Total Device							
Standby power Supply Current		$I_{CC}$	-	-	6	10	mA

: These limits apply when the voltage measured at Pin 3 is with in the range specified.

**Output AC Characteristic**

Characteristic		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Rise Time	Common Emitter	$t_r$	-	-	100	200	ns
	Emitter Follower			-	100	200	
Fall Time	Common Emitter	$t_f$	-	-	25	100	
	Emitter Follower			-	40	100	

**Block Diagram**



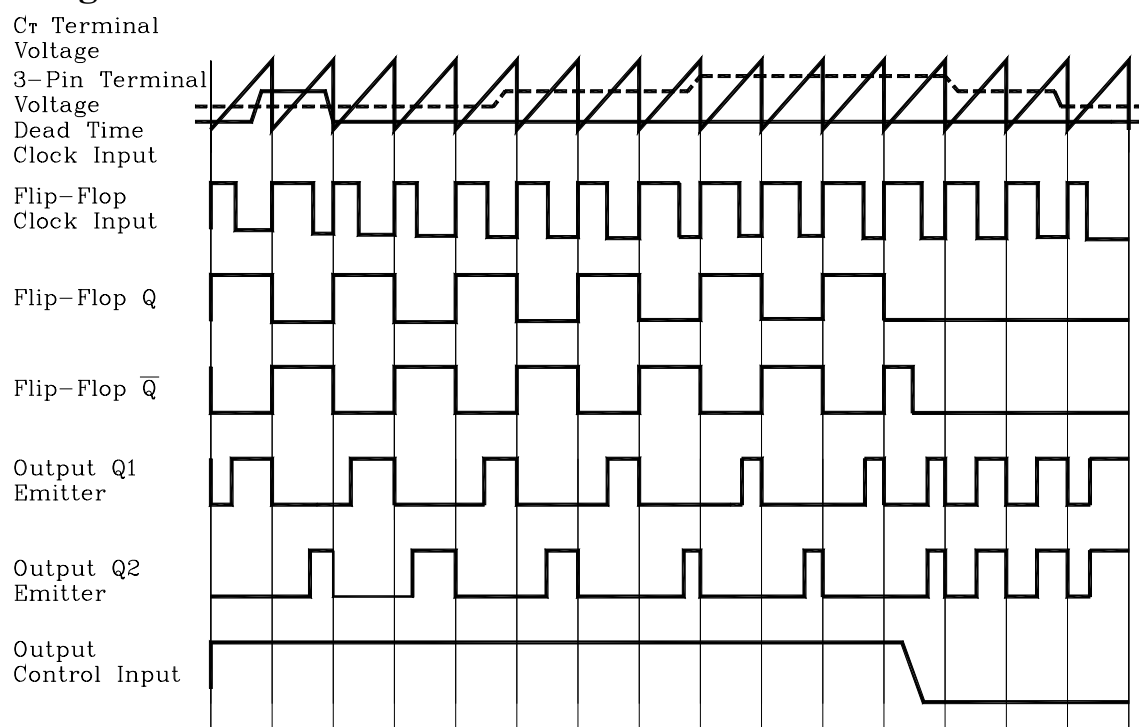
## INFORMATION

The basic oscillator (switching) frequency is controlled by an external resistor ( $R_t$ ) and capacitor ( $C_t$ ). The relationship between the values of  $R_t$ ,  $C_t$  and frequency is shown in.

The level of the sawtooth wave form is compared with an error voltage by the pulse width modulated comparator. The output of the PWM Comparator directs the pulse steering flip flop and the output control logic.

The error voltage is generated by the error amplifier. The error amplifier boosts the voltage difference between the output and the 5V internal reference. See Figure 7 for error amp sensing techniques. The second error amp is typically used to implement current limiting. The output control logic (Pin13) selects either push-pull or single-ended operation of the output transistors (see Figure 6). The dead time control prevents on-state overlap of the output transistors as can be seen in Figure 5. The dead time is approximately 3 to 5% of the total period if the dead time control (pin4) is grounded. This dead time can be increased by connecting the dead time control to a voltage up to 5 V. The frequency response of the error amps can be modified by using external resistors and capacitors. These components are typically connected between the compensation terminal (pin3) and the inverting input of the error amps (pin2 or pin15). The switching frequency of two or more S494 circuits can be synchronized. The timing capacitor,  $C_t$  is connected as shown in Figure 8. Charging current is provided by the master circuit. Discharging is through all the circuits slaved to the master.  $R_t$  is required only for the master circuit.

## Operating Waveform



Test Circuit

Fig.1 Error Amplifier Test Circuit

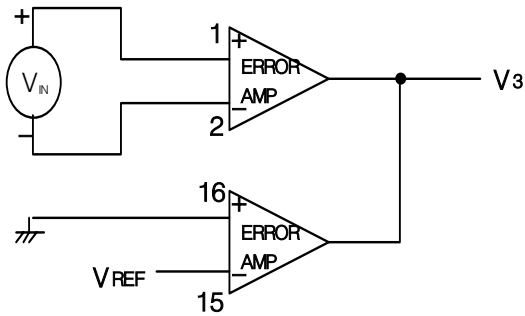


Fig.2 Current Limit sense Amplifier Test Circuit

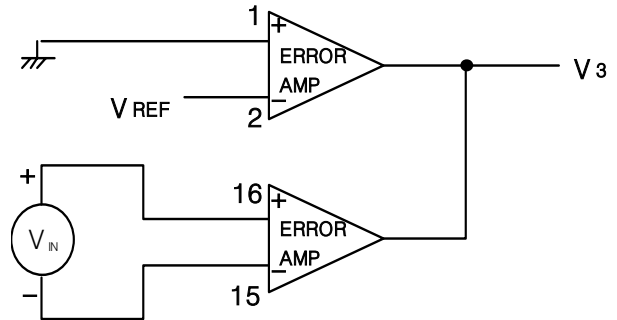


Fig. 3 Common-Emitter Configuration Test circuit and Waveform

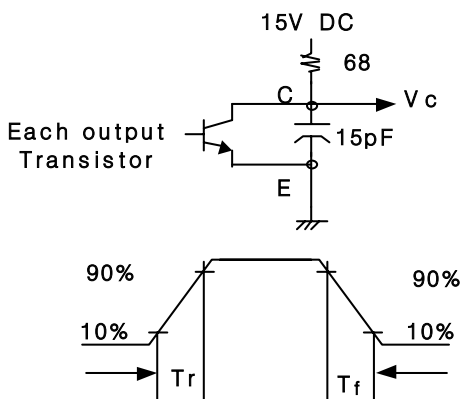


Fig. 5 Dead-Time and Feedback Control Test Circuit

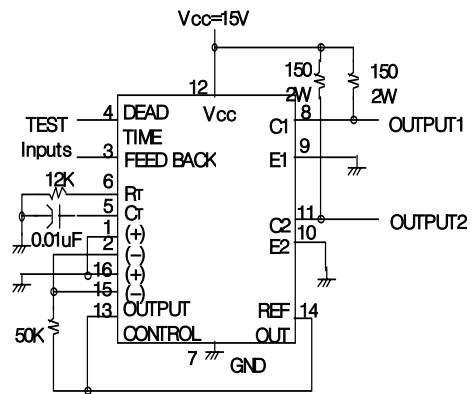


Fig. 4 Emitter-Follower Configuration Test circuit and waveform Voltage waveform



APPLICATION CIRCUIT

Fig. 6 Output Connections for Single-Ended and Push-Pull Configurations

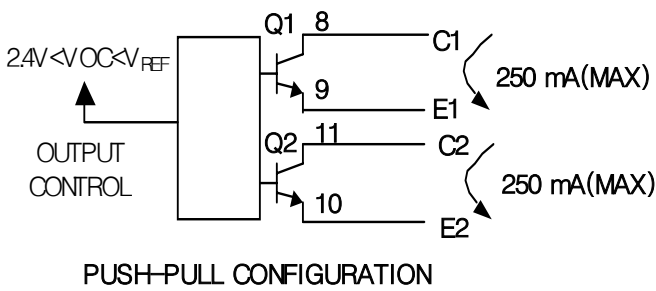
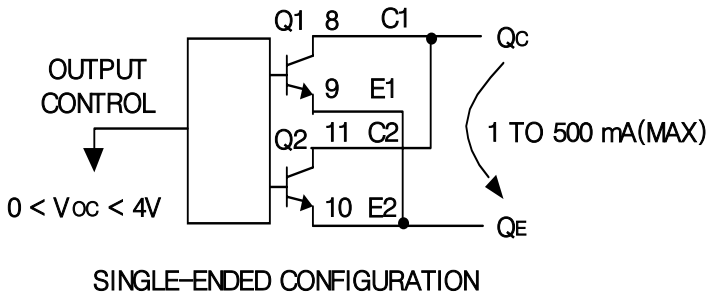


Fig. 7 Error Amplifier Sensing Techniques

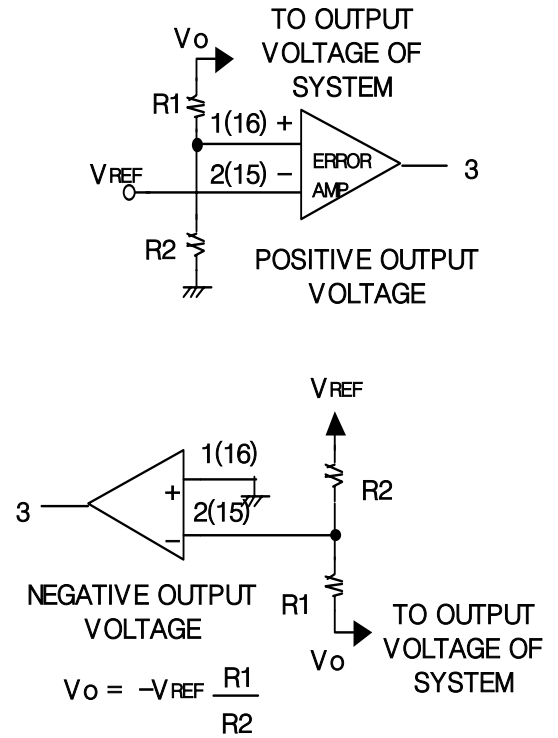


Fig. 8 Slaving Two or More Control Circuits

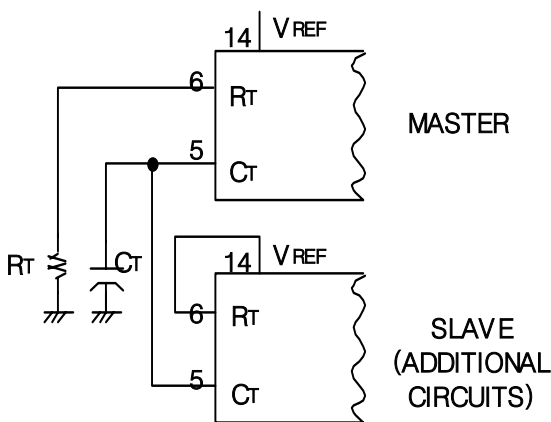
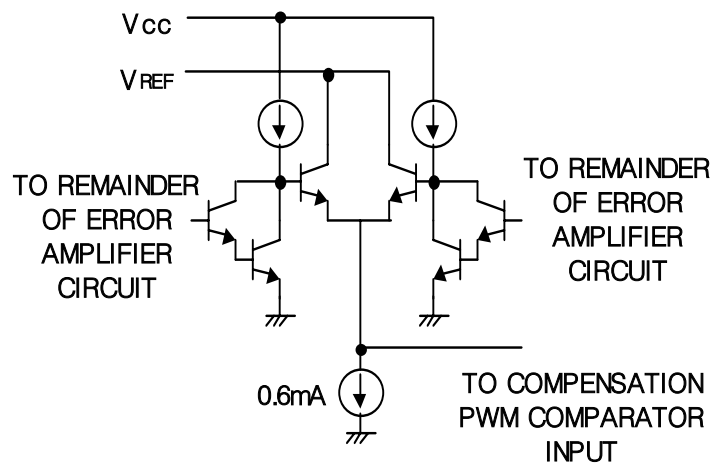


Fig. 9 Error Amplifier and Current Limit Sense Amplifier Output Circuits



Electrical Characteristic Curves

Fig. 1  $V_{CE(sat)} - I_C$

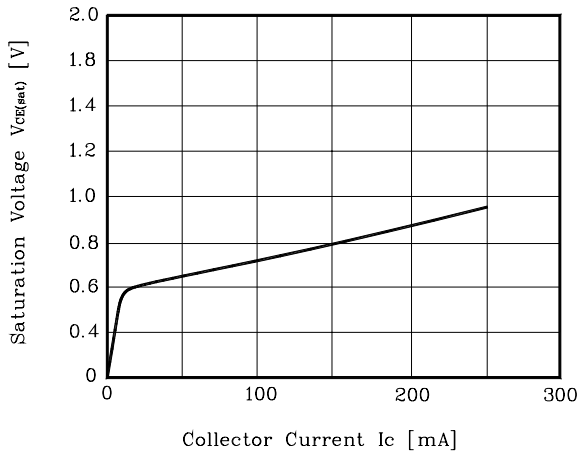


Fig. 2  $V_{CE} - I_E$

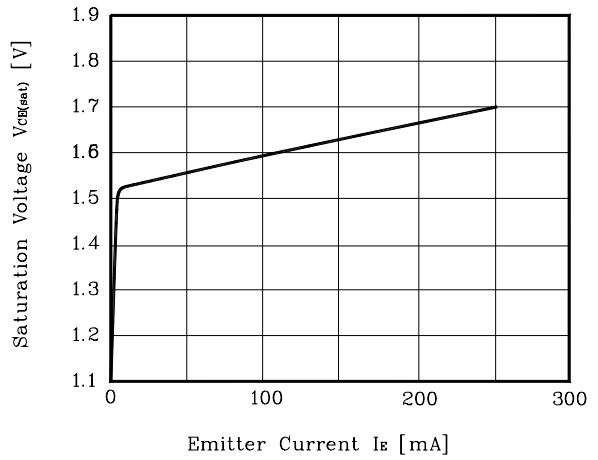


Fig. 3  $t_{osc} - R_T$

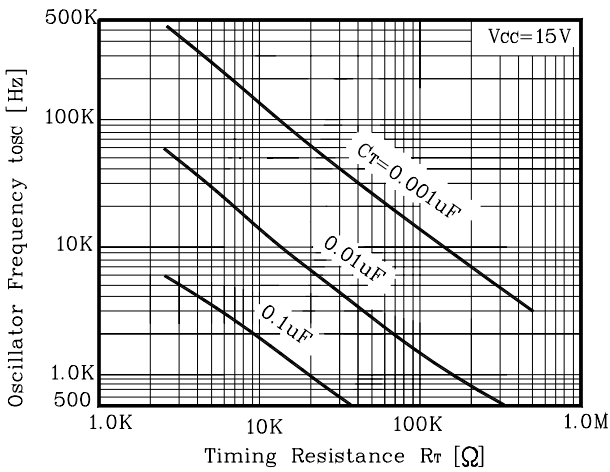


Fig. 4  $A_{VOL}$ , Phase - f

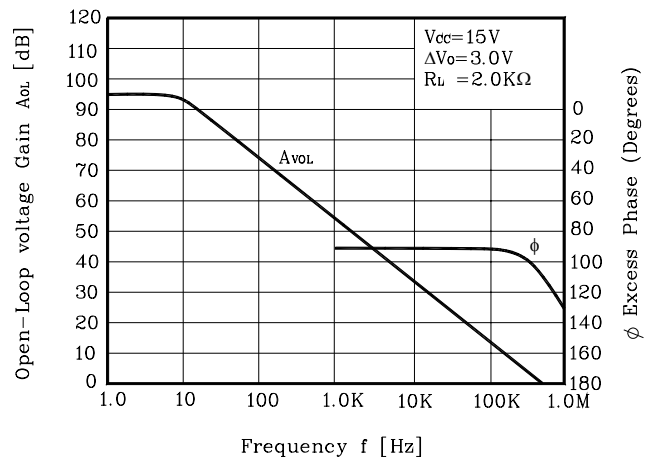
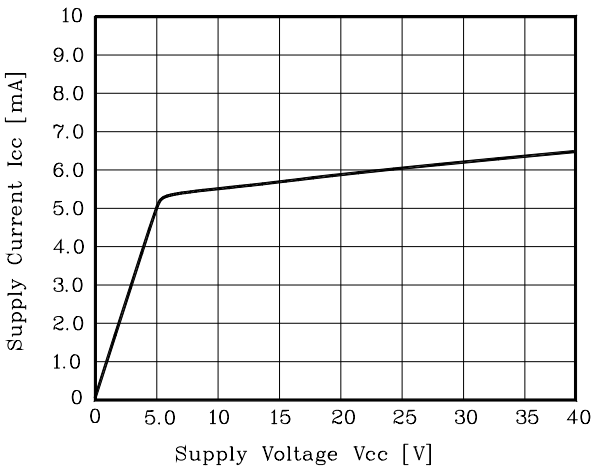


Fig. 5  $I_{CC} - V_{CC}$





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