ADS131M04 4-channel, simultaneously-sampling, 24-bit, delta-sigma ADC

1 Features

- 4 simultaneously sampling differential inputs
- Programmable data rate up to 32 kSPS
- Programmable gain up to 128
- Noise performance:
  - 101-dB dynamic range at gain = 1, 4 kSPS
  - 81-dB dynamic range at gain = 64, 4 kSPS
- Total harmonic distortion: –100 dB
- High-impedance inputs for direct sensor connection:
  - >100-kΩ input impedance for gains = 1, 2, and 4
  - >1-MΩ input impedance for gains = 8, 16, 32, and 64
- Programmable channel-to-channel phase delay calibration with 244-ns resolution with 8.192-MHz f_{CLKIN}
- Current detect mode allows for super low power tamper detection
- Fast startup: first data within 0.5 ms of supply ramp
- Integrated negative charge pump allows input signals below ground
- Crosstalk between channels: –110 dB
- Low-drift internal voltage reference
- Cyclic redundancy check (CRC) on communications and register map
- 2.7-V to 3.6-V analog and digital supplies
- Low power consumption: 3.3 mW at 3-V AVDD and DVDD
- Package: 20-pin TSSOP or 20-pin WQFN
- Operating temperature range: –40°C to +125°C

2 Applications

- Electricity meters: commercial and residential
- Circuit breakers
- Battery test equipment
- Battery management systems

3 Description

The ADS131M04 is a four-channel, simultaneously-sampling, 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) that offers wide dynamic range, low power, and energy-measurement-specific features, making the device excellent for energy metering, power metrology, and circuit breaker applications. The ADC inputs can be directly interfaced to a resistor-divider network or a power transformer to measure voltage or to a current transformer or a Rogowski coil to measure current.

The individual ADC channels can be independently configured depending on the sensor input. A low-noise, programmable gain amplifier (PGA) provides gains ranging from 1 to 128 to amplify low level signals. Additionally, this device integrates channel-to-channel phase calibration and offset and gain calibration registers to help remove signal chain errors.

A low-drift, 1.2-V reference is integrated into the device reducing printed circuit board (PCB) area. Cyclic redundancy check (CRC) options can be individually enabled on the data input, data output, and register map to ensure communication integrity.

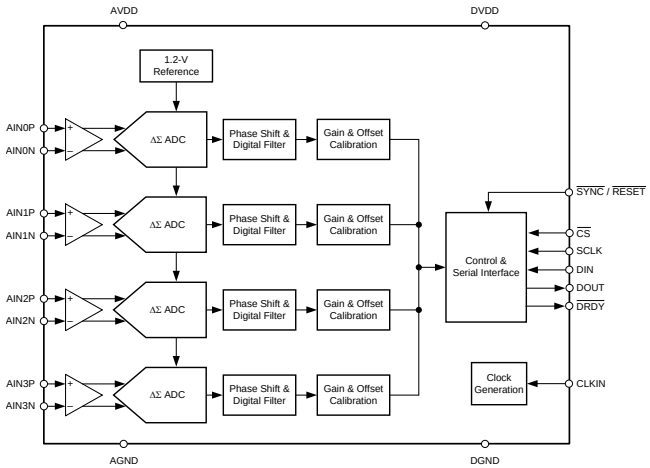
The complete analog front-end (AFE) solution is offered in a 20-pin TSSOP or leadless 20-pin WQFN package and is specified over the industrial temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS131M04	TSSOP (20)	6.50 mm × 4.40 mm
	WQFN (20)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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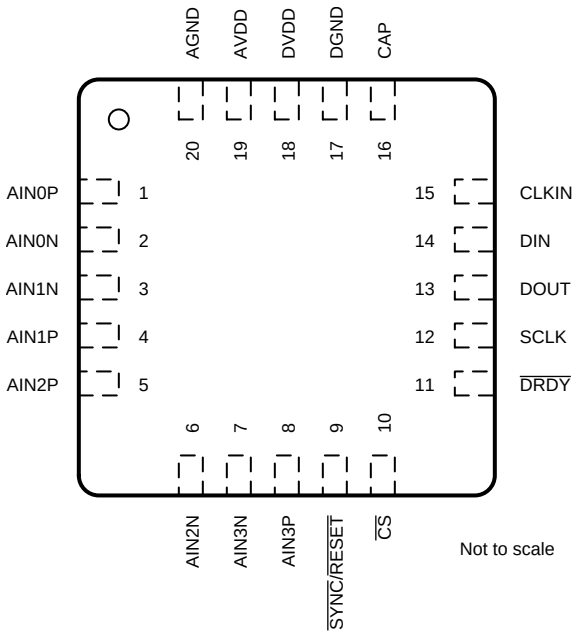
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2019	*	Initial release.

5 Pin Configuration and Functions

ADS131M04: RUK Package
20-Pin WQFN
Top View



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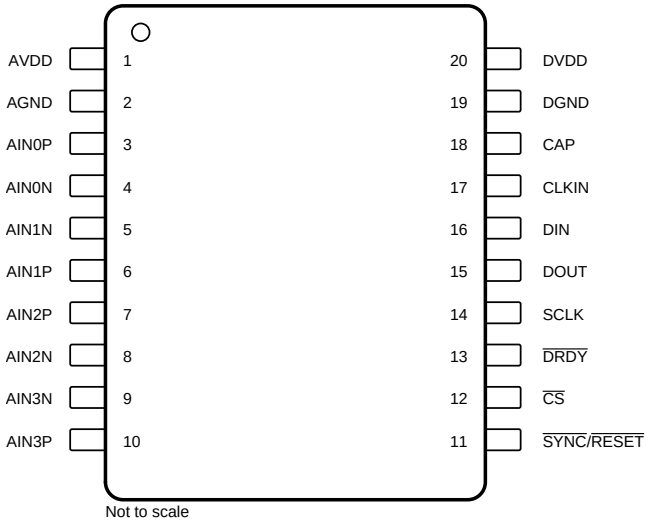
ADS131M04: PW Package
20-Pin TSSOP
Top View



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Pin Functions: SBAS890

PIN			I/O	DESCRIPTION
NAME	NO.			
	WQFN	TSSOP		
AGND	20	2	Supply	Analog ground
AIN0N	2	4	Analog input	Negative analog input 1
AIN0P	1	3	Analog input	Positive analog input 1
AIN1N	3	5	Analog input	Negative analog input 2
AIN1P	4	6	Analog input	Positive analog input 2
AIN2N	6	8	Analog input	Negative analog input 3
AIN2P	5	7	Analog input	Positive analog input 3
AIN3N	7	9	Analog input	Negative analog input 4
AIN3P	8	10	Analog input	Positive analog input 4
AVDD	19	1	Supply	Analog supply. Connect a 1-µF capacitor to AGND.
CAP	16	18	Analog output	Digital low-dropout (LDO) regulator output. Connect a 220-nF capacitor to DGND.
CLKIN	15	17	Digital input	Master clock input
$\overline{CS}$	10	12	Digital input	Chip select; active low
DGND	17	19	Supply	Digital ground
DIN	14	16	Digital input	Serial data input
DOUT	13	15	Digital output	Serial data output
$\overline{DRDY}$	11	13	Digital output	Data ready; active low
DVDD	18	20	Supply	Digital I/O supply. Connect a 1-µF capacitor to DGND.
SCLK	12	14	Digital input	Serial data clock
$\overline{SYNC}/\overline{RESET}$	9	11	Digital input	Conversion synchronization or system reset; active low

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6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AGND	–0.3	3.9	V
	AGND to DGND	–0.3	0.3	
	DVDD to DGND	–0.3	3.9	
Analog input voltage	AINxP, AINxN	AGND – 1.6	AVDD + 0.3	V
Digital input voltage	$\overline{CS}$, CLKIN, DIN, SCLK, $\overline{SYNC}$/$\overline{RESET}$	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous, all pins except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVDD to AGND	2.7	3.0	3.6	V
		AGND to DGND	–0.3	0	0.3	
	Digital power supply	DVDD to DGND	2.7	3.0	3.6	V
		DVDD to DGND, DVDD shorted to CAP	1.65	1.8	2	
ANALOG INPUTS						
$V_{AINxP/N}$(1)	Absolute input voltage	Gain = 1, 2, or 4	AGND – 1.3		AVDD	V
		Gains = 8, 16, 32, 64 or 128	AGND – 1.3		AVDD - 1.8	
V_{IN}	Differential input voltage	$V_{IN} = V_{AINxP} - V_{AINxN}$	$-V_{REF}$ / Gain		V_{REF} / Gain	V
EXTERNAL CLOCK SOURCE						
f_{CLKIN}	External clock frequency	High-resolution mode	1	8.192	8.3	MHz
		Low-power mode	1	4.096	4.15	
		Very-low-power mode	0.2	2.048	2.08	
	Duty cycle		40	50	50	%
DIGITAL INPUTS						
	Input voltage		DGND		DVDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

(1) The subscript "x" signifies the channel. For example, the positive analog input to channel 0 is named AIN0P. Refer to the Pin Configurations and Functions section for the pin names.

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6.4 Thermal Information

THERMAL METRIC(1)		ADS131M04		UNIT
		RUK (QFN)	PW (TSSOP)	
		PINS	PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	94.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	34.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	46.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	2.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	46.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 3 V, DVDD = 3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
Z_{in}	Differential input impedance	Gain = 1, 2, or 4		300		kΩ
		Gain = 8, 16, 32, or 64		1		MΩ
		All other power modes		See Table 3		
ADC CHARACTERISTICS						
	Resolution			24		Bits
	Gain settings			1, 2, 4, 8, 16, 32, 64, 128		
	Data rate	High-resolution mode, f_{CLKIN} = 8.192 MHz	250		32k	SPS
		Low-power mode, f_{CLKIN} = 4.096 MHz	125		16k	
		Very low-power mode, f_{CLKIN} = 2.048 MHz	62.5		8k	
	Startup time	Measured from supplies at 90% to first $\overline{DRDY}$ falling edge		0.5		ms
ADC PERFORMANCE						
INL	Integral nonlinearity (best fit)			6		ppm of FSR
V_{IO}	Input offset voltage			750		µV
	Offset temperature drift			1		µV/°C
	Gain error(1)			±0.1		% of FS
	Gain temperature drift(1)			1		ppm/°C
DC CMRR	DC common-mode rejection ratio			100		dB
DC PSRR	DC power-supply rejection ratio	AVDD		75		dB
		DVDD		88		
	Dynamic range	Gain = 1	99	102		dB
		Gain = 64		80		dB
		All other gain settings		See Table 2		
	Crosstalk	f_{IN} = 50 Hz or 60 Hz		–110		dB
SNR	Signal-to-noise ratio	f_{IN} = 50 Hz or 60 Hz, gain = 1, V_{IN} = -0.5 dBFS, normalized		98		dB
		f_{IN} = 50 Hz or 60 Hz, gain = 64, V_{IN} = -0.5 dBFS, normalized		79		
THD	Total harmonic distortion	f_{IN} = 50 Hz or 60 Hz (up to 50 harmonics), V_{IN} = -0.5 dBFS		–104		dB
SFDR	Spurious-free dynamic range	f_{IN} = 50 Hz or 60 Hz (up to 50 harmonics), V_{IN} = -0.5 dBFS		105		dB
AC CMRR	AC common-mode rejection ratio	f_{CM} = 50 Hz or 60 Hz		91		dB
AC PSRR	AC power-supply rejection ratio	AVDD supply, f_{PS} = 50 Hz or 60 Hz		75		dB
		DVDD supply, f_{PS} = 50 Hz or 60 Hz		85		
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Internal reference voltage			1.2		V
	Accuracy	T_A = 25°C		0.1		%
	Temperature drift			±12		ppm/°C
DIGITAL INPUTS/OUTPUTS						

(1) Gain error measumrents include internal reference error.

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Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C;

all specifications are at AVDD = 3 V, DVDD = 3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Logic input level, low		DGND		0.2 DVDD	V
V_{IH}	Logic input level, high		0.8 DVDD		DVDD	V
V_{OL}	Logic output level, low	I_{OL} = -1 mA			0.2 DVDD	V
V_{OH}	Logic output level, high	I_{OH} = 1 mA	0.8 DVDD			V
I_{IN}	Input current	DGND < $V_{Digital\ Input}$ < DVDD	–1		1	µA
POWER SUPPLY						
I_{AVDD}	Analog supply current	High-resolution mode		3.5	4.0	mA
		Low-power mode		2.0	2.2	
		Very-low-power mode		1.0	1.2	
		Current detect mode		TBD		µA
		Standy mode		0.3		
		All other gain settings		See TBD section		
I_{DVDD}	Digital supply current(2)	High-resolution mode		0.4	0.5	mA
		Low-power mode		0.2	0.3	
		Very-low-power mode		0.1	0.2	
		Current detect mode		TBD		µA
		Standy mode		1		
P_D	Power dissipation	High-resolution mode		12		mW
		Low-power mode		6.6		
		Very-low-power mode		3.3		
		Current detect mode		TBD		µW
		Standy mode		3.9		

(2) Currents measured with SPI idle.

6.6 Timing Requirements

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT(1)
1.65 V ≤ DVDD ≤ 2.0 V					
$t_{w(CLL)}$	Pulse duration, CLKIN low	49			ns
$t_{w(CLH)}$	Pulse duration, CLKIN high	49			ns
$t_{c(SC)}$	SCLK period	64			ns
$t_{w(SCL)}$	Pulse duration, SCLK low	32			ns
$t_{w(SCH)}$	Pulse duration, SCLK high	32			ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	16			ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10			ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	20			ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling egde	5			ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	8			ns
$t_{w(RSL)}$	Pulse duration, $\overline{SYNC}/\overline{RESET}$ low to generate device reset	2048			t_{CLKIN}
$t_{w(SYL)}$	Pulse duration, $\overline{SYNC}/\overline{RESET}$ low for synchronization	1		2047	t_{CLKIN}
$t_{su(SY)}$	Setup time, $\overline{SYNC}/\overline{RESET}$ valid before CLKIN rising edge	10			ns
2.7 V ≤ DVDD ≤ 3.6 V					
$t_{w(CLL)}$	Pulse duration, CLKIN low	49			ns

(1) t_{CLKIN} = 1 / f_{CLKIN}.

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Timing Requirements (continued)

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT(1)
$t_{w(CLH)}$	Pulse duration, CLKIN high	49			ns
$t_{c(SC)}$	SCLK period	40			ns
$t_{w(SCL)}$	Pulse duration, SCLK low	20			ns
$t_{w(SCH)}$	Pulse duration, SCLK high	20			ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	16			ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10			ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	15			ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling egde	5			ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	8			ns
$t_{w(RSL)}$	Pulse duration, $\overline{SYNC}/\overline{RESET}$ low to generate device reset	2048			t_{CLKIN}
$t_{w(SYL)}$	Pulse duration, $\overline{SYNC}/\overline{RESET}$ low for synchronization	1		2047	t_{CLKIN}
$t_{su(SY)}$	Setup time, $\overline{SYNC}/\overline{RESET}$ valid before CLKIN rising edge	10			ns

6.7 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT(1)
1.65 V ≤ DVDD ≤ 2.0 V						
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven				50	ns
$t_{p(SCDO)}$	Progapation delay time, SCLK rising edge to valid new DOUT				26	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedace				50	ns
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high			4		t_{CLKIN}
$t_{w(DRL)}$	Pulse duration, $\overline{DRDY}$ low			4		t_{CLKIN}
	SPI timeout		32768			t_{CLKIN}
t_{POR}	Power-on-reset time	Measured from supplies at 90%		TBD		µs
t_{REGACQ}	Register default acquisition time			5		µs
2.7 V ≤ DVDD ≤ 3.6 V						
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven				50	ns
$t_{p(SCDO)}$	Progapation delay time, SCLK rising edge to valid new DOUT				15	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedace				50	ns
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high			4		t_{CLKIN}
$t_{w(DRL)}$	Pulse duration, $\overline{DRDY}$ low			4		t_{CLKIN}
	SPI timeout		32768			t_{CLKIN}
t_{POR}	Power-on-reset time	Measured from supplies at 90%		TBD		µs
t_{REGACQ}	Register default acquisition time			5		µs

(1) $t_{CLKIN} = 1 / f_{CLKIN}$.

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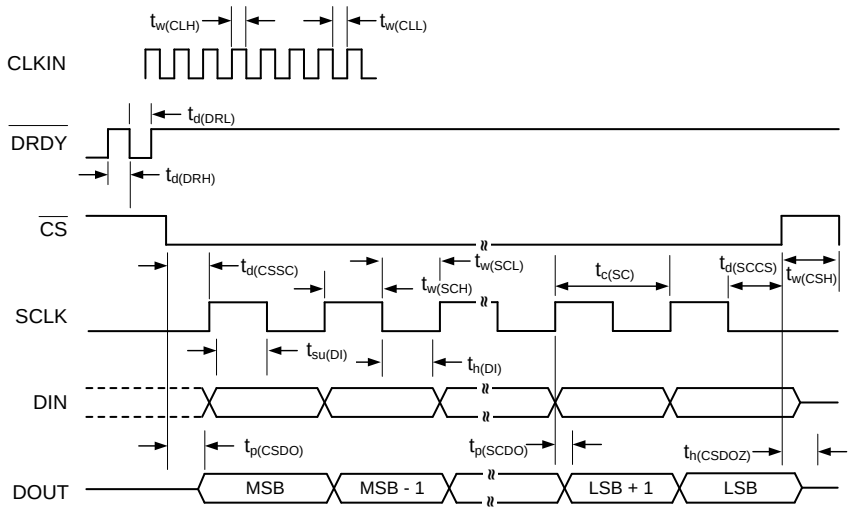

NOTE: SPI settings are CPOL = 0 and CPHA = 1. $\overline{CS}$ transitions must take place when SCLK is low.

Figure 1. SPI Timing Diagram

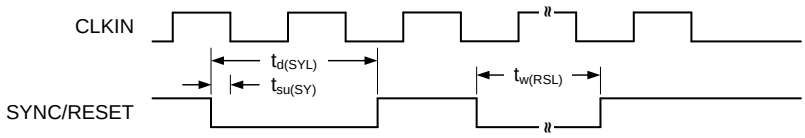

Figure 2. $\overline{SYNC}/\overline{RESET}$ Timing Requirements

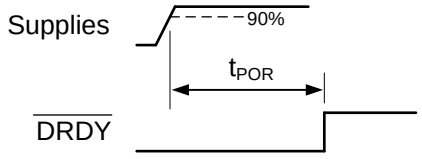

Figure 3. Power-On-Reset Timing

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7 Parameter Measurement Information

7.1 Noise Measurements

Adjust the data rate and gain to optimize the ADS131M04 noise performance. When averaging is increased by reducing the data rate, noise drops correspondingly. Table 1 summarizes the ADS131M04 noise performance using the 1.2-V internal reference and a 3.0-V analog power supply. The data are representative of typical noise performance at T_A = 25°C when f_{CLKIN} = 8.192 MHz. The modulator clock frequency $f_{MOD} = f_{CLKIN} / 2$. The data shown are typical input-referred noise results with the analog inputs shorted together and taking an average of multiple readings across all channels. A minimum 1 second of consecutive readings are used to calculate the RMS noise for each reading. Table 2 shows the dynamic range and effective resolution calculated from the noise data. Equation 1 calculates dynamic range. Equation 2 calculates effective resolution. In each case, V_{REF} corresponds to the internal 1.2-V reference.

$$\text{Dynamic Range} = 20 \times \log\left(\frac{V_{REF}}{\sqrt{2} \times \text{Gain} \times V_{RMS}}\right) \quad (1)$$

$$\text{Effective Resolution} = \log_2\left(\frac{2 \times V_{REF}}{\text{Gain} \times V_{RMS}}\right) \quad (2)$$

Table 1. Noise (μV_{RMS}) at T_A = 25°C

OSR	DATA RATE (kSPS), f_{CLKIN} = 8.192 MHz	GAIN							
		1	2	4	8	16	32	64	128
16384	0.25	2.63	2.48	2.37	1.36	0.79	0.44	0.44	0.43
8192	0.5	3.47	3.14	3.04	1.68	0.95	0.57	0.56	0.57
4096	1	4.64	4.22	4.02	2.19	1.26	0.77	0.75	0.76
2048	2	6.06	5.39	5.08	2.84	1.61	0.99	1.02	1.01
1024	4	7.39	6.44	6.04	3.42	2.01	1.23	1.24	1.24
512	8	10.45	9.12	8.58	4.95	2.96	1.86	1.83	1.87
256	16	15.05	12.78	12.05	6.98	4.18	2.58	2.63	2.58
128	32	24.54	19.23	17.26	10.09	6.11	3.76	3.85	3.79

Table 2. Dynamic Range (Effective Resolution) at T_A = 25°C

OSR	DATA RATE (kSPS), f_{CLKIN} = 8.192 MHz	GAIN							
		1	2	4	8	16	32	64	128
16384	0.25	110 (19.8)	105 (18.9)	99 (17.9)	98 (17.8)	97 (17.5)	96 (17.4)	90 (16.4)	84 (15.4)
8192	0.5	108 (19.4)	103 (18.5)	97 (17.6)	96 (17.4)	95 (17.3)	93 (17.0)	87 (16.0)	81 (15.0)
4096	1	105 (19.0)	100 (18.1)	94 (17.2)	94 (17.1)	93 (16.9)	91 (16.6)	85 (15.6)	79 (14.6)
2048	2	103 (18.6)	98 (17.8)	92 (16.8)	91 (16.7)	90 (16.5)	89 (16.2)	82 (15.2)	76 (14.2)
1024	4	101 (18.3)	96 (17.5)	91 (16.6)	90 (16.4)	88 (16.2)	87 (15.9)	81 (14.9)	75 (13.9)
512	8	98 (17.8)	93 (17.0)	88 (16.1)	87 (15.9)	85 (15.6)	83 (15.3)	77 (14.3)	71 (13.3)
256	16	95 (17.3)	90 (16.5)	85 (15.6)	84 (15.4)	82 (15.1)	80 (14.8)	74 (13.8)	68 (12.8)
128	32	91 (16.6)	87 (15.9)	82 (15.1)	80 (14.9)	79 (14.6)	77 (14.3)	71 (13.2)	65 (12.3)

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7.2 Input Impedance Measurements

The ADS131M04 input impedance depends on the PGA gain setting and the master clock frequency. The input impedance for gains of 4 and lower follows the formula given in Equation 4. The input impedance does not follow a formula for higher gains and is therefore based on device characterization. See the *Programmable Gain Amplifier (PGA)* section for more details about the analog inputs. Table 3 shows typical input impedance measurements for all gain settings and for three different master clock frequencies at room temperature.

Table 3. Input Impedance (MΩ) at T_A = 25°C

f_{CLKIN} (MHz)	GAIN							
	1	2	4	8	16	32	64	128
8.192	0.317	0.317	0.317	3.02	1.55	1.12	1.12	1.12
4.096	0.634	0.634	0.634	108	88.5	6.31	6.31	6.31
2.048	1.268	1.268	1.268	389	463	10	10	10

8 Detailed Description

8.1 Overview

The ADS131M04 is a low-power, four-channel, simultaneously sampling, 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with a low-drift internal reference voltage. The dynamic range, size, feature set, and power consumption are optimized for cost-sensitive applications requiring simultaneous sampling.

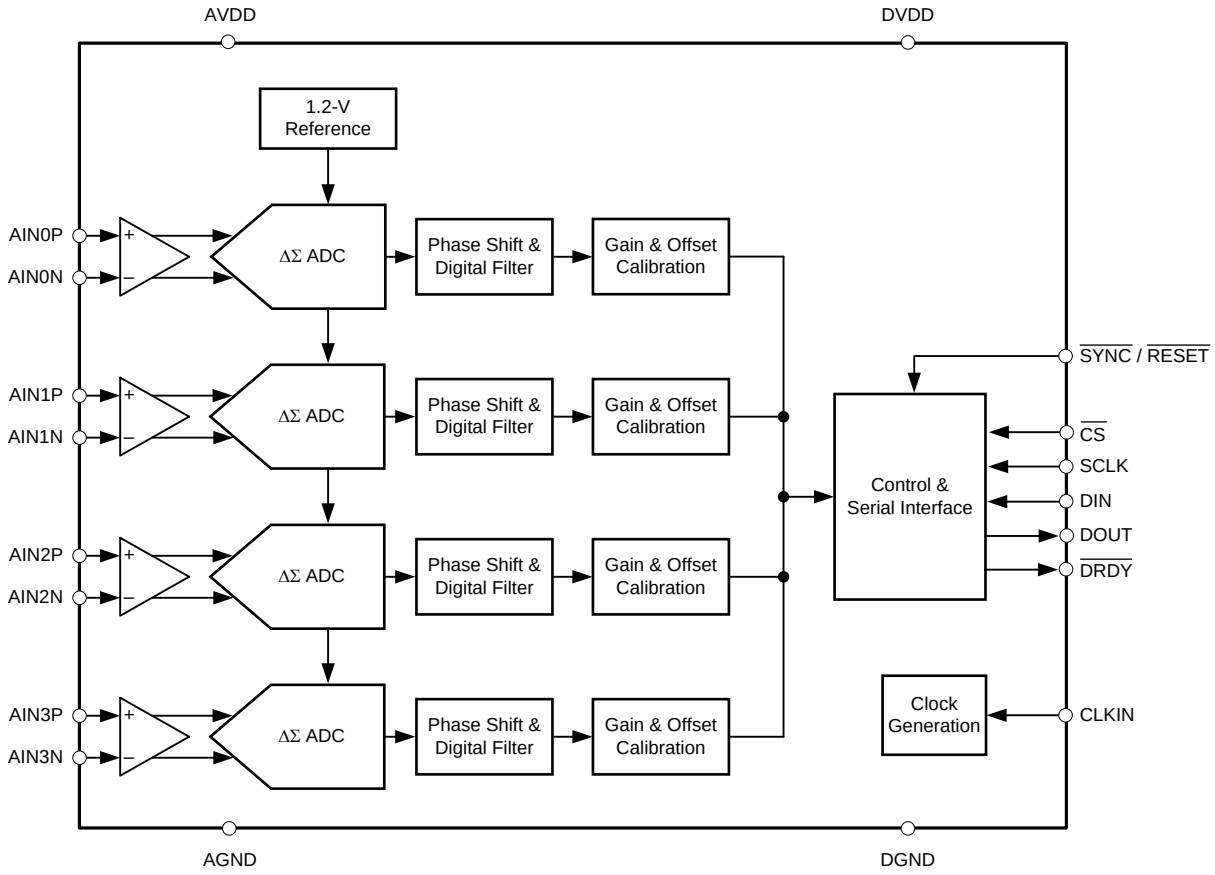
The ADS131M04 requires both analog and digital supplies. The analog power supply (AVDD – AGND) can operate between 2.7 V and 3.6 V. An integrated negative charge pump allows absolute input voltages as low as 1.3 V below AGND, which enables measurements of input signals varying around ground with a single-ended power supply. The digital power supply (DVDD – DGND) accepts both 1.8-V and 3.3-V supplies. The device features a programmable gain amplifier (PGA) with gains up to 128. An integrated input precharge buffer enabled at gains greater than 4 ensures high input impedance at high PGA gain settings. The ADC receives its reference voltage from an integrated 1.2-V reference. The device allows differential input voltages as large as the reference. Three power-scaling modes allow designers to trade power for ADC dynamic range.

Each channel on the ADS131M04 contains a digital decimation filter that demodulates the output of the ΔΣ modulators. The filter enables data rates as high as 32 kSPS per channel in high-resolution mode. The relative phase of the samples can be configured between channels, thus enabling an accurate compensation for the sensor phase response. Offset and gain calibration registers can be programmed to automatically adjust output samples for measured offset and gain errors. *Functional Block Diagram* section provides a detailed diagram of the ADS131M04.

The device communicates via an serial programming interface (SPI)-compatible interface. Several SPI commands and internal registers control the operation of the ADS131M04. Other devices can easily be added to the same SPI bus by adding discrete $\overline{CS}$ control lines. The $\overline{SYNC}$/$\overline{RESET}$ pin can be used to synchronize conversions between multiple ADS131M04 devices as well as to maintain synchronization with external events.

ADVANCE INFORMATION

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input ESD Protection Circuitry

Basic electrostatic discharge (ESD) circuitry protects the ADS131M04 inputs from ESD and overvoltage events in conjunction with external circuits and assemblies. Figure 4 shows a simplified representation of the ESD circuit. The protection for input voltages exceeding AVDD can be modeled as a simple diode.

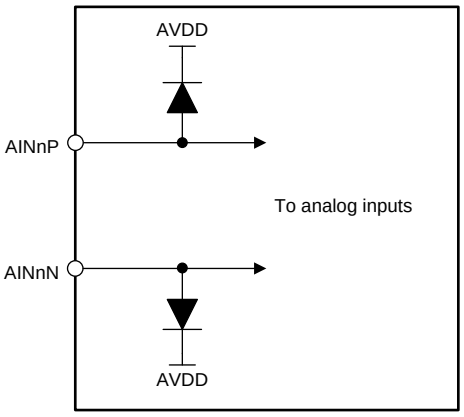


Figure 4. Input ESD Protection Circuitry

Feature Description (continued)

The ADS131M04 has an integrated negative charge pump that allows for input voltages below AGND with a unipolar supply. Consequently, shunt diodes between the inputs and AGND cannot be used to clamp excessive negative input voltages. Instead, the same diode that clamps overvoltage is used to clamp undervoltage at its reverse breakdown voltage. Take care to prevent input voltages or currents from exceeding the limits provided in the *Absolute Maximum Ratings* table.

8.3.2 Input Multiplexer

Each channel of the ADS131M04 has a dedicated input multiplexer. The multiplexer controls which signals are routed to the ADC channels. Configure the input multiplexer using the MUXn[1:0] bits in the CHn_CFG register. The input multiplexer allows the following inputs to be connected to the ADC channel:

- The analog input pins corresponding to the given channel
- Shorted to AGND, which is helpful for offset calibration
- DC test signal

See the *Internal Test Signals* section for more information about the test signals. Figure 5 shows a diagram of the input multiplexer on the ADS131M04.

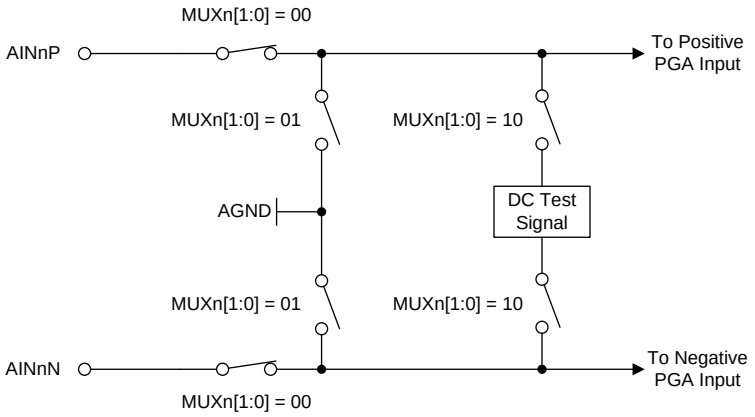


Figure 5. Input Multiplexer

8.3.3 Programmable Gain Amplifier (PGA)

Each channel of the ADS131M04 features an integrated programmable gain amplifier (PGA) that provides gains of 1, 2, 4, 8, 16, 32, 64, and 128. The gains for all channels are individually controlled by the PGAGAINn bits for each channel in the GAIN1 register.

Varying the PGA gain scales the differential full-scale input voltage range (FSR) of the ADC. Equation 3 describes the relationship between FSR and gain. Equation 3 uses the internal reference voltage, 1.2 V, as the scaling factor without accounting for gain error caused by tolerance in the reference voltage.

$$\text{FSR} = \pm 1.2\ \text{V} / \text{Gain} \quad (3)$$

Table 4 shows the corresponding full-scale ranges for each gain setting.

Table 4. Full-Scale Range

GAIN SETTING	FSR
1	±1.2 V
2	±600 mV
4	±300 mV
8	±150 mV
16	±75 mV
32	±37.5 mV
64	±18.75 mV
128	±9.375 mV

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The input impedance of the PGA dominates the input impedance characteristics of the ADS131M04. The PGA input impedance for gain settings up to 4 behaves according to Equation 4 without accounting for device tolerance and change over temperature. Minimize output impedance of the circuit that drives the ADS131M04 inputs to obtain the best possible gain error, INL, and distortion performance.

$$317\ k\Omega \times 4.096\ MHz / f_{MOD} \quad (4)$$

where:

- f_{MOD} is the ΔΣ modulator frequency, $f_{CLKIN} / 2$

The device uses an input precharge buffer for PGA gain settings of 8 and higher. There is no formula to govern the input impedance in these settings. The specified input impedance is based on characterization. The typical values can be found in Table 3.

8.3.4 Voltage Reference

The ADS131M04 uses an internally-generated, low-drift, band-gap voltage to supply the reference for the ADC. The reference has a nominal voltage of 1.2 V, allowing the differential input voltage to swing from –1.2 V to 1.2 V. The reference circuitry starts up very quickly to accommodate the fast-startup feature of this device. The device waits until after the reference circuitry is fully settled before generating conversion data. There is no delay or wait time after the first conversion result is ready.

8.3.5 Clocking and Power Modes

An LVCMOS clock must be provided at the CLKIN pin continuously when the ADS131M04 is running in normal operation. The frequency of the clock can be scaled in conjunction with the power mode to provide a tradeoff between power and dynamic range.

The PWR[1:0] bits in the CLOCK register allow the device to be configured in one of three power modes: high-resolution (HR) mode, low-power (LP) mode, and very-low-power (VLP) mode. Changing the PWR[1:0] bits scale the bias internal currents to achieve the expected power levels. The external clock frequency must follow the guidance provided in the *Recommended Operating Conditions* table corresponding to the intended power mode in order for the device to perform according to the specified behavior.

8.3.6 ΔΣ Modulator

The ADS131M04 uses a delta-sigma (ΔΣ) modulator to convert the analog input voltage to a one's density modulated digital bit-stream. The ΔΣ modulator oversamples the input voltage at a frequency many times greater than the output data rate. The modulator frequency, f_{MOD} of the ADS131M04 is equal to half the frequency of the clock provided at the CLKIN pin.

The output of the modulator is fed back to the modulator input through a digital-to-analog converter (DAC) as a means of error correction. This feedback mechanism shapes the modulator quantization noise in the frequency domain to make the noise more dense at higher frequencies and less dense in the band of interest. The digital decimation filter following the ΔΣ modulator significantly attenuates the out-of-band modulator quantization noise, allowing the device to provide excellent dynamic range.

8.3.7 Digital Decimation Filter

The digital decimation filter significantly attenuates the out-of-band quantization noise from the ΔΣ modulator that is shaped in the frequency domain. The digital filter is a linear phase, finite impulse response (FIR), low-pass, third-order sinc filter ($sinc^3$). The filter demodulates the output of the ΔΣ modulator by averaging. The data passing through the filter is decimated, or downsampled, to reduce the output frequency from the modulator frequency to the data rate. The decimation factor is called the *oversampling ratio (OSR)*. The OSR is configurable and is set by the OSR[2:0] bits in the CLOCK register.

The OSR dictates the period for which the filter averages the modulator output that determines the filter bandwidth. The filter bandwidth directly affects the noise performance of the ADC because lower bandwidth results in lower noise whereas higher bandwidth results in higher noise. See Table 1 for the noise specifications for various OSR settings. There are eight OSR settings in the ADS131M04, allowing eight different data rate settings for any given master clock frequency.

Equation 5 calculates the z-domain transfer function for the digital filter. Equation 6 calculates the transfer function in terms of the continuous-time frequency parameter *f*.

$$|H(z)| = \left| \frac{1 - Z^{-N}}{1 - Z^{-1}} \right|^3 \quad (5)$$

where:

- N is the OSR

$$H(f)| = \left| \frac{\sin\left(\frac{N\pi f}{f_{MOD}}\right)}{N \times \sin\left(\frac{\pi f}{f_{MOD}}\right)} \right|^3 \quad (6)$$

where:

- N is the OSR

The filter has infinite attenuation at integer multiples of the data rate except for integer multiples of f_{MOD}. Like all digital filters, the digital filter response on the ADS131M04 repeats at integer multiples of the modulator frequency, f_{MOD}. The data rate and filter notch frequencies scale with f_{MOD}.

When possible, plan frequencies for unrelated periodic processes in the application for integer multiples of the data rate such that any parasitic effect they have on data acquisition is effectively cancelled by the notches of the digital filter. Avoid frequencies near integer multiples of f_{MOD} whenever possible because tones in these bands can alias to the band of interest.

Figure 6 to Figure 8 show the digital filter response.

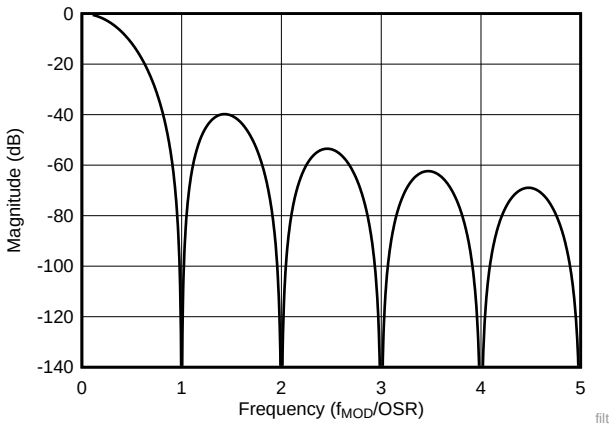

Figure 6. Sinc^3 Digital Filter Response

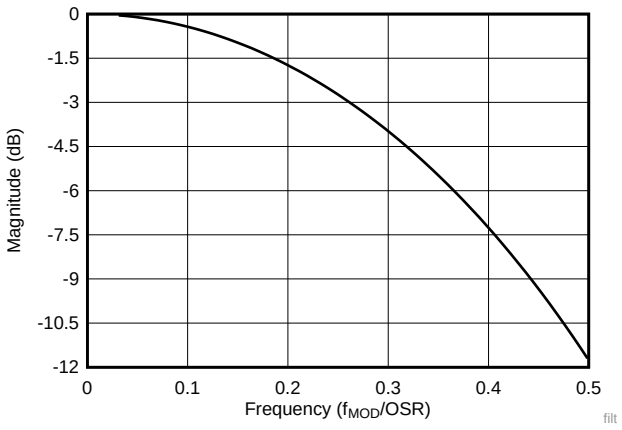

Figure 7. Sinc^3 Digital Filter Response, Pass-Band Detail

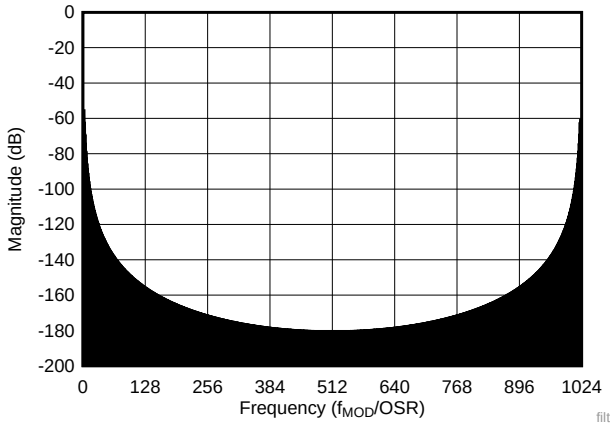

Figure 8. Sinc^3 Digital Filter Response, OSR 1024, Stop-Band Detail

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8.3.7.1 Fast-Startup Response

The ADS131M04 starts up and generates conversion data very quickly following a supply ramp or reset. This response is achieved in part by using a dual digital filter path. When the device first starts up, data are generated using a first-order sinc filter. After two samples, the device switches to and remains in the sinc^3 filter setting until the next time the device is powered down or reset. Figure 9 through Figure 11 show the digital filter response of the fast-settling filter with the sinc^3 filter response superimposed to illustrate the contrast. The fast-settling filter settling time is counterbalanced by wider bandwidth and less stop-band attenuation. Consequently, the noise performance obtainable from using this digital filter is not as high as with the sinc^3 filter. The first two samples available from the ADS131M04 after a supply ramp or reset have the noise performance and frequency response corresponding to the fast-settling filter, whereas subsequent samples have the noise performance and frequency response consistent with the sinc^3 filter. See the *Fast Startup* section for more details regarding the fast startup capabilities of the ADS131M04.

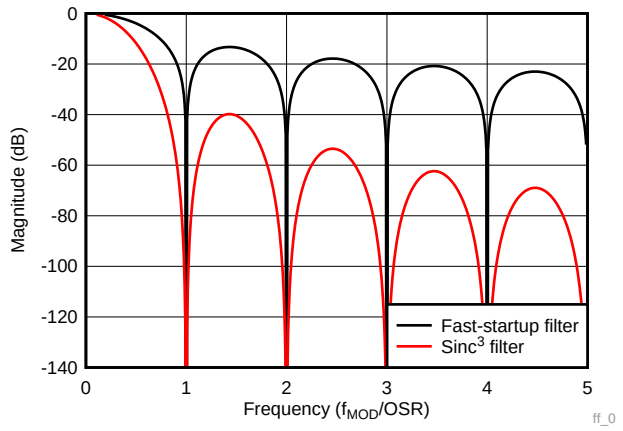

Figure 9. Fast-Settling and Sinc^3 Digital Filter Response

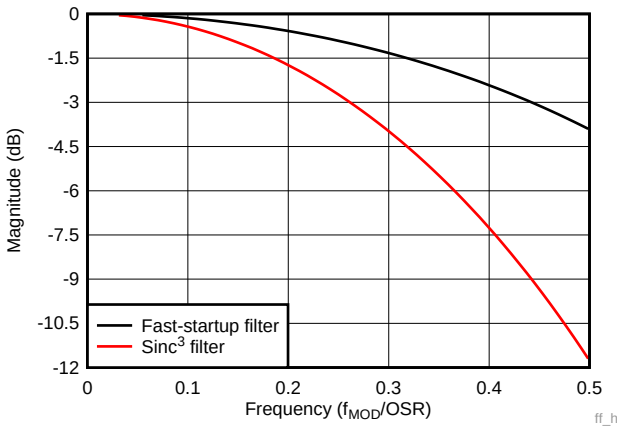

Figure 10. Fast-Settling and Sinc^3 Digital Filter Response, Pass-Band Detail

FPO

Figure 11. Fast-Settling and Sinc^3 Digital Filter Response, OSR 1024, Stop-Band Detail

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8.3.8 Internal Test Signals

The ADS131M04 features an internal analog test signal that is useful for troubleshooting and diagnosis. A DC test signal can be applied to the channel inputs through the input multiplexer. The multiplexer is controlled through the MUXn[1:0] bits in the CHn_CFG register. The test signals are created by internally dividing the reference voltage. The same signal is shared by all channels.

The test signal is nominally 2/15 × V_{REF}. The test signal automatically adjusts its voltage level with the gain setting such that the ADC always measures a signal that is 2/15 × $V_{Diff\ Max}$. For example, at a gain of 1, this voltage equates to 160 mV. At a gain of 2, this voltage is 80 mV.

8.3.9 Channel Phase Calibration

The ADS131M04 allows fine adjustment of the sample phase between channels through the use of channel phase calibration. This feature is helpful when different channels are measuring the outputs of different types of sensors that have different phase responses. For example, in power metrology applications, voltage can be measured by a voltage divider, whereas current is measured using a current transformer that exhibits a phase difference between its input and output signals. The differences in phase between the voltage and current measurement must be compensated to measure the power and related parameters accurately.

The phase setting of channels is configured by the PHASEn[9:0] bits in the CHn_CFG register corresponding to the channel whose phase adjustment is desired. The register value is a 10-bit two's complement value corresponding to the number of modulator clock cycles of phase offset compared to a reference phase of 0.

The mechanism for achieving phase adjustment derives from the ΔΣ architecture. The ΔΣ modulator produces samples continuously at the modulator frequency, f_{MOD}. These samples are filtered and decimated to the output data rate by the digital filter. The ratio between f_{MOD} and the data rate is the oversampling ratio (OSR). Each conversion result corresponds to an OSR number of modulator samples provided to the digital filter. When the different channels of the ADS131M04 have no programmed phase offset between them, the modulator clock cycles corresponding to the conversion results of the different channels are aligned in the time domain. Figure 12 shows an example scenario where the voltage input to channel 1 has no phase offset from channel 0.

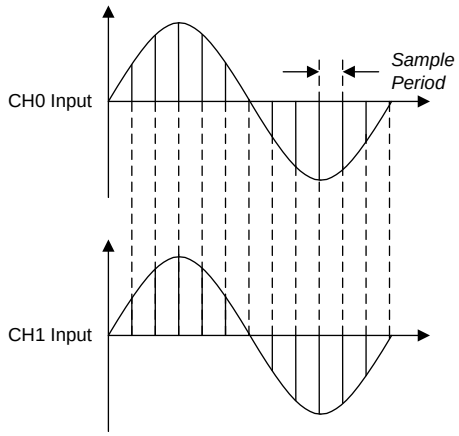

Figure 12. Two Channel Outputs With Equal Phase Settings

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However, the sample period of one channel can be shifted with respect to another. If the inputs to both channels are sinusoids of the same frequency and the samples for these channels are retrieved by the host at the same time, the effect is that the phase of the channel with the modified sample period appears *shifted*. Figure 13 shows how the period corresponding to the samples are shifted between channels. Figure 14 shows how the samples appear as having generated a phase shift when they are retrieved by the host.

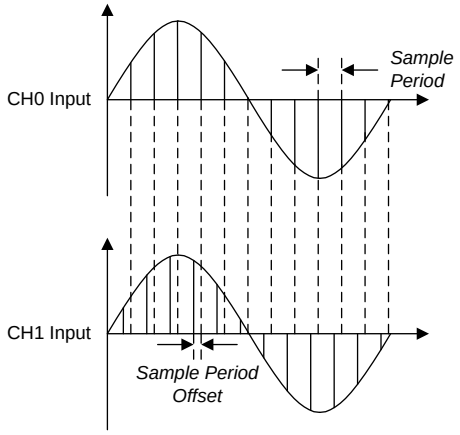

Figure 13. Channel 1 With a Positive Sample Phase Shift With Respect to Channel 0

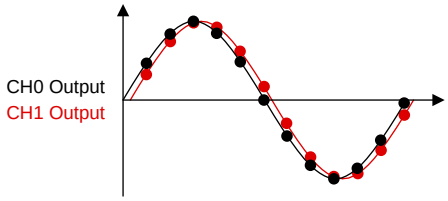

Figure 14. Channels 1 and 0 From the Perspective of the Host

The valid setting range is from –OSR / 2 to (OSR / 2) – 1, except for OSRs greater than 1024, where the phase calibration setting is limited to –512 to 511. If a value outside of –OSR / 2 and (OSR / 2) – 1 is programmed, the device internally clips the value to the nearest limit. For example, if the OSR setting is programmed to 64 and the PHASEn[9:0] bits are programmed to 0001100100b corresponding to 100 modulator clock cycles, the device adjusts the phase of the channel by 31 because that value is the upper limit of phase calibration for that OSR setting. Table 5 gives the range of phase calibration settings for various OSR settings.

Table 5. Phase Calibration Setting Limits for Different OSR Settings

OSR SETTING	PHASE OFFSET RANGE (t_{MOD})	PHASEn[9:0] BITS RANGE
128	–64 to 63	11 1100 0000b to 00 0011 1111b
256	–128 to 127	11 1000 0000b to 00 0111 1111b
512	–256 to 255	11 0000 0000b to 00 1111 1111b
1024	–512 to 511	10 0000 0000b to 01 1111 1111b
2048	–512 to 511	10 0000 0000b to 01 1111 1111b
4096	–512 to 511	10 0000 0000b to 01 1111 1111b
8192	–512 to 511	10 0000 0000b to 01 1111 1111b
16384	–512 to 511	10 0000 0000b to 01 1111 1111b

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To create a phase shift larger than half the sample period for OSRs less than 2048, create an integer multiple sample period phase shift by modifying the indexes of the data points between channels with respect to one another in software. Subsequently, use the internal phase calibration function on the ADS131M04 to create the remaining fractional sample period phase shift. For example, to create a phase shift of 2.25 samples between channels 0 and 1, create a phase shift of two samples by aligning sample N in the channel 0 output data stream with sample N+2 in the channel 1 output data stream in the host software. Make the remaining 0.25 sample adjustment using the ADS131M04 phase calibration function.

The phase calibration settings of the channels affect the timing of the data interrupt signal $\overline{\text{DRDY}}$. See the *Data Ready (DRDY)* section for more details regarding how phase calibration affects $\overline{\text{DRDY}}$.

8.3.10 Calibration Registers

The calibration registers allow for the automatic computation of calibrated ADC conversion results from pre-programmed values. The host can rely on the device to automatically correct for system gain and offset after the error correction terms are programmed into the corresponding device registers.

The offset calibration registers are used to correct for system offset error, otherwise known as *zero error*. Offset error corresponds to the ADC output when the input to the system is zero. The ADS131M04 corrects for offset errors by subtracting the contents of the OCALn[23:0] register bits in the CHn_OCAL_MSB and CHn_OCAL_LSB registers from the conversion result for that channel prior to delivering the channel data to the interface for retrieval by the host. There are separate CHn_OCAL_MSB and CHnOCAL_LSB registers for each channel, which allows separate offset calibration terms to be programmed for each channel. The contents of the OCALn[23:0] bits are interpreted by the device as 24-bit two's complement values, the form of which corresponds exactly to that of the ADC data.

The gain calibration registers are used to correct for system gain error. Gain error corresponds to the deviation of gain of the system from its ideal value. The ADS131M04 corrects for gain errors by multiplying the ADC conversion result by a value resulting from the contents of the GCALn[23:0] register bits in the CHn_GCAL_MSB and CHn_GCAL_LSB registers prior to delivering the conversion result to the interface for retrieval by the host. There are separate CHn_GCAL_MSB and CHn_GCAL_LSB registers for each channel, which allows separate gain calibration terms to be programmed for each channel. The contents of the GCALn[23:0] bits are interpreted by the device as 24-bit unsigned values corresponding to linear steps ranging from gains of 0 to $2 - (1 / 2^{23})$. Table 6 describes the relationship between the GCALn[23:0] bit values and the realized gain calibration factor.

Table 6. GCALn[23:0] Bit Mapping

GCALn[23:0] VALUE	GAIN CALIBRATION FACTOR
000000h	0
000001h	1.19×10^{-7}
800000h	1
FFFFFEh	$2 - 2.38 \times 10^{-7}$
FFFFFFh	$2 - 1.19 \times 10^{-7}$

The calibration registers do not need to be enabled because they are always in use. The OCALn[23:0] bits have a default value of 000000h resulting in no offset correction. Similarly, the GCALn[23:0] bits default to 800000h resulting in a gain calibration factor of 1.

Figure 15 shows a block diagram illustrating the mechanics of the calibration registers on one channel of the ADS131M04.

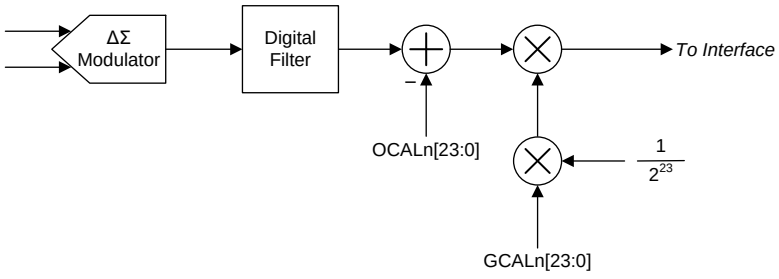

Figure 15. Calibration Block Diagram

8.3.11 Fast Startup

The ADS131M04 begins generating conversion data shortly after startup. This feature is useful for applications such as circuit breakers powered from the mains that require a fast determination of the input voltage soon after power is applied to the device. Fast startup is accomplished via two mechanisms. First, the device internal power-supply circuitry is designed specifically to enable fast startup. Second, the digital decimation filter dynamically switches from a fast-settling filter to a $sinc^3$ filter when the $sinc^3$ filter has had time to settle.

After supplies are ramped to 90% of their final value, the device requires t_{POR} for the internal circuitry to settle. The end of t_{POR} is indicated by a transition of $\overline{DRDY}$ from low to high. The transition of $\overline{DRDY}$ from low to high also indicates the SPI interface is ready to accept commands.

The $\Delta\Sigma$ modulators of the ADS131M04 begin sampling the input signal after a modulator settling time of $8 \times t_{MOD}$ following the end of t_{POR}. The device waits until CLKIN toggles after t_{POR} for the modulators to begin settling. Therefore, provide a valid clock signal on CLKIN as soon as possible after the supply ramp to achieve the fastest possible startup time.

The data generated by the $\Delta\Sigma$ modulators are fed to the digital filter blocks following the modulator settling. The data are provided to both the fast-settling filters and the $sinc^3$ filters. The fast-settling filter requires only one data rate period to provide settled data. Meanwhile, the $sinc^3$ filter requires three data rate periods to settle. The fast-settling filter generates the output data for the two interim ADC output samples indicated by $\overline{DRDY}$ transitioning from high to low when the $sinc^3$ filter is settling. The device disables the fast-settling filter and provides conversion data from the $sinc^3$ filter for the third and following samples.

The fast-settling filter provides conversion data that are significantly noisier than the data that comes from the $sinc^3$ filter, but allows the device to provide settled conversion data during the lengthy settling time of the more accurate $sinc^3$ digital filter. Figure 9 and Figure 11 compare the frequency domain transfer functions of the fast-settling filter to the $sinc^3$ filter. If the level of precision provided by the fast-settling filter is insufficient even for the first samples immediately following startup, ignore the first two instances of $\overline{DRDY}$ toggling from high to low and begin collecting data on the third instance.

8.3.11.1 Startup Following Reset

The startup process is similar following a RESET command or a pin reset using the $\overline{SYNC}/\overline{RESET}$ pin to what occurs at power up. There is no t_{POR} in the case of a command or pin reset because the supplies are already ramped. However, in either case, the device waits for the modulator settling time of $8 \times t_{MOD}$ before providing modulator samples to the two digital filters. The fast-settling filter is enabled for the first two output samples.

8.3.12 Communication Cyclic Redundancy Check (CRC)

The ADS131M04 features a cyclic redundancy check (CRC) engine on both input and output data to mitigate SPI communication errors. The CRC word is 16 bits wide for either input or output CRC. Coverage includes all words in the frame where the CRC occurs, including padded bits in a 32-bit word size.

Input CRC is optional and can be enabled and disabled by writing the RX_CRC_EN bit in the MODE register. Input CRC is disabled by default. The device checks the provided input CRC against the CRC generated based on the input data. A CRC error occurs if the CRC words do not match. The device does not execute any commands for a failed CRC check if the received command is anything other than WREG where the number of registers to write is more than 1. The device writes registers when the data are shifted into the device during a WREG command. Therefore, the registers are written before the input CRC is provided during a WREG command. The device sets the CRC_ERR bit in the STATUS register for all cases of a CRC error.

Output CRC is not optional and always appears at the end of the output frame. The host can ignore the data if output CRC is not used.

There are two types of CRC available: CCITT CRC and ANSI CRC (CRC-16). The CRC setting determines the algorithm for both the input and output CRC. The CRC type is programmed by the CRC_TYPE bit in the MODE register. Table 7 lists the details of the two CRC types.

Table 7. CRC Types

CRC TYPE	POLYNOMIAL	BINARY POLYNOMIAL
CCITT CRC	$x^{16} + x^{12} + x^5 + 1$	0001 0000 0010 0001
ANSI CRC	$x^{16} + x^{15} + x^2 + 1$	1000 0000 0000 0101

8.3.13 CRC Register Map

The ADS131M04 performs a CRC on its own register map as a means to check for unintended changes to the registers. Enable the CRC register map by setting the REG_CRC_EN bit in the MODE register. When enabled, the device constantly calculates the CRC register map using each bit in the writable register space.

The calculated CRC is a 16-bit value and is stored in the REGMAP_CRC register. The calculation is done using one register map bit per CLKIN period and constantly checks the result against the previous calculation. The REG_MAP bit in the STATUS register is set to flag the host if the CRC register map changes, including changes resulting from register writes. The bit is cleared by reading the STATUS register, or by the STATUS register being output as a response to the NULL command.

8.4 Device Functional Modes

Figure 16 shows a state diagram depicting the major functional modes of the ADS131M04 and the transitions between them.

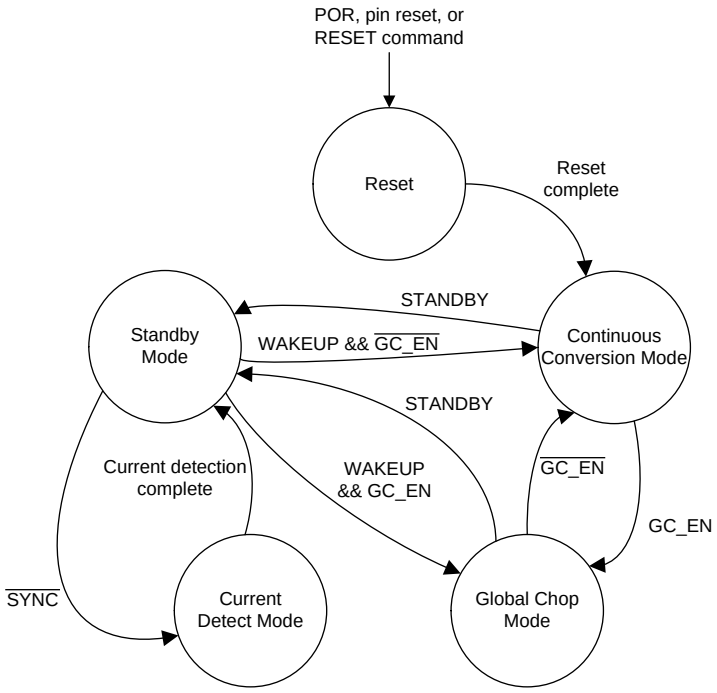

Figure 16. State Diagram Depicting Device Functional Modes

8.4.1 Power-Up and Reset

The ADS131M04 is reset in one of three ways: either by a power-on reset (POR), by the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin, or by a RESET command. After a reset occurs, the configuration registers are reset to the default values and the device begins generating conversion data as soon as they are available.

8.4.1.1 Power-On Reset

Power-on reset (POR) is the reset that occurs when a valid operating voltage is first applied to the supplies. The POR process requires t_{POR} from when the supply voltages reach 90% of their nominal value. Internal circuitry powers up and the registers are set to their default state during this time. The $\overline{\text{DRDY}}$ pin transitions from low to high immediately after t_{POR} indicating the SPI interface is ready for communication. The device ignores any SPI communication before this point.

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Device Functional Modes (continued)

8.4.1.2 $\overline{\text{SYNC}}/\overline{\text{RESET}}$ Pin

The $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin is an active low, dual-function pin that generates a reset if the pin is held low longer than $t_{w(RSL)}$. The device maintains a reset state until $\overline{\text{SYNC}}/\overline{\text{RESET}}$ is returned high. The host must wait for at least t_{REGACQ} after $\overline{\text{SYNC}}/\overline{\text{RESET}}$ is brought high for the registers to assume their default values before communicating with the device via SPI. Conversion data are generated immediately after the registers are reset to their default values, as described in the *Startup Following Reset* section.

8.4.1.3 RESET Command

The ADS131M04 can be reset via an SPI command (0011h). The device communicates in frames of a fixed length. See the *SPI Communication Frames* section for details regarding SPI data framing on the ADS131M04. The RESET command occurs in the first word of the data frame, but the command is not latched by the device until the entire frame is complete. Six words are required to complete a frame on the ADS131M04.

A reset occurs immediately after the command is latched. The host must wait for t_{REGACQ} before communicating with the device to ensure the registers have assumed their default settings. Conversion data are generated immediately after the registers are reset to their default values, as described in the *Startup Following Reset* section.

8.4.2 Conversion Modes

There are two ADC conversion modes on the ADS131M04: continuous conversion and global chop mode. Continuous conversion mode is a mode where ADC conversions are generated constantly by the ADC at a rate defined by f_{MOD} / OSR. Global chop mode differs from continuous conversion mode because global chop periodically chops (or swaps) the inputs, which reduces system offset errors at the cost of settling time between the points when the inputs are swapped. In either continuous conversion or global chop mode, there are three power modes that provide flexible options to scale power with bandwidth and dynamic range. The *Power Modes* section discusses these power modes in further detail.

8.4.2.1 Continuous Conversion Mode

Continuous conversion mode is the mode in which ADC data are generated constantly at the rate of f_{MOD} / OSR. New data are indicated by a $\overline{\text{DRDY}}$ falling edge at this rate. Continuous conversion mode is intended for measuring AC signals because this mode allows for higher output data rates than global chop mode.

8.4.2.2 Global Chop Mode

In global chop mode, the ADC swaps its inputs prior to generating each sample in order to reduce the offset error inherent to the inputs caused by slight mismatch in the internal circuitry. This mode is intended for applications that measure DC input signals resulting from very low offset errors introduced by the application.

This mode always uses the sinc^3 digital filter, which requires 3 × OSR / f_{MOD} to generate a settled result. Therefore, the device waits for 3 × OSR / f_{MOD} after the modulator begins sampling for the filter to settle before providing a sample result to the host.

The ADS131M04 allows a programmable delay between the end of the previous sample period and the beginning of the subsequent sample period after the inputs are chopped. This delay is to allow for the external input circuitry to settle because the chopping switches interface directly with the pins. The GC_DLY[3:0] bits in the CFG register configure the delay after chopping. The delay is measured in modulator clock periods from 2 to 65,536.

Phase calibration is automatically disabled in global chop mode. A $\overline{\text{DRDY}}$ falling edge is generated each time a new sample is generated. The test signal cannot be measured in global chop mode. Equation 7 describes the sample period in global chop mode.

$$t_{SAMPLE} = t_{GC\_DLY} + 3 \times OSR / f_{MOD} \quad (7)$$

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Device Functional Modes (continued)

8.4.2.3 Power Modes

In both continuous conversion and global chop modes, there are three selectable power modes that allow the scaling of power with bandwidth and performance: high-resolution (HR) mode, low-power (LP) mode, and very-low-power (VLP) mode. The mode is selected by the PWR[1:0] bits in the CLOCK register. See the *Recommended Operating Conditions* table for restrictions on the CLKIN frequency for each power mode.

8.4.3 Standby Mode

Standby mode is a low-power state in which all channels are disabled, and the reference and other non-essential circuitry are powered down. This mode differs from completely powering down the device because the device retains its register settings. Enter standby mode by sending the STANDBY command (0022h). Stop toggling CLKIN when the device is in standby mode to minimize device power consumption. Exit standby mode by sending the WAKEUP command (0033h). The device waits for $t_{MODSETTLE}$ before beginning conversions after exiting standby mode.

8.4.4 Current Detect Mode

Current detect mode is a special mode that is helpful for applications requiring tamper detection when the equipment is in a low-power state. In this mode, the ADS131M04 collects a configurable number of samples at 2.7 kSPS and compares the absolute value of the results to a programmable threshold. If a configurable number of results exceed the threshold, the host is notified via a DRDY falling edge and the device returns to standby mode. Enter current detect mode by providing a negative pulse on SYNC/RESET with a pulse duration less than t_{SRLRST} when in standby mode. Current detect mode can only be entered from standby mode.

The device uses a limited power operating mode to generate conversions in current detect mode. The conversion results are only used for comparison by the internal digital threshold comparator and are not accessible by the host. The device uses an internal oscillator that enables the device to capture the data without the use of the external clock input. Do not toggle CLKIN when in current detect mode to minimize device power consumption.

Current detect mode is configured in the CFG, THRSHLD_MSB, and THRSHLD_LSB registers. Enable and disable current detect mode by toggling the CD_EN bit in the CFG register. The THRSHLD_MSB and THRSHLD_LSB registers contain the CD_THRSH[23:0] bits that represent the digital comparator threshold value during current detection.

The programmable values in CD_NUM[2:0] configure the number of samples that must exceed the threshold for a detection to occur. The purpose of requiring multiple samples for detection is to control noisy values that may exceed the threshold, but do not represent a high enough power level to warrant action by the host. In summary, the conversion result must exceed the value programmed in CD_THRSH[23:0] a number of times as represented by the value stored in CD_NUM[2:0].

The number of samples used for current detection are programmed by the CD_LEN[2:0] bits in the CFG register. The number of samples used for current detection range from 128 to 3584.

The device can be configured to notify the host based on any of the results from either individual channels, all channels, or any combination of channels. The CD_ALLCH bit in the CFG register determines how many channels are required to exceed the programmed thresholds to trigger a current detection. When the bit is 1, all enabled channels are required to meet the current detection requirements in order for the host to be notified. If the bit is 0, any enabled channel triggers a current detection notification if the requirements are met. Enable and disable channels using the CHn_EN bits in the CLK register to control which combination of channels must meet the requirements to trigger a current detection notification.

Figure 17 illustrates a flow chart depicting the current detection process on the ADS131M04.

Device Functional Modes (continued)

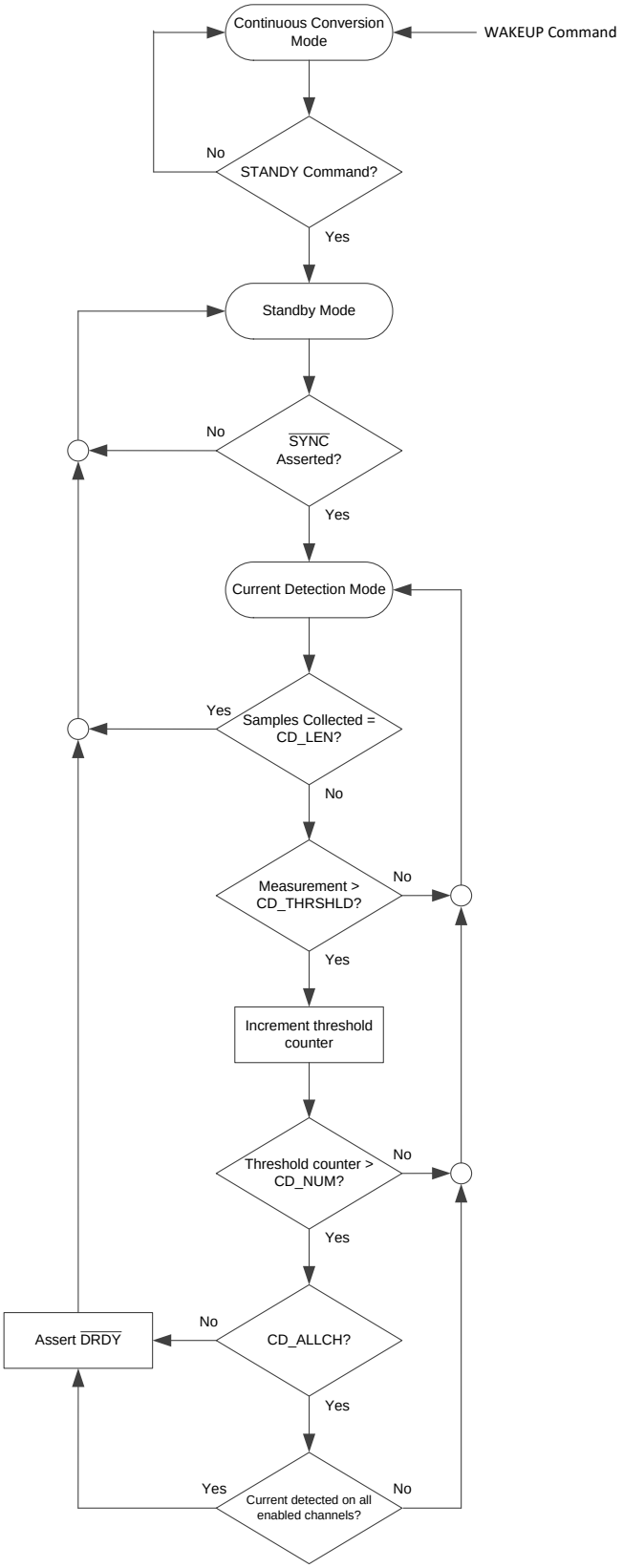

Figure 17. Current Detect Mode Flow Chart

8.5 Programming

8.5.1 Interface

The ADS131M04 uses an SPI-compatible interface to configure the device and retrieve conversion data. The device always acts as an SPI slave; SCLK and $\overline{CS}$ are inputs to the interface. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, the SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. The interface is full-duplex, meaning data can be sent and received simultaneously by the interface. The device includes the typical SPI signals: SCLK, $\overline{CS}$, DIN (MOSI), and DOUT (MISO). In addition, there are two other digital pins that provide additional functionality. The $\overline{DRDY}$ pin serves as a flag to the host to indicate new data. The $\overline{SYNC}/\overline{RESET}$ pin is a dual-function pin that allows synchronization of conversions to an external event and allows for a hardware device reset.

8.5.1.1 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin is an active low input signal that selects the device for communication. The device ignores any communication and DOUT is high impedance when $\overline{CS}$ is held high. Hold $\overline{CS}$ low for the duration of a communication frame to ensure proper communication. The interface is reset each time $\overline{CS}$ is taken high.

8.5.1.2 Serial Data Clock (SCLK)

The SCLK pin is an input that serves as the serial clock for the interface. Output data on the DOUT pin transition on the rising edge of SCLK and input data on DIN are latched on the falling edge of SCLK.

8.5.1.3 Serial Data Input (DIN)

The DIN pin is the master out, slave in (MOSI) pin for the device. Serial commands are shifted in through the DIN pin by the device with each SCLK falling edge when the $\overline{CS}$ pin is low.

8.5.1.4 Serial Data Output (DOUT)

The DOUT pin is the master in, slave out (MISO) pin for the device. The device shifts out command responses and ADC conversion data serially with each rising SCLK edge when the $\overline{CS}$ pin is low. This pin assumes a high-impedance state when $\overline{CS}$ is high.

8.5.1.5 Data Ready ($\overline{DRDY}$)

The $\overline{DRDY}$ pin is an active low output that indicates when new conversion data are ready in conversion mode or that the requirements are met for current detection when in current detect mode. Connect the $\overline{DRDY}$ pin to an input on the host to trigger periodic data retrieval in conversion mode. The period between each $\overline{DRDY}$ falling edge is the data rate period.

The timing of $\overline{DRDY}$ with respect to the sampling of a given channel on the ADS131M04 depends on the phase calibration setting of the channel and the state of the DRDY_SEL[1:0] bits in the MODE register. Setting the DRDY_SEL[1:0] bits to 00b configures $\overline{DRDY}$ to assert when the channel with the largest positive phase calibration setting, or the most lagging, has a new conversion result. When the bits are 01b, the device asserts $\overline{DRDY}$ each time any channel data are ready. Finally, setting the bits to either 10b or 11b configures the device to assert $\overline{DRDY}$ when the channel with the most negative phase calibration setting, or the most leading, has new conversion data. Changing the DRDY_SEL[1:0] bits has no effect on $\overline{DRDY}$ behavior in global chop mode because phase calibration is automatically disabled in global chop mode.

The DRDY_HIZ bit in the MODE register configures the state of the $\overline{DRDY}$ pin when deasserted. By default the bit is 0b, meaning the pin is actively driven high using a push-pull output stage. When the bit is 1b, $\overline{DRDY}$ behaves like an open-drain digital output. Use a 100-kΩ pullup resistor to pull the pin high when $\overline{DRDY}$ is not asserted.

The DRDY_FMT bit in the MODE register determines the format of the $\overline{DRDY}$ signal. When the bit is 0b, new data are indicated by $\overline{DRDY}$ changing from high to low and remaining low until either all of the conversion data are shifted out of the device, or remaining low and going high briefly before the next time $\overline{DRDY}$ transitions low. When the DRDY_FMT bit is 1b, new data are indicated by a short negative pulse on the $\overline{DRDY}$ pin. If the host does not read conversion data after the $\overline{DRDY}$ pulse when DRDY_FMT is 1b, the device skips a conversion result and does not provide another $\overline{DRDY}$ pulse until the second following instance when data are ready because of how the pulse is generated.

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Programming (continued)

8.5.1.6 Conversion Synchronization or System Reset ($\overline{SYNC}$/$\overline{RESET}$)

The $\overline{SYNC}$/$\overline{RESET}$ pin is a multi-function digital input pin that serves primarily to allow the host to synchronize conversions to an external process or to reset the device. See the *Synchronization* section for more details regarding the synchronization function. See the *SYNC/RESET Pin* section for more details regarding how the pin is reset.

8.5.1.7 SPI Communication Frames

SPI communication on the ADS131M04 is performed in frames. Each SPI communication frame consists of several words. The word size is configurable as either 16 bits, 24 bits, or 32 bits by programming the WLENGTH[1:0] bits in the MODE register.

The interface is full duplex, meaning that the interface is capable of transmitting data on DOUT while simultaneously receiving data on DIN. The input frame that the host writes on DIN always begins with a command. The first word on the output frame that the device writes on DOUT always begins with the response to the command that was written on the previous input frame. The number of words in a command depends on the command provided. For most commands, there are six words in a frame. On DIN, the host provides the command, the command CRC if input CRC is enabled or a word of zeros if input CRC is disabled, and four additional words of zeros. Simultaneously on DOUT, the device outputs the response from the previous frame command, four words of ADC data representing the four ADC channels, and a CRC word. Figure 18 shows a typical single word command frame structure.

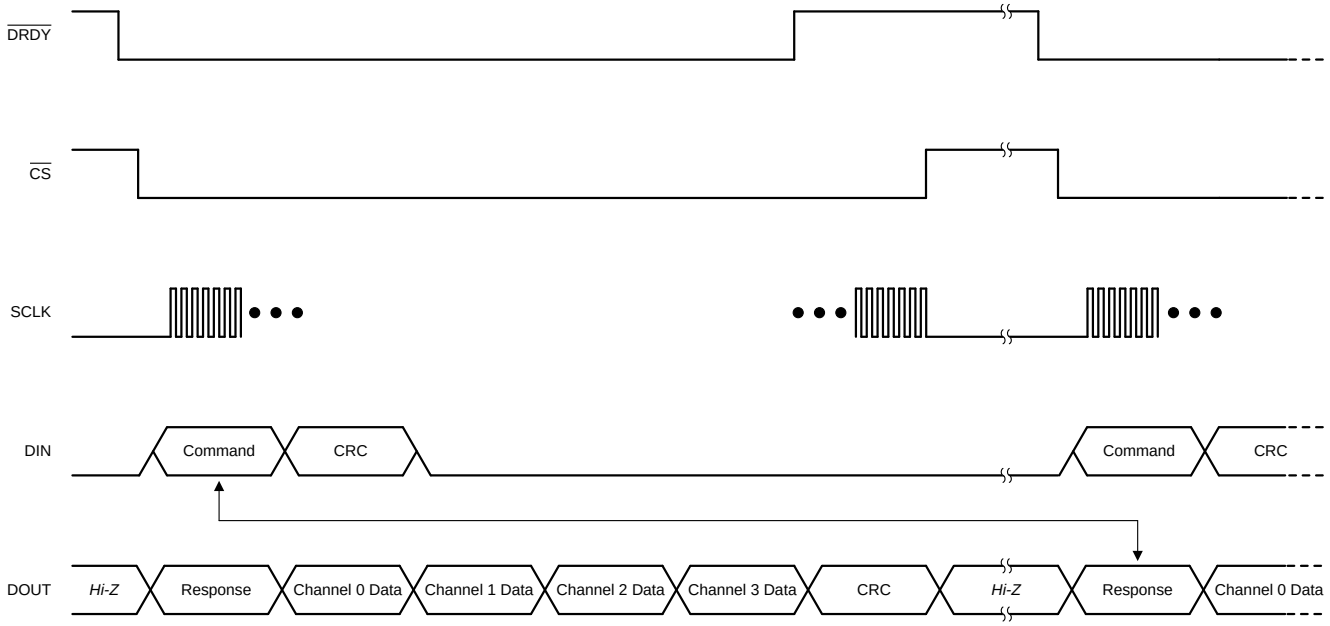

Figure 18. Typical Communication Frame

There are some commands that require more than six words. In the case of a read register (RREG) command where more than a single register is read, the response to the command contains the acknowledgment of the command followed by the register contents requested, which may require a larger frame depending on how many registers are read. See the *RREG* section for more details on the RREG command.

In the case of a write register (WREG) command where more than a single register is written, the frame extends to accommodate the additional data required to communicate the register data that is to be written. See the *WREG* section for more details on the WREG command.

See the *Commands* section for a list of all valid commands and their corresponding responses on the ADS131M04.

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Programming (continued)

8.5.1.8 SPI Communication Words

An SPI communication frame with the ADS131M04 is made of words. Words on DIN can contain commands, register settings during a register write, or a CRC of the input data. Words on DOUT can contain command responses, register settings during a register read, ADC conversion data, or CRC of the output data.

Words can be 16, 24, or 32 bits. The word size is configured by the WLENGTH[1:0] bits in the MODE register. The device defaults to a 24-bit word size. Commands, responses, CRC, and registers always contain 16 bits of actual data. These words are always most significant bit (MSB) aligned, and therefore the least significant bits (LSBs) are zero-padded to accommodate 24- or 32-bit word sizes. ADC conversion data are nominally 24 bits. The ADC data has its eight LSBs truncated when the device is configured for 16-bit communication. There are two options for 32-bit communication available for ADC data that are configured by the WLENGTH[1:0] bits in the MODE register. Either the ADC data can be LSB padded with zeros or the data can be MSB sign extended.

8.5.1.9 ADC Conversion Data

The device provides conversion data for each channel at the data rate. The time when data are available relative to $\overline{\text{DRDY}}$ asserting is determined by the channel phase calibration setting and the DRDY_SEL[1:0] bits in the MODE register when in continuous conversion mode. All data are available immediately following $\overline{\text{DRDY}}$ assertion in global chop mode. The conversion status of all channels is available as the DRDY[3:0] bits in the STATUS register. The STATUS register contents are automatically output as the response to the NULL command.

Conversion data are 24 bits. The data LSBs are truncated when the device operates with a 16-bit word size. The LSBs are zero padded or the MSBs sign extended when operating with a 32-bit word size by configuring the WLENGTH[1:0] bits in the MODE register.

Data iares given in binary two's complement. Use Equation 8 to calculate the size of one code (LSB).

$$1\ \text{LSB} = (2.4 / \text{Gain}) / 2^{24} = +\text{FSR} / 2^{23} \quad (8)$$

A positive full-scale input [$V_{IN} \geq (+\text{FSR} – 1\ \text{LSB}) = 1.2 / \text{Gain} – 1\ \text{LSB})$] produces an output code of 7FFFFFh and a negative full-scale input ($V_{IN} \leq –\text{FSR} = –1.2 / \text{Gain}$) produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale.

Table 8 summarizes the ideal output codes for different input signals.

Table 8. Ideal Output Code versus Input Signal

INPUT SIGNAL, $V_{IN} = V_{AINP} – V_{AINN}$	IDEAL OUTPUT CODE
≥ FSR ($2^{23} – 1$) / 2^{23}	7FFFFFh
FSR / 2^{23}	000001h
0	000000h
–FSR / 2^{23}	FFFFFFh
≤ –FSR	800000h

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Figure 19 shows the mapping of the analog input signal to the output codes.

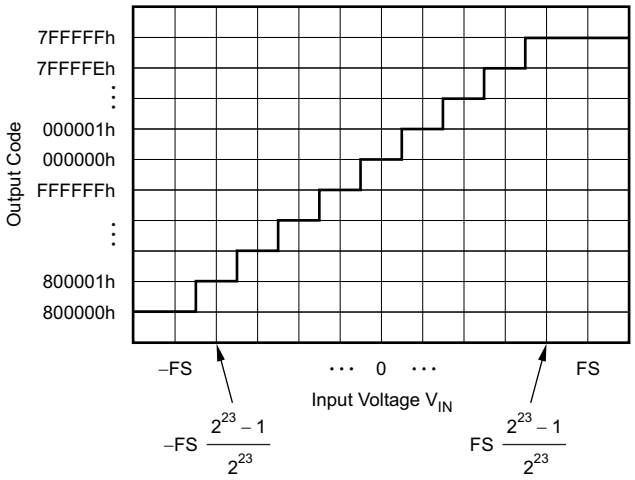

Figure 19. Code Transition Diagram

8.5.1.9.1 Collecting Data for the First Time or After a Pause in Data Collection

Take special precaution when collecting data for the first time or when beginning to collect data again after a pause. The internal mechanism that outputs data contains a first-in-first-out (FIFO) buffer that can store two samples of data per channel at a time. The DRDY flag for each channel in the STATUS register remains set until both samples for each channel are read from the device. This condition is not obvious under normal circumstances when the host is reading each consecutive sample from the device. In that case, the samples are cleared from the device each time new data are generated so the DRDY flag for each channel in the STATUS register is cleared with each read. However, both slots of the FIFO are full if a sample is missed or if data are not read for a period of time. Either strobe the SYNC/RESET pin to re-synchronize conversions and clear the FIFOs, or quickly read two data packets quickly when data are read for the first time or after a gap in reading data. This process ensures predictable DRDY pin behavior. See the *Synchronization* section for information about the synchronization feature. These methods do not need to be employed if each channel data was read for each output data period from when the ADC was enabled.

Figure 20 illustrates an example of how to collect data after a period of the ADC running, but where no data are being collected. In this instance, the SYNC/RESET pin is used to clear the internal FIFOs and realign the ADS131M04 output data with the host.

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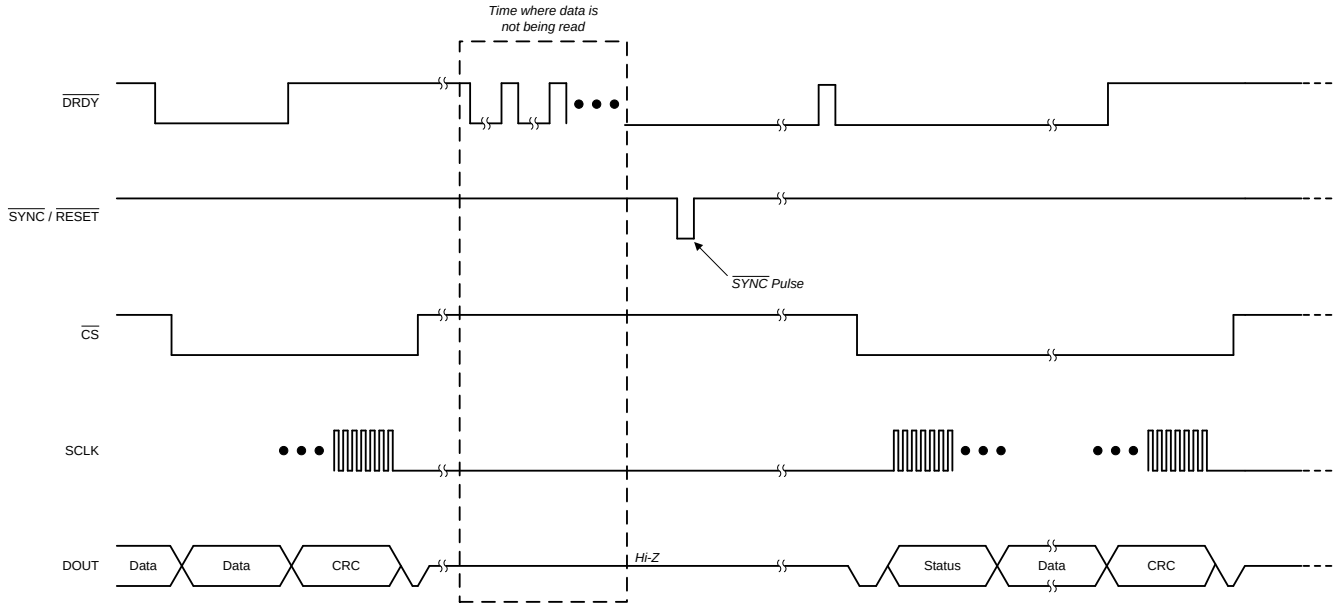

Figure 20. Collecting Data After a Hiatus Using the SYNC/RESET Pin

Another functionally equivalent method for clearing the FIFO after a hiatus in collecting data is to begin by reading two samples in quick succession. Figure 21 depicts this method. This example shows when the DRDY_FMT bit in the MODE register is set to 0 indicating DRDY is a level output. There is a very narrow pulse on DRDY immediately after the first set of data are shifted out of the device. This pulse may be too narrow for some microcontrollers to detect. Therefore, do not rely upon this pulse but instead immediately read out the second data set after the first data set. The host operates synchronous to the device after the second word is read from the device.

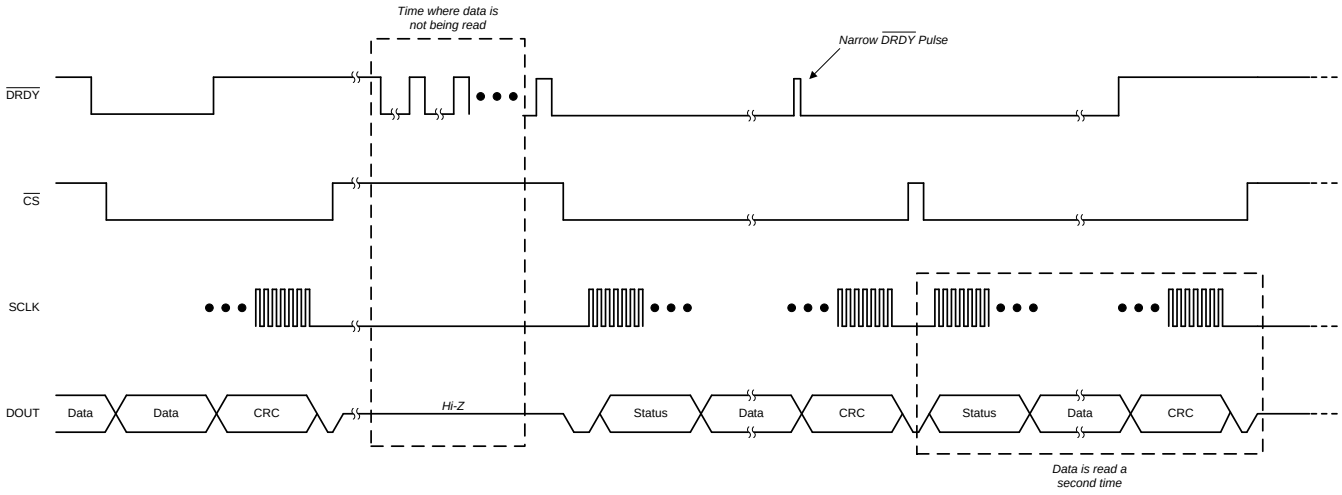

Figure 21. Collecting Data After a Hiatus by Reading Data Twice

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8.5.1.10 Commands

Table 9 contains a list of all valid commands, a short description of their functionality, their binary command word, and the expected response that appears in the following frame.

Table 9. Command Definitions

COMMAND	DESCRIPTION	COMMAND WORD	RESPONSE
NULL	No operation	0000 0000 0000 0000	STATUS register
RESET	Reset the device	0000 0000 0001 0001	1111 1111 0010 0100
RREG	Read nnn nnnn plus 1 registers beginning at address a aaaa a	101a aaaa annn nnnn	dddd dddd dddd dddd or 111a aaa annn nnnn(1)
WREG	Write nnn nnnn plus 1 registers beginning at address a aaaa a	011a aaaa annn nnnn	010a aaaa ammm mmmm(2)
STANDBY	Place the device into standby mode	0000 0000 0010 0010	0000 0000 0010 0010
WAKEUP	Wake the device from standby mode to conversion mode	0000 0000 0011 0011	0000 0000 0011 0011
LOCK	Lock the interface such that only the NULL, UNLOCK, and RREG commands are valid	0000 0101 0101 0101	0000 0101 0101 0101
UNLOCK	Unlock the interface after the interface is locked	0000 0110 0101 0101	0000 0110 0101 0101

(1) When nnn nnnn is 0, the response is the requested register data dddd dddd dddd dddd. When nnn nnnn is greater than 0, the response begins with 111a aaaa annn nnnn, followed by the register data.
(2) In this case mmm mmmm represents the number of registers that are actually written minus one. This value may be less than nnn nnnn in some cases.

8.5.1.10.1 NULL (0000 0000 0000 0000)

The NULL command is the *no-operation* command that results in no registers read or written, and the state of the device remains unchanged. The intended use case for the NULL command is during typical ADC data capture.

The command response for the NULL command is the contents of the STATUS register. Any invalid command also gives the NULL response.

8.5.1.10.2 RESET (0000 0000 0001 0001)

The RESET command resets the ADC to its register defaults. The command is latched by the device at the end of the frame. A reset occurs immediately after the command is latched. The host must wait for t_{REGACQ} before communicating with the device to ensure the registers have assumed their default settings. See the *RESET Command* section for more information regarding the operation of the reset command.

8.5.1.10.3 RREG (101a aaaa annn nnnn)

The RREG command allows device registers to be read. The binary format of the command word is 101a aaaa annn nnnn, where a aaaa a is the binary address of the register to begin reading and nnn nnnn is the unsigned binary number of consecutive registers to read minus one. There are two cases for reading registers on the ADS131M04. When reading a single register (nnn nnnn = 000 0000b), the device outputs the register contents in the command response word of the following frame. If multiple registers are read using a single command (nnn nnnn > 000 0000b), the device forgoes outputting the ADC conversion data and instead outputs the requested register data sequentially in order of addresses.

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8.5.1.10.3.1 Reading a Single Register

A single register is read from the device when nnn nnnn is specified as zero in the RREG command word. Like all SPI commands on the ADS131M04, the response occurs on the output in the frame following the command. Instead of a unique acknowledgment word, the response word is the contents of the register whose address is specified in the command word. Figure 22 shows an example of reading a single register.

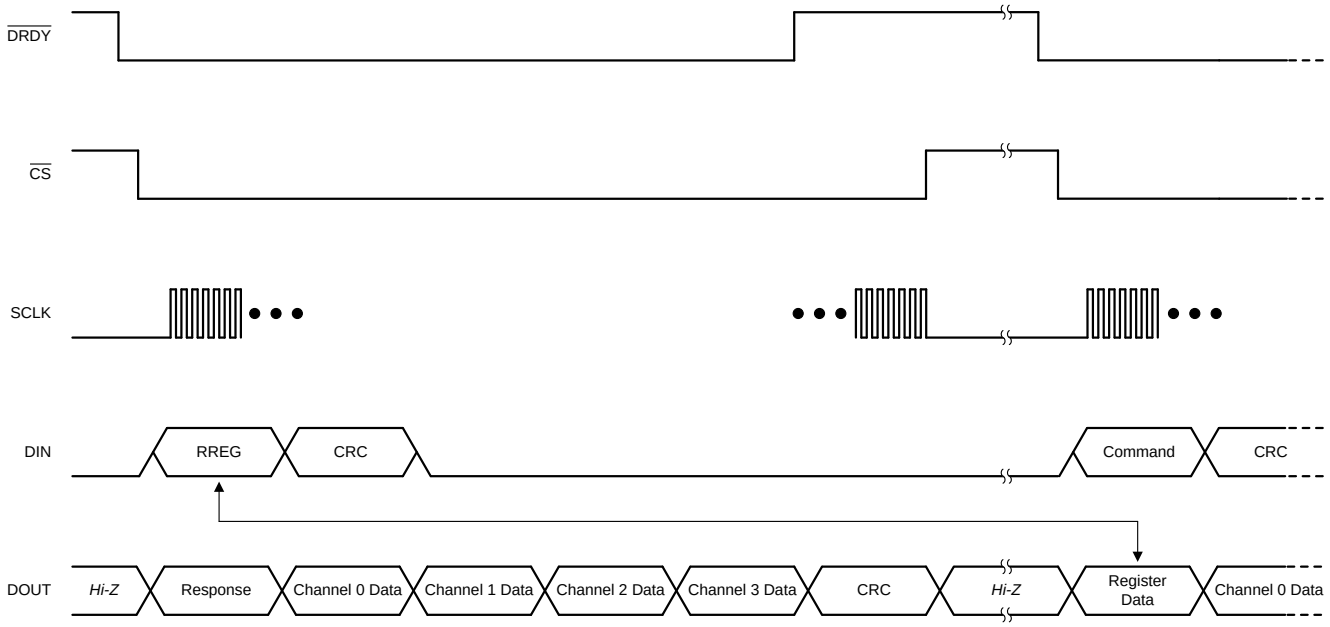

Figure 22. Reading a Single Register

8.5.1.10.3.2 Reading Multiple Registers

Multiple registers are read from the device when nnn nnnn is specified as a number greater than zero in the RREG command word. Like all SPI commands on the ADS131M04, the response occurs on the output in the frame following the command. Instead of a single acknowledgment word, the response spans multiple words in order to shift out all requested registers. Continue toggling SCLK to accommodate the entire data stream. ADC conversion data are not output in the frame following a command to read multiple registers. Figure 23 shows an example of reading multiple registers.

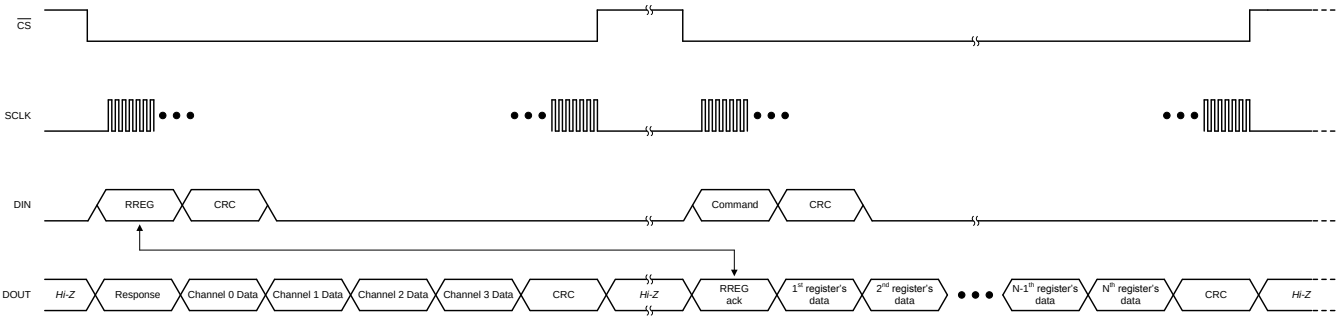

Figure 23. Reading Multiple Registers

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8.5.1.10.4 WREG (011a aaaa annn nnnn)

The WREG command allows writing an arbitrary number of contiguous device registers. The binary format of the command word is 011a aaaa annn nnnn, where a aaaa a is the binary address of the register to begin writing and nnn nnnn is the unsigned binary number of consecutive registers to write minus one. Insert the data to be written immediately following the command word. Write the intended contents of each register into individual words, MSB aligned.

If the input CRC is enabled, write this CRC at the end of the frame. The registers are written to the device as they are shifted into DIN. Therefore, a CRC error does not prevent an erroneous value from being written to a register. An input CRC error during a WREG command causes the CRC_ERR bit in the STATUS register to be set.

The device ignores writes to read-only registers or to out-of-bounds addresses. Gaps in the register map address space are still included in the parameter nnn nnnn, but are not writeable so no change is made to them. The response to the WREG command that occurs in the following frame appears as 010a aaaa ammm mmmm where mmm mmmm is the number of registers actually written minus one. This number can be checked by the host against nnn nnnn to ensure the expected number of registers are written.

Figure 24 shows a typical WREG sequence. In this example, the number of registers to write is larger than the number of ADC channels and, therefore, the frame is extended beyond the ADC channels and output CRC word. Extend the frame to complete shifting out the ADC data output and output CRC when the host writes fewer registers than the number of ADC channels.

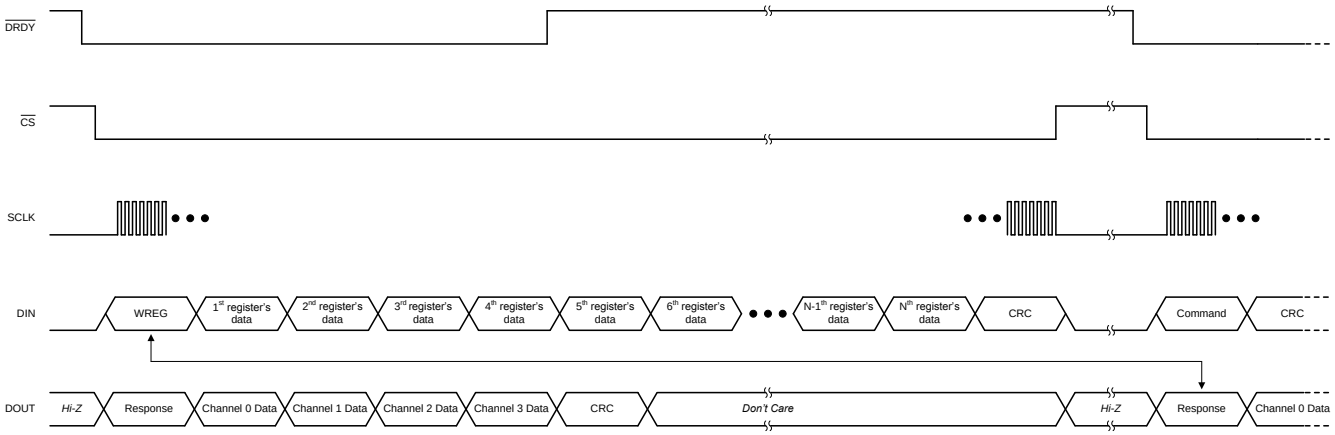

Figure 24. Writing Registers

8.5.1.10.5 STANDBY (0000 0000 0010 0010)

The STANDBY command places the device in a low-power standby mode. The command is latched by the device at the end of the frame. The device enters standby mode immediately after the command is latched. See the *Standby Mode* section for more information about standby mode. This command has no effect if the device is already in STANDBY mode.

8.5.1.10.6 WAKEUP (0000 0000 0011 0011)

The WAKEUP command returns the device to conversion mode from standby mode. This command has no effect if the device is already in conversion mode.

8.5.1.10.7 LOCK (0000 0101 0101 0101)

The LOCK command locks the interface, preventing the device from accidentally latching unwanted commands that can change the state of the device. When the interface is locked, the device only responds to the NULL, RREG, and UNLOCK commands. The device continues to output conversion data during this time.

8.5.1.10.8 UNLOCK (0000 0110 0110 0110)

The UNLOCK command unlocks the interface that was locked by the LOCK command.

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8.5.1.11 Short SPI Frames

The SPI frame can be shortened to only send commands and receive responses if the ADCs are disabled and no ADC data are being output by the device. Read out all of the expected output data words from each sample period if the ADCs are enabled. Reading all of the data output with each frame ensures predictable $\overline{\text{DRDY}}$ pin behavior. If reading out all the data on each output data period is not feasible, see the *Collecting Data for the First Time or After a Pause in Data Collection* section on how to begin reading data again after a pause from when the ADCs were last enabled.

8.5.2 Synchronization

Synchronization can be performed by the host to ensure the ADC conversions are synchronized to an external event. For example, synchronization can realign the data capture to the expected timing of the host if a glitch on the clock causes the host and device to become out of synchronization. Synchronization is not available in global chop mode.

Provide a negative pulse on the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin whose duration is less than t_{SRLRST} but greater than a CLKIN period to use the synchronization feature. The device internally compares the leading negative edge of the pulse to its internal clock that tracks the data rate. The internal data rate clock has timing equivalent to the $\overline{\text{DRDY}}$ pin if configured to assert with a phase calibration setting of 0b. If the negative edge on $\overline{\text{SYNC}}/\overline{\text{RESET}}$ aligns with the internal data rate clock, the device is determined to be synchronized and therefore no action is taken. If there is misalignment, the digital filters on the device are reset to be synchronized with the pulse.

The phase calibration settings on all channels are retained during synchronization. Thus, channels with non-zero phase calibration settings generate conversion results less than a data rate period after the synchronization event occurs. However, the results can be corrupted and are not settled until the respective channels have at least three conversion cycles for the sinc^3 filter to settle.

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8.6 Registers

Table 10 lists the memory-mapped registers for the ADS131M04 registers. Consider any register offset addresses not listed in Table 10 as reserved locations and therefore do not modify the register contents of these registers.

Table 10. ADS131M04 Registers

Address	Acronym	Register Name	Section
0h	ID	ID register	ID Register (Address = 0h) [reset = 2400h]
1h	STATUS	Status register	STATUS Register (Address = 1h) [reset = 500h]
2h	MODE	Mode register	MODE Register (Address = 2h) [reset = 510h]
3h	CLOCK	Clock register	CLOCK Register (Address = 3h) [reset = F0Eh]
4h	GAIN1	Gain register	GAIN1 Register (Address = 4h) [reset = 0h]
5h	RESERVED	Reserved register	RESERVED Register (Address = 05h) [reset = 0h]
6h	CFG	Configuration register	CFG Register (Address = 6h) [reset = 600h]
7h	THRSHLD_MSB	Threshold MSB register	THRSHLD_MSB Register (Address = 7h) [reset = 0h]
8h	THRSHLD_LSB	Threshold LSB register	THRSHLD_LSB Register (Address = 8h) [reset = 0h]
9h	CH0_CFG	Channel 0 configuration register	CHn_CFG Register (Address = 9h, Eh, 13h, 18h) [reset = 0h]
Ah	CH0_OCAL_MSB	Channel 0 offset calibration MSB register	CHn_OCAL_MSB Register (Address = Ah, Fh, 14h, 19h) [reset = 0h]
Bh	CH0_OCAL_LSB	Channel 0 offset calibration LSB register	CHn_OCAL_LSB Register (Address = Bh, 10h, 15h, 1Ah) [reset = 0h]
Ch	CH0_GCAL_MSB	Channel 0 gain calibration MSB register	CHn_GCAL_MSB Register (Address = Ch, 11h, 16h, 1Bh) [reset = 0h]
Dh	CH0_GCAL_LSB	Channel 0 gain calibration LSB register	CHn_GCAL_LSB Register (Address = Dh, 12h, 17h, 1Ch) [reset = 0h]
Eh	CH1_CFG	Channel 1 configuration register	CHn_CFG Register (Address = 9h, Eh, 13h, 18h) [reset = 0h]
Fh	CH1_OCAL_MSB	Channel 1 offset calibration MSB register	CHn_OCAL_MSB Register (Address = Ah, Fh, 14h, 19h) [reset = 0h]

Table 10. ADS131M04 Registers (continued)

Address	Acronym	Register Name	Section
10h	CH1_OCAL_LSB	Channel 1 offset calibration LSB register	CHn_OCAL_LSB Register (Address = Bh, 10h, 15h, 1Ah) [reset = 0h]
11h	CH1_GCAL_MSB	Channel 1 gain calibration MSB register	CHn_GCAL_MSB Register (Address = Ch, 11h, 16h, 1Bh) [reset = 0h]
12h	CH1_GCAL_LSB	Channel 1 gain calibration LSB register	CHn_GCAL_LSB Register (Address = Dh, 12h, 17h, 1Ch) [reset = 0h]
13h	CH2_CFG	Channel 2 configuration register	CHn_CFG Register (Address = 9h, Eh, 13h, 18h) [reset = 0h]
14h	CH2_OCAL_MSB	Channel 2 offset calibration MSB register	CHn_OCAL_MSB Register (Address = Ah, Fh, 14h, 19h) [reset = 0h]
15h	CH2_OCAL_LSB	Channel 2 offset calibration LSB register	CHn_OCAL_LSB Register (Address = Bh, 10h, 15h, 1Ah) [reset = 0h]
16h	CH2_GCAL_MSB	Channel 2 gain calibration MSB register	CHn_GCAL_MSB Register (Address = Ch, 11h, 16h, 1Bh) [reset = 0h]
17h	CH2_GCAL_LSB	Channel 2 gain calibration LSB register	CHn_GCAL_LSB Register (Address = Dh, 12h, 17h, 1Ch) [reset = 0h]
18h	CH3_CFG	Channel 3 configuration register	CHn_CFG Register (Address = 9h, Eh, 13h, 18h) [reset = 0h]
19h	CH3_OCAL_MSB	Channel 3 offset calibration MSB register	CHn_OCAL_MSB Register (Address = Ah, Fh, 14h, 19h) [reset = 0h]
1Ah	CH3_OCAL_LSB	Channel 3 offset calibration LSB register	CHn_OCAL_LSB Register (Address = Bh, 10h, 15h, 1Ah) [reset = 0h]
1Bh	CH3_GCAL_MSB	Channel 3 gain calibration MSB register	CHn_GCAL_MSB Register (Address = Ch, 11h, 16h, 1Bh) [reset = 0h]
1Ch	CH3_GCAL_LSB	Channel 3 gain calibration LSB register	CHn_GCAL_LSB Register (Address = Dh, 12h, 17h, 1Ch) [reset = 0h]
3Eh	REGMAP_CRC	CRC register map register	REGMAP_CRC Register (Address = 3Eh) [reset = 0h]
3Fh	RESERVED	Reserved register	RESERVED Register (Address = 3Fh) [reset = 0h]

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Complex bit access types are encoded to fit into small table cells. Table 11 shows the codes that are used for access types in this section.

Table 11. ADS131M04 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value.
Register Array Variables		
n		When this variable is used in a register name, an offset, or an address, this variable refers to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.

8.6.1 ID Register (Address = 0h) [reset = 2400h]

The ID register is shown in Figure 25 and described in Table 12.

Return to Summary Table.

Figure 25. ID Register

15	14	13	12	11	10	9	8
RESERVED			RESERVED	CHANCNT			
R-1h			R-0h	R-4h			
7	6	5	4	3	2	1	0
REVID							
R-0h							

Table 12. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	1h	Reserved
12	RESERVED	R	0h	Reserved
11:8	CHANCNT	R	4h	Channel count, always reads 4h
7:0	REVID	R	0h	Revision ID

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8.6.2 STATUS Register (Address = 1h) [reset = 500h]

The STATUS register is shown in Figure 26 and described in Table 13.

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Figure 26. STATUS Register

15	14	13	12	11	10	9	8
LOCK	F_RESYNC	REG_MAP	CRC_ERR	CRC_TYPE	RESET	WLENGTH	
R-0h	R-0h	R-0h	R-0h	R-0h	R-1h	R-1h	
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	DRDY3	DRDY2	DRDY1	DRDY0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-1h	R-0h

Table 13. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LOCK	R	0h	SPI interface lock indicator. 0b = Unlocked (default) 1b = Locked
14	F_RESYNC	R	0h	ADC resynchronization fault indicator. 0b = No fault (default) 1b = Fault occurred
13	REG_MAP	R	0h	Register map CRC fault. 0b = No change in the register map CRC (default) 1b = Register map CRC changed
12	CRC_ERR	R	0h	SPI input CRC error indicator. 0b = No CRC error (default) 1b = Input CRC error occurred
11	CRC_TYPE	R	0h	CRC type. 0b = 16-bit CCITT (default) 1b = 16-bit ANSI
10	RESET	R	1h	Reset status. 0b = No reset 1b = Reset occurred (default)
9:8	WLENGTH	R	1h	Data word length. 0b = 16 bits 1b = 24 bits (default) 10b = 32 bits: LSB zero padding 11b = 32 bits: MSB sign extension
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	DRDY3	R	0h	Channel 3 ADC data available indicator. 0b = No new data are available 1b = New data are available
2	DRDY2	R	0h	Channel 2 ADC data available indicator. 0b = No new data are available 1b = New data are available

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Table 13. STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DRDY1	R	1h	Channel 1 ADC data available indicator. 0b = No new data are available 1b = New data are available
0	DRDY0	R	0h	Channel 0 ADC data available indicator. 0b = No new data are available 1b = New data are available

8.6.3 MODE Register (Address = 2h) [reset = 510h]

The MODE register is shown in Figure 27 and described in Table 14.

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Figure 27. MODE Register

15	14	13	12	11	10	9	8
RESERVED		REG_CRC_EN	RX_CRC_EN	CRC_TYPE	RESET	WLENGTH	
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	
7	6	5	4	3	2	1	0
RESERVED		RESERVED	TIMEOUT	DRDY_SEL		DRDY_HiZ	DRDY_FMT
R/W-0h		R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h

Table 14. MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	0h	Reserved
13	REG_CRC_EN	R/W	0h	CRC register map enable. 0b = CRC register map disabled (default) 1b = CRC register map enabled
12	RX_CRC_EN	R/W	0h	SPI input CRC enable. 0b = Disabled (default) 1b = Enabled
11	CRC_TYPE	R/W	0h	SPI input and output, CRC register map type. 0b = 16-bit CCITT (default) 1b = 16-bit ANSI
10	RESET	R/W	1h	Reset. 0b = No reset, write to clear in STATUS register 1b = Reset occurred (default), no effect if written
9:8	WLENGTH	R/W	1h	Data word length. 0b = 16 bits 1b = 24 bits (default) 10b = 32 bits: LSB zero padding 11b = 32 bits: MSB sign extension
7:6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	TIMEOUT	R/W	1h	SPI timeout enable. 0b = Disabled 1b = Enabled (default)
3:2	DRDY_SEL	R/W	0h	$\overline{\text{DRDY}}$ pin signal source selection. 0b = Most lagging enabled channel (default) 1b = Logic OR of all enabled channels 10b = Most leading enabled channel 11b = Most leading enabled channel
1	DRDY_HiZ	R/W	0h	$\overline{\text{DRDY}}$ pin state when conversion data are not available. 0b = Logic high (default) 1b = High impedance
0	DRDY_FMT	R/W	0h	$\overline{\text{DRDY}}$ signal format when conversion data are available. 0b = Logic low (default) 1b = Negative pulse with a fixed duration

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8.6.4 CLOCK Register (Address = 3h) [reset = F0Eh]

The CLOCK register is shown in Figure 28 and described in Table 15.

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Figure 28. CLOCK Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	CH3_EN	CH2_EN	CH1_EN	CH0_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	OSR			PWR	
R/W-0h	R/W-0h	R/W-0h	R/W-3h			R/W-2h	

Table 15. CLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	CH3_EN	R/W	0h	Enable channel 3 ADC. 0b = Disabled 1b = Enabled (default)
10	CH2_EN	R/W	0h	Enable channel 2 ADC. 0b = Disabled 1b = Enabled (default)
9	CH1_EN	R/W	0h	Enable channel 1 ADC. 0b = Disabled 1b = Enabled (default)
8	CH0_EN	R/W	0h	Enable channel 0 ADC. 0b = Disabled 1b = Enabled (default)
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4:2	OSR	R/W	3h	The oversampling ratio of the modulator for a 4- and 8-channel silicon. 0b = 128 1b = 256 10b = 512 11b = 1024 (default) 100b = 2048 101b = 4096 110b = 8192 111b = 16384
1:0	PWR	R/W	2h	Power modes. 0b = Very-low-power 1b = Low-power 10b = High-resolution (default) 11b = High-resolution

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8.6.5 GAIN1 Register (Address = 4h) [reset = 0h]

The GAIN1 register is shown in Figure 29 and described in Table 16.

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Figure 29. GAIN1 Register

15	14	13	12	11	10	9	8
RESERVED	PGAGAIN3			RESERVED	PGAGAIN2		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	PGAGAIN1			RESERVED	PGAGAIN0		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

Table 16. GAIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved
14:12	PGAGAIN3	R/W	0h	PGA gain for channel 3. 0b = Gain of 1 (default) 1b = Gain of 2 10b = Gain of 4 11b = Gain of 8 100b = Gain of 16 101b = Gain of 32 110b = Gain of 64 111b = Gain of 128
11	RESERVED	R/W	0h	Reserved
10:8	PGAGAIN2	R/W	0h	PGA gain for channel 2. 0b = Gain of 1 (default) 1b = Gain of 2 10b = Gain of 4 11b = Gain of 8 100b = Gain of 16 101b = Gain of 32 110b = Gain of 64 111b = Gain of 128
7	RESERVED	R/W	0h	Reserved
6:4	PGAGAIN1	R/W	0h	PGA gain for channel 1. 0b = Gain of 1 (default) 1b = Gain of 2 10b = Gain of 4 11b = Gain of 8 100b = Gain of 16 101b = Gain of 32 110b = Gain of 64 111b = Gain of 128
3	RESERVED	R/W	0h	Reserved

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Table 16. GAIN1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	PGAGAIN0	R/W	0h	PGA gain for channel 0. 0b = Gain of 1 (default) 1b = Gain of 2 10b = Gain of 4 11b = Gain of 8 100b = Gain of 16 101b = Gain of 32 110b = Gain of 64 111b = Gain of 128

8.6.6 RESERVED Register (Address = 05h) [reset = 0h]

The RESERVED register is shown in Figure 30 and described in Table 17.

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Figure 30. RESERVED Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0h															

Table 17. RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	0h	Reserved. Only write 0000h to this register.

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8.6.7 CFG Register (Address = 6h) [reset = 600h]

The CFG register is shown in Figure 31 and described in Table 18.

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Figure 31. CFG Register

15	14	13	12	11	10	9	8
RESERVED			GC_DLY				GC_EN
R/W-0h			R/W-3h				R/W-0h
7	6	5	4	3	2	1	0
CD_ALLCH	CD_NUM			CD_LEN			CD_EN
R/W-0h	R/W-0h			R/W-0h			R/W-0h

Table 18. CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R/W	0h	Reserved
12:9	GC_DLY	R/W	3h	Global chop delay in the modulator clock periods before measurement begins. 0b = 2 1b = 4 10b = 8 11b = 16 (default) 100b = 32 101b = 64 110b = 128 111b = 256 1000b = 512 1001b = 1024 1010b = 2048 1011b = 4096 1100b = 8192 1101b = 16384 1110b = 32768 1111b = 65536
8	GC_EN	R/W	0h	Global chop enable. 0b = Disabled (default) 1b = Enabled
7	CD_ALLCH	R/W	0h	Current-detect channels required to trigger a detect. 0b = Any channel (default) 1b = All channels
6:4	CD_NUM	R/W	0h	Number of current-detect exceeded thresholds required to trigger a detection. 0b = 1 (default) 1b = 2 10b = 4 11b = 8 100b = 16 101b = 32 110b = 64 111b = 128

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Table 18. CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:1	CD_LEN	R/W	0h	Current-detect measurement length in conversion periods. 0b = 128 (default) 1b = 256 10b = 512 11b = 768 100b = 1280 101b = 1792 110b = 2560 111b = 3584
0	CD_EN	R/W	0h	Current-detect mode enable. 0b = Disabled (default) 1b = Enabled

8.6.8 THRSHLD_MSB Register (Address = 7h) [reset = 0h]

The THRSHLD_MSB register is shown in Figure 32 and described in Table 19.

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Figure 32. THRSHLD_MSB Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CD_TH_MSB															
R/W-0h															

Table 19. THRSHLD_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CD_TH_MSB	R/W	0h	Current-detect mode threshold MSB.

8.6.9 THRSHLD_LSB Register (Address = 8h) [reset = 0h]

The THRSHLD_LSB register is shown in Figure 33 and described in Table 20.

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Figure 33. THRSHLD_LSB Register

15	14	13	12	11	10	9	8
CD_TH_LSB							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 20. THRSHLD_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	CD_TH_LSB	R/W	0h	Current-detect mode threshold LSB.
7:0	RESERVED	R	0h	Reserved

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8.6.10 CHn_CFG Register (Address = 9h, Eh, 13h, 18h) [reset = 0h]

The CHn_CFG register is shown in Figure 34 and described in Table 21.

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Figure 34. CHn_CFG Register

15	14	13	12	11	10	9	8
PHASEn							
R/W-0h							
7	6	5	4	3	2	1	0
PHASEn		RESERVED				MUXn	
R/W-0h		R-0h				R/W-0h	

Table 21. CH0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	PHASEn	R/W	0h	Channel n phase delay.
5:2	RESERVED	R	0h	Reserved
1:0	MUXn	R/W	0h	Channel n input select. 0b = AINnP and AINnN (default) 1b = ADC inputs shorted 10b = DC diagnostic signal 10b = Do not use

8.6.11 CHn_OCAL_MSB Register (Address = Ah, Fh, 14h, 19h) [reset = 0h]

The CHn_OCAL_MSB register is shown in Figure 35 and described in Table 22.

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Figure 35. CHn_OCAL_MSB Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OCALn_MSB															
R/W-0h															

Table 22. CH0_OCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OCALn_MSB	R/W	0h	Channel n offset calibration register bits [23:8].

8.6.12 CHn_OCAL_LSB Register (Address = Bh, 10h, 15h, 1Ah) [reset = 0h]

The CHn_OCAL_LSB register is shown in Figure 36 and described in Table 23.

Return to Summary Table.

Figure 36. CHn_OCAL_LSB Register

15	14	13	12	11	10	9	8
OCALn_LSB							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 23. CHn_OCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	OCALn_LSB	R/W	0h	Channel n offset calibration register bits [7:0].
7:0	RESERVED	R	0h	Reserved

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8.6.13 CHn_GCAL_MSB Register (Address = Ch, 11h, 16h, 1Bh) [reset = 0h]

The CHn_GCAL_MSB register is shown in Figure 37 and described in Table 24.

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Figure 37. CHn_GCAL_MSB Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GCALn_MSB															
R/W-80h															

Table 24. CHn_GCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	GCALn_MSB	R/W	80h	Channel n gain calibration register bits [23:8].

8.6.14 CHn_GCAL_LSB Register (Address = Dh, 12h, 17h, 1Ch) [reset = 0h]

The CHn_GCAL_LSB register is shown in Figure 38 and described in Table 25.

Return to Summary Table.

Figure 38. CHn_GCAL_LSB Register

15	14	13	12	11	10	9	8
GCALn_LSB							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 25. CH0_GCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	GCALn_LSB	R/W	0h	Channel n gain calibration register bits [7:0].
7:0	RESERVED	R	0h	Reserved

8.6.15 REGMAP_CRC Register (Address = 3Eh) [reset = 0h]

The REGMAP_CRC register is shown in Figure 39 and described in Table 26.

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Figure 39. REGMAP_CRC Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG_CRC															
R-0h															

Table 26. REGMAP_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	REG_CRC	R	0h	CRC register map.

8.6.16 RESERVED Register (Address = 3Fh) [reset = 0h]

The RESERVED register is shown in Figure 40 and described in Table 27.

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Figure 40. RESERVED Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-0h															

Table 27. RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	0h	Reserved

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Unused Inputs and Outputs

Leave any unused analog inputs floating or connected to AVSS.

Do not float unused digital inputs because excessive power-supply leakage current can result. Tie all unused digital inputs to the appropriate levels, DVDD or DGND. Leave the $\overline{\text{DRDY}}$ pin unconnected if unused.

9.1.2 Power Metrology Applications

Each channel of the ADS131M04 is identical, giving designers the flexibility to sense voltage or current with any channel. Simultaneous sampling allows the application to calculate instantaneous power for any simultaneous voltage and current measurement. This section provides several diagrams depicting the common energy metrology configuration that can be used with the ADS131M04.

Figure 41 shows a two-phase (or split phase) metrology front that uses current transformers (CTs) to measure the current on two live phases and two dividers to measure the voltage between the live phases and neutral. Figure 42 shows a configuration similar to Figure 41, but where the voltage is measured between the phases and the neutral current is measured directly with a CT.

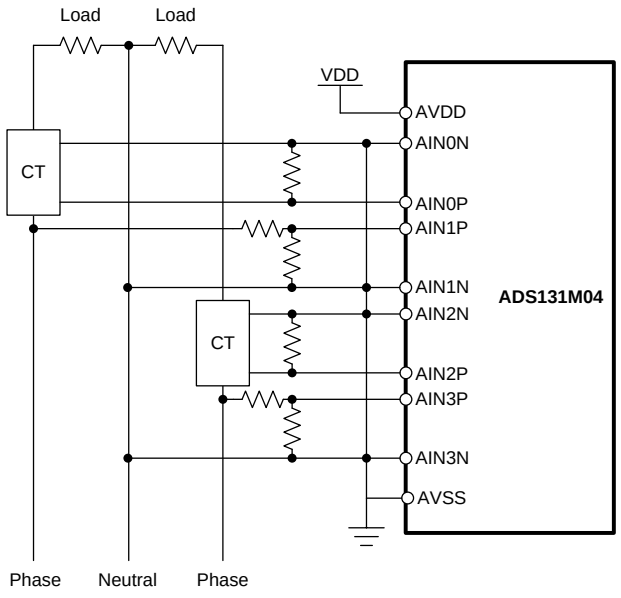

Figure 41. Two-Phase CTs for Live Currents, With Voltages Measured to Neutral

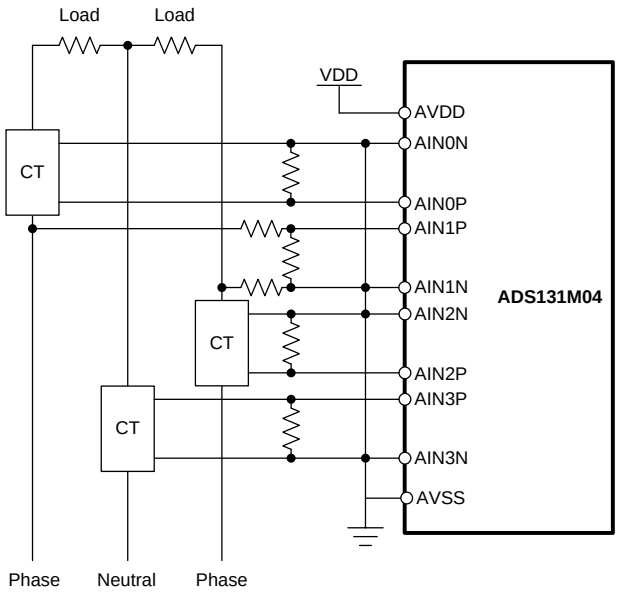

Figure 42. Two-Phase CTs for Live, Neutral Currents, With Voltages Measured Between Phases

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Application Information (continued)

Figure 43 shows a single phase configuration where live and neutral currents are monitored using CTs, the live phase voltage is measured using a voltage divider, and the final channel is used for an auxiliary measurement. This auxiliary measurement can be temperature if connected to an external thermocouple, thermistor, or other voltage output temperature sensor. Otherwise this measurement can sense any other signal that requires monitoring on the board. Figure 44 is similar to Figure 43 but shows a configuration where the live current is measured using a shunt and the neutral current is measured using a CT. This circuit requires that the ADS131M04 ground must float with the phase voltage. The phase voltage is measured using a voltage divider, but the higher resistor voltage is measured. The resistors are sized such that the majority of the voltage drop from live to neutral occurs on the resistor whose voltage is not measured. A Rogowski coil can alternatively be used to sense current in the following examples wherever a CT is used. The integration to determine the current flowing through the Rogowski coil is done digitally if that modification is made. RC antialiasing filters are not shown in the following diagrams for simplicity, but are recommended for all channels.

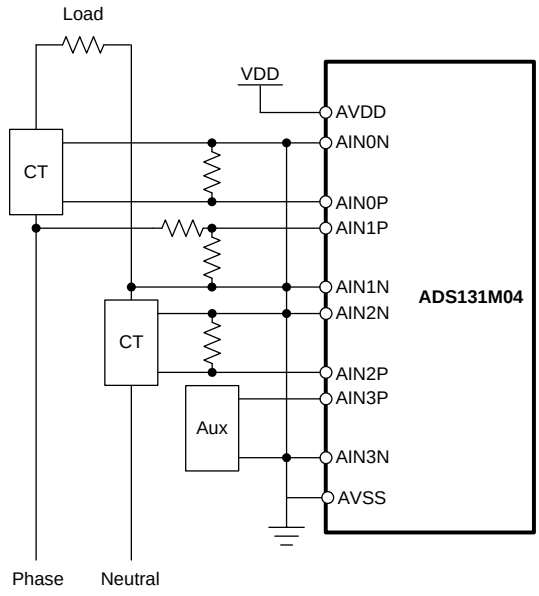

Figure 43. Single-Phase CT for Live, Neutral Currents, With Phase and Auxiliary Voltages Measured

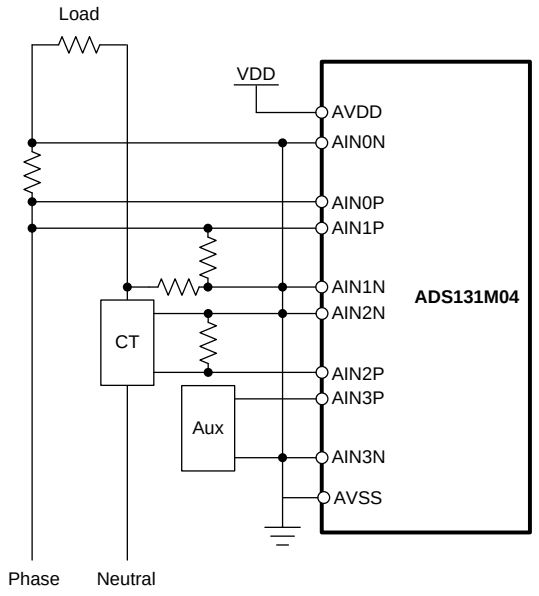

Figure 44. Single-Phase, Shunt for Live Current, CT for Neutral Current, With Phase and Auxiliary Voltages Measured

ADVANCE INFORMATION

Application Information (continued)

9.1.3 Multiple Device Configuration

Multiple devices can be arranged to capture all signals simultaneously. The same clock must be provided to all devices and the SYNC/RESET pins must be strobed simultaneously at least one time to align the sample periods internally to each device. The phase settings of each device can be changed uniquely, but the host must take care to record which channel in the group of devices represents the *zero* phase.

The devices can also share the SPI bus where only the $\overline{CS}$ pins for each device are unique. Each device can be addressed sequentially by asserting $\overline{CS}$ for the device that the host wishes to communicate with. The DOUT pin remains high impedance when the $\overline{CS}$ pin is high, allowing the DOUT lines to be shared between devices as long as no two lines sharing the bus simultaneously have their $\overline{CS}$ pins low. Figure 45 shows multiple devices configured for simultaneous data acquisition while sharing the SPI bus.

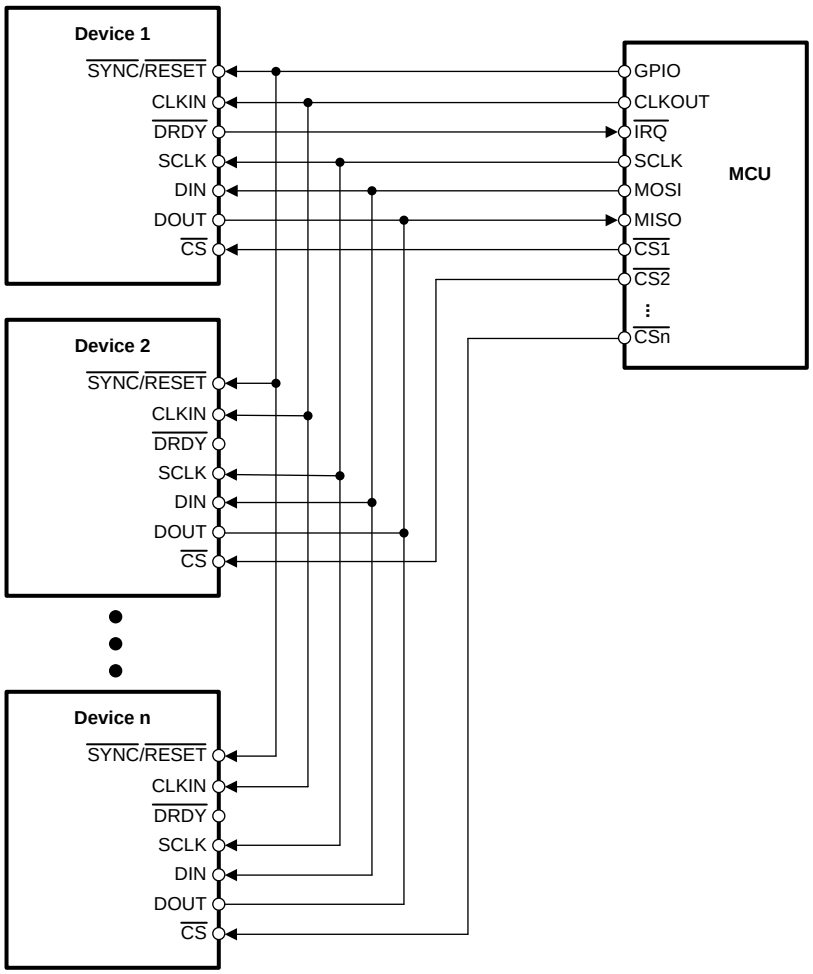

Figure 45. Multiple Device Configuration

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9.2 Typical Application

This section describes a class 0.1 split-phase energy measurement front-end using the ADS131M04. The ADC samples the outputs of the CTs and voltage dividers to measure the current and voltage (respectively) of each leg of the AC mains. The design can achieve high accuracy across a wide input current range (0.05 A–100 A) and supports high sampling frequencies necessary for advanced power quality features such as individual harmonic analysis. Using the ADS131M04 to sample the CT output provides designers greater flexibility in the choice of metrology microcontrollers when compared to an integrated system-on-a-chip (SoC) and dedicated application-specific products.

Figure 46 shows the front-end for the split-phase energy measurement design.

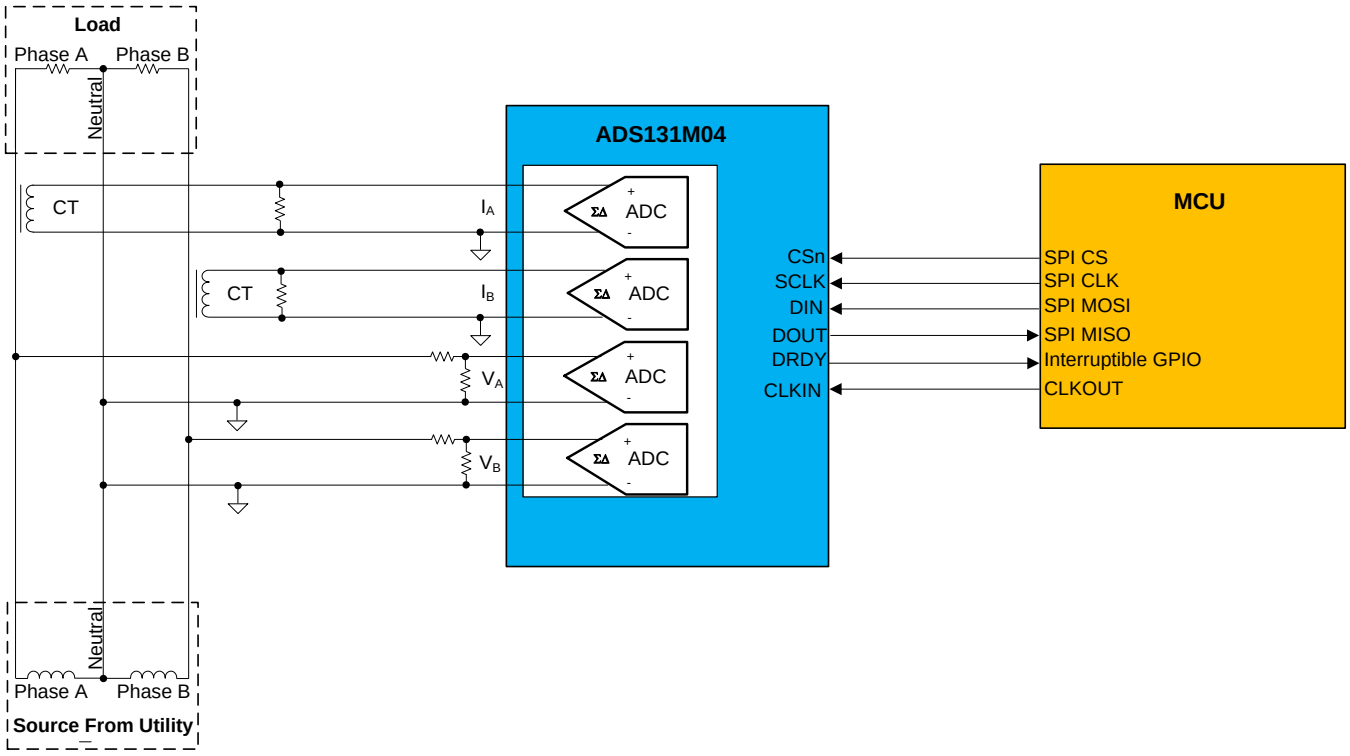

Figure 46. Split-Phase Metrology Design Front-End

9.2.1 Design Requirements

Table 28. Key System Specifications

FEATURES	DESCRIPTION
Number of phases	1 phase (split-phase with two voltages measured), 1 phase (split-phase with one voltage measured), 2 phases
E-meter accuracy class	Class 0.1
Current sensor	Current transformer
Current range	0.05 A–100 A
System nominal frequency	50 Hz or 60 Hz
Measured parameters	• Active, reactive, apparent power and energy • Root mean square (RMS) current and voltage • Power factor • Line frequency

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9.2.2 Detailed Design Procedure

A current sensor connects to the current channels and a simple voltage divider is used for the corresponding voltage. The CT has an associated burden resistor that must be connected at all times to protect the measuring device. The selection of the CT and the burden resistor is made based on the manufacturer and current range required for energy measurements.

The choice of voltage divider resistors for the voltage channel is selected to ensure the mains voltage is divided down to adhere to the normal input ranges of the ADS131M04. Because the ADS131M04 ADCs have a large dynamic range and a large dynamic range is not needed to measure voltage, the voltage front-end circuitry is purposely selected so that the maximum voltage at the inputs of the voltage channel ADCs are only a fraction of the full-scale voltage. By reducing the voltage fed to the ADS131M04 voltage ADCs, system-level voltage-to-current crosstalk (which actually affects metrology accuracy more than voltage ADC accuracy) is reduced at the cost of voltage accuracy, thereby resulting in more accurate energy measurements at lower currents.

In this design, the ADS131M04 interacts with a microcontroller (MCU) in the following manner:

- The CLKIN clock used by the ADS131M04 device is provided by the MCU
- When new ADC samples are ready, the ADS131M04 device asserts its $\overline{\text{DRDY}}$ pin, which alerts the MCU that new samples are available
- After being alerted of new samples, the MCU uses one of its SPI interfaces to retrieve the voltage and current samples from the ADS131M04

9.2.2.1 Voltage Measurement Front-End

The nominal voltage from the mains is from 100 V–240 V so this voltage must be scaled down to be sensed by an ADC. Figure 47 shows the analog front-end used for this voltage scaling.

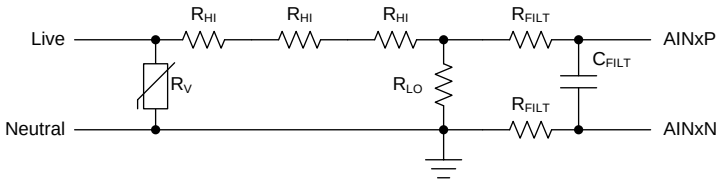

Figure 47. Voltage Measurement Front-End

In the analog front-end for voltage consists of a spike protection varistor (R_V), a voltage divider network (R_{HI} and R_{LO}), and an RC low-pass filter (R_{FILT} and C_{FILT}).

At lower currents, voltage-to-current crosstalk affects active energy accuracy much more than voltage accuracy if a power offset calibration is not performed. To maximize the accuracy at these lower currents, the entire ADC range is not used for voltage channels in this design. Because the ADCs of the ADS131M04 are high-accuracy ADCs, using the reduced ADC range for the voltage channels in this design still provides more than enough accuracy for measuring voltage. Equation 9 shows how to calculate the range of differential voltages fed to the voltage ADC channel for a given mains voltage and the selected voltage divider resistor values.

$$V_{ADC} = \pm V_{RMS} \times \sqrt{2} \times \frac{R_{LO}}{3R_{HI} + R_{LO}} \tag{9}$$

R_{HI} is 300 kΩ and R_{LO} is 750 Ω in this design. Based on Equation 9 and the selected resistor values, for a mains voltage of 120 V (as measured between the line and neutral), the input signal to the voltage ADC has a voltage swing of ±128 mV (91 mV_{RMS}) when using the two-voltage configuration. This voltage is well within the ±1.2-V input voltage that can be sensed by the ADS131M04 for the selected PGA gain value of 1 that is used for the voltage channels.

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9.2.2.2 Current Measurement Front-End

The analog front-end for current inputs is different from the analog front-end for the voltage inputs. Figure 48 shows the analog front-end used for a current channel.

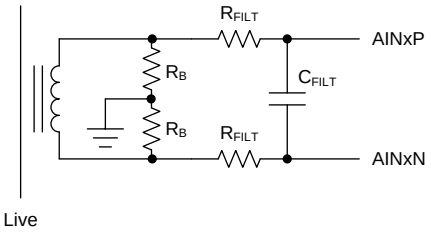

Figure 48. Current Measurement Front-End

The analog front-end for current consists of burden resistors for current transformers (R_B) and an RC low-pass filter (R_{FILT} and C_{FILT}) that functions as an antialias filter.

For best THD performance, instead of using one burden resistor, two identical burden resistors in series are used with the common point being connected to GND. This split-burden resistor configuration ensures that the waveforms fed to the positive and negative terminals of the ADC are 180 degrees out-of-phase with each other, which provides the best THD results with this ADC. The total burden resistance is selected based on the current range used and the turns ratio specification of the CT (this design uses CTs with a turns ratio of 2000). The total value of the burden resistor for this design is 12.98 Ω.

Equation 10 shows how to calculate the range of differential voltages fed to the current ADC channel for a given maximum current, CT turns ratio, and burden resistor value.

$$V_{ADC} = \pm I_{RMS} \times 2R_B \times \sqrt{2} / N_{CT} \quad (10)$$

Based on the maximum RMS current of 100 A, CT turns ratio N_{CT} of 2000, and a burden resistor R_B of 12.98 Ω of this design, the input signal to the current ADC has a voltage swing of ±918 mV maximum (649 mV_{RMS}) when the maximum current rating of the meter (100 A) is applied. This ±918-mV maximum input voltage is well within the ±1.2-V input range of the device for the selected PGA gain of 1 that is used for the current channels.

9.2.2.3 ADC Setup

The ADS131M04 receives its clock from the MCU in this design. The ADS131M04 is configured in HR mode and the MCU provides an 8.192-MHz master clock, which is in the allowable frequency range for HR mode. The MCU SPI port that is used to communicate with the ADS131M04 is configured to CPOL = 0 and CPHA = 1. The SPI clock frequency is configured to be 8.192 MHz so that all conversion data can be shifted out of the device successfully within the sample period. When powered on, the MCU configures the ADS131M04 registers with the following settings using SPI register writes.

- GAIN1 register settings: PGA gain of 1 is used for all four ADC channels.
- CHx_CNG register settings (where x is the channel number): All four ADC channel inputs are connected to the external ADC pins and the channel phase delay set to 0 for each channel. The channel phase setting can also be configured in this register. This design uses an integer number of output samples for phase calibration so the processing is done in software completely.
- CLOCK register settings: 512 OSR, all channels enabled, and HR mode.

After the ADS131M04 registers are properly initialized, the MCU is configured to generate a GPIO interrupt whenever a falling edge occurs on the $\overline{DRDY}$ pin, which indicates that the ADS131M04 has new samples available.

The clock fed to the CLKIN pin of the ADS131M04 is internally divided by two to generate the modulator clock. The output data rate of the ADS131M04 is therefore f_{MOD} / OSR = f_{CLKIN} / (2 × OSR) = 8 kSPS.

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9.2.2.4 Calibration

Certain signal chain errors can be easily corrected through a single room temperature calibration. The ADS131M04 has the capability to store calibration values and use the values to correct the results in real time. Among those errors that can be corrected in real time with the ADS131M04 are offset error, gain error, and phase error.

Offset calibration is performed by determining the measured output of the signal chain when the input is zero voltage for a voltage channel or zero current for a current channel. The value can be measured and recorded in external non-volatile memory for each channel. When the system is deployed, these values can be provided to the CHn_OCAL_MSB and CHn_OCAL_LSB registers for the corresponding channels. The ADS131M04 then subtracts these values from its conversion results prior to providing them to the host.

Similar to offset error correction, system gain error can be determined prior to deployment and can be used to correct the gain error on each channel in real time. Gain error is defined as the percentage difference in the ADC transfer function from its PGA gain corrected ideal value of 1. This error can be determined by measuring the results from both a maximum and minimum input signal, finding the difference between these results, and dividing by the difference between the ideal difference. Equation 11 describes how to calculate gain error.

$$\text{Gain Error} = 1 - \frac{V,I_{\text{Max,Measured}} - V,I_{\text{Min,Measured}}}{V,I_{\text{Max}} - V,I_{\text{Min}}} \tag{11}$$

To correct for gain error, divide each offset-corrected conversion result by the measured gain. The ADS131M04 multiplies each conversion result by the calibration factor stored in the CHn_GCAL_MSB and CHn_GCAL_LSB registers according to the method described in the *Calibration Registers* section. The host can program the measured inverted gain values for each channel into these registers to have them automatically corrected for each sample.

The ADS131M04 can also correct for system phase error introduced by sensors. For this design, the CT introduces some phase error into the system. This design uses a software method for phase correction, but the ADS131M04 can perform this function in real time. The system must first measure the phase relationships between the various channels. Then, define one channel as *phase 0*. Subsequently, the PHASEn bits in the CHn_CFG registers corresponding to the various other channels can be edited to correct their phase relationship relative to the phase 0 channels.

9.2.2.5 Formulae

This section briefly describes the formulas used for the power and energy calculations. Voltage and current samples are obtained at a sampling rate of 8000 Hz. All samples that are taken in approximately one-second (1 sec) frames are kept and used to obtain the RMS values for voltage and current for each phase.

Power and energy are calculated for active and reactive energy samples of one frame. These samples are phase-corrected. Then phase active and reactive powers are calculated through the following formulas:

$$P_{\text{Actual.ph}} = \frac{1}{N_{\text{samples}}} \sum_{n=0}^{N_{\text{samples}}-1} v[n] \times i[n] \tag{12}$$

$$P_{\text{Reactive.ph}} = \frac{1}{N_{\text{samples}}} \sum_{n=0}^{N_{\text{samples}}-1} v\left[n - n_{90^\circ}\right] \times i[n] \tag{13}$$

$$P^2_{\text{Apparent.ph}} = P^2_{\text{Actual.ph}} + P^2_{\text{Reactive.ph}}$$

where:

- v[n] = Voltage sample
- i[n] = Current sample
- $N_{samples}$ = Number of samples in the approximately 1-second frame
- v[n-$n_{90°}$] = Voltage sample with a 90° phase shift
- $P_{ACTUAL,ph}$ = Instantaneous actual power for the measured phase
- $P_{REACTIVE}$ = Instantaneous reactive power for the measured phase
- $P_{APPARENT,ph}$ = Instantaneous apparent power for the measured phase (14)

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The 90° phase shift approach is used for two reasons:

1. This approach allows accurate measurement of the reactive power for very small currents
2. This approach conforms to the measurement method specified by IEC and ANSI standards

The calculated mains frequency is used to calculate the 90° shifted voltage sample. Because the frequency of the mains varies, the mains frequency is first measured accurately to phase shift the voltage samples accordingly.

To get an exact 90° phase shift, interpolation is used between two samples. For these two samples, a voltage sample slightly more than 90 degrees before the current sample and a voltage sample slightly less than 90° before the current sample are used. The phase shift implementation of the application consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap FIR filter.

The cumulative power values can be calculated by summing the per phase power results. The cumulative energy can be calculated by multiplying the cumulative power by the number of samples in the packet.

The host calculates the frequency in terms of samples-per-mains cycle by counting zero crossings of the sine wave. Equation 15 converts this result from a samples-per-mains cycle to Hertz.

$$\text{Frequency (Hz)} = \text{Data rate (samples / second)} / \text{Frequency (samples / cycle)} \quad (15)$$

After the active power and apparent power are calculated, the absolute value of the power factor is calculated. In the internal representation of power factor of the system, a positive power factor corresponds to a capacitive load and a negative power factor corresponds to an inductive load. The sign of the internal representation of power factor is determined by whether the current leads or lags voltage, which is determined in the background process. Therefore, Equation 16 and Equation 17 calculate the internal representation of the power factor:

$$PF = P_{ACTUAL} / P_{APPARENT}, \text{ if capacitive load} \quad (16)$$

$$PF = -P_{ACTUAL} / P_{APPARENT}, \text{ if inductive load} \quad (17)$$

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9.2.2.6 Test Methodology

A source generator was used to provide the voltages and currents to the system. In this design, a nominal voltage of 120 V between the line and neutral, a calibration current of 10 A, and a nominal frequency of 60 Hz were used for each phase.

When the voltages and currents are applied to the system, the design outputs the cumulative active energy pulses and cumulative reactive energy pulses at a rate of 6400 pulses per kilowatt hour. This pulse output was fed into a reference meter that determined the energy percentage error based on the actual energy provided to the system and the measured energy as determined by the active and reactive energy output pulse of the system.

For the cumulative active energy error, cumulative reactive energy error testing, and individual phase active energy testing, the current was varied from 50 mA to 100 A. For cumulative active energy and individual phase error testing, a phase shift of 0°, 60°, and −60° was applied between the voltage and current waveforms fed to the design. Based on the error from the active energy output pulse, several plots of active energy percentage error versus current were created for 0°, 60°, and –60° phase shifts. For cumulative reactive energy error testing, a similar process was followed except that 30°, 60°, –30°, and –60° phase shifts were used, and cumulative reactive energy error was plotted instead of cumulative active energy error. In the cumulative active and reactive energy testing, the sum of the energy reading of each phase was tested for accuracy. In contrast, the individual phase energy readings (both phase A and phase B) were tested for the individual phase active energy testing. When testing the individual energy accuracy of a phase, the other phase is disabled by providing 0-A input for the current of the other phase so that the cumulative active energy reading can ideally be equal to the individual phase voltage, which allows the cumulative energy pulse output to be used for testing individual phase accuracy.

In addition to testing active energy by varying current, active energy was also tested by varying the RMS voltage from 240 V–15 V and measuring the active energy percentage error. This voltage variation testing was specifically done for the cumulative two-voltage active energy test and the individual phase active energy tests.

Another set of energy tests performed were frequency variation tests. For this test, the frequency was varied by ±2 Hz from its 60-Hz nominal frequency. This test was conducted at 0.5 A and 10 A at phase shifts of 0°, 60°, and −60°. The resulting active energy error under these conditions are logged in the *Results* section.

For the voltage testing, a 10-A current was applied for each phase and the voltage was varied from 9 V–270 V on each phase simultaneously. The voltage was not varied beyond 270 V because of the 275-V varistor present on the board, which can be removed for testing at voltages beyond 275 V. After applying each voltage, the resulting RMS voltage reading was logged for each phase after the readings stabilized. When the measured RMS voltage readings are obtained, the actual RMS voltage readings are obtained from the reference meter. The RMS voltage percentage error is calculated using the results measured by the design and the reference meter output. A similar process is used to calculate the RMS current percentage error by using 120 V for each phase and varying current from 50 mA to 100 A.

9.2.2.7 Results

The front-end was calibrated before obtaining the following results. The active energy results are within 0.1% at 0° phase shift. At 60° and –60° phase shift, which is allowed to have relaxed accuracy in electricity meter standards, the trend where the results deviate at higher currents is from the CT phase shift varying across current. Additionally, the active energy versus voltage results and the RMS voltage results illustrate that good accuracy results are able to be obtained despite using only a fraction of the ADC range for the voltage channels.

Table 29 shows the active energy accuracy results for phase A with changing voltage. Table 30 shows the active energy results for phase A with varying current. Figure 49 shows a plot of the values in Table 30.

Table 29. Phase A Active Energy % Error Versus Voltage

VOLTAGE (V)	% ERROR
240	0.0113
120	–0.0067
60	–0.01
30	–0.012
15	–0.015

Table 30. Phase A Active Energy % Error Versus Current

CURRENT (A)	0°	60°	–60°	CURRENT (A)	0°	60°	–60°
0.05	–0.02	0.007	–0.062	30.00	0.0007	–0.002	0.006
0.10	–0.025	0.017	–0.057	40.00	0.002	–0.007	0.013
0.25	–0.007	0.031	–0.051	50.00	–0.009	–0.04	0.032
0.50	0.001	0.029	–0.031	60.00	–0.0007	–0.049	0.0445
1.00	0.0075	0.034	–0.021	70.00	0.0003	–0.052	0.058
2.00	0	0.04	–0.036	80.00	0.004	–0.064	0.074
5.00	0.003	0.019	–0.019	90.00	0.01	–0.065	0.0845
10.00	0.007	0.009	–0.004	100.00	0.014	–0.07	0.101
20.00	–0.007	0.006	–0.013				

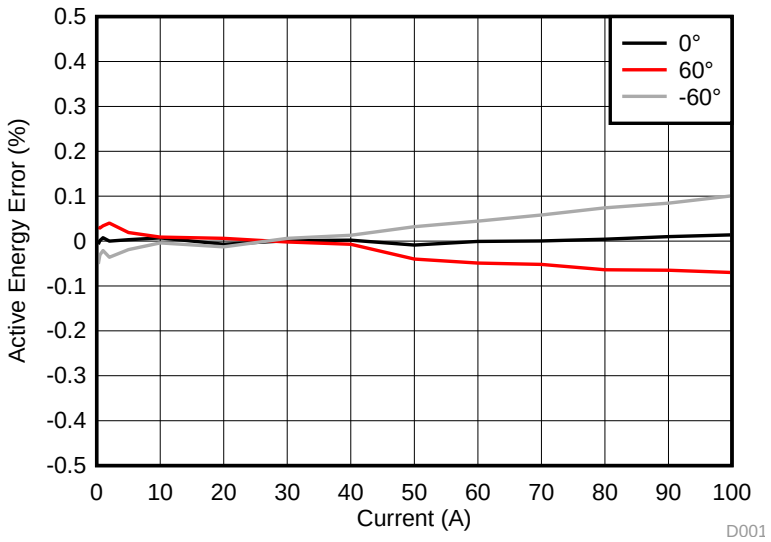

Figure 49. Phase A Active Energy % Error Versus Current

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Table 31 shows the active energy accuracy results for phase B with changing voltage. Table 32 shows the active energy results for phase B with varying current. Figure 50 shows a plot of the values in Table 32.

Table 31. Phase B Active Energy % Error Versus Voltage, Two-Voltage Mode

VOLTAGE (V)	% ERROR
240	0.011
120	–0.0003
60	–0.004
30	–0.0047
15	–0.0067

Table 32. Phase B Active Energy % Error Versus Current

CURRENT (A)	0°	60°	–60°
0.05	–0.032	–0.007	–0.122
0.10	–0.019	0.019	–0.083
0.25	–0.019	0.032	–0.058
0.50	–0.007	0.045	–0.062
1.00	–0.007	0.045	–0.045
2.00	–0.015	0.032	–0.06
5.00	–0.007	0.026	–0.036
10.00	–0.0087	0.009	–0.025
20.00	–0.019	–0.019	–0.028
30.00	–0.019	–0.036	–0.011
40.00	–0.023	–0.045	0
50.00	–0.014	–0.06	0.0395
60.00	–0.011	–0.075	0.045
70.00	–0.01	–0.074	0.054
80.00.	–0.0077	–0.08	0.064
90.00	0.003	–0.068	0.066
100.00	0.011	–0.042	0.052

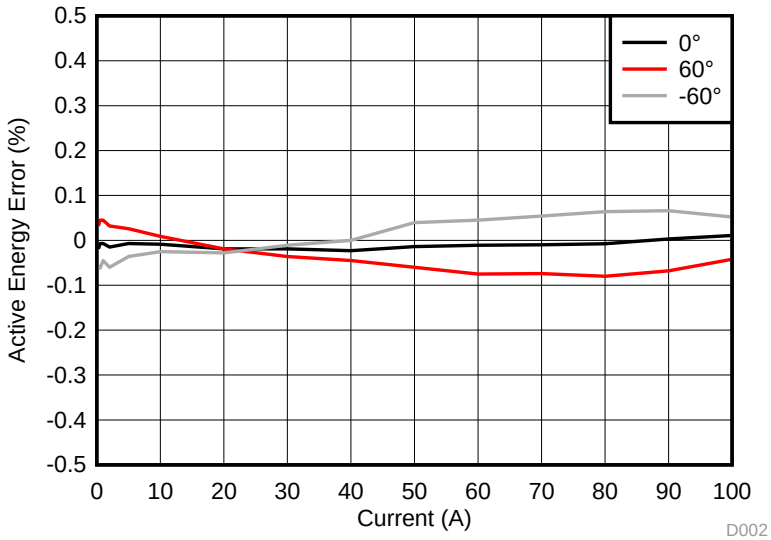

Figure 50. Phase B Active Energy % Error Versus Current

Table 33 shows the cumulative active energy accuracy results with changing voltage. Table 34 shows the cumulative active energy results with varying current. Figure 51 shows a plot of the values in Table 34.

Table 33. Cumulative Phase Active Energy % Error Versus Voltage, Two-Voltage Mode

VOLTAGE (V)	% ERROR
240	0.0353
120	0.022
60	0.016
30	0.014
15	0.013

Table 34. Cumulative Phase Active Energy % Error Versus Current

CURRENT (A)	0°	60°	–60°
0.05	0.019	0.045	–0.032
0.10	0.006	0.058	–0.032
0.25	0.0125	0.045	–0.0385
0.50	0.006	0.032	–0.032
1.00	0.015	0.045	–0.019
2.00	0.003	0.045	–0.039
5.00	0.006	0.024	–0.012
10.00	0.01	0.0165	0
20.00	–0.007	0.002	–0.013
30.00	0.002	–0.007	0.0085
40.00	0	–0.016	0.019
50.00	–0.003	–0.035	0.042
60.00	0.002	–0.047	0.053
70.00	0.009	–0.047	0.063
80.00.	0.007	–0.05	0.067
90.00	0.013	–0.045	0.08
100.00	0.0223	–0.04	0.092

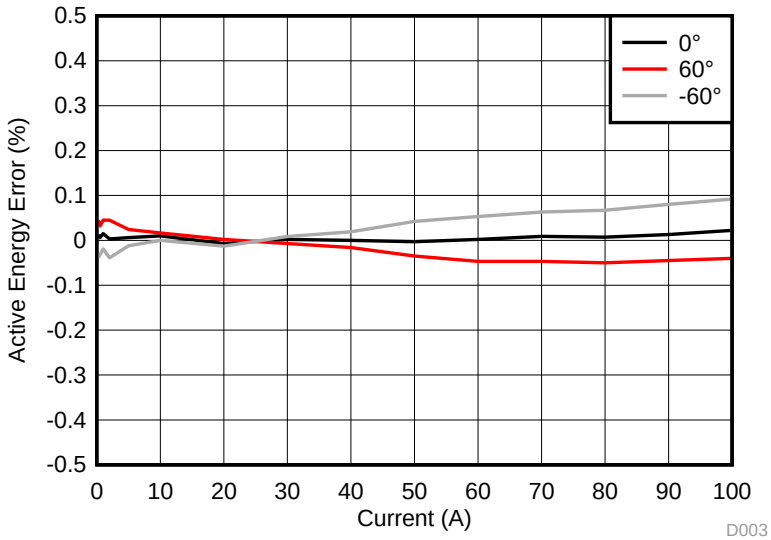

Figure 51. Cumulative Phase Active Energy % Error Versus Current

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Table 35 shows the cumulative reactive energy accuracy results with changing current. Figure 52 shows a plot of the values in Table 34.

Table 35. Cumulative Reactive Energy % Error Versus Current

CURRENT (A)	30°	60°	–30°	–60°
0.05	–0.003	0.004	–0.023	–0.027
0.10	–0.037	–0.013	0.011	–0.008
0.25	–0.067	–0.027	0.043	0.002
1.00	–0.044	–0.021	0.0415	0.011
5.00	–0.036	–0.0183	0.022	0.001
10.00	–0.03	–0.012	0.014	–0.003
20.00	–0.041	–0.026	–0.0035	–0.013
40.00	–0.01	–0.016	–0.021	–0.016
60.00	0.025	–0.0007	–0.047	–0.0247
80.00	0.041	0.0085	–0.048	–0.021
100.00	0.054	0.02	–0.044	–0.012

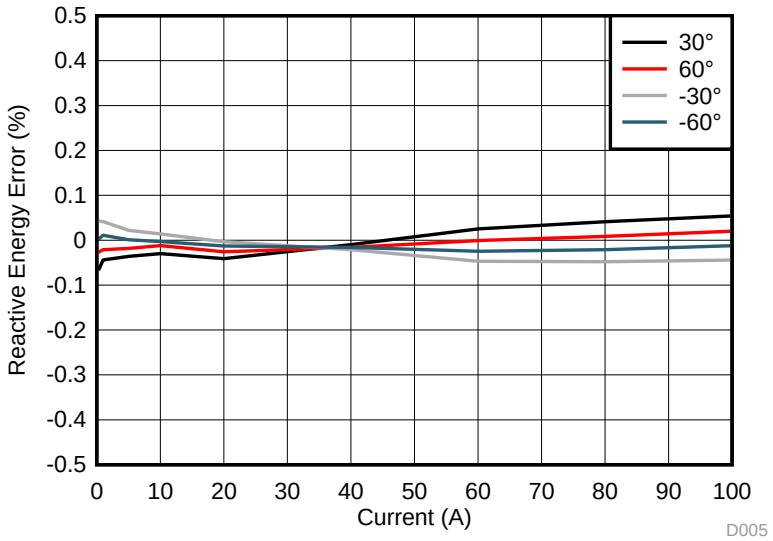

Figure 52. Cumulative Reactive Energy % Error Versus Current

Table 36 lists the cumulative active energy measurements across currents for the nominal frequency, 60 Hz, and for frequencies ±2 Hz around nominal.

Table 36. Cumulative Active Energy Measurement Error Versus Frequency, ±2 Hz From Nominal Frequency

CONDITIONS	58 Hz	60 Hz	62 Hz
0.5 A, 0	0.006	0.0017	–0.007
0.5 A, 60	0.058	0.032	0.032
0.5 A, 300	–0.045	–0.032	–0.032
10 A, 0	0.0047	–0.001	–0.0033
10 A, 60	0.025	0.0073	0.008
10 A, 300	–0.0105	–0.009	–0.013

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Table 37 lists the phase A current measurement results across currents. Figure 53 shows a plot of the results in Table 37.

Table 37. Phase A RMS Current % Error

CURRENT (A)	GUI CURRENT READING (A)	REFERENCE METER READING (A)	% ERROR
0.05	0.050053	0.050031	0.0440
0.10	0.100039	0.099988	0.0510
0.25	0.250034	0.24997	0.0256
0.50	0.50005	0.49992	0.0260
1.00	1.00017	0.99979	0.0380
2.00	2.00021	1.9996	0.0305
5.00	5.00039	4.9986	0.0358
10.00	10.0013	9.9971	0.0420
20.00	20.0007	19.993	0.0385
30.00	30.0025	29.991	0.0383
40.00	40.0038	39.988	0.0395
50.00	50.0054	49.989	0.0328
60.00	60.0066	59.984	0.0377
70.00	70.0091	69.981	0.0402
80.00.	80.0127	79.981	0.0396
90.00	90.018	89.976	0.0467
100.00	100.024	99.974	0.0500

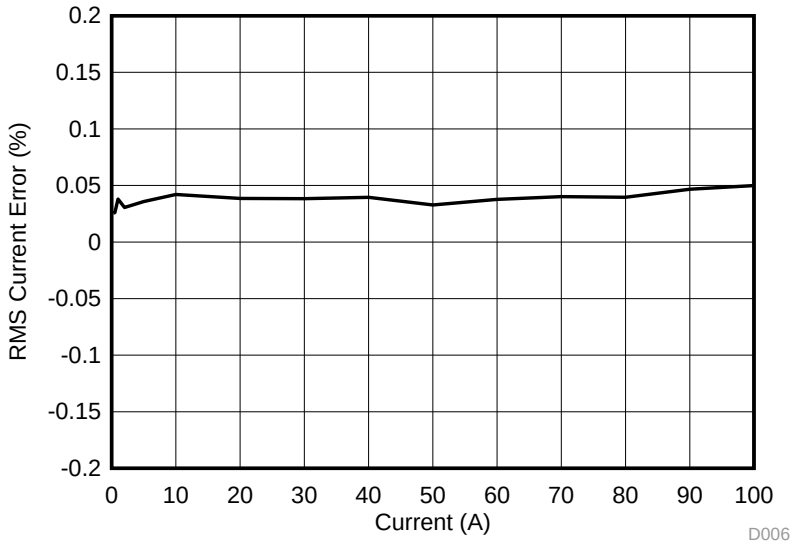


Figure 53. Phase A RMS Current % Error

ADVANCE INFORMATION

Table 38 lists the phase B current measurement results across currents. Figure 54 shows a plot of the results in Table 38.

Table 38. Phase B RMS Current % Error

CURRENT (A)	GUI CURRENT READING (A)	REFERENCE METER READING (A)	% ERROR
0.05	0.050083	0.05005	0.0659
0.10	0.100055	0.10002	0.0350
0.25	0.250019	0.24996	0.0236
0.50	0.500016	0.49989	0.0252
1.00	1.00008	0.99984	0.0240
2.00	2.00016	1.9999	0.0130
5.00	4.99979	4.9987	0.0218
10.00	9.99998	9.9982	0.0178
20.00	19.9986	19.998	0.0030
30.00	29.9948	29.992	0.0093
40.00	39.9936	39.99	0.0090
50.00	49.9918	49.983	0.0176
60.00	59.9906	59.979	0.0193
70.00	69.9921	69.981	0.0159
80.00.	79.9924	79.976	0.0205
90.00	89.9942	89.97	0.0269
100.00	99.9997	99.97	0.0297

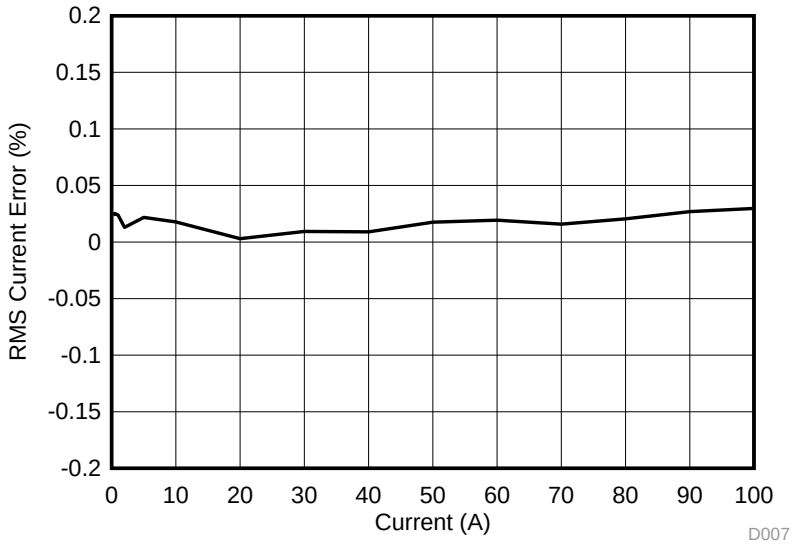


Figure 54. Phase B RMS Current % Error

Table 39 lists the phase A voltage measurement results across voltage. Figure 55 shows a plot of the results in Table 39.

Table 39. Phase A RMS Voltage % Error

VOLTAGE (V)	GUI VOLTAGE READING (V)	REFERENCE METER READING (V)	% ERROR
9	9.002	9.0034	–0.0155
10	10.003	10.004	–0.0100
30	29.999	30.002	–0.0100
50	50.002	49.999	0.0060
70	70.004	70.001	0.0043
90	90.007	89.999	0.0089
100	100.01	100	0.0100
120	120.016	120	0.0133
140	140.025	140.01	0.0107
160	160.028	160	0.0175
180	180.035	180	0.0194
200	200.049	200	0.0245
220	220.057	220	0.0259
230	230.067	230	0.0291
240.	240.074	240	0.0308
260	260.087	260.02	0.0258
270	270.104	270.03	0.0274

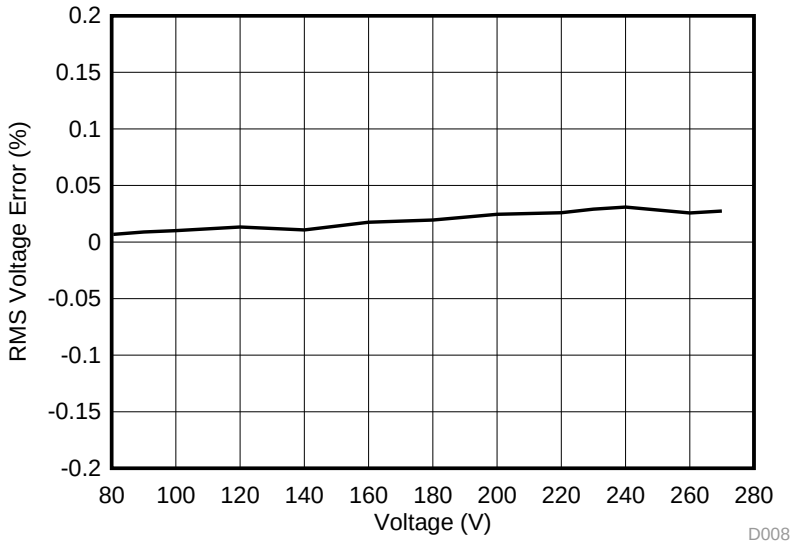


Figure 55. Phase A RMS Voltage % Error

ADVANCE INFORMATION

Table 40 lists the phase B voltage measurement results across voltage. Figure 56 shows a plot of the results in Table 40.

Table 40. Phase B RMS Voltage % Error

VOLTAGE (V)	GUI VOLTAGE READING (V)	REFERENCE METER READING (V)	% ERROR
9	8.999	9	–0.0111
10	9.99995	9.9995	0.0045
30	29.997	29.997	0.0000
50	49.999	49.995	0.0080
70	70.002	70	0.0029
90	90.009	90.002	0.0078
100	100.01	100	0.0100
120	120.017	120	0.0142
140	140.027	140.01	0.0121
160	160.03	160.01	0.0125
180	180.042	180	0.0233
200	200.056	200.01	0.0230
220	220.069	220.01	0.0268
230	230.079	230.02	0.0256
240.	250.087	250.02	0.0268
260	260.103	260.03	0.0281
270	270.114	270.03	0.0311

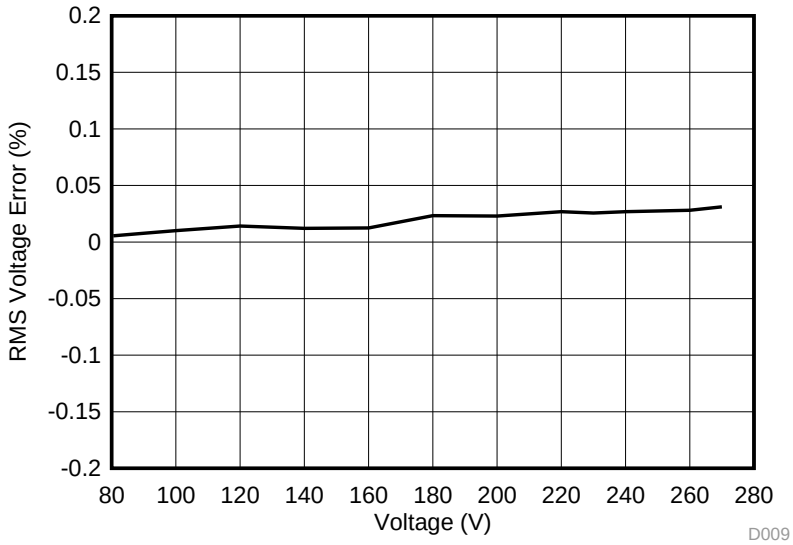


Figure 56. Phase B RMS Voltage % Error

10 Power Supply Recommendations

10.1 CAP Pin

The ADS131M04 core digital voltage operates from 1.8 V, created from an internal LDO from DVDD. The CAP pin outputs the LDO voltage created from the DVDD supply and requires an external bypass capacitor. When operating from V_{DVDD} > 2.7 V, place a 220-nF capacitor on the CAP pin to DGND. If V_{DVDD} ≤ 2 V, tie the CAP pin directly to the DVDD pin and decouple the star-connected pins using a 100-nF capacitor to GND.

10.2 Power-Supply Sequencing

The power supplies can be sequenced in any order but the analog and digital inputs must never exceed the respective analog or digital power-supply voltage limits.

10.3 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. AVDD and DVDD must be decoupled with at least a 100-nF capacitor. Place the bypass capacitors as close to the power-supply pins of the device as possible with low-impedance connections. Using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics are recommended for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins can offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. The analog and digital ground are recommended to be connected together as close to the device as possible.

11 Layout

11.1 Layout Guidelines

Use a low-impedance connection for ground so that return currents flow undisturbed back to the respective sources. For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer. Keep connections to the ground plane as short and direct as possible. When using vias to connect to the ground layer, use multiple vias in parallel to reduce impedance to ground. Figure 57 shows the proper component placement for the system.

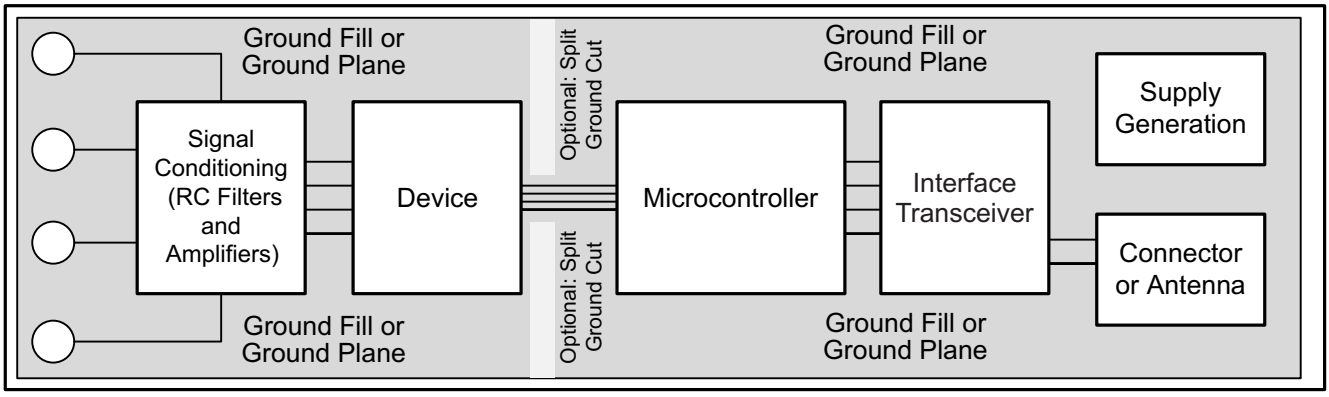


Figure 57. System Component Placement

ADVANCE INFORMATION

Layout Guidelines (continued)

A mixed-signal layout sometimes incorporates separate analog and digital ground planes that are tied together at one location; however, separating the ground planes is not necessary when analog, digital, and power-supply components are properly placed. Proper placement of components partitions the analog, digital, and power-supply circuitry into different PCB regions to prevent digital return currents from coupling into sensitive analog circuitry. If ground plane separation is necessary, then make the connection at the ADC. Connecting individual ground planes at multiple locations creates ground loops, and is not recommended. A single ground plane for the analog and digital grounds avoids ground loops.

Bypass the supply pins with a low-ESR ceramic capacitor. The placement of the bypass capacitors must be as close as possible to the supply pins using short, direct traces. For optimum performance, the ground-side connections of the bypass capacitors must also be made with low-impedance connections. The supply current flows through the bypass capacitor pin first and then to the supply pin to make the bypassing most effective (also known as a Kelvin connection). If multiple ADCs are on the same PCB, use wide power-supply traces or dedicated power-supply planes to minimize the potential of crosstalk between ADCs.

If external filtering is used for the analog inputs, use C0G-type ceramic capacitors when possible. C0G capacitors have stable properties and low-noise characteristics. Ideally, route differential signals as pairs to minimize the loop area between the traces. Route digital circuit traces (such as clock signals) away from all analog pins.

Treat the AVSS pin as a sensitive analog signal and connect directly to the supply ground with proper shielding.

The SCLK input of the serial interface must be free from noise and glitches. Even with relatively slow SCLK frequencies, short digital signal rise and fall times can cause excessive ringing and noise. For best performance, keep the digital signal traces short, using termination resistors as needed, and make sure all digital signals are routed directly above the ground plane with minimal use of vias.

11.2 Layout Example

Figure 58 illustrates an example layout of the ADS131M04 requiring a minimum of two PCB layers. In general, analog signals and planes are partitioned to the left and digital signals and planes to the right.

Layout Example (continued)

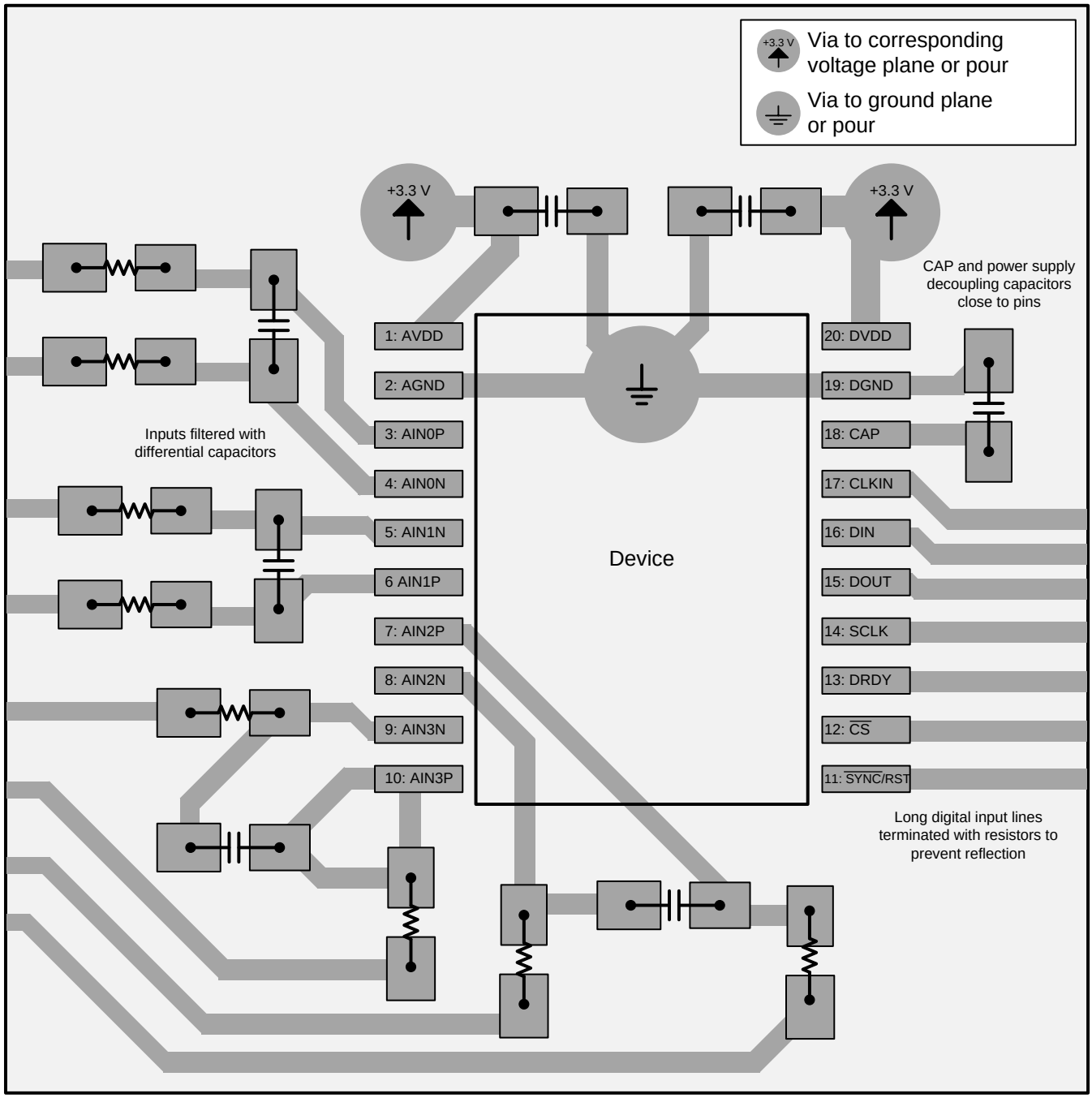


Figure 58. Layout Example

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

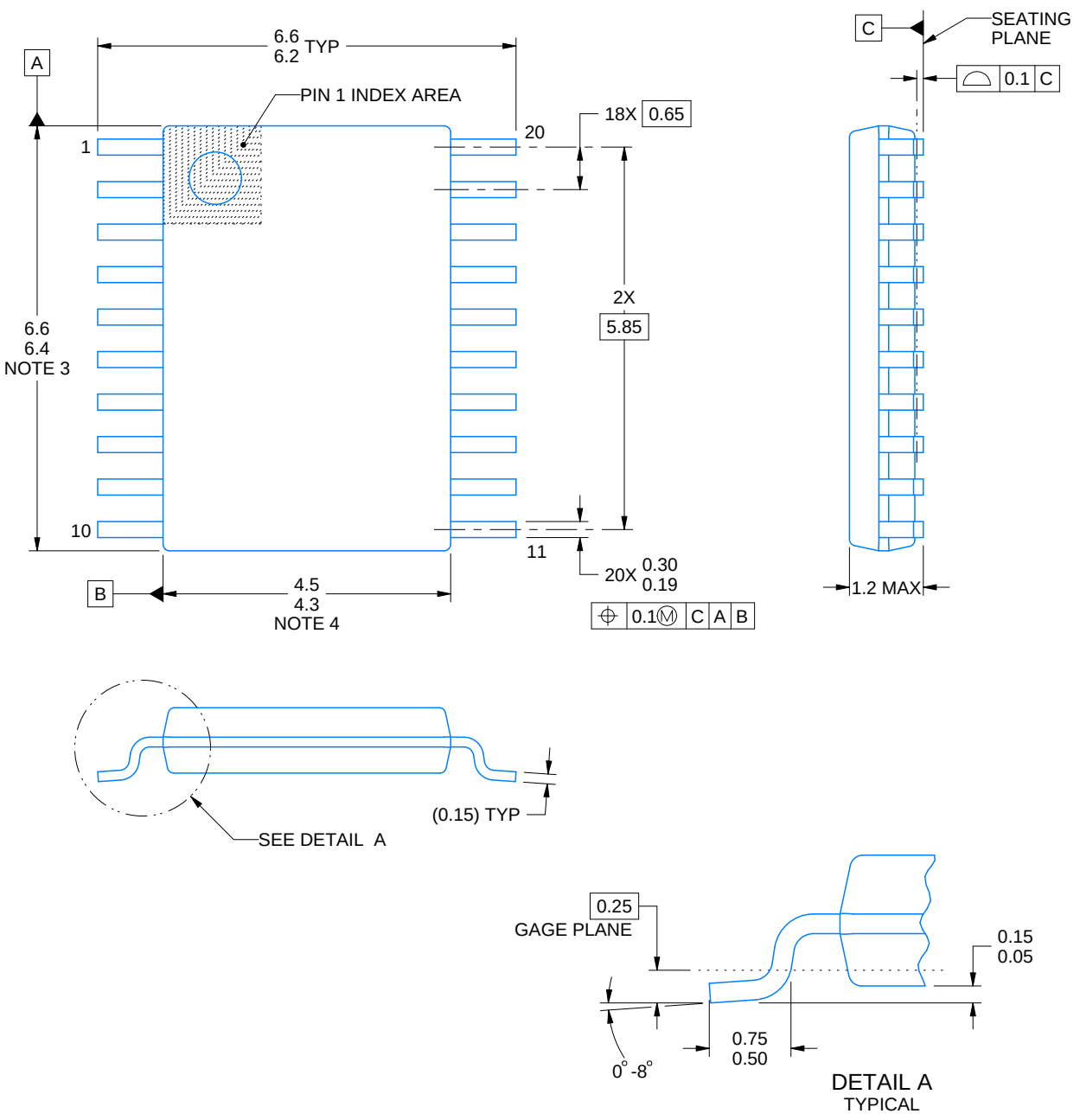
ADVANCE INFORMATION

PACKAGE OUTLINE

PW0020A

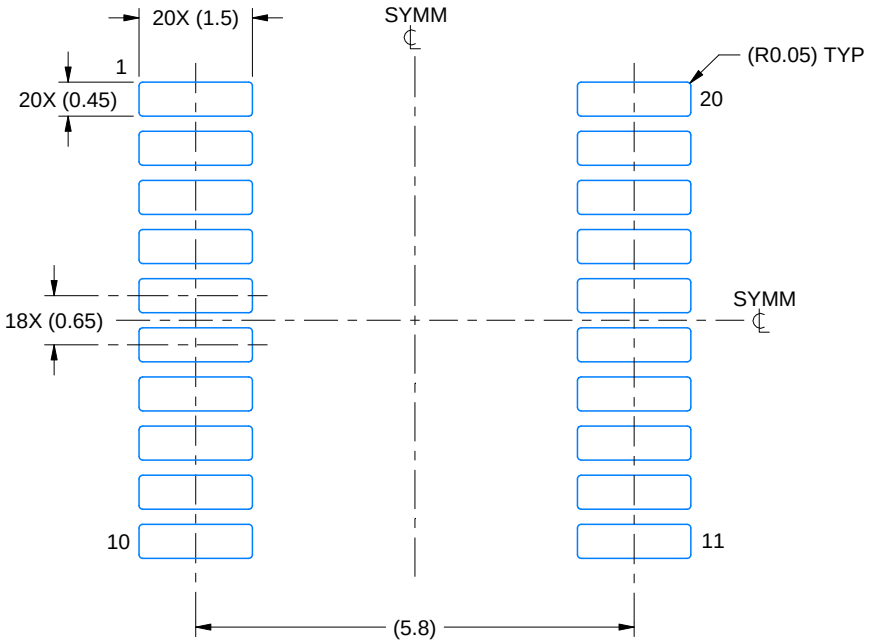
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



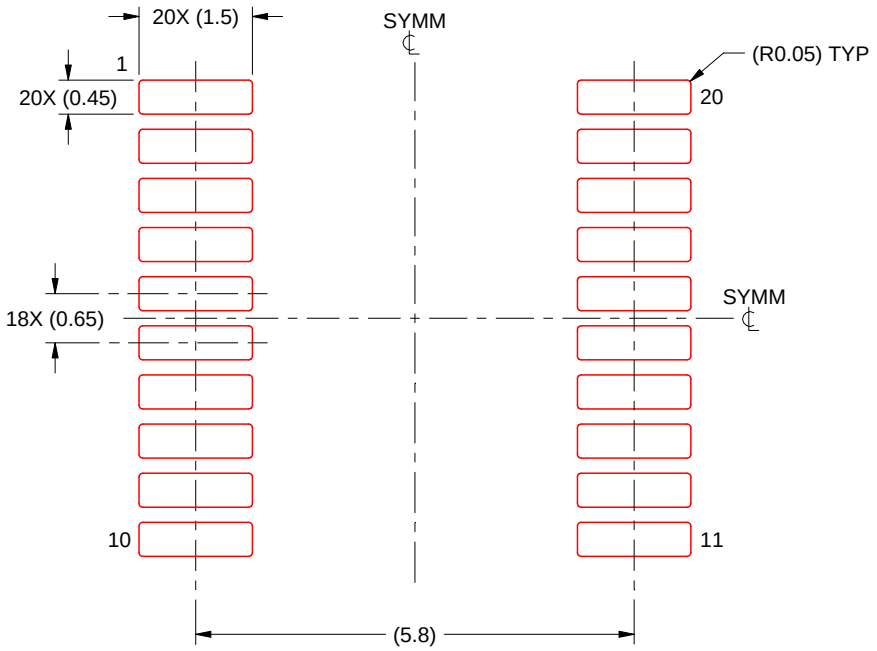
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS131M04IPW	PREVIEW	TSSOP	PW	20	70	TBD	Call TI	Call TI	-40 to 125		
ADS131M04IPWR	PREVIEW	TSSOP	PW	20	2000	TBD	Call TI	Call TI	-40 to 125		
ADS131M04IPWT	PREVIEW	TSSOP	PW	20	250	TBD	Call TI	Call TI	-40 to 125		
ADS131M04IRUKR	PREVIEW	WQFN	RUK	20	3000	TBD	Call TI	Call TI	-40 to 125		
PADS131M04IPWR	ACTIVE	TSSOP	PW	20	2000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

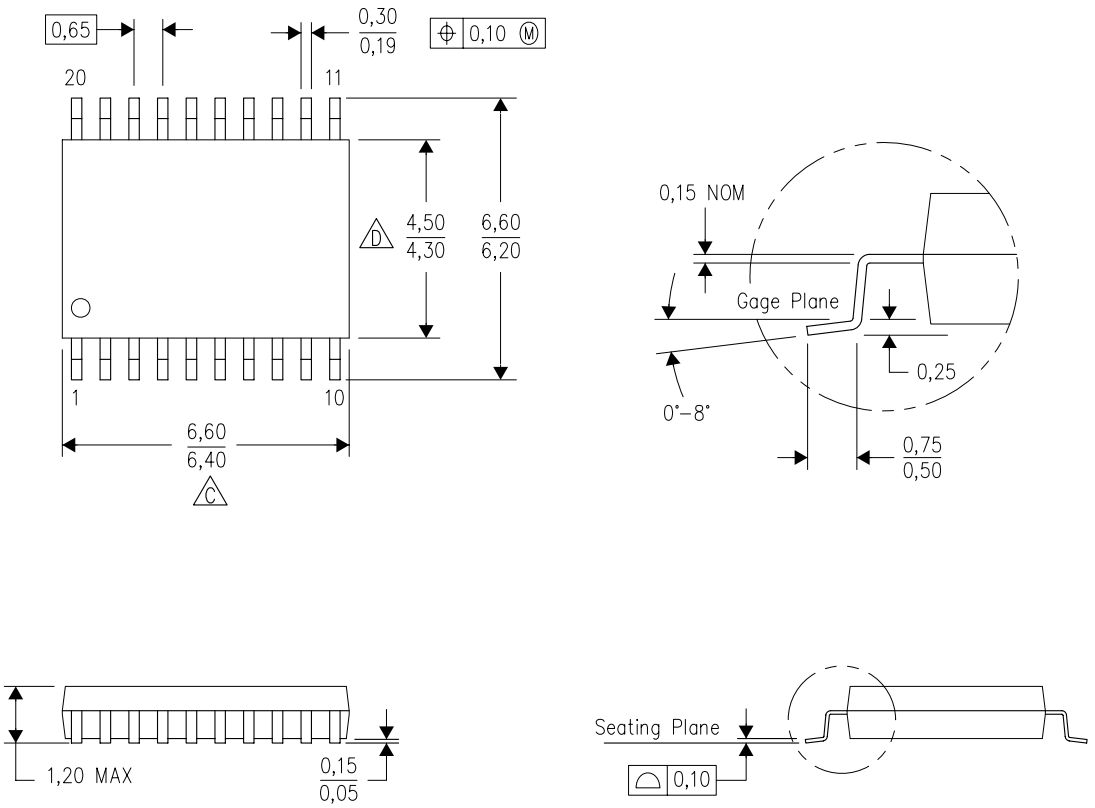
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

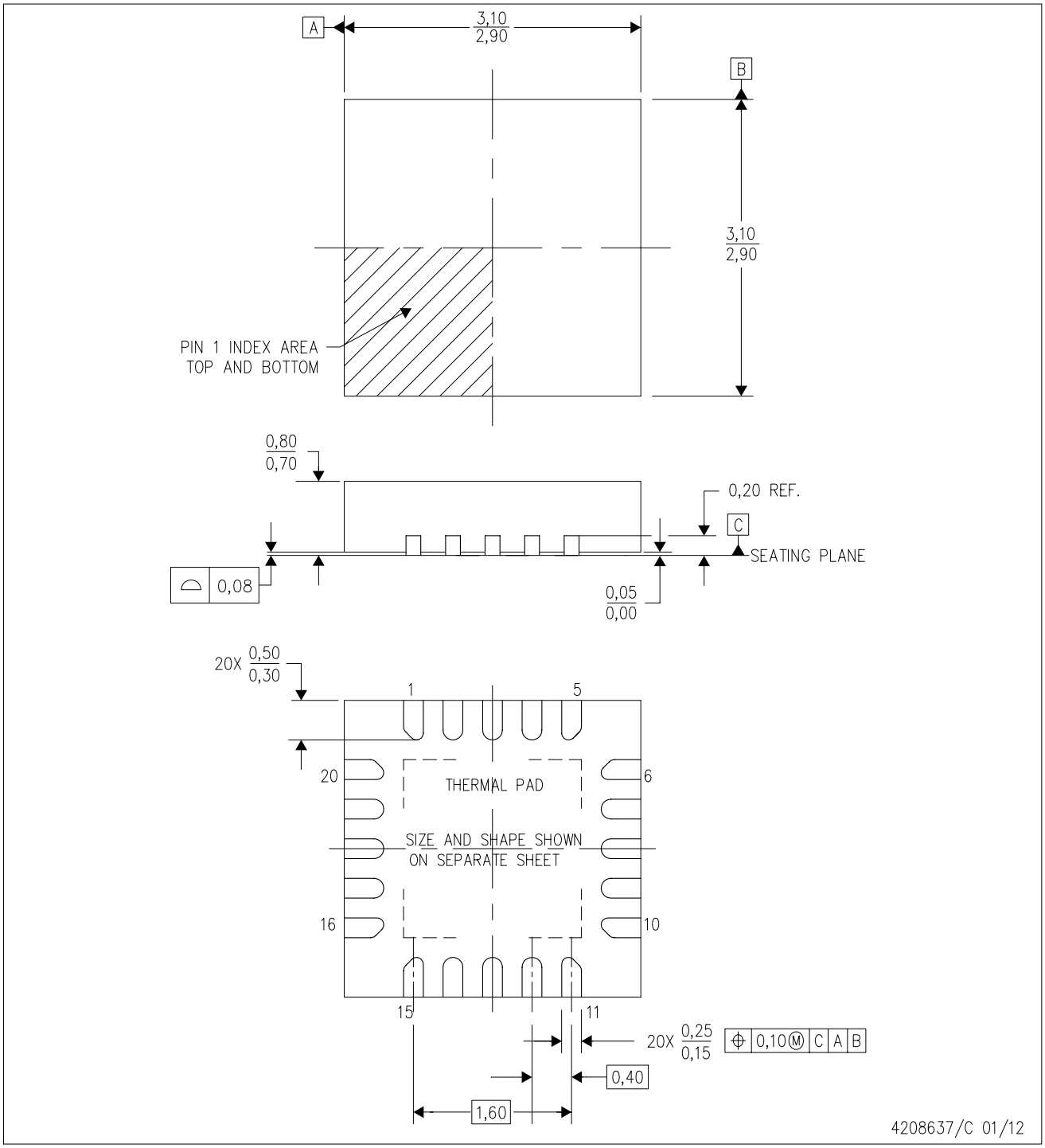
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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