12- and 14-Bit Hybrid Synchro/ Resolver-to-Digital Converters

SDC/RDC1767/1768

FEATURES
Internal Isolating Transformers
14-Bit or 12-Bit Resolution
Three Accuracy Options
Three-State Latched Output
Continuous Tracking—Even During Data Transfer
Simple Data Transfer
***Analog Velocity Output**
***Error Output**
Laser Trimmed—No External Adjustments
MIL Spec/Hi Rel Options Available
Hermetically Sealed

APPLICATIONS
Avionic Systems
Servo Mechanisms
Coordinate Conversion
Axis Transformation
Antenna Monitoring
Artillery Fire Control Systems
Engine Controllers

GENERAL DESCRIPTION

The SDC/RDC1767 and SDC/RDC1768 are hybrid, continuous tracking synchro- or resolver-to-digital converters which employ a type 2 servo loop and contain three-state latches on the digital outputs.

The input signals can either be 3-wire synchro plus reference or 4-wire resolver format plus reference depending on the option; and the outputs are presented in TTL compatible parallel natural binary buffered by three-state latches.

The three-state output facility, which has separate $\overline{\text{ENABLE}}$ inputs for the most significant 8 bits and the least significant 4 bits (or 6 bits in the case of the SDC/RDC1768), not only simplifies multiplexing of more than one device onto a single data bus, but also enables the $\overline{\text{INHIBIT}}$ to be used without opening the internal converter loop.

An outstanding feature of these converters is that although the profile height is only 0.28 inches (7.1mm) they contain internal transformers which provide for true isolation on the signal and reference inputs.

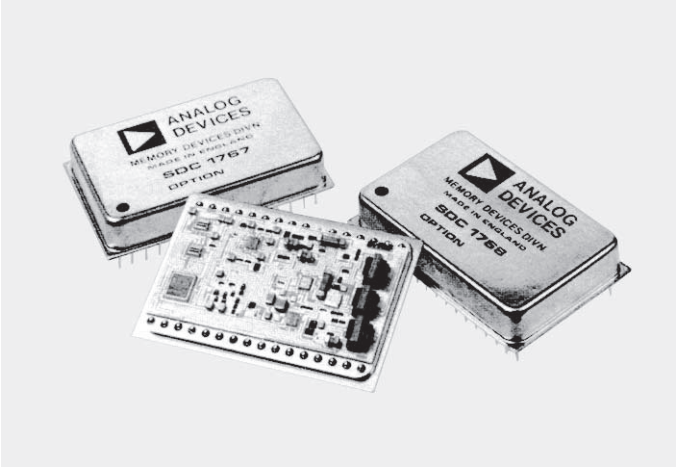
The converters are hermetically sealed in a metal 32-pin dual-in-line package.

To ensure a high level of reliability each converter receives a stringent pre-cap visual inspection, constant acceleration, final electrical test, burn-in and gross leak test.

Devices that are processed in accordance with MIL-STD-883, Method 5008, Class B, receive further levels of testing and screening to ensure extremely high levels of reliability.

*Unique Feature

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MODELS AVAILABLE

The two synchro/resolver-to-digital converters described in this data sheet differ primarily in the areas of resolution, accuracy and dynamic performance as follows:

Model SDC1767XYZ is a 12-bit converter with an accuracy of ± 8.5 arc minutes and a resolution of 5.3 arc minutes, with the addition of analog velocity output—error output and increased tracking rate, over our model SDC1742.

Model SDC1768XYZ is a 14-bit converter with an overall accuracy of ± 5.3 arc minutes and a resolution of 1.3 arc minutes with the addition of analog velocity output—error output, over our model SDC1740.

Both models have an operating temperature range of $-55°C$ to $+125°C$.

The XYZ code defines the option as follows: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the signal and reference voltage and whether it will accept synchro or resolver format.

More information about the option codes is given under the heading of "Ordering Information".

P.O. Box 280; Norwood, Massachusetts 02062 U.S.A.
Tel: 617/329-4700 **Twx: 710/394-6577**
Telex: 924491 **Cables: ANALOG NORWOODMASS**

SPECIFICATIONS (typical @ +25°C, unless otherwise noted)

Models	SDC/RDC1767	SDC/RDC1768
ACCURACY[1,2] (max error on all options)	±8.5 arc min	±5.3 arc min
RESOLUTION	12 Bits (1LSB = 5.3 arc min)	14 Bits (1LSB = 1.3 arc min)
OUTPUT	12-Bits Parallel Natural Binary	14-Bit Parallel Natural Binary
SIGNAL & REFERENCE FREQUENCY	400Hz or 2.6kHz	*
SIGNAL VOLTAGE (Line-to-Line)	90V, 26V or 11.8V rms	*
SIGNAL IMPEDANCE		
90V Signal	200k (Resistive)	*
26V Signal	57.7k (Resistive)	*
11.8V Signal	26k (Resistive)	*
REFERENCE VOLTAGE	115V, 26V or 11.8V rms	*
REFERENCE IMPEDANCE		
115V Reference	120k (Resistive)	*
26V Reference	27k (Resistive)	*
11.8V Reference	12.3k (Resistive)	*
TRANSFORMER ISOLATION	350V dc	*
TRACKING RATE (min)	36 R.P.S.	18 R.P.S.
ACCELERATION CONSTANT (K_a)	156,800/sec^2	55,000/sec^2
STEP RESPONSE (179° Step for Settling to 1LSB of Error)	55ms	150ms
POWER LINES		
+15V	14mA (typ) 17mA (max)	*
−15V	14mA (typ) 16mA (max)	*
+5V	60mA (typ) 72mA (max)	*
POWER DISSIPATION	0.72 Watts (typ) 0.86 Watts (max)	* *
DATA LOGIC OUTPUT[3]	6 TTL Loads	*
BUSY OUTPUT LOGIC LOADING[2]	2 TTL Loads	*
BUSY LOGIC OUTPUT WIDTH	1.2μs (typ) 3μs (max)	*
VELOCITY OUTPUT		
Scaling	±10V ±1mA @ max tracking rate for the converter (max tracking rate = guaranteed min plus 50%)	
ERROR OUTPUT ±1mA max		
Normal Operation	<±30mV	*
Error Condition	>±200mV	*
INHIBIT INPUT (to INHIBIT)	Logic "0" 1 TTL Load	*
ENABLE INPUTS (to ENABLE)[4]	Logic "0" 1 TTL Load	*
TEMPERATURE RANGE	Option 4YZ	
Operating	−55°C to +125°C	*
Storage	−65°C to +150°C	*
DIMENSIONS	1.74" × 1.14" × 0.28" (44.2 × 28.9 × 7.1mm)	* *
WEIGHT	0.8 oz (23 grams)	*

NOTES

[1] Specified over the appropriate operating temperature range and for: (a) ±10% signal and reference amplitude variation; (b) 10% signal and reference harmonic distortion; (c) ±15% power supply variation; (d) ±10% variation in reference frequency.

[2] 2.6kHz options accuracy decreases 1 × 1.3 arc min on SDC/RDC1768.

[3] Schottky logic loading rules apply.

[4] $\overline{\text{ENABLE M}}$ enable most significant 8 bits. $\overline{\text{ENABLE L}}$ enable least significant 4 bits (or 6 bits for SDC/RDC1768).

*Specifications same as SDC/RDC1767.

Specifications subject to change without notice.

THEORY OF OPERATION

If the unit is a synchro-to-digital converter the 3-wire synchro output will be connected to S1, S2 and S3 on the unit and the Scott T transformer pair will convert these signals into resolver format.

$$\text{i.e.,} \quad V_1 = K\,E_O \sin \omega t \sin \theta$$
$$V_2 = K\,E_O \sin \omega t \cos \theta$$

Where θ is the angle of the synchro shaft.

If the unit is a resolver-to-digital converter, the 4-wire resolver output will be connected to S1, S2, S3 and S4 on the unit and the transformers will act purely as isolators.

To understand the conversion process, assume that the current word state of the up-down counter is ϕ.

The V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give:

$$K\,E_O \sin \omega t \sin \theta \cos \phi$$
$$\text{and} \quad K\,E_O \sin \omega t \cos \theta \sin \phi$$

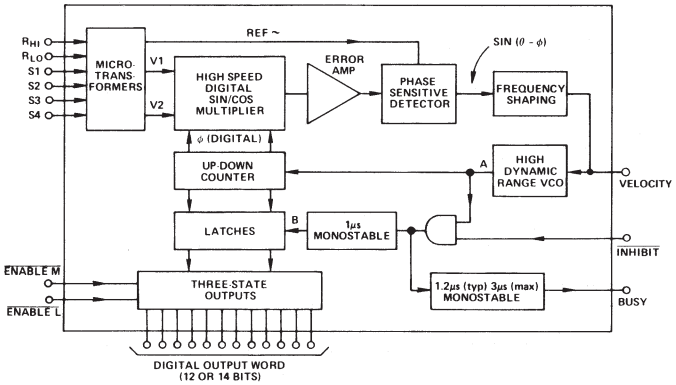
These signals are subtracted by the error amplifier to give:

$$K\,E_O \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$$
$$\text{or} \quad K\,E_O \sin \omega t \sin (\theta - \phi)$$

A phase sensitive detector, integrator and Voltage Controlled Oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ) equals, within the rated accuracy of the converter, the synchro shaft angle θ.

Assuming that the "$\overline{\text{INHIBIT}}$" is at a logic high state, then the digital word θ will be strobed into the latches 1μs after the updown counter has been updated. If the three state "$\overline{\text{ENABLE}}$" is at a logic low, then the digital output word will be presented to the output pins of the unit.



Functional Diagram

DATA TRANSFER

Data transfer from the converters is straightforward.

Consider the timing sequence shown in the timing diagram which assumes that the input to the converter is changing.

From this diagram, it can be seen that there are two ways to transfer data.

One method is to detect the state of the BUSY signal, which is high for up to 1.2μs (typical) while the updown counters and latches are settling, and transfer data when it is in a low state.

An alternative method is to use the "$\overline{\text{INHIBIT}}$" input. As can be seen from the functional diagram, application of the "$\overline{\text{INHIBIT}}$" prevents the two monostables being triggered and consequently the latches being updated. Therefore, it follows that data will always be valid after 3μs has elapsed from the application of the $\overline{\text{INHIBIT}}$ (i.e., taken to logic low). It can also be seen that this method of data transfer is valid regardless of when $\overline{\text{INHIBIT}}$ is
applied.

The three-state $\overline{\text{ENABLE}}$ can be used at any time in order to present the data in the latches to the output pins. $\overline{\text{ENABLE M}}$ enables the most significant 8 bits while $\overline{\text{ENABLE L}}$ enables the least significant 4 bits (6 bits in the case of the SDC/RDC1768).

Note that the operation of the internal converter loop cannot be affected in any way by the logic state present on the $\overline{\text{INHIBIT}}$ and $\overline{\text{ENABLE}}$ pins.

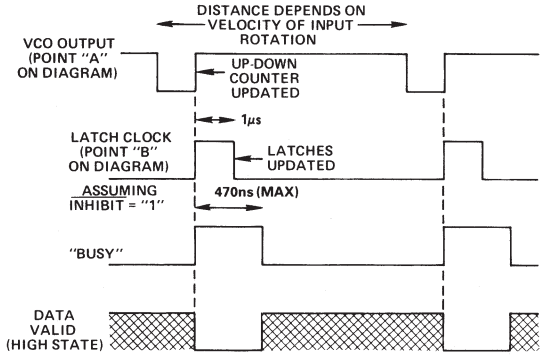


Figure 1. Timing Diagram

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12 (LSB 1767)	0.0879
13	0.0439
14 (LSB 1768)	0.0220

Table I. Bit Weight Table

CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, should be connected to the "+15V", "−15V" and "+5V" pins with the common connection to the ground pin "GND". It is suggested that a parallel combination of a 0.1μF and a 6.8μF capacitor is placed in each of the three positions from "+15V" to "GND", from "−15V" to "GND" and from "+5V" to "GND".

The pin marked "case" is connected electrically to the case and should be taken to a convenient zero volt potential in the system.

The digital output is taken from pin "1" through to pin "12" for the SDC/RDC1767 and pin "1" through to pin "14" for the SDC/RDC1768 where pin "1" is the MSB.

The reference connections are made to "R_{HI}" and "R_{LO}".

In the case of a synchro, the signals are connected to "S1", "S2" and "S3" according to the folowing convention:

$$E_{S1-S3} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } \theta$$
$$E_{S3-S2} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } (\theta + 120°)$$
$$E_{S2-S1} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } (\theta + 240°)$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$$E_{S1-S3} = E_{RLO-RHI} \text{ Sin } \omega t \text{ Sin } \theta$$

$$E_{S2-S4} = E_{RHI-RLO} \text{ Sin } \omega t \text{ Cos } \theta$$

The "BUSY", "$\overline{\text{INHIBIT}}$" and "$\overline{\text{ENABLE}}$" pins should be connected as described under the heading "Data Transfer".

RESISTIVE SCALING OF INPUTS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

To calculate the values of the external scaling resistors in the case of a synchro converter, add 1.11kΩ per extra volt of signal in series with "S1", "S2" and "S3", and 1kΩ per extra volt of reference in series with "R_{HI}".

In the case of a resolver-to-digital converter, add 2.22kΩ in series with "S1" and "S2" per extra volt of signal and 1kΩ per extra volt of reference in series with "R_{HI}".

VELOCITY OUTPUT

An internal control signal of the Type II tracking converter is voltage proportional to the input angular velocity. The voltage is negative for increasing angle and positive for decreasing angle. The values of these voltages for the different models is shown under the specification section. This voltage forming part of the internal control closed loop is not tightly controlled or characterized.

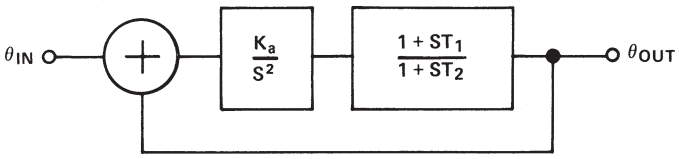
ERROR OUTPUT

An output voltage is provided that originates in the control loop near the Sin (θ – 0) null point. This voltage is not linear with error and should only be used as a BUILT IN TEST POINT.

While the converter is operating within the specified limits this voltage will remain below ±30mV. However, if the converter fails to track the input angle, or when the input acceleration is too great, there will be a sudden transition to ±200mV.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below:



Open loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_a}{S^2} \cdot \frac{1 + ST_1}{1 + ST_2}$$

Closed loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + ST_1}{1 + ST_1 + \frac{S^2}{K_a} + \frac{S^3 T_2}{K_a}}$$

Model SDC/RDC1767

where $K_a = 156{,}800$
$T_1 = 0.00622$
$T_2 = 0.00119$

Refer: – Figure 2

Model SDC/RDC1768

where $K_a = 55{,}000$
$T_1 = 0.0056$
$T_2 = 0.00085$

Refer: – Figure 3

ACCELERATION ERROR

A tracking converter employing a type 2 servo loop does not suffer any velocity lag; however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$K_a = \frac{\text{Input acceleration}}{\text{Error in output angle}}$$

The numerator and denominator have the same units. K_a does not define maximum acceleration only the error due to acceleration, maximum acceleration is in the region of 5 times the K_a figure.

An example using the K_a of the SDC/RDC1768.

Acceleration of 5 revolutions sec^{-2} with $K_a = 55{,}000$

$$\text{error in LSB's} = \frac{5 \times 16{,}384}{55{,}000} = 1.5\text{LSB}.$$

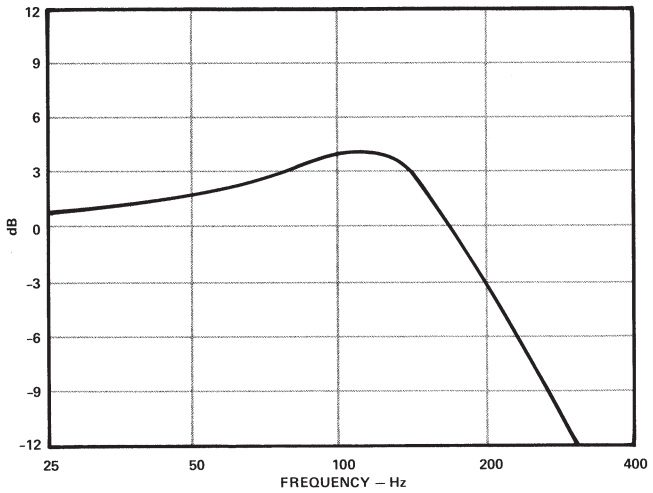


Figure 2.

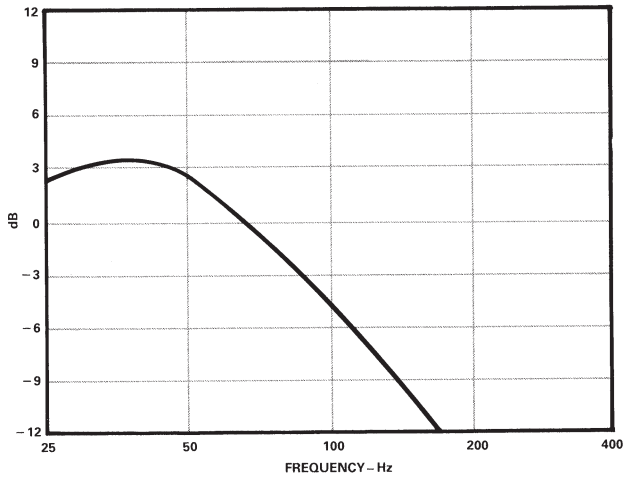


Figure 3.

ABSOLUTE MAXIMUM INPUTS

$+V_S$[1] to GND	0V to +17V dc
$-V_S$[1] to GND	0V to −17V dc
+5V[2]	0V to +5.5V dc
R_{HI} to GND	±350V dc
S_1, S_2, S_3, S_4 to GND	±350V dc
Case to GND	±20V dc
Any Logical Input	−0.4V to +5.5V dc

CAUTION:

1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
2. The +5 volt power supply must *never* go below GND potential.

OTHER PRODUCTS

Many other hybrid products concerned with the conversion of synchro data are manufactured by us, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application, please contact our Applications Engineering Department.

The *IRDC1732* is a low cost hybrid Inductosyn™ or resolver-to-digital converter with a tri-state latched 12-bit natural binary output.

The *DRC1765* and *DRC1766* are 14- and 16-bit natural binary latched input hybrid digital-to-resolver converters. The accuracies available are ±2 and ±4 arc mins., and the outputs of ±10V can supply 4.3mA peak.

The *DRC1745* and *DRC1746* are 14- and 16-bit natural binary latched output hybrid digital-to-resolver converters. The accuracies available are ±2 and ±4 arc mins., and the outputs can supply ±2VA at 7V rms.

The *SDC1740*, *SDC1741* and *SDC1742* are hybrid synchro-to-digital converters with transformer isolation similar to the SDC1767, SDC1768 described in this data sheet, but without the velocity and error output, and at reduced cost.

As well as this range of hybrid converters, we manufacture an extensive range of modular products for synchro data conversion, with operating temperature ranges of 0 to +70°C and −55°C to +105°C.

Inductosyn is a trademark of Farrand Industries Inc.

RELIABILITY

The reliability of these products is very high due to the extensive use custom chip circuits that decreases the active components.

Calculations of the MTBF figure under various environmental conditions are available on request.

As an example of the Mean Time Between Failures (MTBF) calculated according to MIL-HDBK-217D, the curve below shows the MTBF in years versus case temperature in Naval Sheltered conditions.

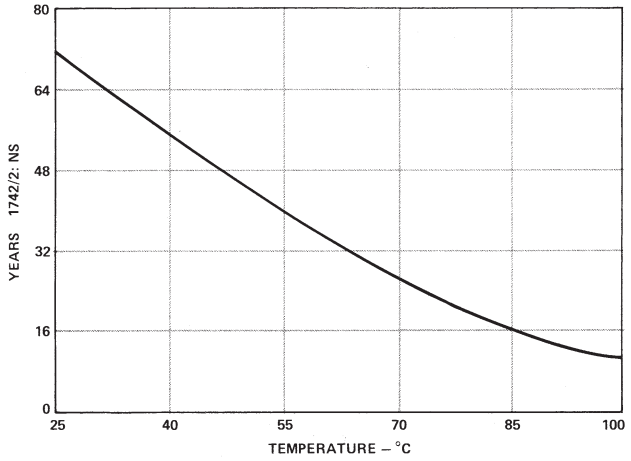
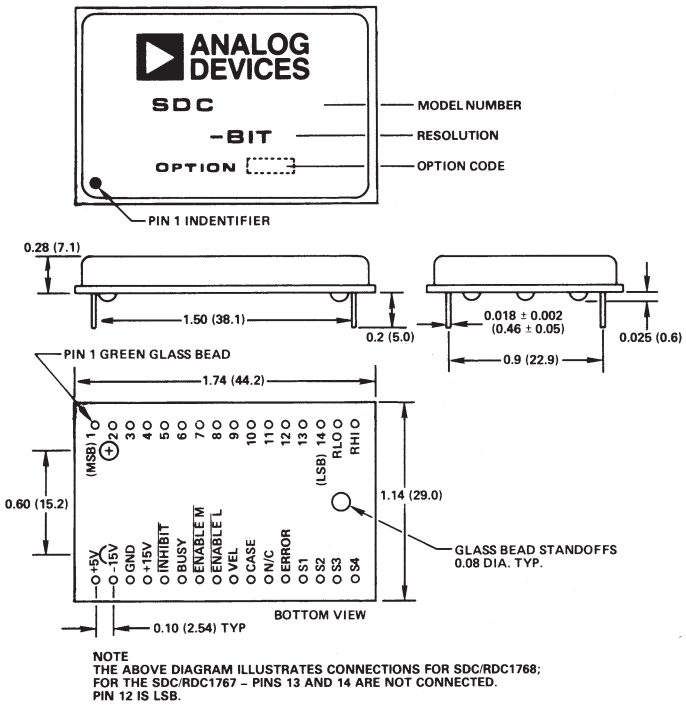


Figure 4.

OUTLINE DIMENSIONS
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).



NOTE
THE ABOVE DIAGRAM ILLUSTRATES CONNECTIONS FOR SDC/RDC1768; FOR THE SDC/RDC1767 – PINS 13 AND 14 ARE NOT CONNECTED. PIN 12 IS LSB.

C830–20–4/84

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

PROCESS	CONDITIONS
1. Pre-Cap Visual Inspection	In-House Criteria
2. Constant Acceleration	5000G
3. Burn-In	160 hrs. at 125°C
4. Gross Leak Test	In-House Criteria
5. Final Electrical Test	Performed at 25°C

PROCESSING TO MIL-STD-883

All models ordered to the requirements of MIL-STD-883, Method 5008, Class B are identified with a /883B suffix, and receive the following processing:

1. Pre-Cap Visual Inspection	2017
2. Stabilization Bake	1008, 24 hours @ +150°C
3. Temperature Cycling	1010, Test Condition C, 10 Cycles, −65°C to +150°C
4. Constant Acceleration	2001, Y_1 plane, 5000G
5. Seal Test, Fine and Gross	1014, Test Condition A and C
6. Operating Burn-In	1015, Test Condition B, 160 hours @ +125°C
7. Final Electrical Testing	Performed at max and min operating temperatures
8. External Visual Inspection	2009

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by an option code in order to fully define them. All the standard options and their option codes are shown below. For options not shown, please consult the factory.

SDC 1767 X Y Z

SDC = Synchro-to-Digital Converter
RDC = Resolver-to-Digital Converter

1767 = 12-Bit Resolution, ±8.5 arc min Accuracy
1768 = 14-Bit Resolution, ±5.3 arc min Accuracy

X = 4 −55°C to +125°C Operating Temperature Range

Y = 1 400Hz Reference Frequency
Y = 4 2.6kHz Reference Frequency

Z = 1 Signal	11.8V	Reference	26V	Synchro
Z = 2 Signal	90V	Reference	115V	Synchro
Z = 3 Signal	11.8V	Reference	11.8V	Resolver
Z = 4 Signal	26V	Reference	26V	Resolver
Z = 8 Signal	11.8V	Reference	26V	Resolver

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