20V P-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI5060-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D T_C = +25°C
-20V	2.2mΩ @ V_{GS} = -10V	-150A
	2.55mΩ @ V_{GS} = -4.5V	-120A
	4.0mΩ @ V_{GS} = -2.5V	-90A

Features

- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On State Losses
- <1.1mm Package Profile – Ideal for Thin Applications
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Description

This new generation MOSFET is designed to minimize $R_{DS(ON)}$ and yet maintain superior switching performance. This device is ideal for use in notebook battery power management and load switch.

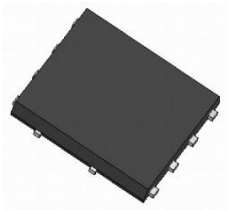
Mechanical Data

- Case: PowerDI®5060-8
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish - Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

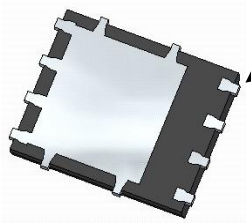
Applications

- Switch

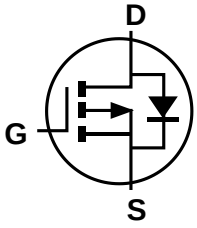
PowerDI5060-8



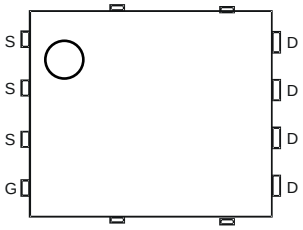
Top View



Bottom View



Internal Schematic



Top View
Pin Configuration

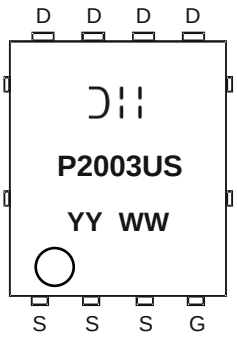
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2003UPS-13	PowerDI5060-8	2,500 / Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

PowerDI5060-8



=Manufacturer's Marking
P2003US = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 17 = 2017)
WW = Week Code (01 to 53)

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	±12	V
Continuous Drain Current, V_{GS} = -10V (Note 7)	T_C = +25°C T_C = +70°C	I_D	-150 -120	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	-350	A
Maximum Continuous Body Diode Forward Current (Note 7)		I_S	-120	A
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)		I_{SM}	-350	A
Avalanche Current, L = 0.1mH (Note 8)		I_{AS}	-32	A
Avalanche Energy, L = 0.1mH (Note 8)		E_{AS}	67	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	1.4	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	90	°C/W
Total Power Dissipation (Note 6)		P_D	2.7	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	46	°C/W
Total Power Dissipation (Note 7)		P_D	80	W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	1.5	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	µA	V_{DS} = -16V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±12V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.5	—	-1.4	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	1.7	2.2	mΩ	V_{GS} = -10V, I_D = -25A
		—	1.9	2.55		V_{GS} = -4.5V, I_D = -20A
		—	2.5	4.0		V_{GS} = -2.5V, I_D = -15A
Diode Forward Voltage	V_{SD}	—	-0.6	-1.1	V	V_{GS} = 0V, I_S = -5A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	8352	—	pF	V_{DS} = -10V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	1406	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	599	—	pF	
Gate Resistance	R_g	—	13.2	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	79	—	nC	V_{DS} = -10V, I_D = -20A
Total Gate Charge (V_{GS} = -10V)	Q_g	—	177	—	nC	
Gate-Source Charge	Q_{gs}	—	14.3	—	nC	
Gate-Drain Charge	Q_{gd}	—	19.8	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	7.8	—	ns	V_{DD} = -10V, V_{GEN} = -4.5V, R_{GEN} = 1Ω, I_D = -10A
Turn-On Rise Time	t_R	—	4.9	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	377	—	ns	
Turn-Off Fall Time	t_F	—	189	—	ns	
Reverse Recovery Time	t_{RR}	—	49	—	ns	I_F = -10A, di/dt = 100A/µs
Reverse Recovery Charge	Q_{RR}	—	39	—	nC	

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Thermal resistance from junction to soldering point (on the exposed drain pad).
8. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

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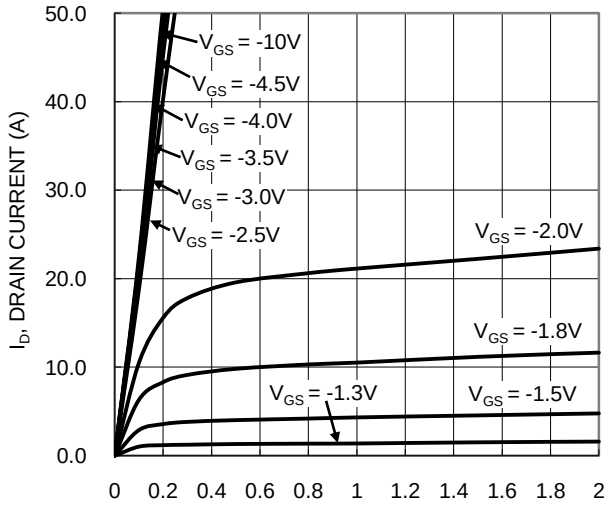


Figure 1.Typical Output Characteristic

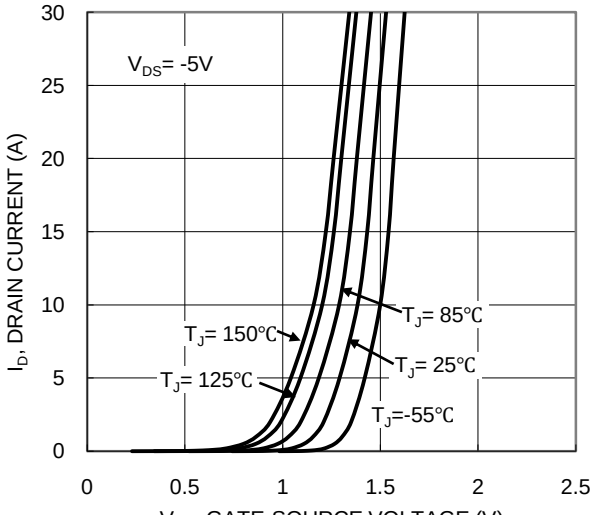


Figure 2. Typical Transfer Characteristic

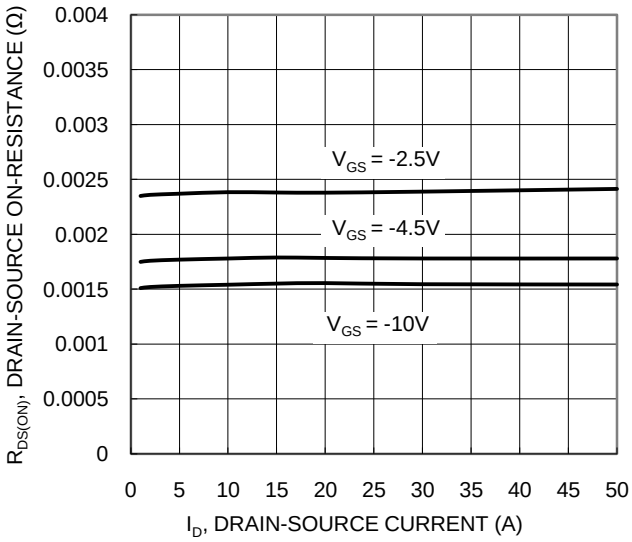


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

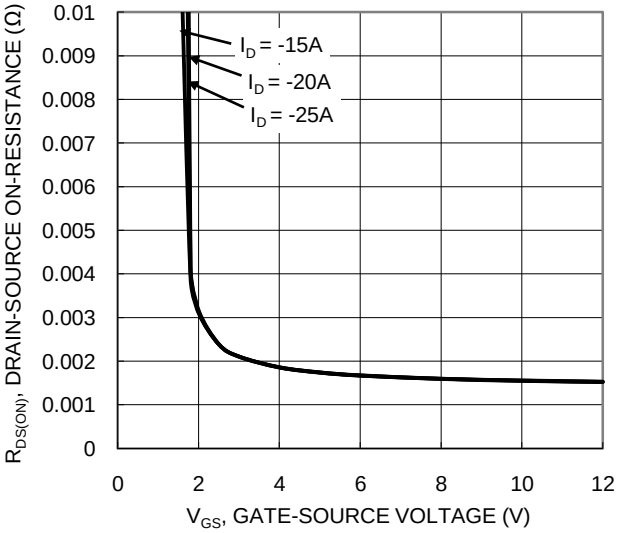


Figure 4. Typical Transfer Characteristic

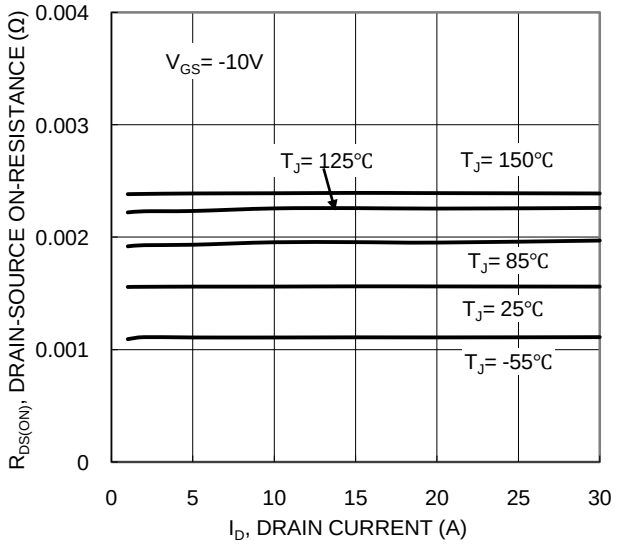


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

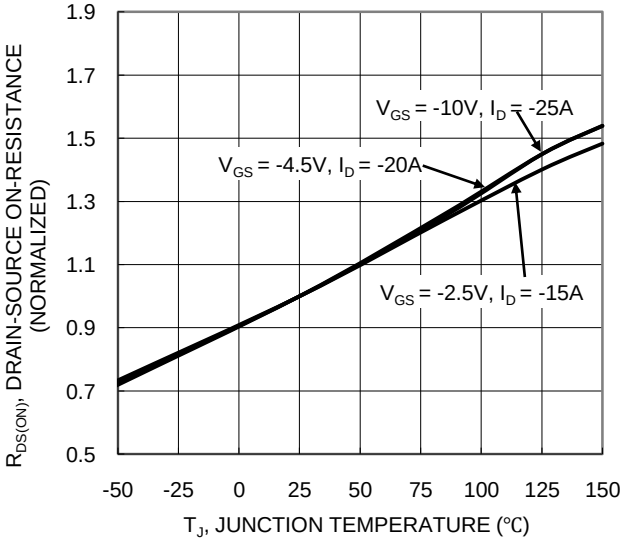


Figure 6. On-Resistance Variation with Junction Temperature

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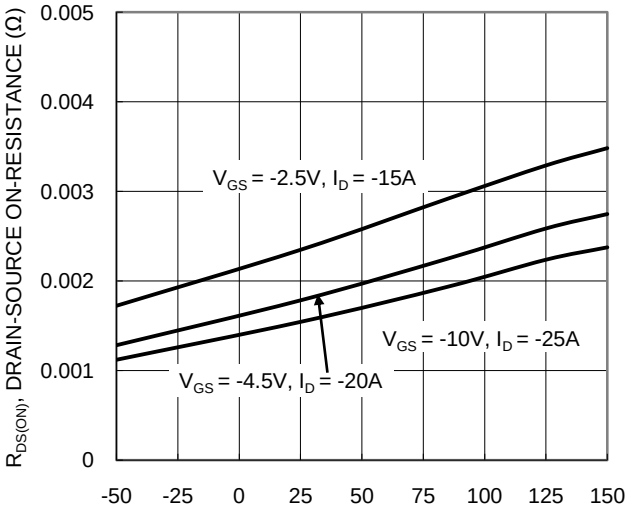


Figure 7. On-Resistance Variation with Junction Temperature

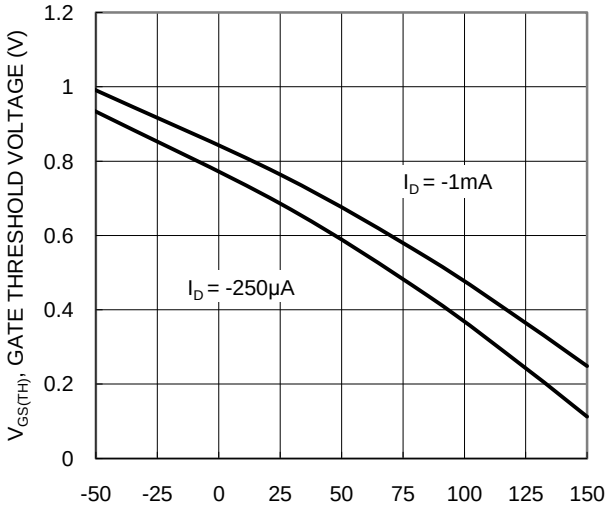


Figure 8. Gate Threshold Variation vs. Junction Temperature

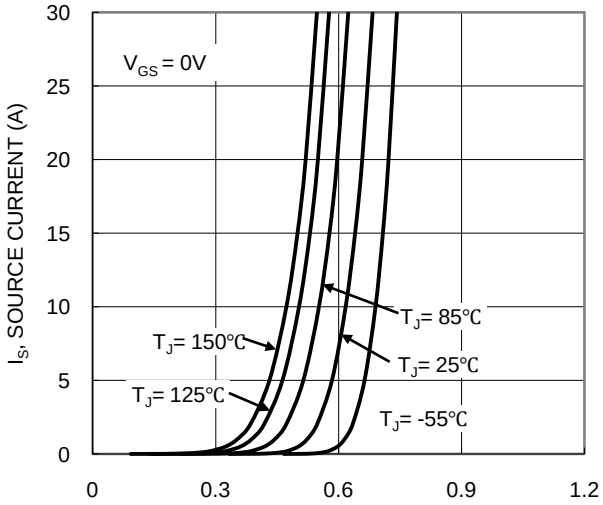


Figure 9. Diode Forward Voltage vs. Current

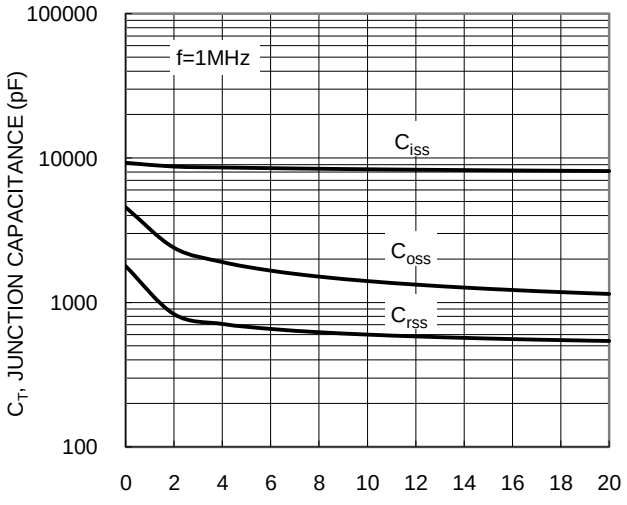


Figure 10. Typical Junction Capacitance

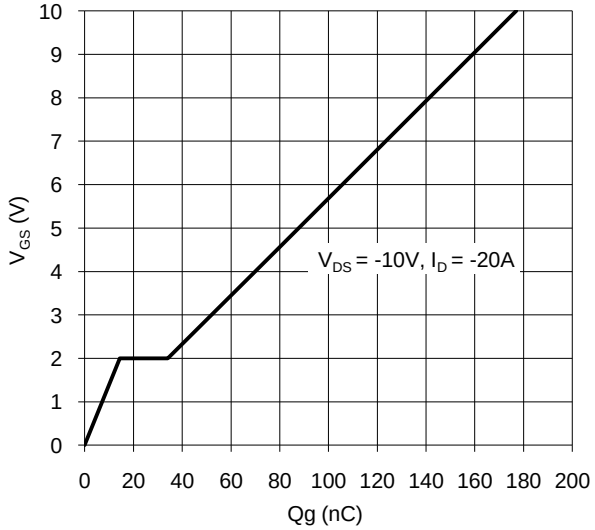


Figure 11. Gate Charge

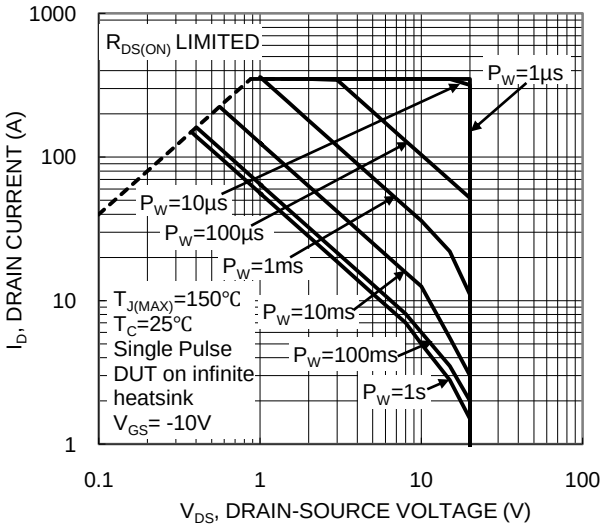


Figure 12. SOA, Safe Operation Area

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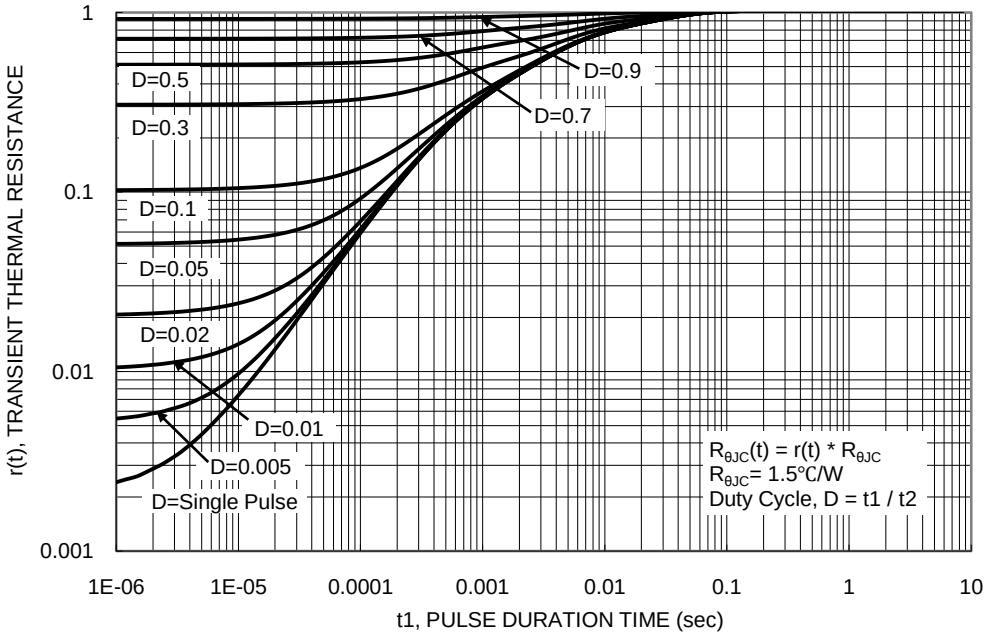


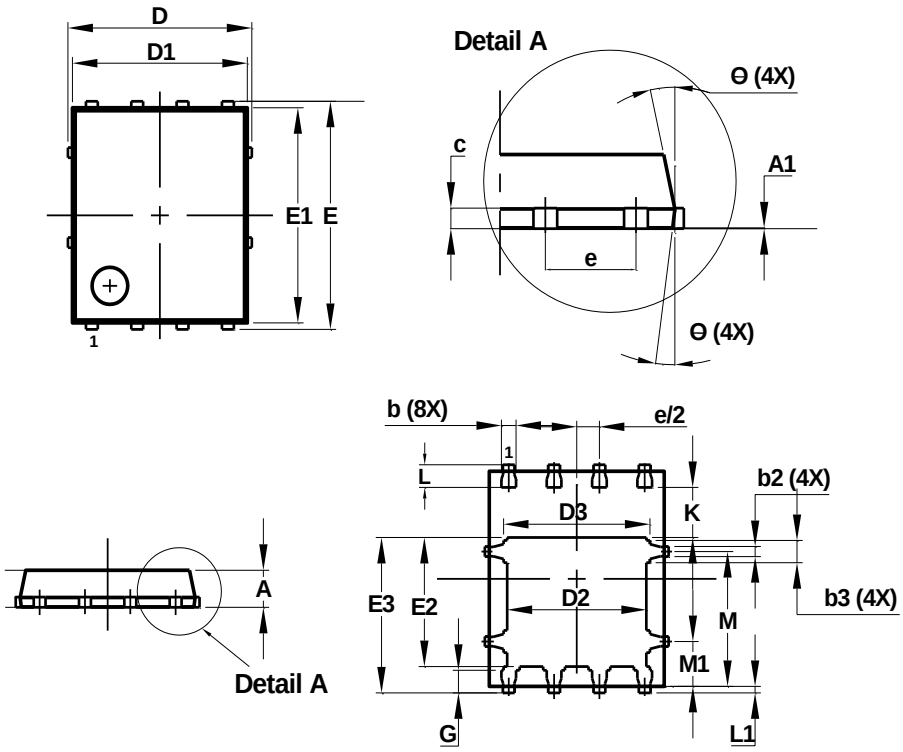
Figure 13. Transient Thermal Resistance

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Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8

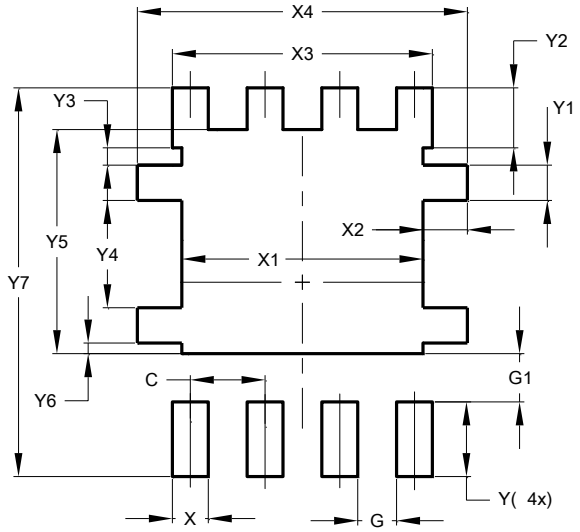


PowerDI5060-8			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0.00	0.05	–
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	–	–
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
Θ	10°	12°	11°
Θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

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