ES29DL320

32Mbit(4M x 8/2M x 16)
CMOS 3.0 Volt-only, Simultaneous Operation Flash Memory

GENERAL FEATURES

- **Single power supply operation**
  - 2.7V - 3.6V for read, program and erase operations
- **Simultaneous Read/Write operations**
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency between read and write operations
- **Multi-Bank architecture**
  - Read may occur in any of the banks not being written or erased
  - Multi-Bank may be grouped by customer to achieve desired bank divisions
- **Top or Bottom boot block**
  - ES29DL320T for Top boot block device
  - ES29DL320B for Bottom boot block device
- **A 256 bytes of extra sector for security code**
  - Factory locked
  - Customer lockable
- **Package Options**
  - 48-pin TSOP
  - 48-ball FBGA
  - All Pb-free products are RoHS-Compliant
- **Low Vcc write inhibit**
- **Manufactured on 0.18um process technology**
- **Compatible with JEDEC standards**
  - Pinout and software compatible with single-power supply flash standard

DEVICE PERFORMANCE

- **Read access time**
  - 70ns/90ns for normal Vcc range (2.7V ~ 3.6V)
- **Program and erase time**
  - Program time : 6us/byte, 8us/word (typical)
  - Accelerated program time : 4us/word (typical)
  - Sector erase time : 0.7sec/sector (typical)
- **Power consumption (typical values)**
  - 15uA in standby or automatic sleep mode
  - 10mA active read current at 5MHz
  - 15mA active write current during program or erase
- **Minimum 100,000 program/erase cycles per sector**
- **20 Year data retention at 125^{o}C**

SOFTWARE FEATURES

- **Erase Suspend / Erase Resume**
- **Data# poll and toggle for program/erase status**
- **CFI (Common Flash Interface) supported**
- **Unlock Bypass Program**
- **Autoselect mode**
- **Auto-sleep mode after t_{ACC} + 30ns**

HARDWARE FEATURES

- **Hardware reset input pin (RESET#)**
  - Provides a hardware reset to device
  - Any internal device operation is terminated and the device returns to read mode by the reset
- **Ready/Busy# output pin (RY/BY#)**
  - Provides a program or erase operational status about whether it is finished for read or still being progressed
- **WP#/ACC input pin**
  - Two outermost boot sectors are protected when WP# is set to low, regardless of sector protection
  - Program speed is accelerated by raising WP#/ACC to a high voltage (8.5V ~ 9.5V)
- **Sector protection / unprotection (RESET# , A9)**
  - Hardware method of locking a sector to prevent any program or erase operation within that sector
  - Two methods are provided :
    - In-system method by RESET# pin
    - A9 high-voltage method for PROM programmers
- **Temporary Sector unprotection (RESET#)**
  - Allows temporary unprotection of previously protected sectors to change data in-system

GENERAL PRODUCT DESCRIPTION

The ES29DL320 is a 32 megabit, 3.0 volt-only flash memory device, organized as 4M x 8 bits (Byte mode) or 2M x 16 bits (Word mode) which is configurable by BYTE#. Eight boot sectors and sixty three main sectors with uniform size are provided : 8K bytes x 8 and 64K bytes x 63. The device is manufactured with ESI's proprietary, high performance and highly reliable 0.18um CMOS flash technology. The device can be programmed or erased in-system with standard 3.0 Volt Vcc supply (2.7V-3.6V) and can also be programmed in standard EPROM programmers. The device offers minimum endurance of 100,000 program/erase cycles and more than 20 years of data retention.

The ES29DL320 offers access time as fast as 70ns or 90ns, allowing operation of high-speed microprocessors without wait states. Three separate control pins are provided to eliminate bus contention : chip enable (CE#), write enable (WE#) and output enable (OE#).

All program and erase operation are automatically and internally performed and controlled by embedded program/erase algorithms built in the device. The device automatically generates and times the necessary high-voltage pulses to be applied to the cells, performs the verification, and counts the number of sequences. Some status bits (DQ7, DQ6 and DQ5) read by data# polling or toggling between consecutive read cycles provide to the users the internal status of program/erase operation: whether it is successfully done or still being progressed.

Extra Security Sector of 256 bytes

In the device, an extra security sector of 256 bytes is provided to customers. This extra sector can be used for various purposes such as storing ESN (Electronic Serial Number) or customer's security codes. Once after the extra sector is written, it can be permanently locked by the device manufacturer(**factory-locked**) or a customer(**customer-lockble**). At the same time, a **lock indicator bit** (**DQ7**) is permanently set to a 1 if the part is factory- locked, or set to 0 if it is customer-lockable.

Therefore, this lock indicator bit (DQ7) can be properly used to avoid that any customer-lockable part is used to replace a factory-locked part. The extra security sector is an extra memory space for customers when it is used as a customer-lockable version. So, it can be read and written like any other sectors. But it should be noted that the number of E/W(Erase and Write) cycles is limited to 300 times (maximum) only in the Security Sector.

Special services such as ESN and factory-locked are available to customers (ESI's **Special-Code service**) The ES29DL320 is completely compatible with the JEDEC standard command set of single power supply Flash. Commands are written to the internal command register using standard write timings of microprocessor and data can be read out from the cell array in the device with the same way as used in other EPROM or flash devices.

Simultaneous Read / Write Operation

The simultaneous read / write architecture provides simultaneous operation by dividing the memory space into multi-bank. Sector addresses are fixed, system software can be used to form user-defined bank groups.

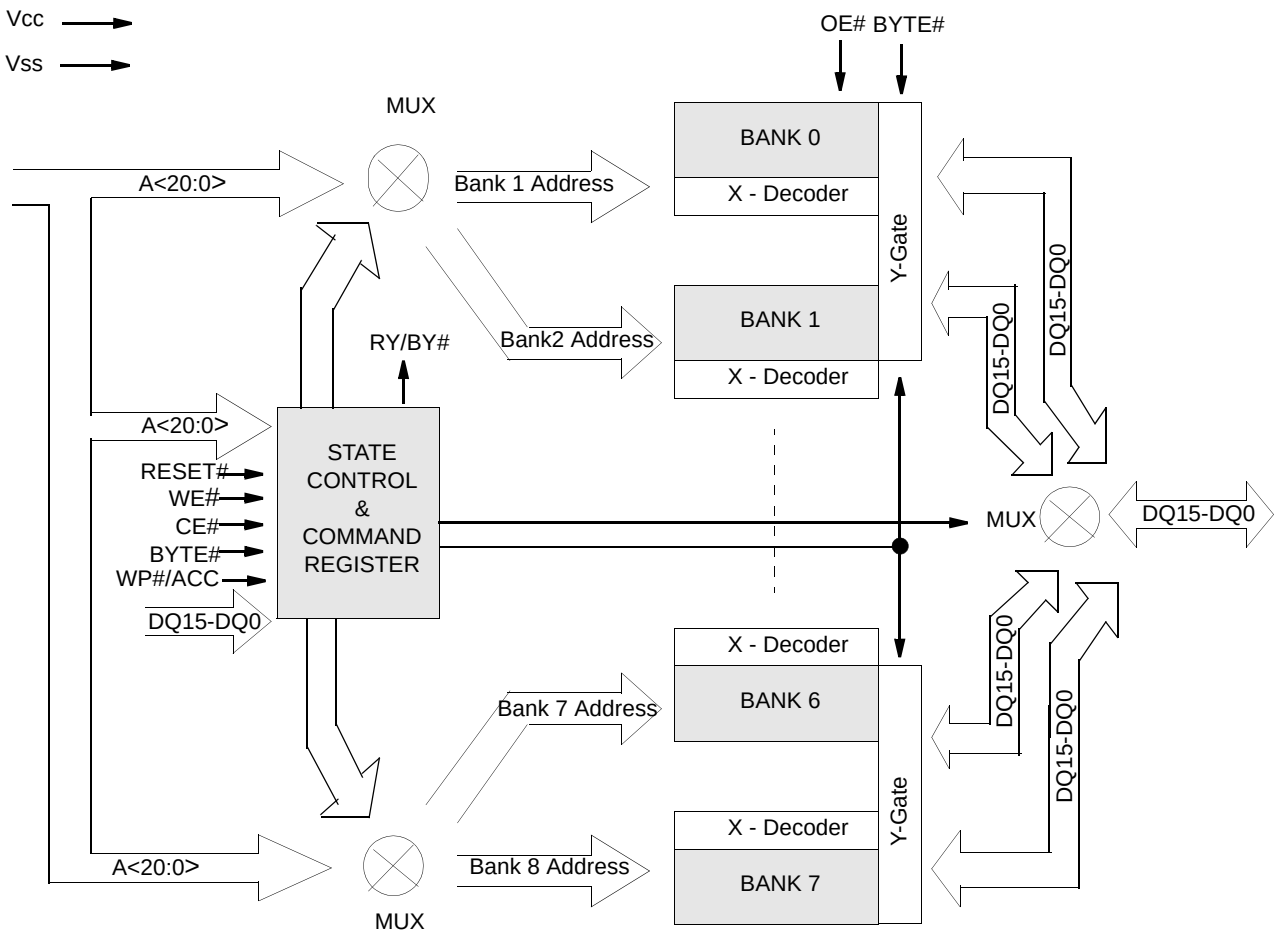
During an erase / program operation, any of the non-busy banks may be read from. Note that only two banks can operate simultaneously. The device allows a host system to program or erase in one bank, then immediately and simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The ES29DL320 can be organized as either a top or bottom boot sector configuration.

PRODUCT SELECTOR GUIDE

Family Part Number	ES29DL320	
Voltage Range	2.7V ~ 3.6V	
Speed Option	**70**	**90**
Max Access Time (ns)	70	90
CE# Access (ns)	70	90
OE# Access (ns)	30	40

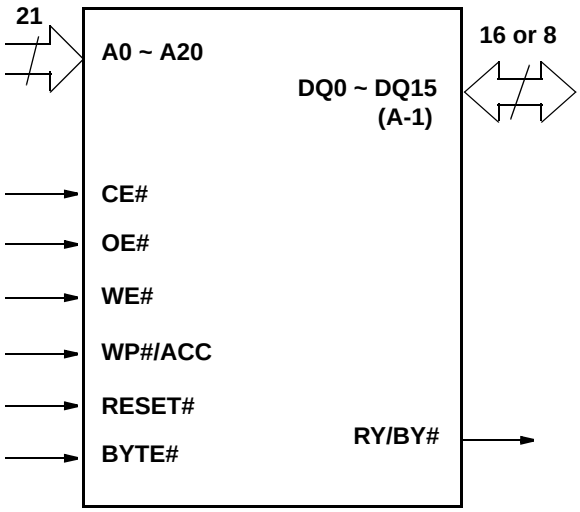
FUNCTION BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Description
A0-A20	21 Addresses
DQ0-DQ14	15 Data Inputs/Outputs
DQ15/A-1	DQ15 (Data Input/Output, Word Mode) A-1 (LSB Address Input, Byte Mode)
CE#	Chip Enable
OE#	Output Enable
WE#	Write Enable
WP#/ACC	Hardware Write Protect/Acceleration Pin
RESET#	Hardware Reset Pin, Active Low
BYTE#	Selects 8-bit or 16-bit mode
RY/BY#	Ready/Busy Output
Vcc	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
Vss	Device Ground
NC	Pin Not Connected Internally

LOGIC SYMBOL



CONNECTION DIAGRAM

48-Ball FBGA 6 x 8 mm)

(Top View, Balls Facing Down)

	C	D	E	F	G	H	J	K
7	A13	A12	A14	A15	A16	BYTE#	DQ15/ A-1	Vss
6	A9	A8	A10	A11	DQ7	DQ14	DQ13	DQ6
5	WE#	RESET#	NC	A19	DQ5	DQ12	Vcc	DQ4
4	RY/ BY#	WP#/ ACC	A18	A20	DQ2	DQ10	DQ11	DQ3
3	A7	A17	A6	A5	DQ0	DQ8	DQ9	DQ1
2	A3	A4	A2	A1	A0	CE#	OE#	Vss

DEVICE BUS OPERATIONS

Several device operational modes are provided in the ES29DL320 device. Commands are used to initiate the device operations. They are latched and stored into internal registers with the address and data information needed to execute the device operation.

The available device operational modes are listed in Table 1 with the required inputs, controls, and the resulting outputs. Each operational mode is described in further detail in the following subsections.

Read

The internal state of the device is set for the read mode and the device is ready for reading array data upon device power-up, or after a hardware reset. To read the stored data from the cell array of the device, CE# and OE# pins should be driven to V_{IL} while WE# pin remains at V_{IH}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins.

Word or byte mode of output data is determined by the BYTE# pin. No additional command is needed in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank stays at the read mode until another operation is activated by writing commands into the internal command register. Refer to the AC read cycle timing diagrams for further details (Fig. 18).

Simultaneous Read/Write Operation

This device is capable of reading data from one bank of memory while programming or erasing in the other bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 33 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the CMOS DC characteristics Table11 for further current specification.

Word/Byte Mode Configuration (BYTE#)

The device data output can be configured by BYTE# into one of two modes : word and byte modes**.** If the BYTE# pin is set at logic ‘1’, the device is configured in word mode, DQ0 - DQ15 are active and controlled by CE# and OE#. If the BYTE# pin is set at logic ‘0’, the device is configured in byte mode, and only data I/O pins DQ0 - DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8 - DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address.

Standby Mode

When the device is not selected or activated in a system, it needs to stay at the standby mode, in which current consumption is greatly reduced with outputs in the high impedance state.

The device enters the CMOS standby mode when CE# and RESET# pins are both held at Vcc±0.3V. (Note that this is a more restricted voltage range than $V_{IH.}$) If CE# and RESET# are held at V_{IH}, but not within Vcc±0.3V, the device will be still in the standby mode, but the standby current will be greater than the CMOS standby current (15uA typically). When the device is in the standby mode, only standard access time (t_{CE}) is required for read access, before it is ready for read data. And even if the device is deselected by CE# pin during erase or programming operation, the device draws active current until the operation is completely done. While the device stays in the standby mode, the output is placed in the high impedance state, independent of the OE# input.

The device can enter the deep power-down mode where current consumption is greatly reduced down to less than 15uA typically by the following three ways:

- **CMOS standby** (CE#, RESET# = Vcc ± 0.3V)
- **During the device reset** (RESET# = Vss ± 0.3V)
- **In Autosleep Mode** (after t_{ACC} + 30ns)

Refer to the CMOS DC characteristics Table11 for further current specification.

Autosleep Mode

The device automatically enters a deep power-down mode called the autosleep mode when addresses remain stable for t_{ACC}+30ns. In this mode, current consumption is greatly reduced (less than 15uA typical), regardless of CE#, WE# and OE# control signals.

Writing Commands

To write a command or command sequences to initiate some operations such as program or erase, the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}. For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to “BYTE# timings for Write Operations” in the Fig. 21 for more information.

Unlock Bypass Mode

To reduce more the programming time, an unlock-bypass mode is provided. Once a bank enters this mode, only two write cycles are required to initiate the programming operation instead of four cycles in the normal program command sequences which are composed of two unlock cycles, program set-up cycle and the last cycle with the program data and addresses. In this mode, two unlock cycles are saved (or bypassed).

Sector Addresses

The entire memory space of cell array is divided into a many of small sectors: 8kbytes x 8 boot sectors and 64Kbytes x 63 main sectors. In erase operation, a single sector, multiple sectors, or the entire device (chip erase) can be selected for erase. The address space that each sector occupies is shown in detail in the Table 3-4.

Accelerated Program Mode

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory. If the system asserts **V_{HH} (8.5~9.5V)** on this pin, the device automatically enters the previously mentioned **Unlock Bypass mode**, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. Only two-cycle program command sequences are required because the unlock bypass mode is automatically activated in this acceleration mode. The device returns to the normal operation when V_{HH} is removed from the WP#/ACC pin. It should be noted that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent or undesired behavior of the device may result.

Autoselect Mode

Flash memories are intended for use in applications where the local CPU alters memory contents. In such applications, manufacturer and device identification (ID) codes must be accessible while the device resides in the target system (the so called “in-system program”). On the other hand, signature codes have been typically accessed by raising A9 pin to a high voltage in PROM programmers. However, multiplexing high voltage onto address lines is not the generally desired system design practice. Therefore, in the ES29DL320 device an **autoselect command** is provided to allow the system to access the signature codes without any high voltage. The conventional **A9 high-voltage method** used in the PROM programmers for signature codes are still supported in this device.

If the system writes the autoselect command sequence, the device enters the Autoselect mode. The system can then read some useful codes such as manufacturer and device ID from the internal registers on DQ7 - DQ0. Standard read cycle timings apply in this mode. In the Autoselect mode, the following four informations can be accessed through either autoselect command method or A9 high-voltage autoselect method. Refer to the Table 2.

- **Manufacturer ID**
- **Device ID**
- **Security sector lock-indicator**
- **Sector protection verify**

Hardware Device Reset (RESET#)

The RESET# pin provides a hardware method of resetting the device to read array data. When the RESET# pin is driven low for at least a period of t_{RP} , the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once after the device is ready to accept another command sequence, to ensure data integrity.

CMOS Standby during Device Reset

Current is reduced for the duration of the RESET# pulse. When RESET# is held at Vss $\pm$ 0.3V, the device draws the greatly reduced CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within Vss$\pm$0.3V, the standby current will be greater.

RY/BY# and Terminating Operations

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is completed, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is completed. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data after the RESET# pin returns to V_{IH}, which requires a time of t_{RH}.

RESET# tied to the System Reset

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory. Refer to the AC Characteristics tables for RESET# parameters and to Fig. 19 for the timing diagram.

SECTOR GROUP PROTECTION

The ES29DL320 features hardware sector group protection. A sector group consists of two or more adjacent sectors that are protected or unprotected at the same time. In the device, sector protection is performed on the group of sectors previously defined in the Table 3-4. Once after a group of sectors are protected, any program or erase operation is not allowed in the protected sector group. The previously protected sectors must be unprotected by one of the unprotect methods provided here before changing data in those sectors. Sector protection can be implemented via two methods.

- **In-system protection**
- **A9 High-voltage protection**

To check whether the sector group protection was successfully executed or not, another operation called “**protect verification**” needs to be performed after the protection operation on a group of sectors. All protection and protect verifications provided in the device are summarized in detail at the Table 1.

In-System Protection

“In-system protection”, the primary method, requires V_{ID} (8.5V~12.5V) on the **RESET#** with A6=0, A1=1, and A0=0. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing. Refer to Fig. 29 for timing diagram and Fig. 3 for the protection algorithm.

A9 High-Voltage Protection

“High-voltage protection”, the alternate method intended only for programming equipment, must force V_{ID} (8.5V~12.5V) on address pin **A9** and control pin **OE#** with A6=0, A1=1 and A0=0. Refer to Fig. 31 for timing diagram and Fig. 5 for the protection algorithm.

SECTOR UNPROTECTION

The previously protected sectors must be unprotected before modifying any data in the sectors. The sector unprotection algorithm unprotects all sectors in parallel. All unprotected sectors must first

be protected prior to the first sector unprotection write cycle to avoid any over-erase due to the intrinsic erase characteristics of the protection cell. After the unprotection operation, all previously protected sectors will need to be individually re-protected. Standard microprocessor bus cycle timings are used in the unprotection and unprotect verification operations. Three unprotect methods are provided in the ES29DL320 device. All unprotection and unprotect verification cycles are summarized in detail at the Table 1.

- **In-system unprotection**
- **A9 High-voltage unprotection**
- **Temporary sector unprotection**

In-System Unprotection

"In-system unprotection", the primary method, requires V_{ID} (8.5V~12.5V) on the **RESET#** with A6=1, A1=1, and A0=0. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing. Refer to Fig. 29 for timing diagram and Fig. 4 for the unprotection algorithm.

A9 High-Voltage Unprotection

"High-voltage unprotection", the alternate method intended only for programming equipment, must force V_{ID} (8.5V~12.5V) on address pin **A9** and control pin **OE#** with A6=1, A1=1 and A0=0. Refer to Fig. 32 for timing diagram and Fig. 6 for the unprotection algorithm.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID} (8.5V~12.5V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Fig. 1 shows the algorithm, and Fig. 27 shows the timing diagrams for this feature.

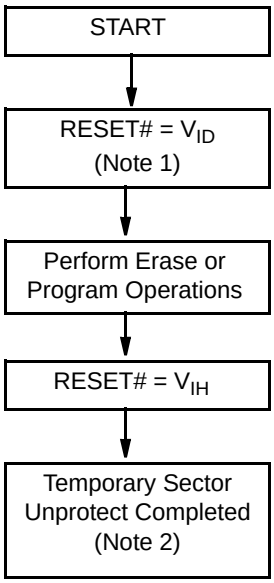
WRITE PROTECT (WP#)

The write protect function provides a hardware method of protecting certain boot sectors without using V_{ID}. This function is one of two provided by the WP#/ACC pin.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the **two "outermost" 8Kbytes boot sectors** independently of whether those sectors were protected or unprotected using the method described in "Sector Group Protection and Unprotection". The two outermost of 8 Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the two outermost 8 Kbyte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in "Sector Group Protection and Unprotection".

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.



Notes:

1. All protected sectors are unprotected (If WP#/ACC = V_{IL}, outermost boot sectors will remain protected).
2. All previously protected sectors are protected once again.

Figure 1. Temporary Sector Unprotect Operation

SECURITY SECTOR

The security sector of the ES29DL320 device provides an extra flash memory space that enables permanent part identification through an Electronic Serial Number (ESN). The security sector uses a S**ecurity Lock-Indicator Bit (DQ7)** to indicate whether or not the security sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field**.** Note that the ES29DL320 has a security sector size of **256 bytes**.

Security Lock-Indicator Bit (DQ7)

In the device, the security sector can be provided in either factory locked version or customer lockable version. The **factory-locked version** is always protected when shipped from the factory, and has the security lock-indicator bit permanently set to a "1". The **customer-lockable version** is shipped with the security sector unprotected, allowing customers to utilize the sector in any manner they choose. The customer-lockable version has the security lock-indicator bit permanently set to a "0". Thus, the security lock-Indicator bit prevents customer-lockble devices from being used to replace devices that are factory locked.

Access to the Security Sector

The security sector can be accessed through a command sequence: **Enter security** and **Exit security** sector commands. After the system has written the Enter security sector command sequence, it may read the security sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the exit security sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device returns to read mode in which the normal boot sectors can be accessed, instead of the security sector.

Factory-Locked Device

In a factory-locked device, the security sector is protected when the device is shipped from the factory. The security sector cannot be modified in any way. The device is available preprogrammed with one of the following:

- **A random, secure ESN (16 bytes) only**
- **Customer code through the ESI's special-code service**
- **Both a random, secure ESN and customer code through the ESI's special-code service.**

ESN (Electronic Serial Number)

In devices that have an ESN, a Bottom Boot device will have the 16-byte (8-word) ESN in sector 0 at addresses 000000h-00000Fh in byte mode (or 000000h-000007h in word mode). In the Top Boot device the ESN will be in sector 70 at addresses 3FFF00h-3FFF0Fh in byte mode (or 1FFF80h-1FFF87h in word mode). Note that in upcoming top boot versions of this device, the ESN will be located in sector 70 at addresses 3FFF00h-3FFF0Fh in byte mode (or 1FFF80h-1FFF87h in word mode).

ESI's Special-Code Service

Customers may opt to have their code programmed by ESI through the ESI's Special-Code service. ESI programs the customer's code, with or without the random ESN. The devices are then shipped from ESI's factory with the Security Sector permanently locked. Contact an ESI representative for details on using ESI's Special-Code service.

Customer-Lockable Device

The customer lockable version allows the security sector to be freely programmed or erased and then permanently locked. Note that the ES29DL320 has a security sector size of 256 bytes (128 words). Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the security sector.

Protection of the Security Sector

The security sector area can be protected using the following procedures: Write the three-cycle **"Enter security sector command"** sequence, and then following the in-system sector protect algorithm as shown in Fig. 2, except that RESET# may be at either V_{IH} or V_{ID}. This allows **in-system protection** of the security sector without raising any device pin to a high voltage. Note that this method is only applicable to the security sector. To verify the protect/ unprotect status of the security sector. follow the algorithm shown in Fig. 2.

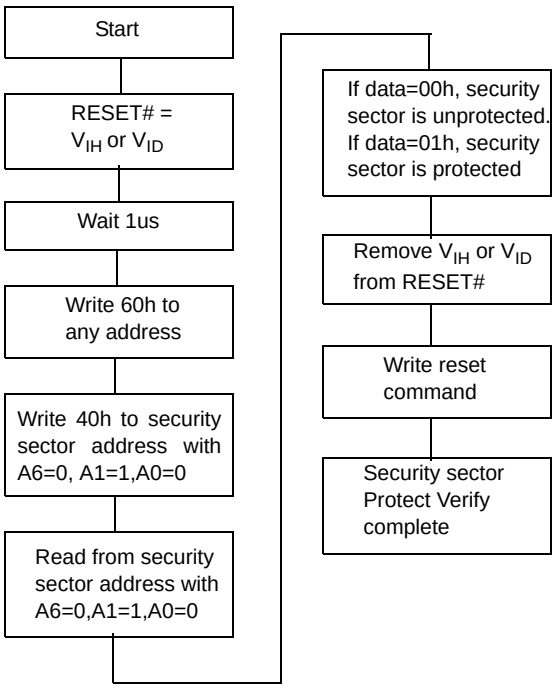


Figure 2. Security Sector Protect Verify

Exit from the Security Sector

Once the Security Sector is locked protected and verified, the system must write the Exit Security Sector Region command sequence to return to reading and writing the remainder of the array.

Caution for the Security Sector Protection

The security sector protection must be used with caution since, once protected, there is no procedure available for unprotecting the security sector area and none of the bits in the security sector memory space can be modified in any way.

HARDWARE DATA PROTECTION

The ES29DL320 device provides some protection measures against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power-up, all internal registers and latches in the device are cleared and the device automatically resets to the read mode. In addition, with its internal state machine built-in the device, any alteration of the memory contents or any initiation of new operation can only occur after successful completion of specific command sequences. And several features are incorporated to prevent inadvertent write cycles resulting from Vcc power-up and power-down transition or system noise.

Low Vcc Write inhibit

When Vcc is less than V_{LKO}, the device does not accept any write cycles. This protects data during Vcc power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until Vcc is greater than V_{LKO}. The system must provide proper signals to the control pins to prevent unintentional writes when Vcc is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical inhibit

Write cycles are inhibited by holding any one of OE#=V_{IL}, CE#=V_{IH} or WE#=V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-up Write Inhibit

If WE#=CE#=V_{IL} and OE#=V_{IH} during power up, the device does not accept any commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

Table 1. ES29DL320 Device Bus Operations

Operation		CE#	OE#	WE#	RESET#	WP#/ACC	Addresses (Note 1)	DQ0 ~ DQ7	DQ8~DQ15	
									BYTE# = V_{IH}	BYTE# = V_{IL}
Read		L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	DQ8~DQ14 = High-Z, DQ15 = A-1
Write		L	H	L	H	(Note 3)	A_{IN}	(Note 4)	(Note 4)	
Accelerated Program		L	H	L	H	V_{HH}	A_{IN}	(Note 4)	(Note 4)	
Standby		Vcc± 0.3V	X	X	Vcc± 0.3V	H	X	High-Z	High-Z	High-Z
Output Disable Reset		L	H	H	H	L/H	X	High-Z	High-Z	
		X	X	X	L	L/H	X	High-Z	High-Z	
In-system	Sector Protect (Note 2)	L	H	L	V_{ID}	L/H	SA,A6=L, A1=H,A0=L	(Note 4)	X	X
	Sector Unprotect (Note 2)	L	H	L	V_{ID}	L/H (Note 3)	SA,A6=H, A1=H,A0=L	(Note 4)	X	X
	Temporary Sector Unprotect	X	X	X	V_{ID}	H (Note 3)	A_{IN}	(Note 4)	(Note 4)	High-Z
A9 High-Voltage Method	Sector protect	L	V_{ID}	L	H	H (Note 3)	SA,A9=V_{ID}, A6=L, A1=H,A0=L	(Note 4)	(Note 4)	High-Z
	Sector unprotect	L	V_{ID}	L	H	H (Note 3)	SA,A9=V_{ID}, A6=H, A1=H,A0=L			

Legend: *L=Logic Low=V_{IL}, H=Logic High=V_{IH}, V_{ID}=8.5 - 12.5V, V_{HH}=8.5 - 9.5V, X=Don't Care, SA=Sector Address, A_{IN}=Address In, D_{IN}=Data In, D_{OUT}=Data Out*

Notes:

1. *Addresses are A20:A0 in word mode (BYTE#=V_{IH}) , A20:A-1 in byte mode (BYTE#=V_{IL}).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector/Sector Block Protection and Unprotection" section.*
3. *If WP#/ACC=V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC=V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If WP#/ACC=V_{HH}, all sectors will be unprotected.*
4. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protection algorithm.*

Table 2. Autoselect Codes (A9 High-Voltage Method)

Description	CE#	OE#	WE#	A20 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ8~DQ15		DQ7~DQ0
												BYTE# = V_{IH}	BYTE# = V_{IL}	
ManufactureID:ESI	L	L	H	BA	X	V_{ID}	X	L	X	L	L	X	X	4Ah
Device ID: ES29DL320	L	L	H	BA	X	V_{ID}	X	L	X	L	H	22h	X	41h(T),81h(B)
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	X	X	01h(protected) 00h(unprotected)
Security Sector Indicator Bit(DQ7)	L	L	H	BA	X	V_{ID}	X	L	X	H	H	X	X	82h(factory-locked), 02h(customer-lockable)

Legend: *T= Top Boot Block, B = Bottom Boot Block, L=Logic Low=V_{IL}, H=Logic High=V_{IH}, BA= Bank Address, SA=Sector Address, X = Don't care.*

Table 3. Top Boot Sector Addresses (ES29DL320T)

Bank	Group	Sector	Sector address A20~A12	Sector Size (Kbytes/Kwords)	(X8) Address Range	(X16) Address Range	Remark
Bank0	SG0	SA0	000000XXX	64/32	000000h~00FFFFh	000000h~07FFFh	Main Sector
		SA1	000001XXX	64/32	010000h~01FFFFh	008000h~0FFFFh	
		SA2	000010XXX	64/32	020000h~02FFFFh	010000h~17FFFh	
		SA3	000011XXX	64/32	030000h~03FFFFh	018000h~01FFFFh	
	SG1	SA4	000100XXX	64/32	040000h~04FFFFh	020000h~027FFFh	
		SA5	000101XXX	64/32	050000h~05FFFFh	028000h~02FFFFh	
		SA6	000110XXX	64/32	060000h~06FFFFh	030000h~037FFFh	
		SA7	000111XXX	64/32	070000h~07FFFFh	038000h~03FFFFh	
Bank1	SG2	SA8	001000XXX	64/32	080000h~08FFFFh	040000h~047FFFh	
		SA9	001001XXX	64/32	090000h~09FFFFh	048000h~04FFFFh	
		SA10	001010XXX	64/32	0A0000h~0AFFFFh	050000h~057FFFh	
		SA11	001011XXX	64/32	0B0000h~0BFFFFh	058000h~05FFFFh	
	SG3	SA12	001100XXX	64/32	0C0000h~0CFFFFh	060000h~067FFFh	
		SA13	001101XXX	64/32	0D0000h~0DFFFFh	068000h~06FFFFh	
		SA14	001110XXX	64/32	0E0000h~0EFFFFh	070000h~077FFFh	
		SA15	001111XXX	64/32	0F0000h~0FFFFFh	078000h~07FFFFh	
Bank2	SG4	SA16	010000XXX	64/32	100000h~10FFFFh	080000h~087FFFh	
		SA17	010001XXX	64/32	110000h~11FFFFh	088000h~08FFFFh	
		SA18	010010XXX	64/32	120000h~12FFFFh	090000h~097FFFh	
		SA19	010011XXX	64/32	130000h~13FFFFh	098000h~09FFFFh	
	SG5	SA20	010100XXX	64/32	140000h~14FFFFh	0A0000h~0A7FFFh	
		SA21	010101XXX	64/32	150000h~15FFFFh	0A8000h~0AFFFFh	
		SA22	010110XXX	64/32	160000h~16FFFFh	0B0000h~0B7FFFh	
		SA23	010111XXX	64/32	170000h~17FFFFh	0B8000h~0BFFFFh	
Bank3	SG6	SA24	011000XXX	64/32	180000h~18FFFFh	0C0000h~0C7FFFh	
		SA25	011001XXX	64/32	190000h~19FFFFh	0C8000h~0CFFFFh	
		SA26	011010XXX	64/32	1A0000h~1AFFFFh	0D0000h~0D7FFFh	
		SA27	011011XXX	64/32	1B0000h~1BFFFFh	0D8000h~0DFFFFh	
	SG7	SA28	011100XXX	64/32	1C0000h~1CFFFFh	0E0000h~0E7FFFh	
		SA29	011101XXX	64/32	1D0000h~1DFFFFh	0E8000h~0EFFFFh	
		SA30	011110XXX	64/32	1E0000h~1EFFFFh	0F0000h~0F7FFFh	
		SA31	011111XXX	64/32	1F0000h~1FFFFFh	0F8000h~0FFFFFh	
Bank4	SG8	SA32	100000XXX	64/32	200000h~20FFFFh	100000h~107FFFh	
		SA33	100001XXX	64/32	210000h~21FFFFh	108000h~10FFFFh	
		SA34	100010XXX	64/32	220000h~22FFFFh	110000h~117FFFh	
		SA35	100011XXX	64/32	230000h~23FFFFh	118000h~11FFFFh	
	SG9	SA36	100100XXX	64/32	240000h~24FFFFh	120000h~127FFFh	
		SA37	100101XXX	64/32	250000h~25FFFFh	128000h~12FFFFh	
		SA38	100110XXX	64/32	260000h~26FFFFh	130000h~137FFFh	
		SA39	100111XXX	64/32	270000h~27FFFFh	138000h~13FFFFh	
Bank5	SG10	SA40	101000XXX	64/32	280000h~28FFFFh	140000h~147FFFh	
		SA41	101001XXX	64/32	290000h~29FFFFh	148000h~14FFFFh	
		SA42	101010XXX	64/32	2A0000h~2AFFFFh	150000h~157FFFh	
		SA43	101011XXX	64/32	2B0000h~2BFFFFh	158000h~15FFFFh	
	SG11	SA44	101100XXX	64/32	2C0000h~2CFFFFh	160000h~167FFFh	
		SA45	101101XXX	64/32	2D0000h~2DFFFFh	168000h~16FFFFh	
		SA46	101110XXX	64/32	2E0000h~2EFFFFh	170000h~177FFFh	
		SA47	101111XXX	64/32	2F0000h~2FFFFFh	178000h~17FFFFh	
Bank6	SG12	SA48	110000XXX	64/32	300000h~30FFFFh	180000h~187FFFh	
		SA49	110001XXX	64/32	310000h~31FFFFh	188000h~18FFFFh	
		SA50	110010XXX	64/32	320000h~32FFFFh	190000h~197FFFh	
		SA51	110011XXX	64/32	330000h~33FFFFh	198000h~19FFFFh	
	SG13	SA52	110100XXX	64/32	340000h~34FFFFh	1A0000h~1A7FFFh	
		SA53	110101XXX	64/32	350000h~35FFFFh	1A8000h~1AFFFFh	
		SA54	110110XXX	64/32	360000h~36FFFFh	1B0000h~1B7FFFh	
		SA55	110111XXX	64/32	370000h~37FFFFh	1B8000h~1BFFFFh	

Table 3. Top Boot Sector Addresses (ES29DL320T) Continued

Bank	Group	Sector	Sector address A20~A12	Sector Size (Kbytes/Kwords)	(X8) Address Range	(X16) Address Range	Remark
Bank7	SG14	SA56	111000XXX	64/32	380000h~38FFFFh	1C0000h~1C7FFFh	Main Sector
		SA57	111001XXX	64/32	390000h~39FFFFh	1C8000h~1CFFFFh	
		SA58	111010XXX	64/32	3A0000h~3AFFFFh	1D0000h~1D7FFFh	
		SA59	111011XXX	64/32	3B0000h~3BFFFFh	1D8000h~1DFFFFh	
	SG15	SA60	111100XXX	64/32	3C0000h~3CFFFFh	1E0000h~1E7FFFh	
		SA61	111101XXX	64/32	3D0000h~3DFFFFh	1E8000h~1EFFFFh	
		SA62	111110XXX	64/32	3E0000h~3EFFFFh	1F0000h~1F7FFFh	
	SG16	SA63	111111000	8/4	3F0000h~3F1FFFh	1F8000h~1F8FFFh	Boot Sector SA69,SA70 protected at WP#/ ACC=low
	SG17	SA64	111111001	8/4	3F2000h~3F3FFFh	1F9000h~1F9FFFh	
	SG18	SA65	111111010	8/4	3F4000h~3F5FFFh	1FA000h~1FAFFFh	
	SG19	SA66	111111011	8/4	3F6000h~3F7FFFh	1FB000h~1FBFFFh	
	SG20	SA67	111111100	8/4	3F8000h~3F9FFFh	1FC000h~1FCFFFh	
	SG21	SA68	111111101	8/4	3FA000h~3FBFFFh	1FD000h~1FDFFFh	
	SG22	SA69	111111110	8/4	3FC000h~3FDFFFh	1FE000h~1FEFFFh	
	SG23	SA70	111111111	8/4	3FE000h~3FFFFFh	1FF000h~1FFFFFh	
Security Sector			111111111	bytes/words (256/128)	3FFF00h~3FFFFFh	1FFF80h~1FFFFFh	

Note:
The addresses range is A20:A-1 in byte mode (BYTE#=V_{IL}) or A20:A0 in word mode (BYTE#=V_{IH}).

Table 4. Bottom Boot Sector Addresses (ES29DL320B)

Bank	Group	Sector	Sector address A20~A12	Sector Size (Kbytes/Kwords)	(X8) Address Range	(X16) Address Range	Remark
Bank0	SG0	SA0	000000000	8/4	000000h~001FFFh	000000h~000FFFh	Boot Sector SA0,SA1 protected at WP#/ ACC=low
	SG1	SA1	000000001	8/4	002000h~003FFFh	001000h~001FFFh	
	SG2	SA2	000000010	8/4	004000h~005FFFh	002000h~002FFFh	
	SG3	SA3	000000011	8/4	006000h~007FFFh	003000h~003FFFh	
	SG4	SA4	000000100	8/4	008000h~009FFFh	004000h~004FFFh	
	SG5	SA5	000000101	8/4	00A000h~00BFFFh	005000h~005FFFh	
	SG6	SA6	000000110	8/4	00C000h~00DFFFh	006000h~006FFFh	
	SG7	SA7	000000111	8/4	00E000h~00FFFFh	007000h~007FFFh	
	SG8	SA8	000001XXX	64/32	010000h~01FFFFh	008000h~00FFFFh	Main Sector
		SA9	000010XXX	64/32	020000h~02FFFFh	010000h~017FFFh	
		SA10	000011XXX	64/32	030000h~03FFFFh	018000h~01FFFFh	
	SG9	SA11	000100XXX	64/32	040000h~04FFFFh	020000h~027FFFh	
		SA12	000101XXX	64/32	050000h~05FFFFh	028000h~02FFFFh	
		SA13	000110XXX	64/32	060000h~06FFFFh	030000h~037FFFh	
		SA14	000111XXX	64/32	070000h~07FFFFh	038000h~03FFFFh	
Bank1	SG10	SA15	001000XXX	64/32	080000h~08FFFFh	040000h~047FFFh	
		SA16	001001XXX	64/32	090000h~09FFFFh	048000h~04FFFFh	
		SA17	001010XXX	64/32	0A0000h~0AFFFFh	050000h~057FFFh	
		SA18	001011XXX	64/32	0B0000h~0BFFFFh	058000h~05FFFFh	
	SG11	SA19	001100XXX	64/32	0C0000h~0CFFFFh	060000h~067FFFh	
		SA20	001101XXX	64/32	0D0000h~0DFFFFh	068000h~06FFFFh	
		SA21	001110XXX	64/32	0E0000h~0EFFFFh	070000h~077FFFh	
		SA22	001111XXX	64/32	0F0000h~0FFFFFh	078000h~07FFFFh	
Bank2	SG12	SA23	010000XXX	64/32	100000h~10FFFFh	080000h~087FFFh	
		SA24	010001XXX	64/32	110000h~11FFFFh	088000h~08FFFFh	
		SA25	010010XXX	64/32	120000h~12FFFFh	090000h~097FFFh	
		SA26	010011XXX	64/32	130000h~13FFFFh	098000h~09FFFFh	
	SG13	SA27	010100XXX	64/32	140000h~14FFFFh	0A0000h~0A7FFFh	
		SA28	010101XXX	64/32	150000h~15FFFFh	0A8000h~0AFFFFh	
		SA29	010110XXX	64/32	160000h~16FFFFh	0B0000h~0B7FFFh	
		SA30	010111XXX	64/32	170000h~17FFFFh	0B8000h~0BFFFFh	
Bank3	SG14	SA31	011000XXX	64/32	180000h~18FFFFh	0C0000h~0C7FFFh	
		SA32	011001XXX	64/32	190000h~19FFFFh	0C8000h~0CFFFFh	
		SA33	011010XXX	64/32	1A0000h~1AFFFFh	0D0000h~0D7FFFh	
		SA34	011011XXX	64/32	1B0000h~1BFFFFh	0D8000h~0DFFFFh	
	SG15	SA35	011100XXX	64/32	1C0000h~1CFFFFh	0E0000h~0E7FFFh	
		SA36	011101XXX	64/32	1D0000h~1DFFFFh	0E8000h~0EFFFFh	
		SA37	011110XXX	64/32	1E0000h~1EFFFFh	0F0000h~0F7FFFh	
		SA38	011111XXX	64/32	1F0000h~1FFFFFh	0F8000h~0FFFFFh	
Bank4	SG16	SA39	100000XXX	64/32	200000h~20FFFFh	100000h~107FFFh	
		SA40	100001XXX	64/32	210000h~21FFFFh	108000h~10FFFFh	
		SA41	100010XXX	64/32	220000h~22FFFFh	110000h~117FFFh	
		SA42	100011XXX	64/32	230000h~23FFFFh	118000h~11FFFFh	
	SG17	SA43	100100XXX	64/32	240000h~24FFFFh	120000h~127FFFh	
		SA44	100101XXX	64/32	250000h~25FFFFh	128000h~12FFFFh	
		SA45	100110XXX	64/32	260000h~26FFFFh	130000h~137FFFh	
		SA46	100111XXX	64/32	270000h~27FFFFh	138000h~13FFFFh	
Bank5	SG18	SA47	101000XXX	64/32	280000h~28FFFFh	140000h~147FFFh	
		SA48	101001XXX	64/32	290000h~29FFFFh	148000h~14FFFFh	
		SA49	101010XXX	64/32	2A0000h~2AFFFFh	150000h~157FFFh	
		SA50	101011XXX	64/32	2B0000h~2BFFFFh	158000h~15FFFFh	
	SG19	SA51	101100XXX	64/32	2C0000h~2CFFFFh	160000h~167FFFh	
		SA52	101101XXX	64/32	2D0000h~2DFFFFh	168000h~16FFFFh	
		SA53	101110XXX	64/32	2E0000h~2EFFFFh	170000h~177FFFh	
		SA54	101111XXX	64/32	2F0000h~2FFFFFh	178000h~17FFFFh	

Table 4. Bottom Boot Sector Addresses (ES29DL320B) Continued

	Group	Sector	Sector address A20~A12	Sector Size (Kbytes/Kwords)	(X8) Address Range	(X16) Address Range	Remark
Bank6	SG20	SA55	110000XXX	64/32	300000h~30FFFFh	180000h~187FFFh	Main Sector
		SA56	110001XXX	64/32	310000h~31FFFFh	188000h~18FFFFh	
		SA57	110010XXX	64/32	320000h~32FFFFh	190000h~197FFFh	
		SA58	110011XXX	64/32	330000h~33FFFFh	198000h~19FFFFh	
	SG21	SA59	110100XXX	64/32	340000h~34FFFFh	1A0000h~1A7FFFh	
		SA60	110101XXX	64/32	350000h~35FFFFh	1A8000h~1AFFFFh	
		SA61	110110XXX	64/32	360000h~36FFFFh	1B0000h~1B7FFFh	
		SA62	110111XXX	64/32	370000h~37FFFFh	1B8000h~1BFFFFh	
Bank7	SG22	SA63	111000XXX	64/32	380000h~38FFFFh	1C0000h~1C7FFFh	
		SA64	111001XXX	64/32	390000h~39FFFFh	1C8000h~1CFFFFh	
		SA65	111010XXX	64/32	3A0000h~3AFFFFh	1D0000h~1D7FFFh	
		SA66	111011XXX	64/32	3B0000h~3BFFFFh	1D8000h~1DFFFFh	
	SG23	SA67	111100XXX	64/32	3C0000h~3CFFFFh	1E0000h~1E7FFFh	
		SA68	111101XXX	64/32	3D0000h~3DFFFFh	1E8000h~1EFFFFh	
		SA69	111110XXX	64/32	3E0000h~3EFFFFh	1F0000h~1F7FFFh	
		SA70	111111XXX	64/32	3F0000h~3FFFFFh	1F8000h~1FFFFFh	
Security Sector			000000000	bytes/words (256/128)	000000h~0000FFh	000000h~00007Fh	

Note:
The addresses range is A20:A-1 in byte mode (BYTE#=V_{IL}) or A20:A0 in word mode (BYTE#=V_{IH}).

In-System Protection / Unprotection Method

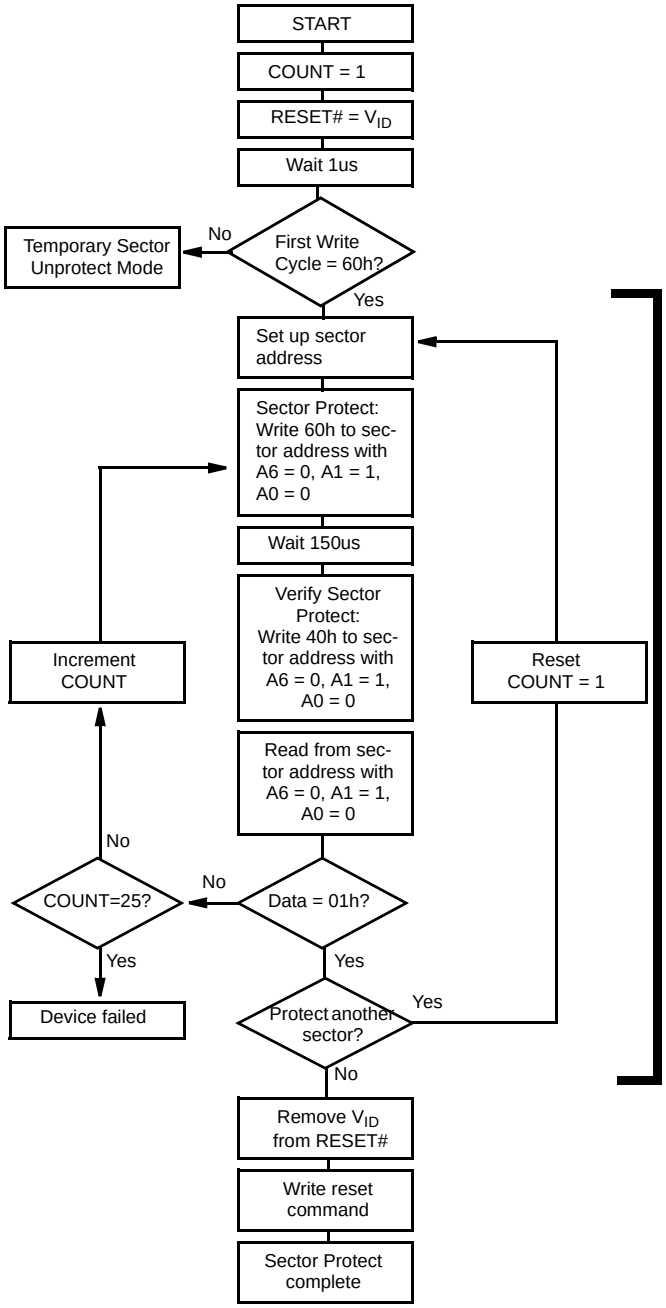


Figure 3. In-System Sector Protect Algorithm

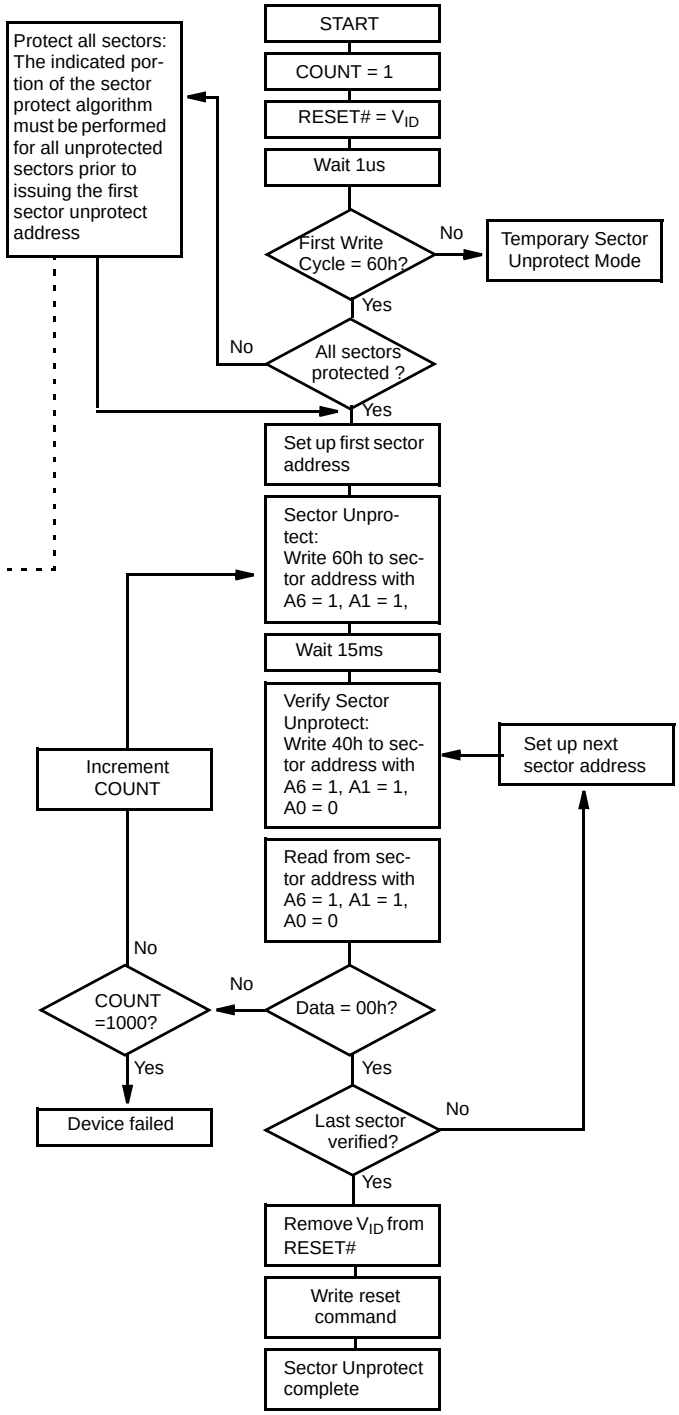


Figure 4. In-System Sector Unprotect Algorithm

A9 High-Voltage Method

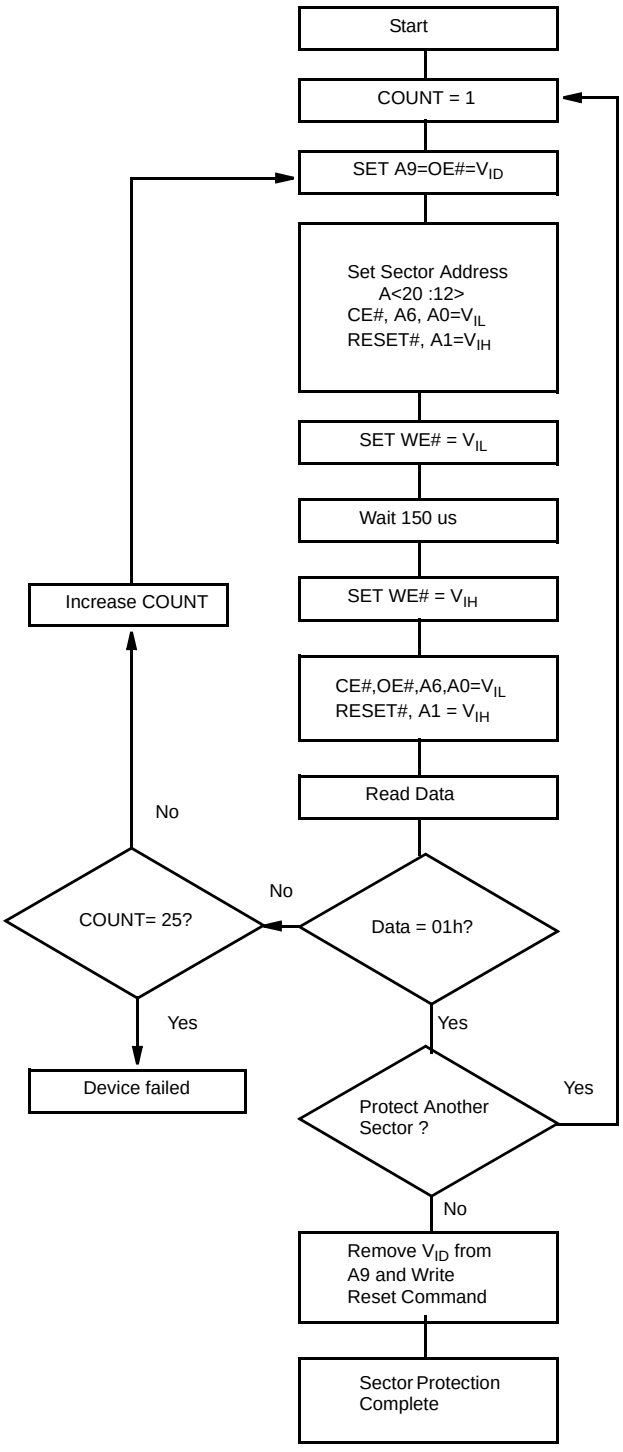


Figure 5. Sector Protection Algorithm (A9 High-Voltage Method)

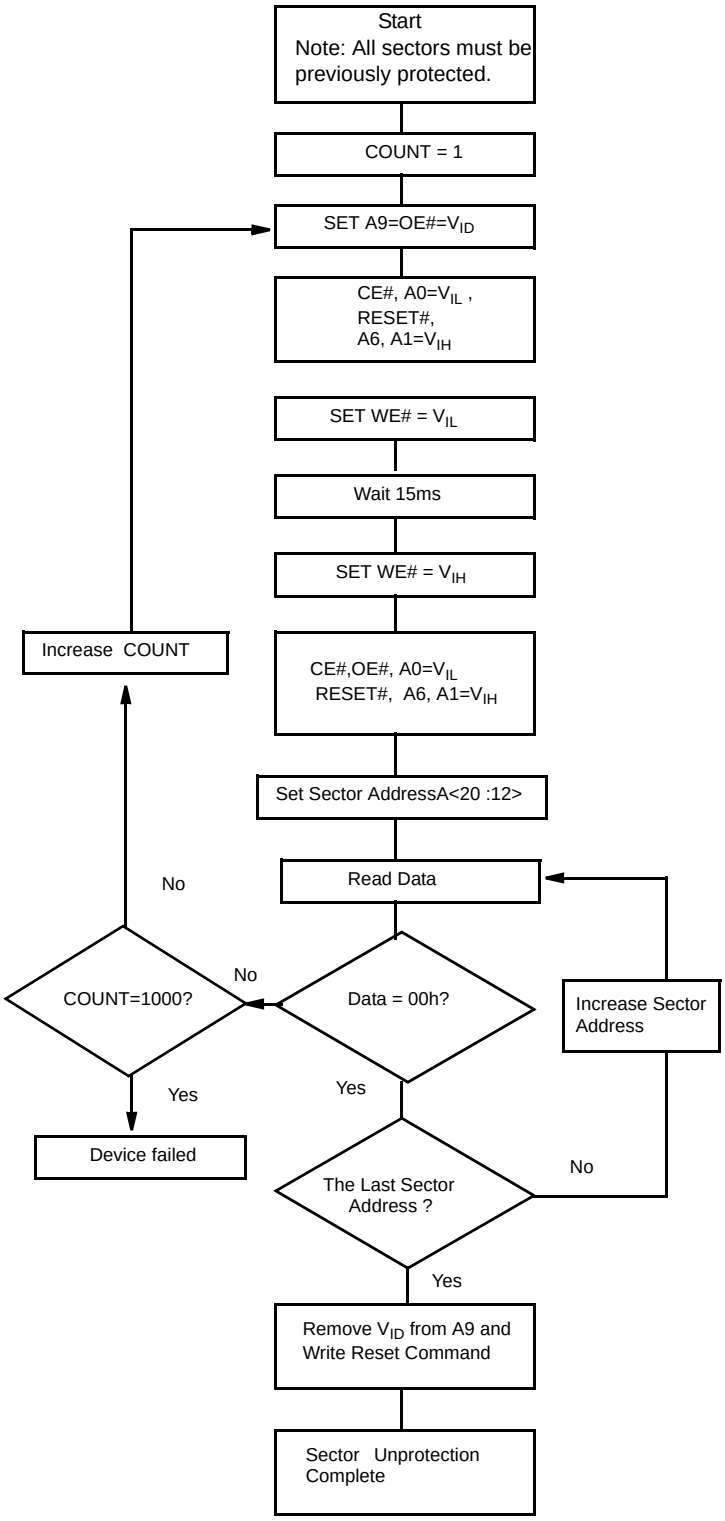


Figure 6. Sector Un-Protection Algorithm (A9 High-Voltage Method)

Common Flash Memory Interface (CFI)

CFI is supported in the ES29DL320 device. The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the **CFI query command**, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 5-8. To terminate reading CFI data, the system must write the **reset command**.The CFI query command can be written to the system when the device is in the **autoselect mode** or the **erase-suspend-read** mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 5-8. When the reset command is written, the device returns respectively to the read mode or erase-suspend-read mode.

Table 5. CFI Query Identification String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set(00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 6. System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0027h	Vcc Min. (write/erase) D7-D4: volt, D3-D0: 100 millivolt
1Ch	38h	0036h	Vcc Max. (write/erase) D7-D4: volt, D3-D0: 100 millivolt
1Dh	3Ah	0000h	Vpp Min. voltage (00h = no Vpp pin present)
1Eh	3Ch	0000h	Vpp Max. voltage (00h = no Vpp pin present)
1Fh	3Eh	0004h	Typical timeout per single byte/word write 2^N us
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N us (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 7. Device Geometry Definition

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0016h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface Description 02 = x8, x16 Asynchronous
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of bytes multi-byte write = 2^N (00h = not supported)
2Ch	58h	0002h	Number of Erase Block Regions within device
2Dh 2Eh	5Ah 5Ch	0007h 0000h	Erase Block Region 1 Information Number of identical size erase block = 0007h+1 =8
2Fh 30h	5Eh 60h	0020h 0000h	Erase Block Region 1 Information Number of identical size erase block = 0020h * 256byte = 8Kbyte
31h 32h	62h 64h	003Eh 0000h	Erase Block Region 2 Information Number of identical size erase block = 003Eh+1 =63
33h 34h	66h 68h	0000h 0001h	Erase Block Region 2 Information Number of identical size erase block = 0100h * 256byte = 64Kbyte
35h 36h	6Ah 6Ch	0000h 0000h	Erase Block Region 3 Information
37h 38h	6Eh 70h	0000h 0000h	Erase Block Region 3 Information
39h 3Ah	72h 74h	0000h 0000h	Erase Block Region 4 Information
3Bh 3Ch	76h 78h	0000h 0000h	Erase Block Region 4 Information

Table 8. Primary Vendor-Specific Extended Query

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0031h	Minor version number, ASCII
45h	8Ah	0000h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (D7-D2)
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0004h	Group Protection 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Unprotect scheme 04 = In-System Method and A9 High-Voltage Method
4Ah	94h	0038h	Simultaneous Operation Number of Sectors (excluding Bank 1)
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	0085h	ACC(Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100mV
4Eh	9Ch	0095h	ACC(Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100mV
4Fh	9Eh	000Xh	Top/Bottom Boot Sector Flag 02h = Bottom Boot Device, 03h = Top Boot Device

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 9 defines the valid register command sequences. Note that writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. A reset command is required to return the device to normal operation.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

READING ARRAY DATA

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system must issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information.The Read-Only Operations table provides the read parameters, and Fig. 18 shows the timing diagram

RESET COMMAND

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the bank to the read mode (or erase-suspend-read mode if that bank was in Erase-Suspend).

Command Definitions

Table 9. ES29DL320 Command Definitions

Command Sequence (Note 1)			Cycles	Bus Cycles (Notes 2~5)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)			1	RA	RD										
Reset (Note 7)			1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X00	4A				
		Byte		AAA		555		(BA)AAA							
	Device ID	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X01	41/81				
		Byte		AAA		555		(BA)AAA		(BA)X02					
	Security Sector Factory Protect (Note10)	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X03	82/02				
		Byte		AAA		555		(BA)AAA		(BA)X06					
	Sector Protect Verify (Note 11)	Word	4	555	AA	2AA	55	(BA)555	90	(SA)X02	00/01				
		Byte		AAA		555		(BA)AAA		(SA)X04					
Enter Security Sector Region		Word	3	555	AA	2AA	55	555	88						
		Byte		AAA		555		AAA							
Exit Security Sector Region		Word	4	555	AA	2AA	55	555	90	XXX	00				
		Byte		AAA		555		AAA							
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program (Note 12)			2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 13)			2	XXX	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend (Note 14)			1	XXX	B0										
Erase Resume (Note 15)			1	XXX	30										
CFI Query (Note 16)		Word	1	55	98										
		Byte		AA											

Legend:

X = Don't care
RA = Address of the memory location to be read.
RD = Data read from location RA during read operation
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A20-A12 uniquely select any sector.
BA = Address of the bank that is being switched to autoselect mode, is in bypass mode, or is being erased.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15-DQ8 are don't care in command sequences, except for RD and PD*
5. *Unless otherwise noted, address bits A20-A11 are don't cares.*
6. *No unlock or command cycles required when bank is in read mode.*
7. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information).*
8. *The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address to obtain the manufacturer ID, device ID, or SecSi Sector factory protect information. Data bits DQ15-DQ8 are don't care. See the Autoselect Command Sequence section for more information.*
9. *The device ID is 41h for top boot device, and 81h for bottom boot device.*
10. *The data is 82h for factory locked and 02h for not* factory *locked.*
11. *The data is 00h for an unprotected sector and 01h for a protected sector.*
12. *The Unlock Bypass command is required prior to the Unlock-Bypass Program command.*
13. *The Unlock Bypass Reset command is required to return to the read mode when the bank is in the unlock bypass mode.*
14. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
15. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
16. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

AUTOSELECT COMMAND

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected, including information about factory-locked or customer lockable version.

Identifier Code	Address	Data
Manufacturer ID	00h	4Ah
Device ID	01h	41h(T), 81h(B)
Security Sector Factory	03h	82 / 02
Sector Group Protect Verify	(SA)02h	00 / 01

Table 9 shows the address and data requirements. This method is an alternative to "A9 high-voltage method" shown in Table 2, which is intended for PROM programmers and requires V_{ID} on address pin A9. The autoselect command sequence may be written to an address within a bank that is either in the read mode or erase-suspend-read mode. The auto-select command may not be written while the device is actively programming or erasing in the other bank. The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence.

- A read cycle at address (BA) XX00h (where BA is the bank address) returns the manufacturer code
- A read cycle at address (BA)XX01h in word mode (or (BA)XX02h in byte mode) returns the device code.
- A read cycle to an address containing a sector address (SA) within the same bank, and the address 02h on A7 - A0 in word mode (or the address 04h on A6 - A-1 in byte mode) returns 01h if the sector is protected, or 00h if it is unprotected. (Refer to Table 2 for valid sector addresses).

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

SECURITY SECTOR COMMAND

In the ES29DL320 device, the security sector region (256 bytes) provides a secured data area containing a random, sixteen-byte electronic serial number(ESN) or customer's security codes. The security sector region can be accessed by issuing the three-cycle **Enter Security Sector command** sequence. The device continues to access the security sector region until the system issues the four-cycle **Exit Security Sector command** sequence. The Exit Security Sector command sequence returns the device to normal operation. Table 9 shows the address and data requirements for both command sequences. Note that the **accelerated programming** function by WP#ACC and **unlock bypass** mode are not available when the device has entered the security sector. Refer to the Fig. 7 for the security sector operation.

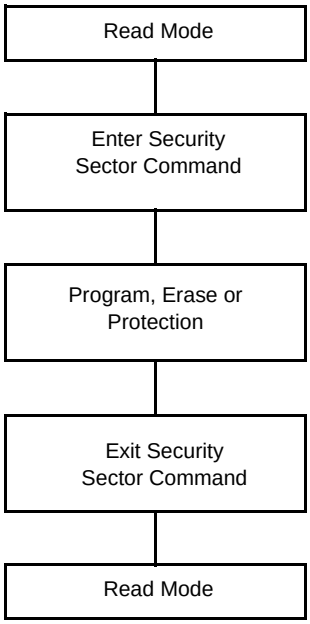
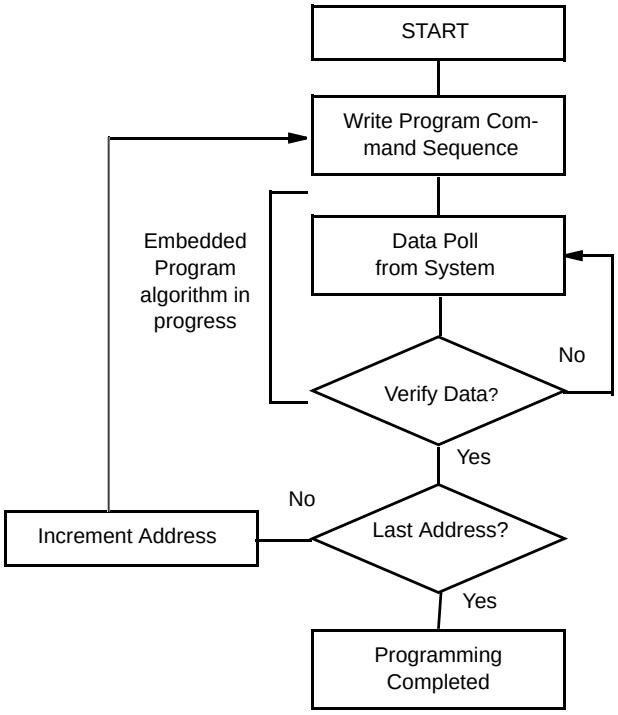


Figure 7. Security Sector Operation

BYTE / WORD PROGRAM

The system may program the device by word or byte, depending on the state of the **BYTE# pin**. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 9 shows the address and data requirements for the byte program command sequence. Note that the autoselect, commands related with the security sector, and CFI modes are unavailable while a programming operation is in progress.



Note: *See Table 9 for program command sequence*

Figure 8. Program Operation

Program Status Bits : DQ7, DQ6 or RY/BY#

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the Write Operation Status section Table 10 for information on these status bits.

Any Commands Ignored during Programming Operation

Any commands written to the device during the Embedded Program algorithm are ignored. Note that a hardware reset can immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming from “0” back to “1”

Programming is allowed in any sequence and across sector boundaries. But a bit cannot be programmed from “0” back to a ”1”. Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still “0”. Only erase operations can convert a “0” to a “1”.

Unlock Bypass

In the ES29DL320 device, an unlock bypass program mode is provided for faster programming operation. In this mode, two cycles of program command sequences can be saved. To enter this mode, an unlock bypass enter command should be first written to the system. The unlock bypass enter command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock-bypass program mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program set-up command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 9 shows the requirements for the command sequence.

During the unlock-bypass mode, only the unlock-bypass program and unlock-bypass reset commands are valid. To exit the unlock-bypass mode, the system must issue the two-cycle unlock-bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need to only contain the data 00h. The bank then returns to the read mode.

- **Unlock Bypass Enter Command**
- **Unlock Bypass Reset Command**
- **Unlock Bypass Program Command**

Unlock Bypass Program during WP#/ACC Accelerated Program Mode

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the unlock bypass mode. The system may then write the two-cycle unlock bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. Note that the WP#/ACC pin must not be at V_{HH} in any operation other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result. Fig. 8 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Fig. 22 for timing diagrams.

CHIP ERASE COMMAND

To erase the entire memory, a chip erase command is used. This command is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The chip erase command erases the entire memory including all other sectors except the protected sectors, but the internal erase operation is performed on a single sector base.

Embedded Erase Algorithm

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

Table 9 shows the address and data requirements for the chip erase command sequence. Note that the autoselect, security sector, and CFI modes are unavailable while an erase operation is in progress.

Erase Status Bits : DQ7, DQ6, DQ2, or RY/BY#

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Write Operation Status section Table 10 for information on these status bits.

Commands Ignored during Erase Operation

Any command written during the chip erase operation are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data to ensure data integrity. Fig. 9 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Fig. 23 section for timing diagrams.

SECTOR ERASE COMMAND

By using a sector erase command, a single sector or multiple sectors can be erased. The sector erase command is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 9 shows the address and data requirements for the sector erase command sequence. Note that the autoselect, security sector, and CFI modes are unavailable while an erase operation is in progress.

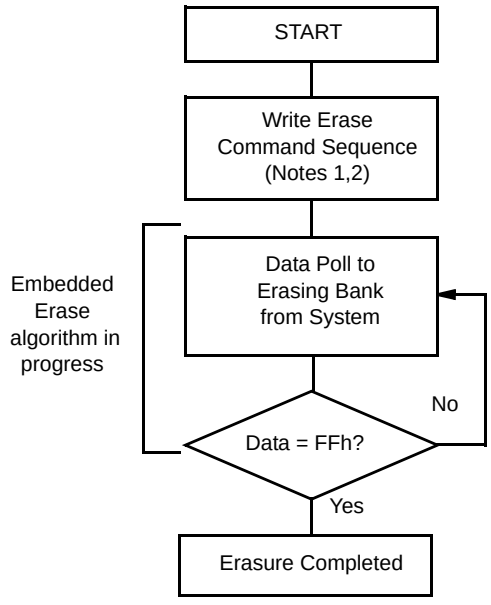
Embedded Sector Erase Algorithm

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings these operations.

Sector Erase Time-out Window and DQ3

After the command sequence is written, a sector erase time-out of **50us** occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50us, otherwise the last address and command may not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. The system can monitor **DQ3** to determine if the sector erase timer has timed out (See the section on DQ3:Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode. The system must rewrite the command sequence and any additional addresses and commands.



Notes:

1. See Table 9 for erase command sequence
2. See the section on DQ3 for information on the sector erase timer

Figure 9. Erase Operation

Status Bits : DQ7,DQ6,DQ2, or RY/BY#

When the Sector Erase Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7,DQ6,DQ2, or RY/BY# in the erasing bank. Refer to the Write Operation Status section Table 10 for information on these status bits.

Valid Command during Sector Erase

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Fig. 9 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Fig. 23 section for timing diagrams.

ERASE SUSPEND/ERASE RESUME

An erase operation is a long-time operation so that two useful commands are provided in the ES29DL320 device Erase Suspend and Erase Resume Commands. Through the two commands, erase operation can be suspended for a while and the suspended operation can be resumed later when it is required. While the erase is suspended, read or program operations can be performed by the system.

Erase Suspend Command, (B0h)

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the **50us time-out** period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of **20us** to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

Read and Program during Erase-Suspend-Read Mode

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7-DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits (Table 10).

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status for the program operation using the DQ7 or DQ6 status bits, just as in the standard Byte Program operation. Refer to the Write Operation Status section for more information.

Autoselect during Erase-Suspend- Read Mode

In the erase-suspend-read mode, the system can also issue the autoselected command sequence. Refer to the Autoselect Mode and Autoselect Command Sequence section for details (Table 9).

Erase Resume Command

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

COMMAND DIAGRAM

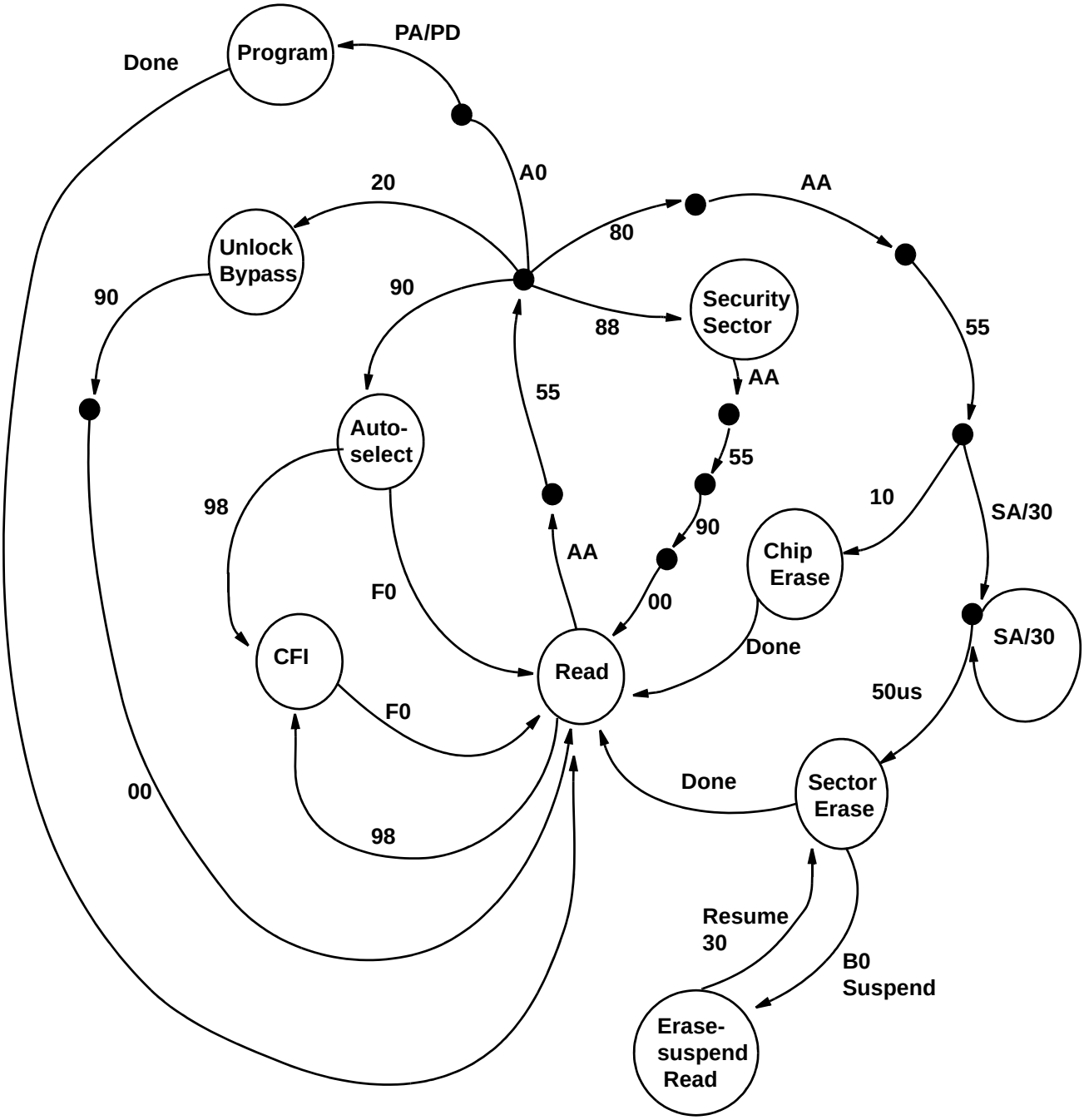


Figure 10. Command Diagram

WRITE OPERATION STATUS

In the ES29DL320 device, several bits are provided to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, DQ7 and RY/BY#. Table 10 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7 (DATA# POLLING)

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During Programming

During the Embedded Program algorithm, the device outputs on DQ7 the **complement** of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a **protected sector**, Data# Polling on DQ7 is active for approximately **250ns**, then that bank returns to the read mode.

During Erase

During the Embedded Erase algorithm, Data# Polling produces a **“0” on DQ7**. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

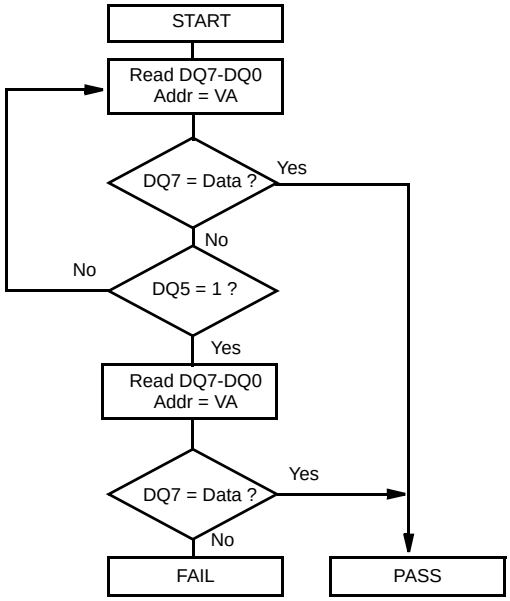
Erase on the Protected Sectors

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately **1.8us**, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Data# Polling Algorithm

Just prior to the completion of an Embedded Program or Ease operation, DQ7 may change asynchronously with DQ0-DQ6 while Output Enable(OE#) is asserted low. That is, this device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0-DQ7 will appear on successive read cycles.

Table 10 shows the outputs for Data# Polling on DQ7. Fig. 11 shows the Data# Polling algorithm. Fig. 24 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address in any non-protected sector address.*

2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5*

Figure 11. Data# Polling Algorithm

RY/BY# (READY/BUSY#)

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to Vcc. If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks in the erase-suspend-read mode. Table 10 shows the outputs for RY/BY#.

DQ6 (TOGGLE BIT I)

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out. During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7(see the subsection on DQ7:Data# Polling). DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 10 shows the outputs for Toggle Bit I on DQ6. Fig. 12 shows the toggle bit algorithm. Fig. 25 in the "AC Characteristics" section shows the toggle bit timing diagrams. Fig. 26 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2 : (Toggle Bit II).

Toggling on the Protected Sectors

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately **1.8us**, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. If a program address falls within a protected sector, DQ6 toggles for approximately **250ns** after the program command sequence is written, then returns to reading array data.

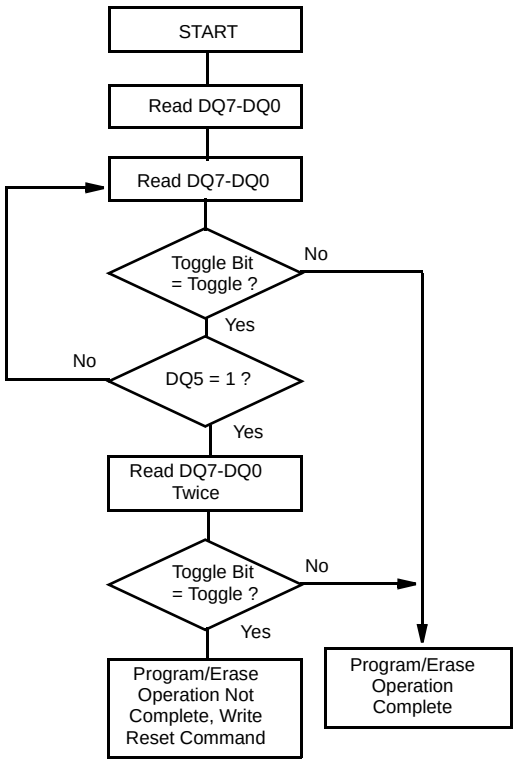
DQ2 (TOGGLE BIT II)

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence DQ2

toggles when the system reads at addresses within those sectors that have been **selected for erasure**. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 10 to compare outputs for DQ2 and DQ6. Fig. 12 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the DQ6: Toggle Bit I subsection. Fig. 25 shows the toggle bit timing diagram. Fig. 26 shows how differently DQ2 operates compared with DQ6.

Reading Toggle Bits DQ6/DQ2

Refer to Fig. 12 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7-DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7-DQ0 on the following read cycle. However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data. The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, this system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Fig. 12).



Note:

The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1". See the subsections on DQ6 and DQ2 for more information.

Figure 12. Toggle Bit Algorithm

DQ5 (EXCEEDED TIMING LIMITS)

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1”, indicating that the program or erase cycle was not successfully completed. The device may output a “1” on DQ5 if the system tries to program a “1” to a location that was previously programmed to “0” Only an erase operation can change a “0” back to a “1”. Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a ”1”. Under both these conditions, the system must write the reset command to return to the read mode.

DQ3 (SECTOR ERASE TIMER)

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase time does not apply to the chip erase command.)

If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a”1”. If the time between additional sector erase commands from the system can be assumed to be less than **50us**, the system need not monitor DQ3. See also the Sector Erase Command Sequence section. After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1”, the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erasure operation is complete. If DQ3 is “0”, the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. In Table 10, DQ3 status operation is well defined and summarized with other status bits, DQ7, DQ6, DQ5, and DQ2.

Table 10. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/ BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes :

1. DQ5 switches to “1” when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.

2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.

3. When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages .....-65°C to +150°C

Ambient Temperature
with Power Applied .....-65°C to +125°C

Voltage with Respect to Ground

Vcc (Note 1) .....-0.5V to +4.0V
A9, OE#, RESET# and WP#/ACC (Note 2) .....-0.5V to +12.5V
WP#/ACC .....-0.5V to +10.5V
All other pins (Note 1) .....-0.5V to Vcc+ 0.5V

Output Short Circuit Current (Note 3) 200mA

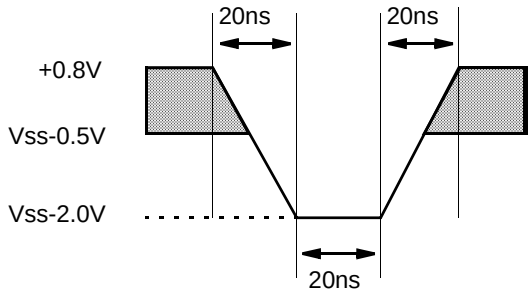
Notes:

1. *Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may overshoot Vss to -2.0V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is Vcc+0.5V. See Fig. 13. During voltage transition, input or I/O pins may overshoot to Vcc+2.0V for periods up to 20ns. See Fig. 13.*

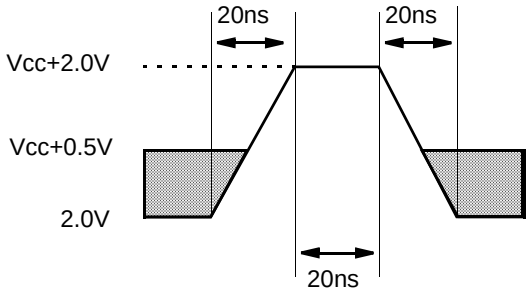
2. *Minimum DC input voltage on pins A9, OE#, RESET#, and WP# /ACC is -0.5V. During voltage transitions, A9, OE#, WP#/ACC, and RESET# may overshoot Vss to -2.0V for periods of up to 20ns. See Fig. 13. Maximum DC input voltage on pin A9 is +12.5V which may overshoot to +14.0V for periods up to 20ns. Maximum DC input voltage on WP#/ACC is +9.5V which may overshoot to +12.0V for periods up to 20ns.*

3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.



Negative Overshoot



Positive Overshoot

Figure 13. Maximum Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices
Ambient Temperature (T_A).....-40°C to +85°C

Commercial Devices
Ambient Temperature (T_A).....0°C to +70°C

Vcc Supply Voltages
Vcc for all devices .....2.7V to 3.6V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Table 11. CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	V_{IN}=Vss to Vcc Vcc=Vcc max				± 1.0	uA
I_{LIT}	A9 Input Load Current	Vcc=Vcc max; A9=12.5V				35	uA
I_{LR}	RESET# Input Load Current	Vcc=Vcc max; RESET#=12.5V				35	uA
I_{LO}	Output Leakage Current	Vout=Vss to Vcc, Vcc=Vcc max				± 1.0	uA
I_{CCI}	Vcc Active Read Current (Notes 1,2)	CE#=V_{IL}, OE#=V_{IH}, Byte mode	5MHz		10	16	mA
			1MHz		2	4	
		CE#=V_{IL}, OE#=V_{IH}, Word mode	5MHz		10	16	
			1MHz		2	4	
I_{CC2}	Vcc Active Write Current (Note 2,3)	CE#=V_{IL}, OE#=V_{IH}, WE#=V_{IL}			15	30	mA
I_{CC3}	Vcc Standby Current (Note 2)	CE#, RESET#= Vcc±0.3V			15	50	uA
I_{CC4}	Vcc Reset Current (Note 2)	RESET#=Vss ± 0.3V			15	50	uA
I_{CC5}	Automatic Sleep Mode (Notes2,4)	V_{IH} = Vcc ± 0.3V V_{IL} = Vss ± 0.3V			15	50	uA
I_{CC6}	Vcc Active Read-While-Program-Current (Notes 1,2)	CE#=V_{IL} OE#=V_{IH},	Byte		21	45	mA
			Word		21	45	
I_{CC7}	Vcc Active Read-While-Program-Current (Notes 1,2)	CE#=V_{IL}, OE#=V_{IH},	Byte		21	45	mA
			Word		21	45	
I_{CC8}	Vcc Active Program-While-Erase-Suspended Current (Notes 2,5)	CE#=V_{IL}, OE#=V_{IH},			17	35	mA
I_{ACC}	ACC Accelerated Program Current, Word or Byte	CE#=V_{IL}, OE#=V_{IH},	ACC pin		5	10	mA
			Vcc pin		15	30	
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			0.7xVcc		Vcc+0.3	V
V_{HH}	Voltage for WP#/ACC Sector Protect/Unprotect and Program Acceleration	Vcc = 3.0V ± 10%		8.5		9.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	Vcc = 3.0V ± 10%		8.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, Vcc = Vcc min				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.0mA, Vcc = Vcc min		0.85 Vcc			V
V_{OH2}		I_{OH} = -100 uA, Vcc = Vcc min		Vcc-0.4			
V_{LKO}	Low Vcc Lock-Out Voltage (Note 5)			2.0		2.5	V

Notes:

*1. The Icc current listed is typically less than 2 mA/MHz, with OE# at V_{IH} , **Typical condition : 25°C, Vcc = 3V***

2. Maximum I_{CC} specifications are tested with Vcc = Vcc max.

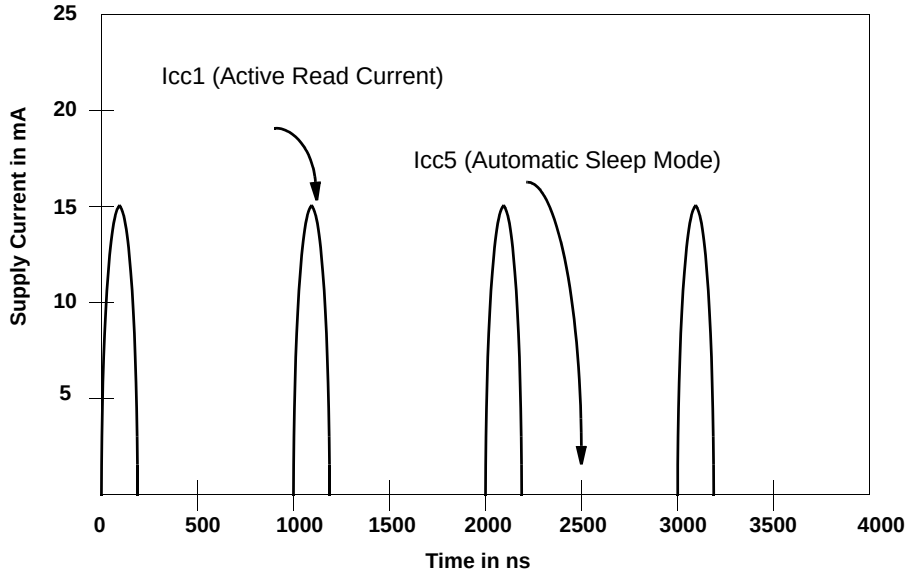
3. Icc active while Embedded Erase or Embedded Program is in progress.

4. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30ns. Typical sleep mode current is 15 uA.

5. Not 100% tested.

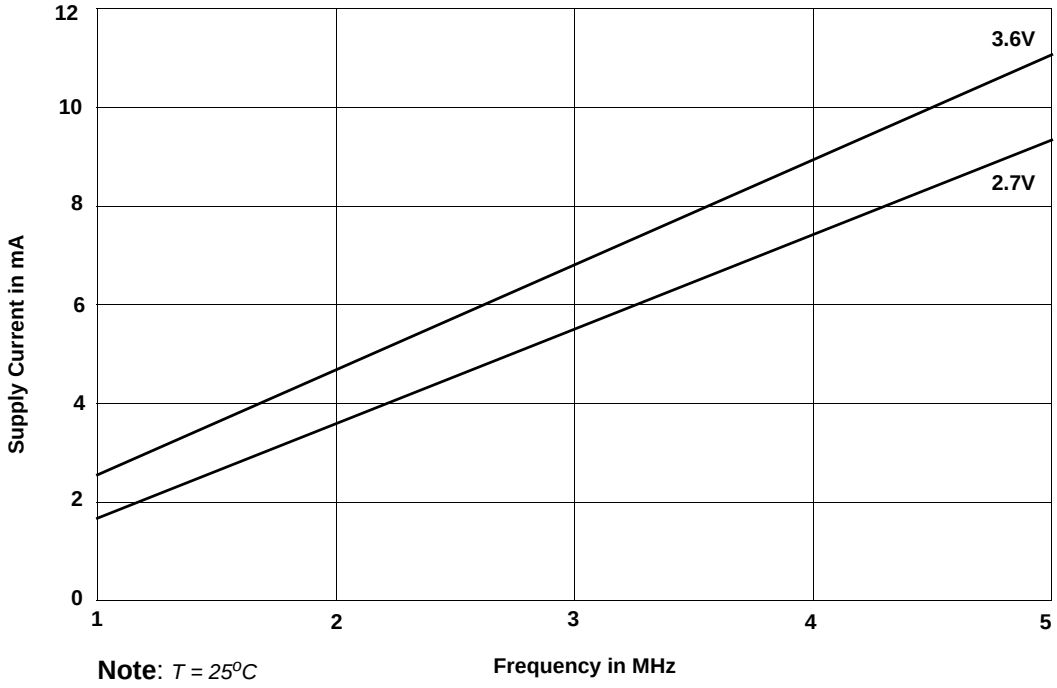
DC CHARACTERISTICS

Zero-Power Flash



Note: *Addresses are switching at 1 MHz*

Figure 14. I_{cc1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: *T = 25°C*

Figure 15. Typical I_{cc1} vs. Frequency

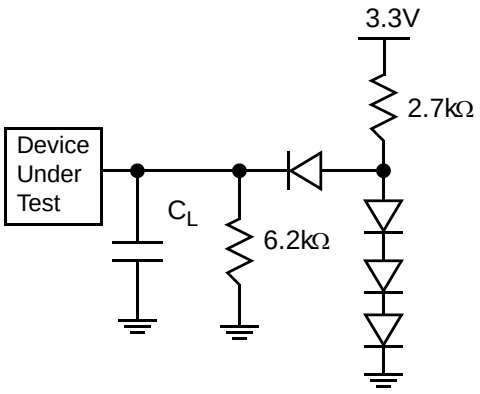


Figure 16. Test Setup

Note: *Diodes are IN3064 or equivalent*

Table 12. Test Specifications

Test Condition	70	90
Output Load	1TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30pF	100pF
Input Rise and Fall Times	5 ns	
Input Pulse Levels	0.0V ~ 3.0V	
Input timing measurement reference levels	1.5V	
Output timing measurement reference levels	1.5V	

Key To Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

Figure 17. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Table 13. Read-Only Operations

Parameter		Description		Test Setup		Speed Option		Unit
JEDEC	Std.					70	90	
t_{AVAV}	t_{RC}	Read Cycle Time(Note 1)			Min	70	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#,OE#=V_{IL}	Max	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE#=V_{IL}	Max	70	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	16		ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	16		ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0		ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0		ns
			Toggle and Data# Polling		Min	10		ns

Note : *1. Not 100% tested*

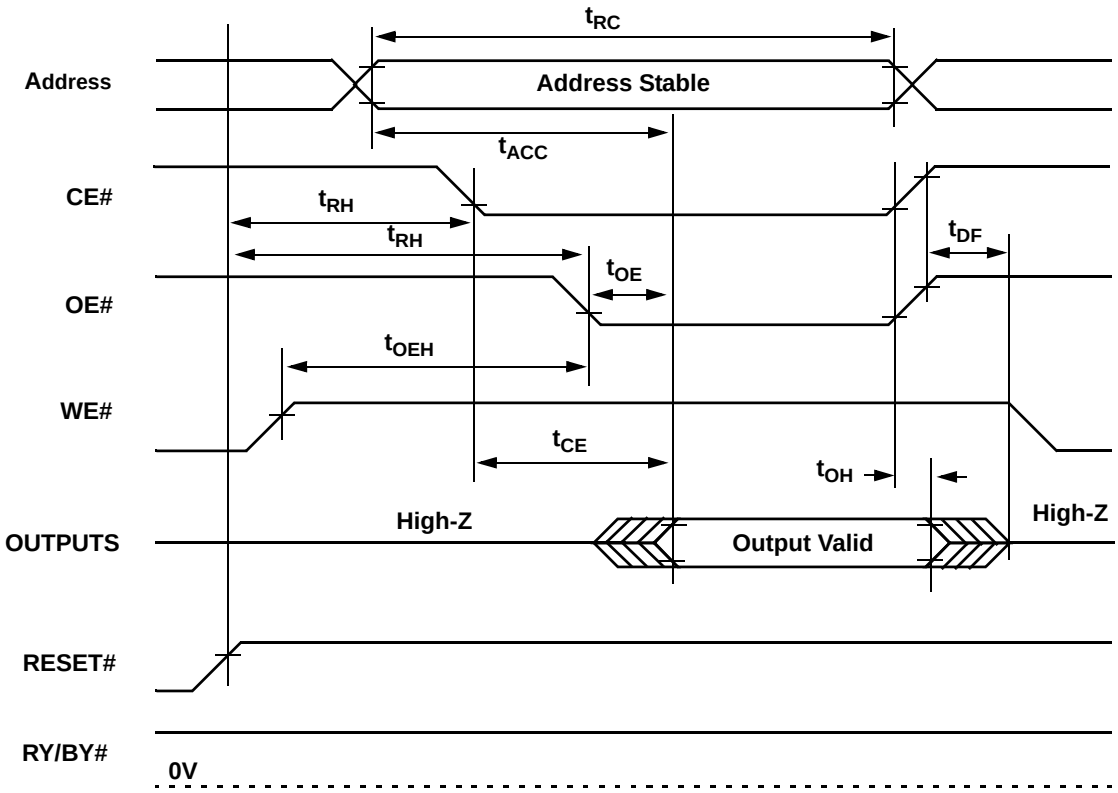


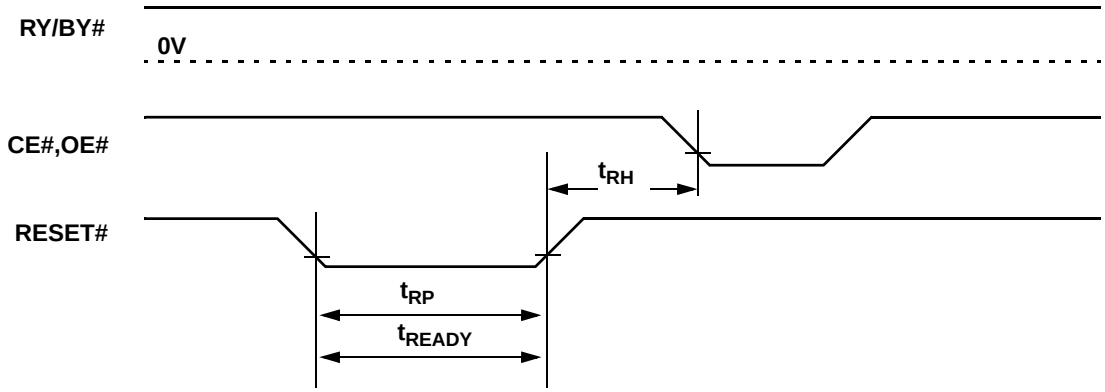
Figure 18. Read Operation Timings

AC CHARACTERISTICS

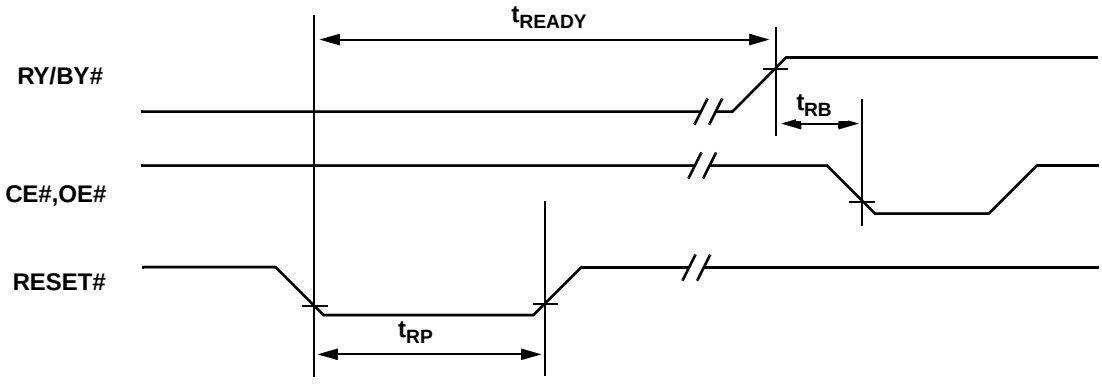
Table 14. Hardware Reset (RESET #)

Parameter		Description		All Speed Options	Unit
JEDEC	Std.				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	**us**
	t_{Ready}	RESET# Pin Low (Not During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	RESET High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	**us**
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note : *Not 100% tested*



(A) Not During Embedded Algorithm



(B) During Embedded Algorithm

Figure 19. Reset Timings

AC CHARACTERISTICS

Table 15. Word/Byte Configuration (BYTE#)

Parameter		Description		70	90	Unit
JEDEC	Std.					
	t_{ELFL}/t_{ELFH}	CE# to BYTE# Switching Low or High	Max	5		ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH Z	Max	30		ns
	t_{FHQV}	BYTE# Switching High to Output Active	Min	70	90	ns

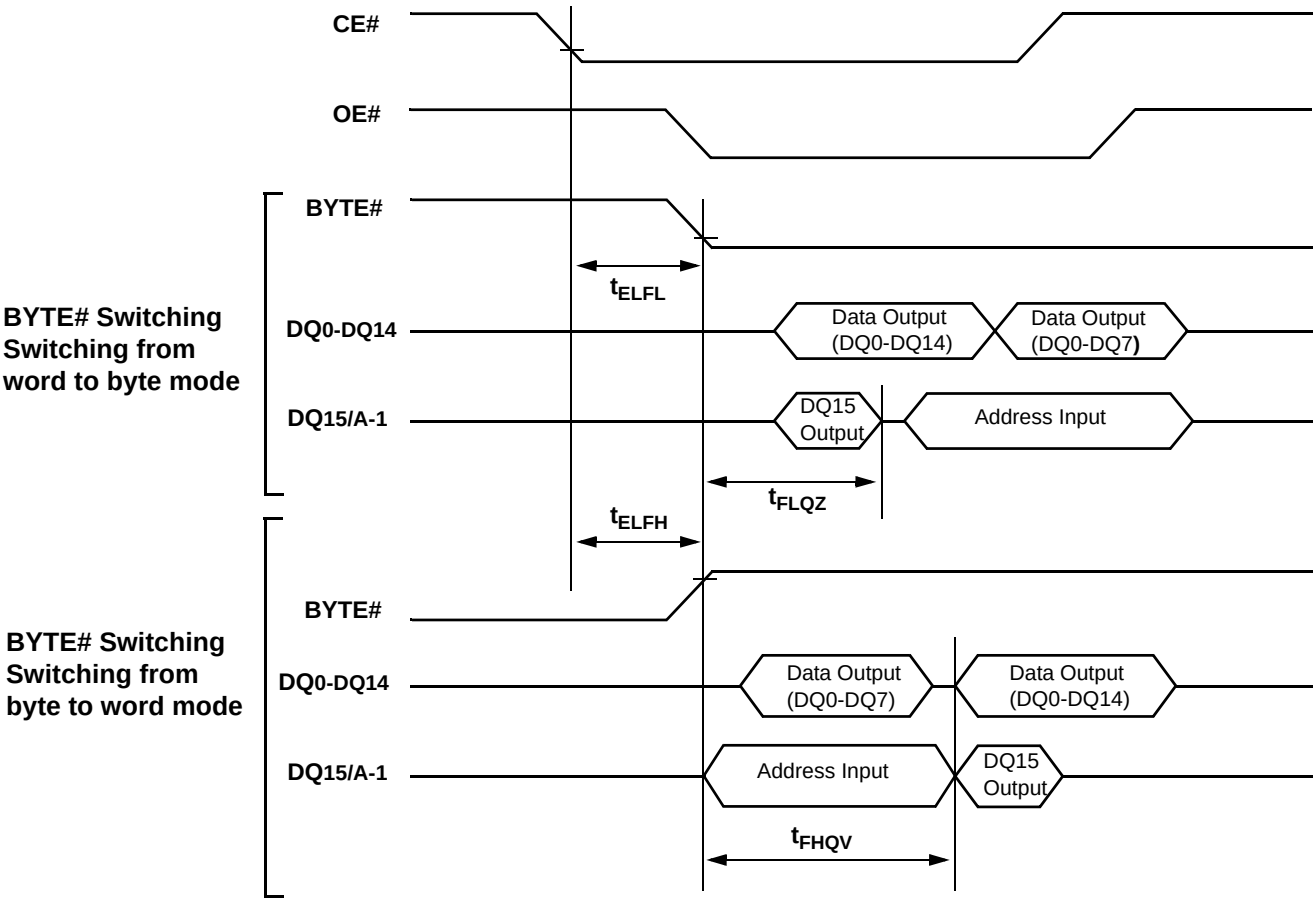
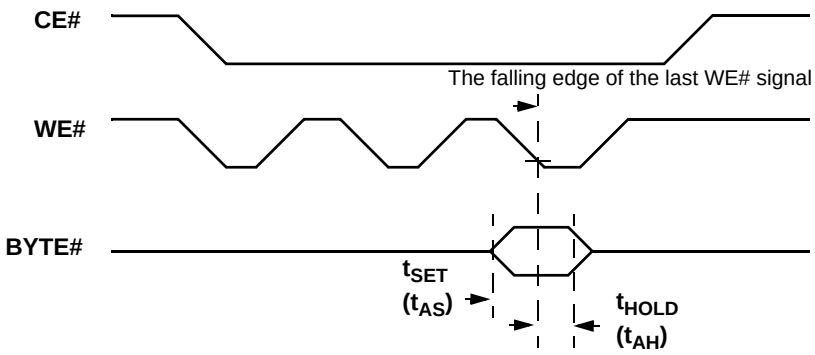


Figure 20. BYTE# Timing for Read Operations



Note : *Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.*

Figure 21. BYTE# Timing for Write Operations

AC CHARACTERISTICS

Table 16. Erase and Program Operations

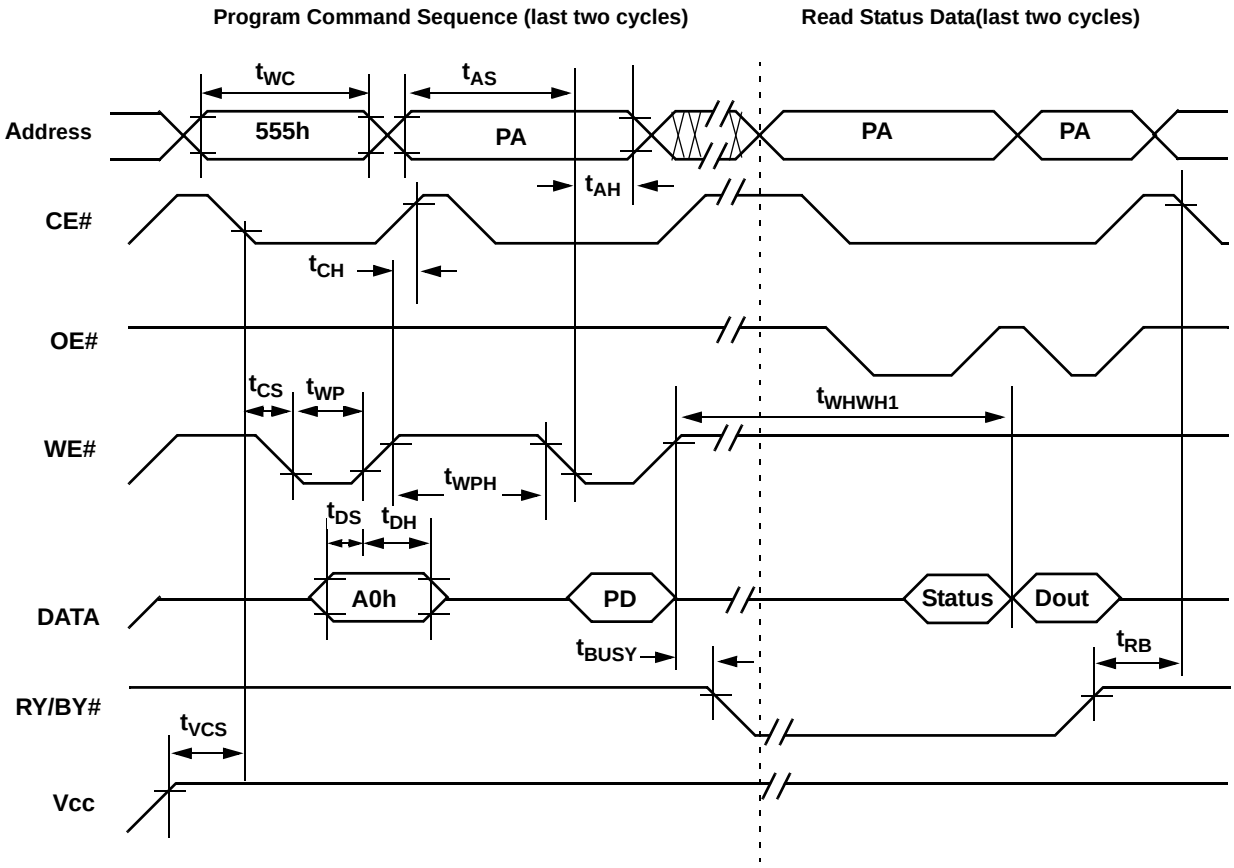
Parameter		Description			70	90	Unit
JEDEC	Std.						
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15		ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0		ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	35	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	30	35	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30		ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	6		us
			Word	Typ	8		
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte (Note 2)		Typ	4		us
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7		sec
	t_{VCS}	Vcc Setup Time (Note 1)		Min	50		us
	t_{RB}	Write Recovery Time from RY/BY#		Min	0		ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Min	90		ns

Notes:

1. Not 100% tested.

2. See the "Erase And Programming Performance" section for more information.

AC CHARACTERISTICS

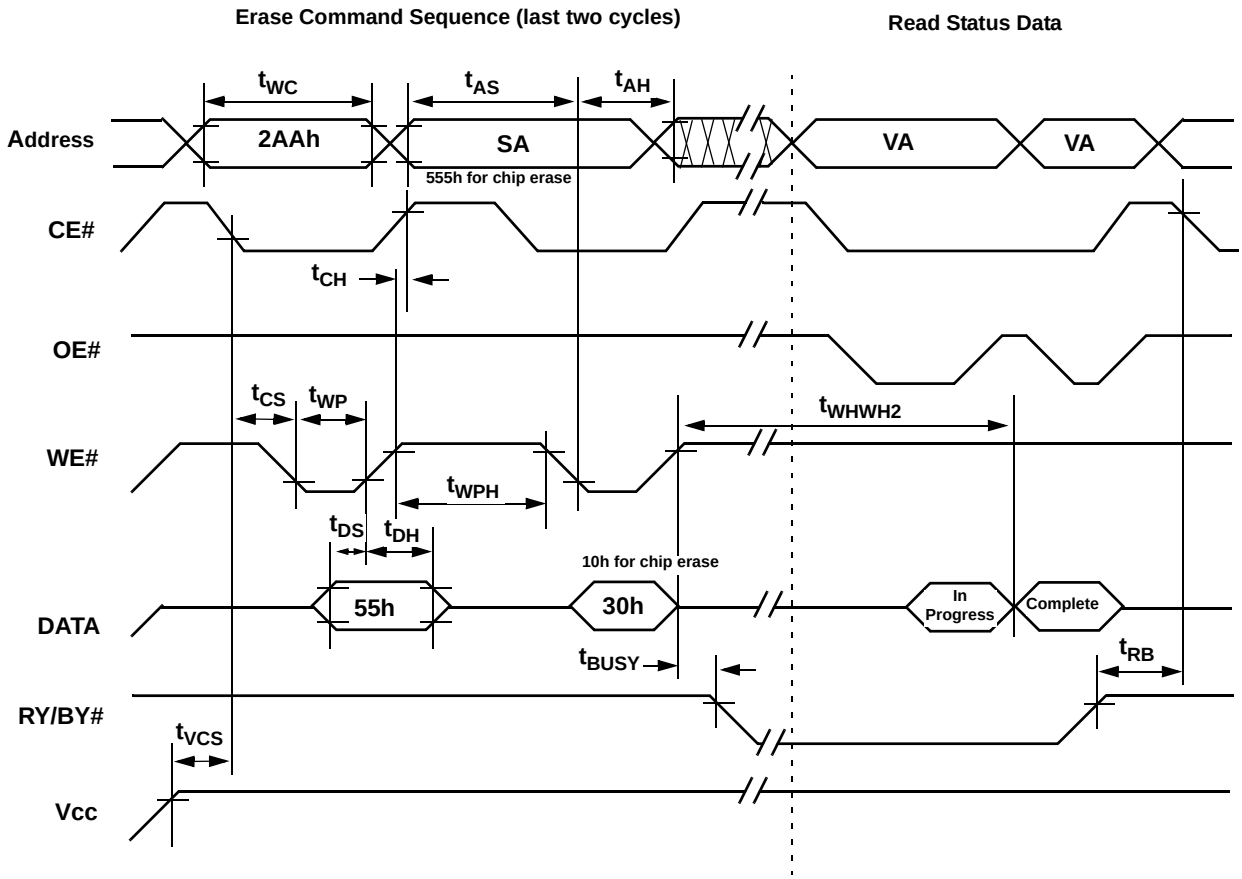


NOTES :

1. PA = program address, PD = program data, Dout is the true data at the program address.
2. Illustration shows device in word mode.

Figure 22. Program Operation Timings

AC CHARACTERISTICS

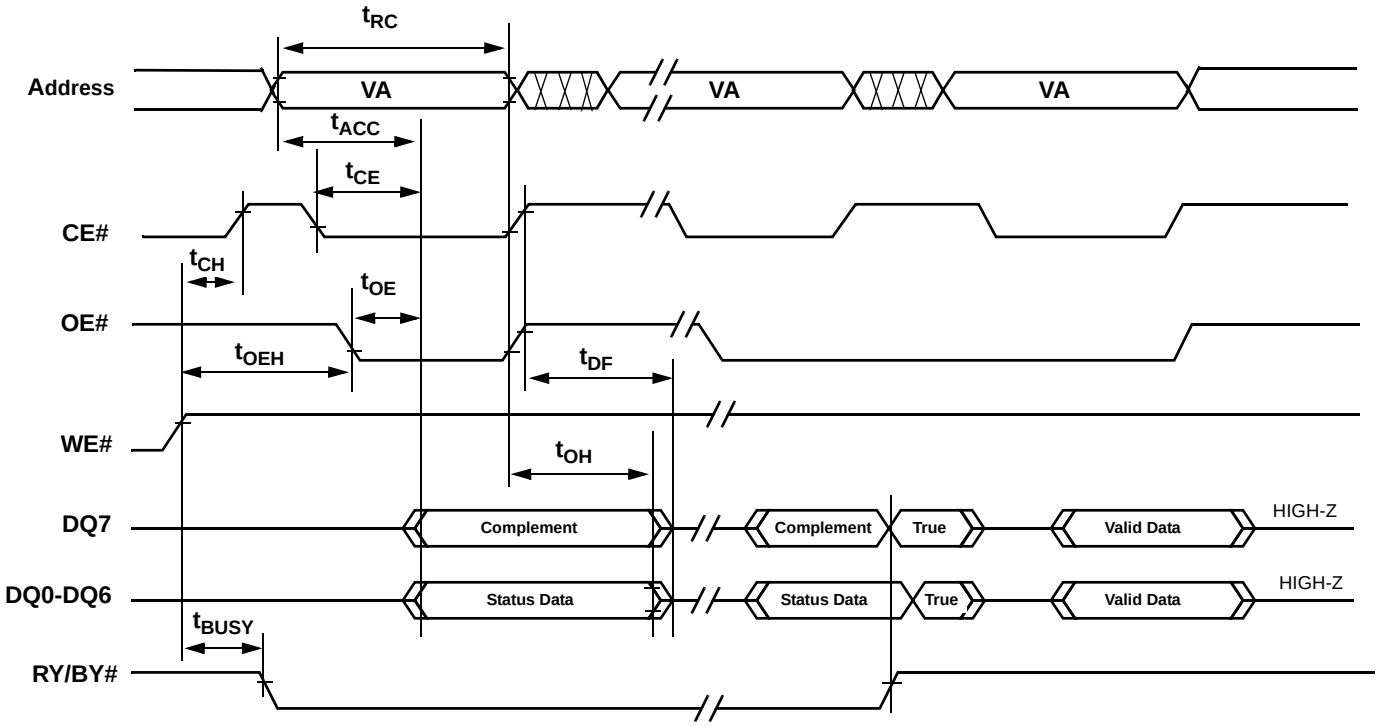


NOTES :

1. SA = sector address(for Sector Erase), VA = valid address for reading status data(see "Write Operation Status").
2. These waveforms are for the word mode.

Figure 23. Chip/Sector Erase Operation Timings

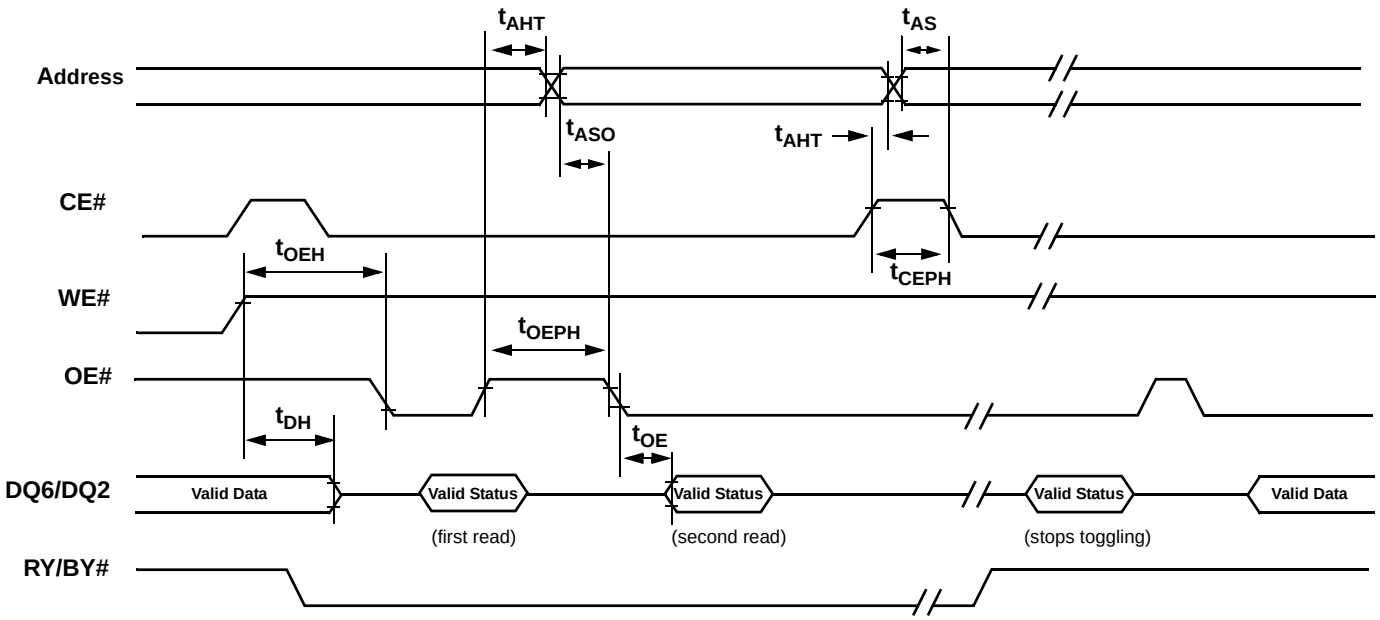
AC CHARACTERISTICS



NOTE : *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle*

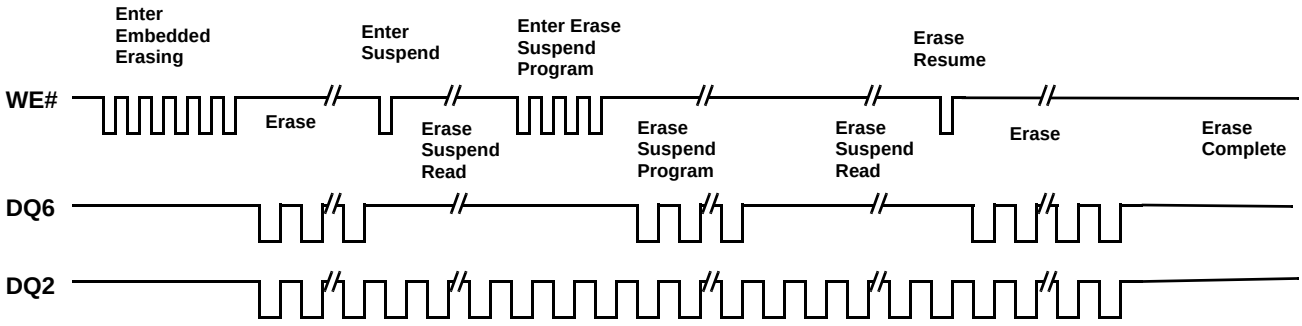
Figure 24. Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS



NOTE : *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 25. Toggle Bit Timings (During Embedded Algorithms)



NOTE : *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 26. DQ2 vs. DQ6

AC CHARACTERISTICS

Table 17. Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std.				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	**us**
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect	Min	4	**us**

Note: *Not 100% tested.*

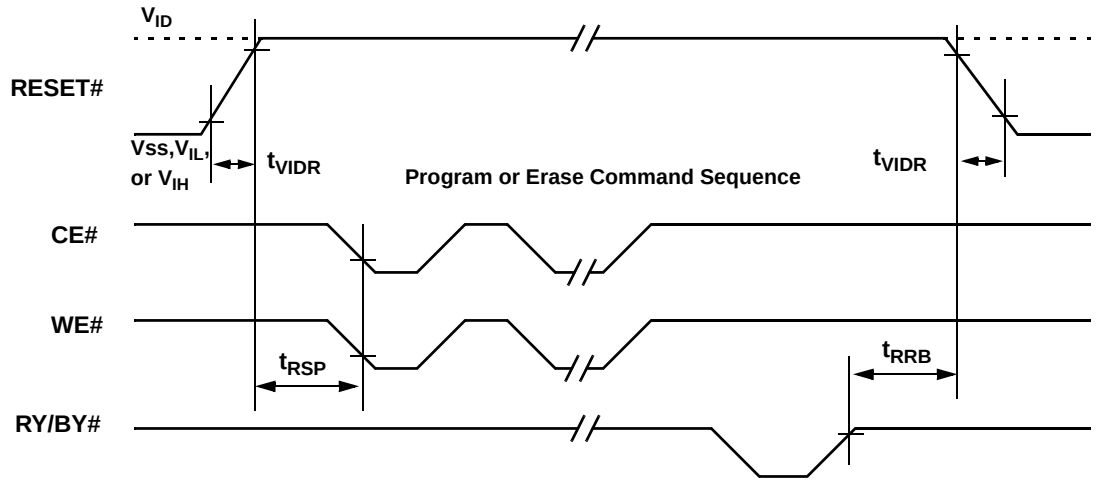


Figure 27. Temporary Sector Unprotect Timing Diagram

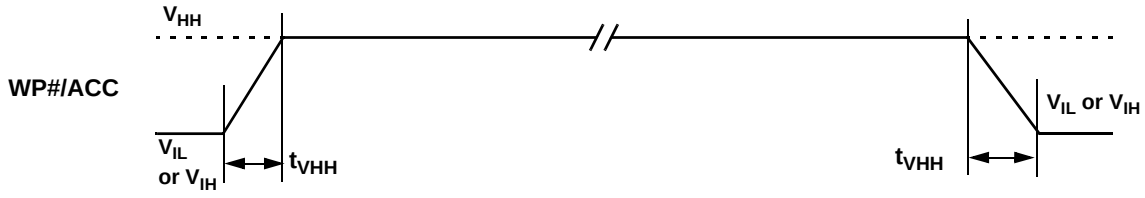
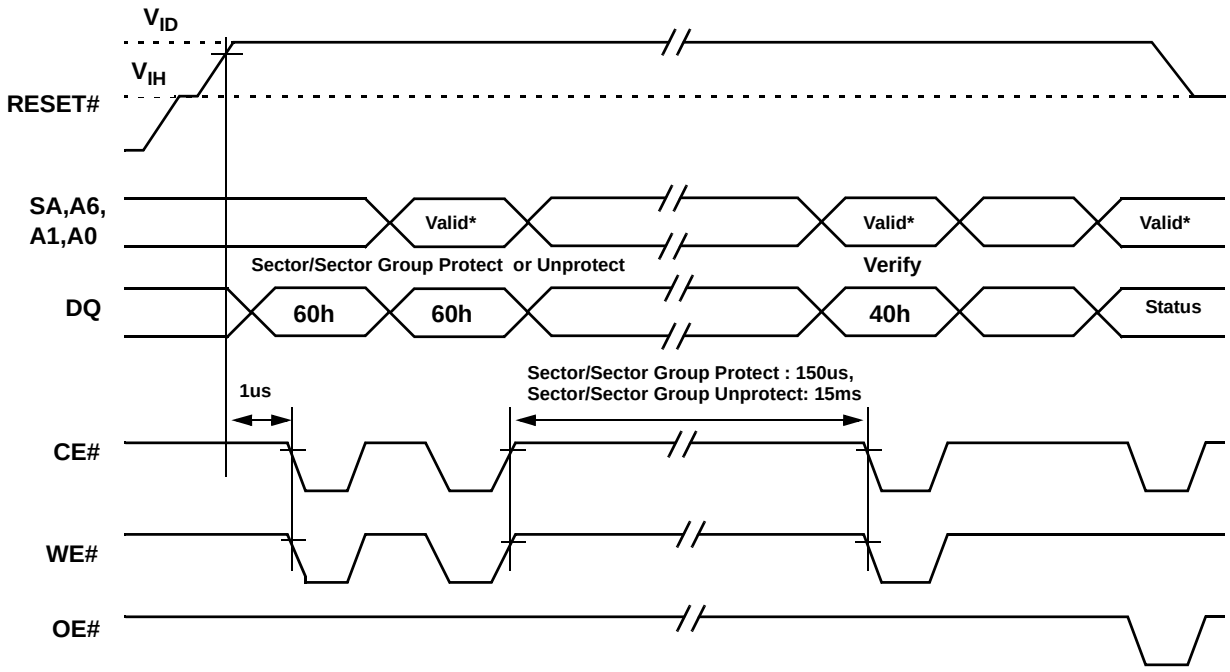


Figure 28. Accelerated Program Timing Diagram

AC CHARACTERISTICS



** For sector protect, A6=0,A1=1,A0=0 For sector unprotect, A6=1,A1=1,A0=0*

Figure 29. Sector/Sector Group Protect & Unprotect Timing Diagram

AC CHARACTERISTICS

Table 18. Alternate CE# Controlled Erase and Program Operations

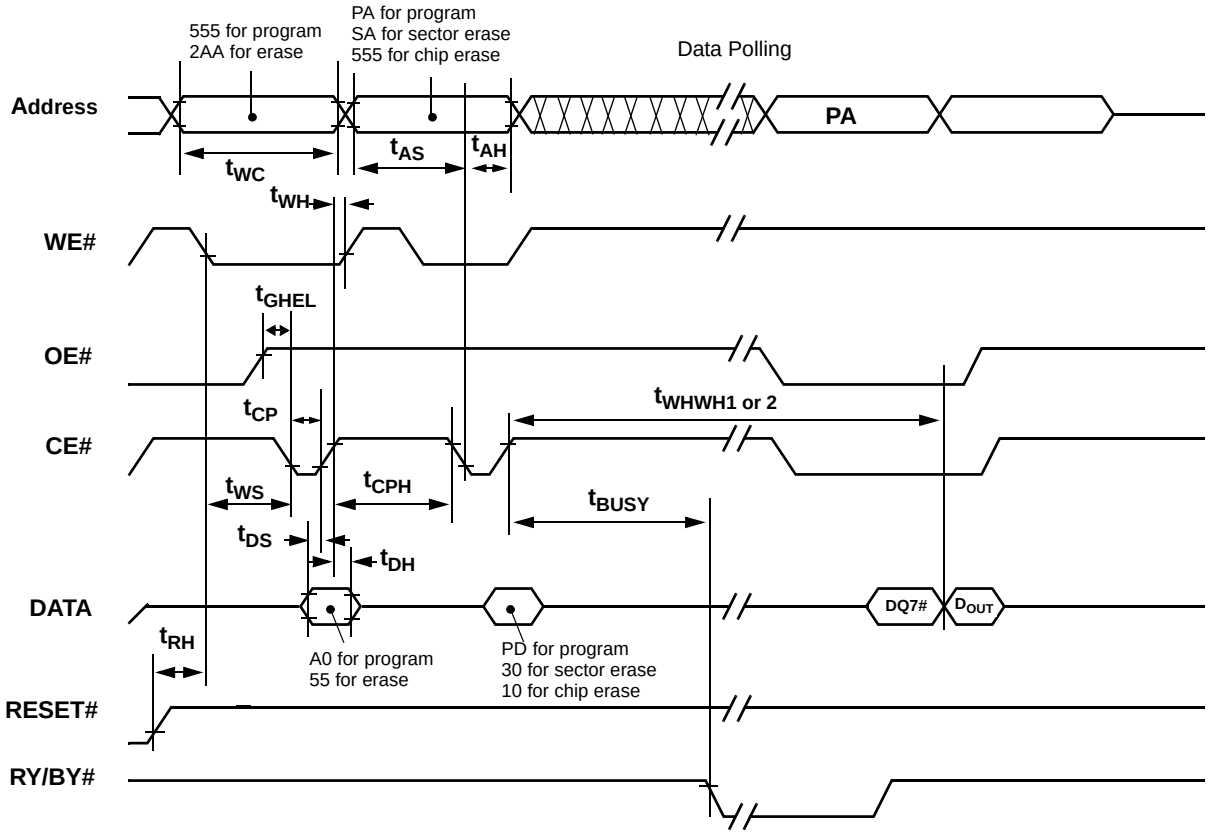
Parameter		Description			70	90	Unit
JEDEC	Std.						
t_{AVAV}	t_{WC}	Write Cycle Time(Note 1)		Min	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	30	35	ns
t_{ELEL}	t_{CPH}	CE# Pulse Width High		Min	30		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	6		us
			Word	Typ	8		
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte (Note 2)		Typ	4		us
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.7		sec

Notes :

1. Not 100% tested

2. See the "Erase And Programming Performance" section for more information.

AC CHARACTERISTICS



NOTES :

1. Figure indicates last two bus cycles of a program or erase operation.
2. PA = program address, SA = sector address, PD = program data
3. DQ7# is the complement of the data written to the device. Dout is the data written to the device.
4. Waveforms are for the word mode.

Figure 30. Alternate CE# Controlled Write(Erase/Program) Operation Timings

Table 19. AC CHARACTERISTICS

Parameter	Description		Value		Unit
t_{OE}	Output Enable to Output Delay	Max	30	40	ns
t_{VIDR}	Voltage Transition Time	Min	500		ns
t_{WPP1}	Write Pulse Width for Protection Operation	Min	150		us
t_{WPP2}	Write Pulse Width for Unprotection Operation	Min	15		ms
t_{OESP}	OE# Setup Time to WE# Active	Min	4		us
t_{CSP}	CE# Setup Time to WE# Active	Min	4		us
t_{ST}	Voltage Setup Time	Min	4		us

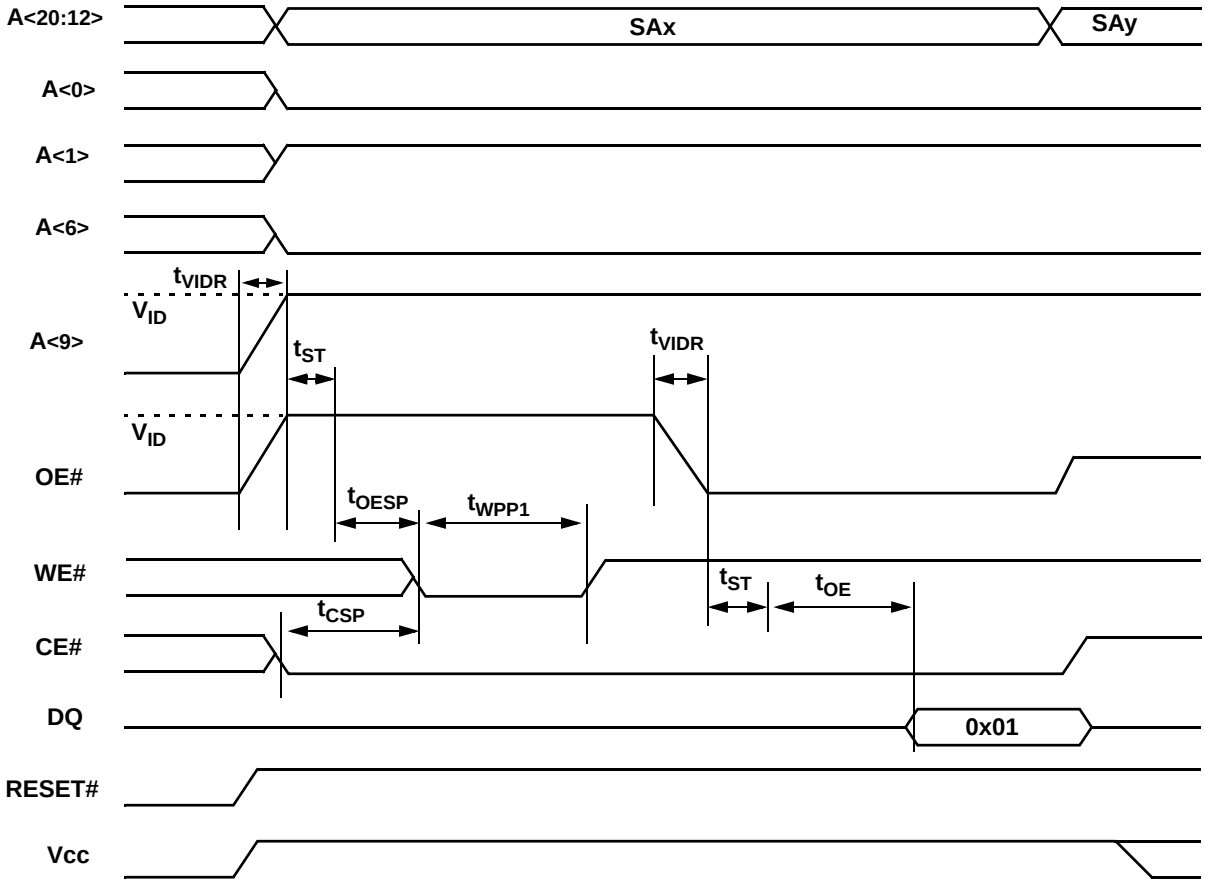
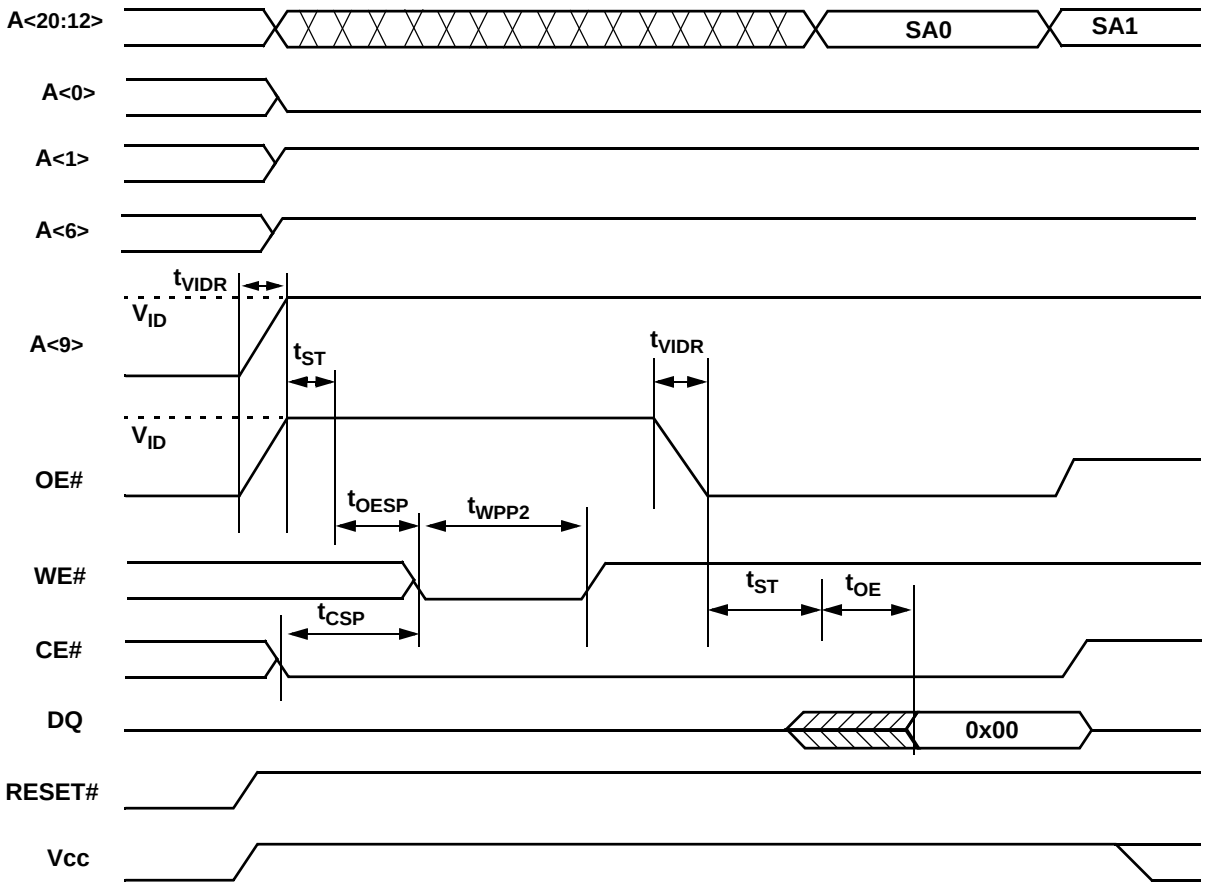


Figure 31. Sector Protection timings (A9 High-Voltage Method)

AC CHARACTERISTICS



NOTE : *It is recommended to verify for all sectors.*

Figure 32. Sector Unprotection timings (A9 High-Voltage Method)

AC CHARACTERISTICS

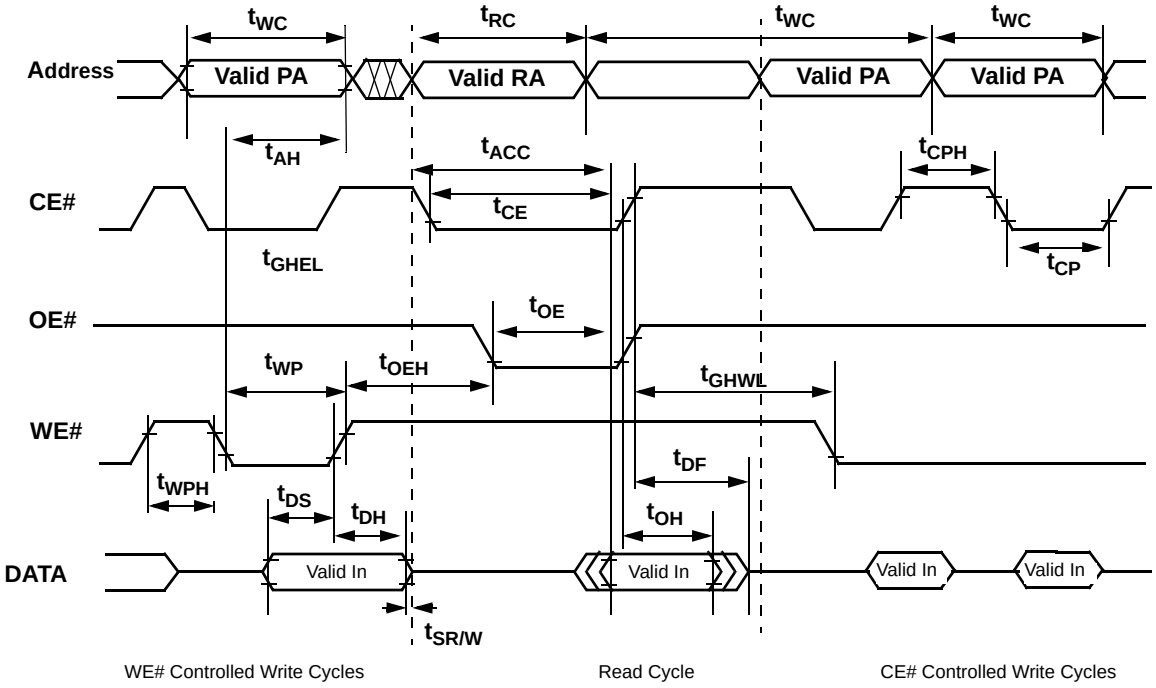


Figure 33. Back-to-back Read/Write Cycle Timings

Table 20. ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.7	15	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		50		sec	
Byte Program Time		6	150	us	Exclude system level overhead (Note 5)
Accelerated Byte/Word Program Time		4	120	us	
Word Program Time		8	210	us	
Chip Program Time (Note 3)	Byte Mode	25	76	sec	
	Word Mode	17	50		

Notes:

1. *Typical program and erase times assume the following conditions: 25^{o}C, 3.0V Vcc, 10,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90^{o}C, Vcc = 2.7V, 100,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two-or-four-bus-cycle sequence for the program command. See Table 9 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

Table 21. LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to Vss on all pins except I/O pins (including A9, OE#, and RESET#)	- 1.0V	12.5V
Input voltage with respect to Vss on all I/O pins	- 1.0V	Vcc + 1.0V
Vcc Current	- 100mA	+100mA

Note: *Includes all pins except Vcc. Test conditions: Vcc = 3.0 V, one pin at a time*

Table 22. TSOP AND BGA PACKAGE CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup		Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TSOP	6	7.5	pF
			FBGA	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TSOP	8.5	12	pF
			FBGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TSOP	7.5	9	pF
			FBGA	3.9	4.7	pF

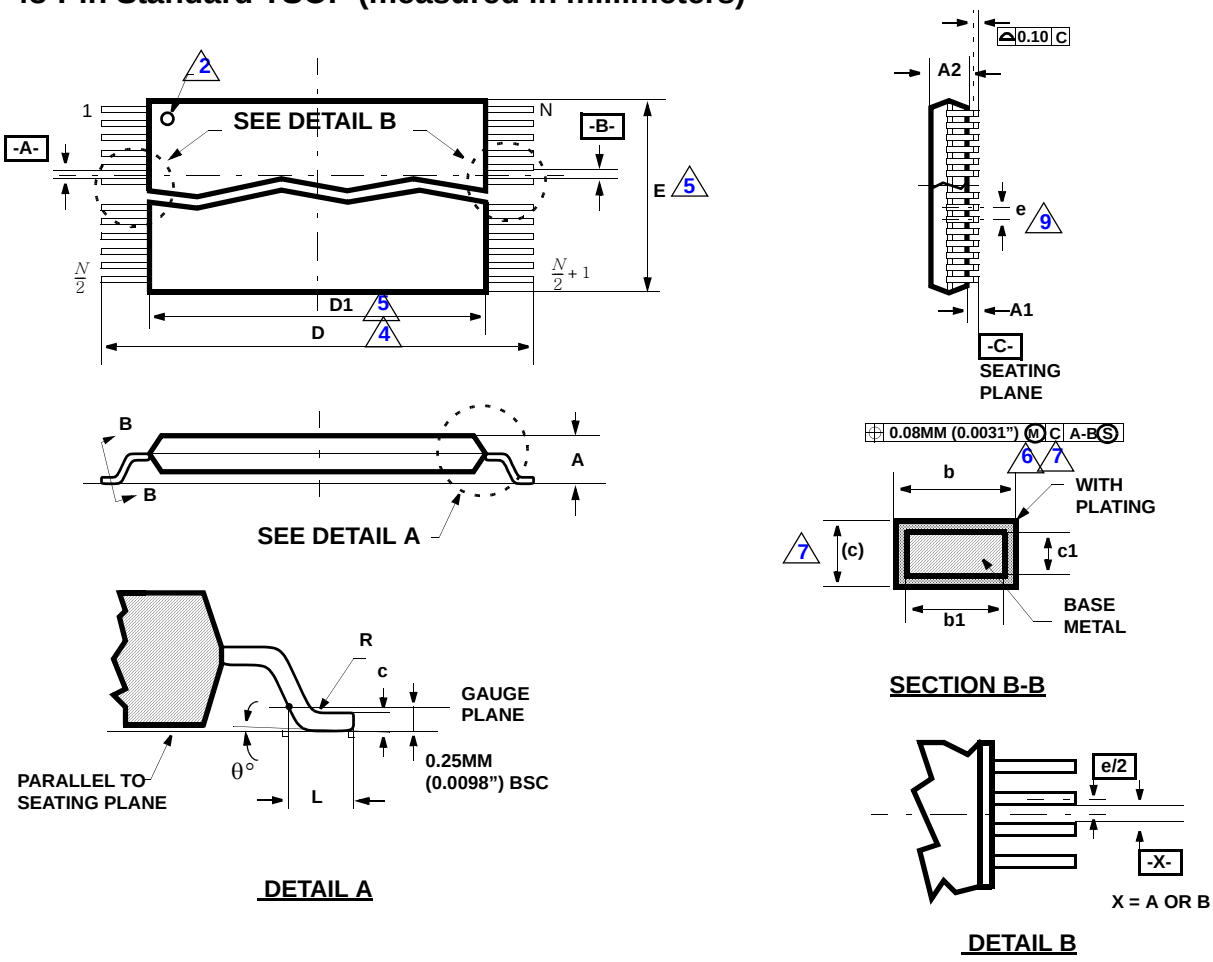
Notes:

1. *Sampled, not 100% tested*
2. *Test conditions TA = 25^{o}C, f=1.0MHz.*

Table 23. DATA RETENTION

Parameter Description	Test conditions	Min	Unit
Minimum Pattern Data Retention Time	150^{o}C	10	Years
	125^{o}C	20	Years

PHYSICAL DIMENSIONS
48-Pin Standard TSOP (measured in millimeters)

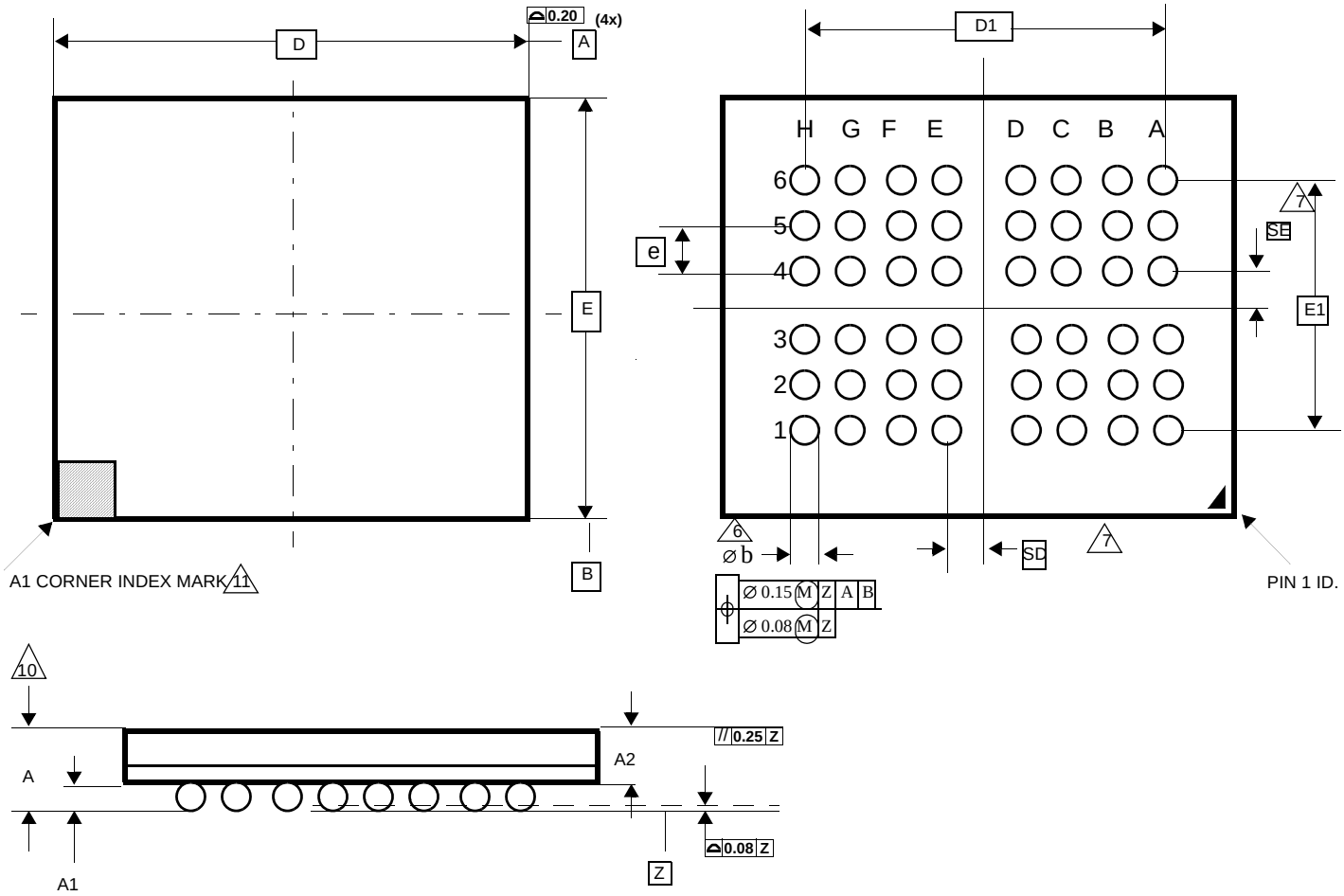


Package	TS 48		
JEDEC	MO-142 (B) DD		
Symbol	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	-	0.16
c	0.10	-	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	-	0.20
N	48		

NOTES:

1. *Controlling dimensions are in millimeters(mm). (Dimensioning and tolerancing conforms to ANSI Y14.5M-1982)*
2. ***Pin 1** identifier for standard pin out (Die up).*
3. ***Pin 1** identifier for reverse pin out (Die down): Ink or Laser mark*
4. *To be determined at the seating plane. The seating plane is defined as the plane of contact that is made when the package leads are allowed to rest freely on a flat horizontal surface.*
5. *Dimension **D1** and **E** do not include mold protrusion. Allowable mold protrusion is 0.15mm (0.0059") per side.*
6. *Dimension **b** does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.0031") total in excess of **b** dimension at max. material condition. Minimum space between protrusion and an adjacent lead to be 0.07mm (0.0028").*
7. *These dimensions apply to the flat section of the lead between 0.10mm (0.0039") and 0.25mm (0.0098") from the lead tip.*
8. *Lead coplanarity shall be within 0.10mm (0.004") as measured from the seating plane.*
9. *Dimension "**e**" is measured at the centerline of the leads.*

PHYSICAL DIMENSIONS
48-Ball FBGA (6 x 8 mm)



PACKAGE	xFBD 048			
JEDEC	N/A			
	6.00 mm x8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A			1.10	OVERALL THICK NESS
A1	0.21	0.25	0.29	BALL HEIGHT
A2	0.7	0.76	0.82	BODY THICKNESS
D		**8.00 BSC**		BODY SIZE
E		**6.00 BSC**		BODY SIZE
D1		5.60 BSC		BALL FOOTPRINT
E1		4.00 BSC		BALL FOOTPRINT
MD		8		ROW MATRIX SIZED DIRECTION
ME		6		ROW MATRIX SIZED DIRECTION
N		48		TOTAL BALL COUNT
b	0.30	0.35	0.40	BALL DIAMETER
e		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC		SOLDER BALL PLACEMENT

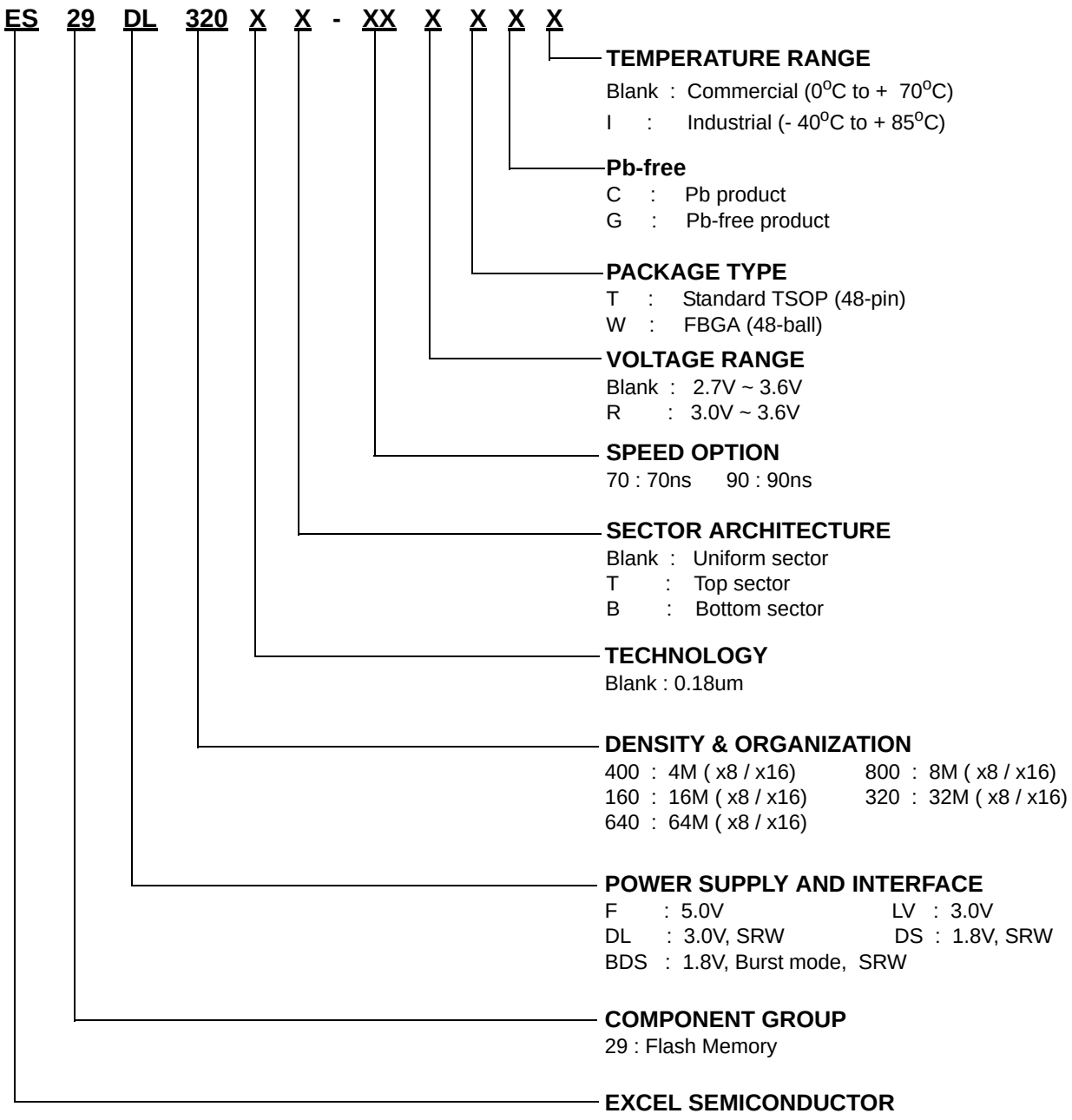
NOTES:

1. *Dimensioning and tolerancing per ASME Y14.5M-1994*
2. *All dimensions are in millimeters.*
3. *Ball position designation per JESD 95-1, SPP-010.*
4. *e represents the solder ball grid pitch.*
5. *Symbol "**MD**" is the ball row matrix size in the "**D**" direction. Symbol "**ME**" is the ball column matrix size in the "**E**" direction. **N** is the maximum number of solder balls for matrix size **MD** X **ME**.*
6. *Dimension "**b**" is measured at the maximum ball diameter in a plane parallel to datum **Z**.*
7. ***SD** and **SE** are measured with respect to datums **A** and **B** and define the position of the center solder ball in the outer row. When there is an odd number of solder balls in the outer row parallel to the **D** or **E** dimension, respectively, **SD** or **SE** = 0.000 when there is an even number of solder balls in the outer row, **SD** or **SE** = e/2*
8. *"**X**" in the package variations denotes part is outer qualification.*
9. *"**+**" in the package drawing indicate the theoretical center of depopulated balls.*
10. *For package thickness **A** is the controlling dimension.*
11. ***A1** corner to be indentified by chamfer, ink mark, metallized markings indention or other means.*

ORDERING INFORMATION

Standard Products

ESI standard products are available in several package and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Product Selection Guide

Industrial Device

Part No.	Speed	Vcc	Boot Sector	Package	Pb	Ball Pitch/Size	Body Size
ES29DL320T-70TGI	70ns	2.7 - 3.6V	Top	48-pin TSOP	Pb-free		
ES29DL320T-70TCI	70ns	2.7 - 3.6V	Top	48-pin TSOP	-		
ES29DL320B-70TGI	70ns	2.7 - 3.6V	Bottom	48-pin TSOP	Pb-free		
ES29DL320B-70TCI	70ns	2.7 - 3.6V	Bottom	48-pin TSOP	-		
ES29DL320T-90TGI	90ns	2.7 - 3.6V	Top	48-pin TSOP	Pb-free		
ES29DL320T-90TCI	90ns	2.7 - 3.6V	Top	48-pin TSOP	-		
ES29DL320B-90TGI	90ns	2.7 - 3.6V	Bottom	48-pin TSOP	Pb-free		
ES29DL320B-90TCI	90ns	2.7 - 3.6V	Bottom	48-pin TSOP	-		
ES29DL320T-70WGI	70ns	2.7 - 3.6V	Top	48-Ball FBGA	Pb-free	0.8mm/0.3mm	6mm x 8mm
ES29DL320T-70WCI	70ns	2.7 - 3.6V	Top	48-Ball FBGA	-	0.8mm/0.3mm	6mm x 8mm
ES29DL320B-70WGI	70ns	2.7 - 3.6V	Bottom	48-Ball FBGA	Pb-free	0.8mm/0.3mm	6mm x 8mm
ES29DL320B-70WCI	70ns	2.7 - 3.6V	Bottom	48-Ball FBGA	-	0.8mm/0.3mm	6mm x 8mm
ES29DL320T-90WGI	90ns	2.7 - 3.6V	Top	48-Ball FBGA	Pb-free	0.8mm/0.3mm	6mm x 8mm
ES29DL320T-90WCI	90ns	2.7 - 3.6V	Top	48-Ball FBGA	-	0.8mm/0.3mm	6mm x 8mm
ES29DL320B-90WGI	90ns	2.7 - 3.6V	Bottom	48-Ball FBGA	Pb-free	0.8mm/0.3mm	6mm x 8mm
ES29DL320B-90WCI	90ns	2.7 - 3.6V	Bottom	48-Ball FBGA	-	0.8mm/0.3mm	6mm x 8mm

Product Selection Guide

Commercial Device

Part No.	Speed	Vcc	Boot Sector	Package	Pb	Ball Pitch/Size	Body Size
ES29DL320T-70TG	70ns	2.7 - 3.6V	Top	48-pin TSOP	Pb-free		
ES29DL320T-70TC	70ns	2.7 - 3.6V	Top	48-pin TSOP	-		
ES29DL320B-70TG	70ns	2.7 - 3.6V	Bottom	48-pin TSOP	Pb-free		
ES29DL320B-70TC	70ns	2.7 - 3.6V	Bottom	48-pin TSOP	-		
ES29DL320T-90TG	90ns	2.7 - 3.6V	Top	48-pin TSOP	Pb-free		
ES29DL320T-90TC	90ns	2.7 - 3.6V	Top	48-pin TSOP	-		
ES29DL320B-90TG	90ns	2.7 - 3.6V	Bottom	48-pin TSOP	Pb-free		
ES29DL320B-90TC	90ns	2.7 - 3.6V	Bottom	48-pin TSOP	-		
ES29DL320T-70WG	70ns	2.7 - 3.6V	Top	48-Ball FBGA	Pb-free	0.8mm/0.3mm	6mm x 8mm
ES29DL320T-70WC	70ns	2.7 - 3.6V	Top	48-Ball FBGA	-	0.8mm/0.3mm	6mm x 8mm
ES29DL320B-70WG	70ns	2.7 - 3.6V	Bottom	48-Ball FBGA	Pb-free	0.8mm/0.3mm	6mm x 8mm
ES29DL320B-70WC	70ns	2.7 - 3.6V	Bottom	48-Ball FBGA	-	0.8mm/0.3mm	6mm x 8mm
ES29DL320T-90WG	90ns	2.7 - 3.6V	Top	48-Ball FBGA	Pb-free	0.8mm/0.3mm	6mm x 8mm
ES29DL320T-90WC	90ns	2.7 - 3.6V	Top	48-Ball FBGA	-	0.8mm/0.3mm	6mm x 8mm
ES29DL320B-90WG	90ns	2.7 - 3.6V	Bottom	48-Ball FBGA	Pb-free	0.8mm/0.3mm	6mm x 8mm
ES29DL320B-90WC	90ns	2.7 - 3.6V	Bottom	48-Ball FBGA	-	0.8mm/0.3mm	6mm x 8mm

Document Title

32M DL Flash Memory

Revision History

Revision Number	Data	Items
Rev. 0A	Mar. 13, 2005	1. Initial Release Version.
Rev. 0B	Jul. 15, 2005	1. Remove 63-Ball Fine-Pitch Ball Grid array Package 2. Remove 64-ball Fortified-Pitch Ball Grid array pacakge 3. Corrected demension of 48-ball FBGA package
Rev. 0C	Jan. 5, 2006	1. Add RoHS-Compliant Package Option
Rev. 0D	Mar. 21, 2006	1. The TECHNOLOGY option from ORDERING INFORMATION is changed from E:0.15um to E:0.18um (2nd Gen.).
Rev. 0E	May. 25, 2006	1. Remove 55ns Speed Option 2. Change TECHNOLOGY Option (Blank : 0.18um) 3. Corrected Device ID 4. Corrected Standby Current

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