SC4901
COMBI-SYNC Secondary Side Synchronous Rectifier and Regulator

POWER MANAGEMENT

Description

SC4901 is a unique secondary side regulator designed for implementing Semtech's proprietary Combi-Sync topology for isolated convertors with multiple outputs. The Combi-Sync is a true all-MOSFET topology that allows synchronous rectification and post regulation of transformer isolated outputs, resulting in higher efficiency and low component count. Details of this unique topology are described in the Application Information section.

Multiple outputs can be synchronously rectified and independently regulated by individual SC4901s. Each output has its own ON/OFF control, soft start, remote sense and current limits. They can be turned on or off without affecting the primary or other outputs. The secondary side control makes it much easier to design tight control loops and implement load current sharing and hot swap features. All devices are synchronised to the transformer winding. The current sense can be either from the output inductor for high efficiency or a resistor for better accuracy. An amplified current signal is provided for external use.

Each device is capable of driving high side MOSFETs with 2A current. The forward drive is configured for direct connection to a 1:1 pulse transformer. SC4901 has an undervoltage lockout with typical turn-on threshold of 4.5V and is available in a low cost TSSOP-16 package

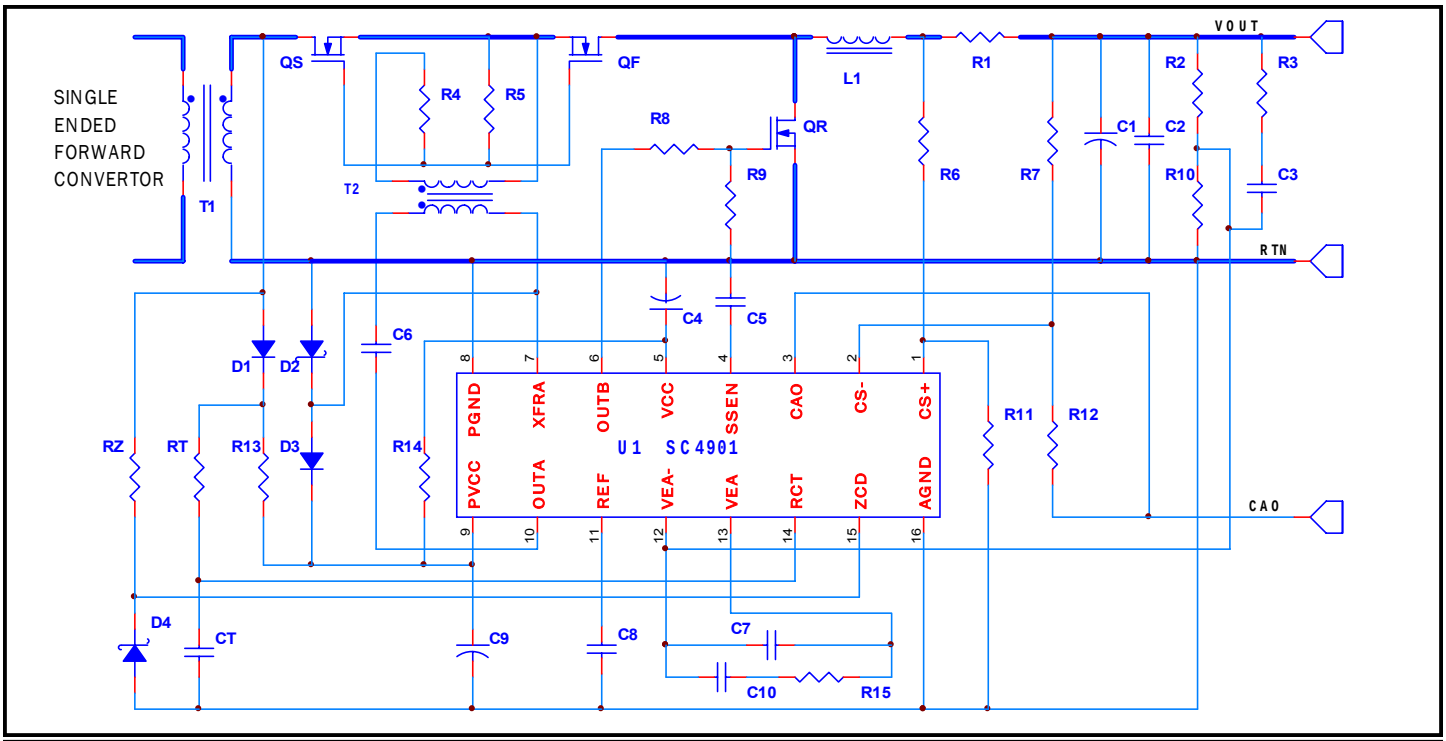
Features

- Single controller performs synchronous rectification and post regulation
- Independent regulation of multiple outputs from a common secondary winding
- Turn on shoot through inherently eliminated
- Primary switch turns ON and OFF with zero current
- No synchronising or any other signals needed across the isolation boundary
- Eliminates the need for a secondary bias supply
- Independent soft start, ON/OFF, remote sense and current limit for each output
- Resistive or inductive current sensing with 2V current signal and 2.5V reference for external applications.
- 4.5 to 18V operation
- Max operating frequency to 1 MHz
- Low profile 16 pin TSSOP package
- Based on Semtech's patented Combi Sync concept

Applications

- Telecom isolated DC to DC converters with multiple low voltage outputs
- High density brick and sub brick modules with independently regulated multiple outputs
- Distributed power architectures
- Isolated VRMs

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction.
Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage	AVCC, PVCC	18	V
Ground voltages	AGND to PGND	+0.3V	V
Output Voltages	OUTA, XFRA, OUTB	PVCC	V
CS+ and CS- common mode voltage	CS+, CS-	VCC - 2	V
ZCD pin wrt to AGND	V_{ZCD}	0 to 6V	V
All other pins wrt AGND		-0.3 to +6	V
Max current into ZCD pin	I_{ZCD}	5 mA	mA
Max current into RCT pin	I_{RCT}	2 mA	mA
OUTA, XFRA Current Source or Sink		+2.0	A
OUTB Current Source or Sink	I_{OUTB}	+1.0	A
Ambient Temperature Range	T_A	-40 to +125	°C
Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-60 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	260	°C
ESD Rating (Human Body Model)	V_{ESD}	2.0	kV

Electrical Characteristics

Unless specified: T_A = 25°C, VCC = 12V

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply					
Operating Current	SSEN = 5V, VCC = 15V I_{OUTX} = 0		7	10	mA
Undervoltage Lockout					
Start Threshold	AVCC rising	4.3	4.5	4.8	V
UVLO Hysteresis	AVCC falling		0.3		V
Soft Start and Enable					
Enable Threshold	V_{ENA}	0.55	0.65	0.75	V
SS Charge Current	I_{SS}	8	10	12	µA
SS Effective Discharge Current	$-I_{SS}$		1.5		µA

Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C, VCC = 12V

Parameter	Test Conditions	Min	Typ	Max	Unit
VREF Reference					
Output Voltage	$T_A = T_J$ = -40 °C to +125°C	2.4	2.5	2.6	V
Output Current	I_{REF}		5		mA
Line Regulation	8V < AVCC < 15V			10	mV
Load Regulation	0 mA < I_{REF} < 5 mA			10	mV
Error Amplifier					
Reference Voltage Level	T_A = 25 °C	0.74	0.750	0.76	V
	$T_A = T_J$ = -40 °C to +125°C	0.735		0.765	V
Input Bias Current			0.1	2	µA
Offset Voltage (1)			2		mV
Open Loop Gain (1)			80		dB
Unity Gain Bandwidth (1)			3		MHz
Slew Rate (1)			2.0		V/µS
Output High Voltage	I_{COMP} = 0.1 mA source	2.7	2.9		V
Output Low Voltage	I_{COMP} = 0.1 mA sink			0.8	V
ZCD and RCT					
Frequency Range	Frequency range Min		50		KHz
	Frequency range Max		1000		
Peak Voltage (1)	Clamped internally		3.0		V
Valley Voltage (1)			1.0		V
Timing Capacitor Discharge Current (1)			11		mA
Current Limit					
Cycle by Cycle Threshold	V_{CAO}	2.3	2.5	2.7	V
Hiccup Mode Threshold	VEA- falling		0.375		V
Delay to Output (1)			75		nS
Current Amplifier offset			2	5	mV

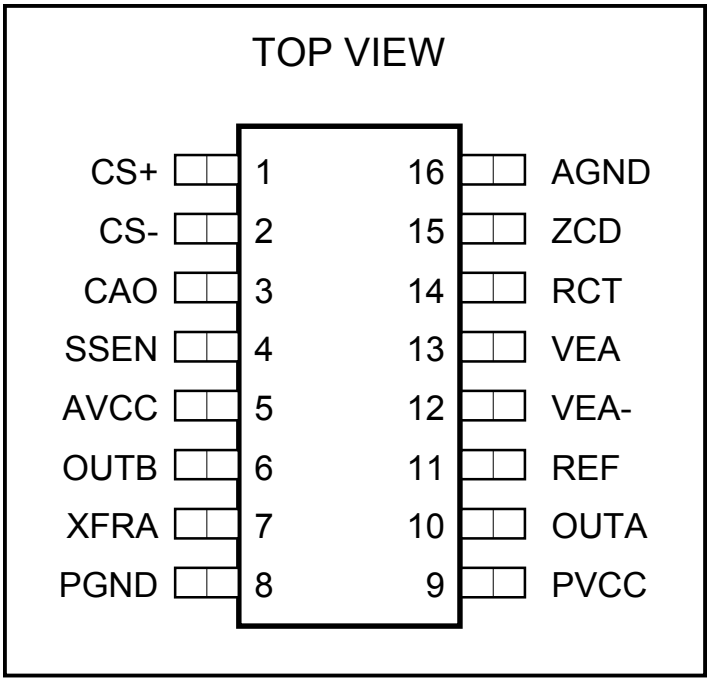
Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C, V_{CC} = 12V

Parameter	Test Conditions	Min	Typ	Max	Unit
Output Drivers					
Output High Voltage OUTA (1)	I_{OUTA} = 0.2 A Source	10	10.5		V
Output High Voltage OUTB (1)	I_{OUTB} = 0.1 A Source	10	10.5		V
Output Low Voltage - OUTA (1)	I_{OUTA} = 0.2 A Sink		1	1.2	V
Output Low Voltage - XFRA (1)	I_{XFRA} = 0.2 A Sink		1	1.2	V
Output Low Voltage - OUTB (1)	I_{OUTB} = 0.1 A Sink		1	1.2	V
Rise and Fall Time	C_{OUTA} = 2000 pF		30		nS
	C_{OUTB} = 1000 pF		30		nS
OUTA Falling to OUTB Rising	$T_A = T_J$ = -40 °C to +125°C	85	110	135	nS

Notes:
(1) Assured by design. Not tested in production.

Pin Configurations



Ordering Information

Part Number	Package	Temp. Range (T_A)
SC4901ITSTRT(2)	TSSOP-16(1)	-40°C to +125°C

Notes:

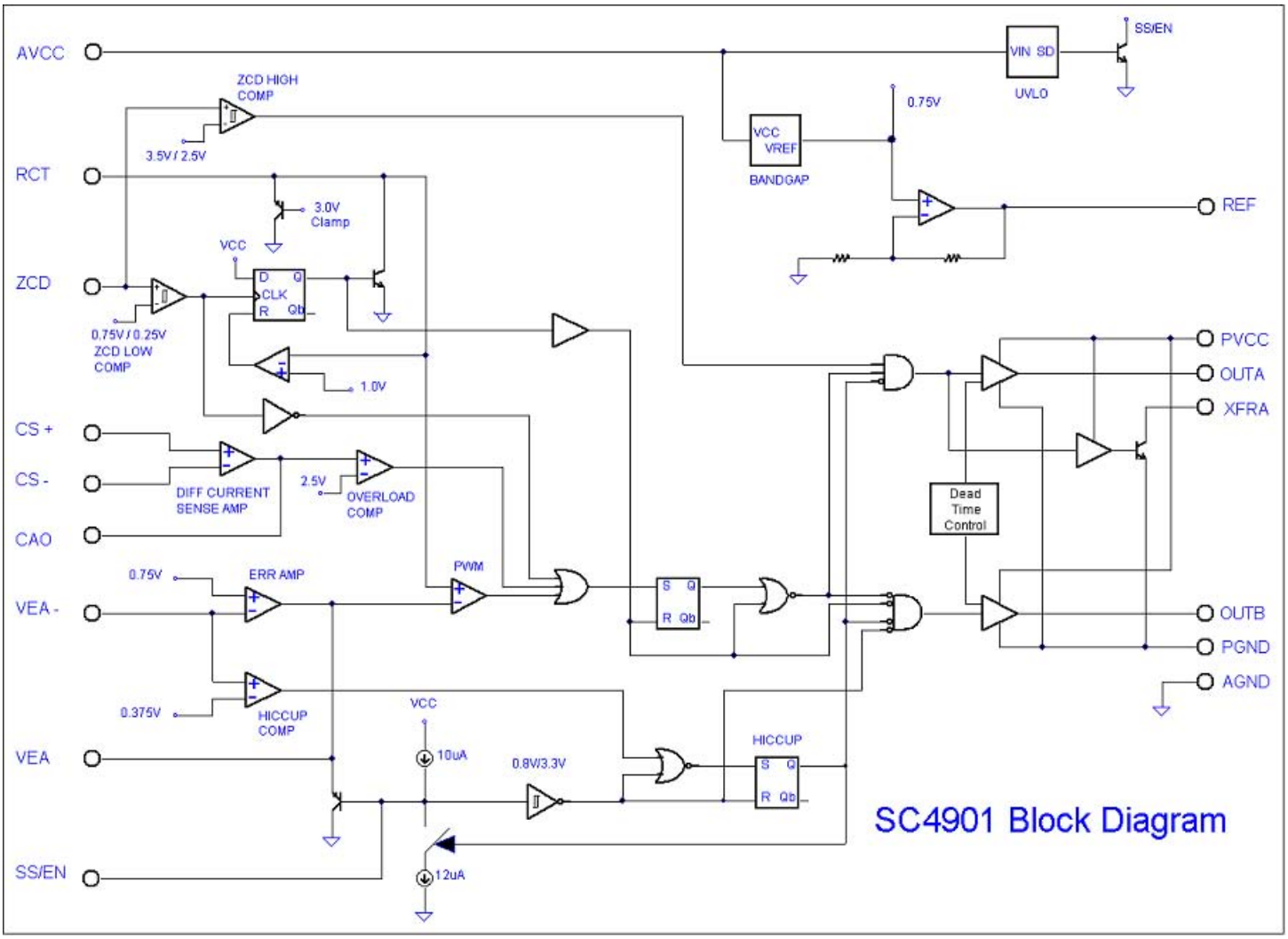
1) Only available in tape and reel packaging. A reel contains 2500 devices.

2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

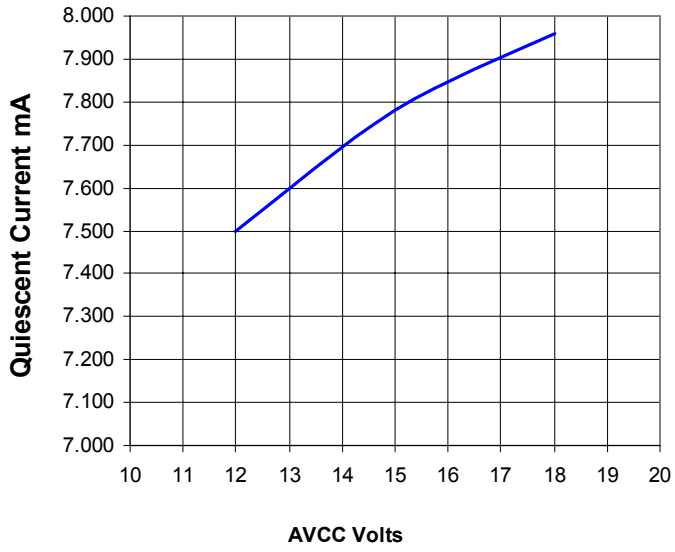
Pin #	Pin Name	Pin Function
1	CS+	Current sense non inverting input to the differential current amplifier. Maximum differential wrt to CS- is 200 mV.
2	CS-	Current sense inverting input to the differential current amplifier.
3	CAO	Output of the differential current amplifier. Current limit threshold is set to 2.5V at this pin.
4	SSEN	Soft Start and Enable pin. Taking this pin below 0.65V will shut down both the gate drives
5	AVCC	Analog supply voltage. Max rating is up to 18V.
6	OUTB	Gate drive for the low side rectifying MOSFET.
7	XFRA	Transformer connection for the gate driver of the bidirectional forward MOSFET pair. High current sinking open collector terminal synchronised to OUTA. Connect the lower end of the gate drive transformer to this pin.
8	PGND	Ground return for gate drive currents.
9	PVCC	Power supply for the gate drive circuits. Bypass with a minimum of 10 uF electrolytic and a 1 uF Ceramic capacitor to PGND.
10	OUTA	Gate drive for the high side bidirectional forward MOSFET pair.
11	REF	Reference out voltage of 2.5V for external use. Up to 5 mA can be drawn from the pin.
12	VEA-	Output voltage sense feedback to error amplifier inverting input. Reference level is 0.75V
13	VEA	Error amplifier output for feedback compensation.
14	RCT	Connection pin for the timing resistor and capacitor.
15	ZCD	Zero Crossover Detect. Detects the transitions of the transformer secondary and synchronises the ramp set up by RCT components. Internally clamped to AGND on the low side
16	AGND	Analog Ground for all the signal return paths.

Block Diagram

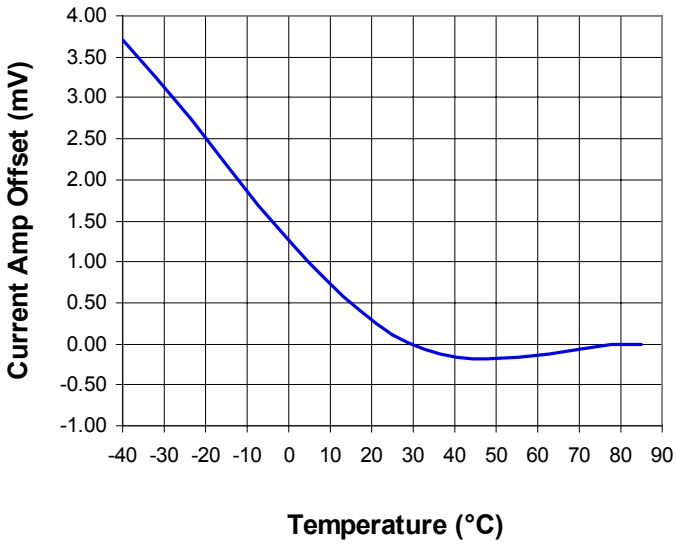


Charecteristic Curves

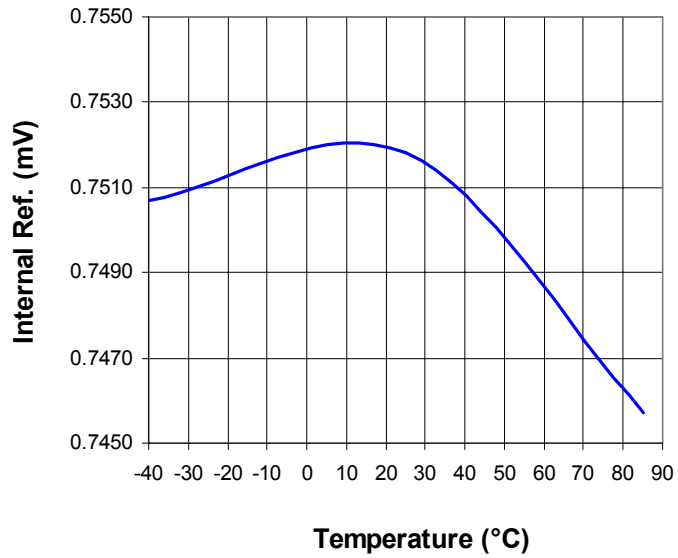
Quiescent Current vs AVCC



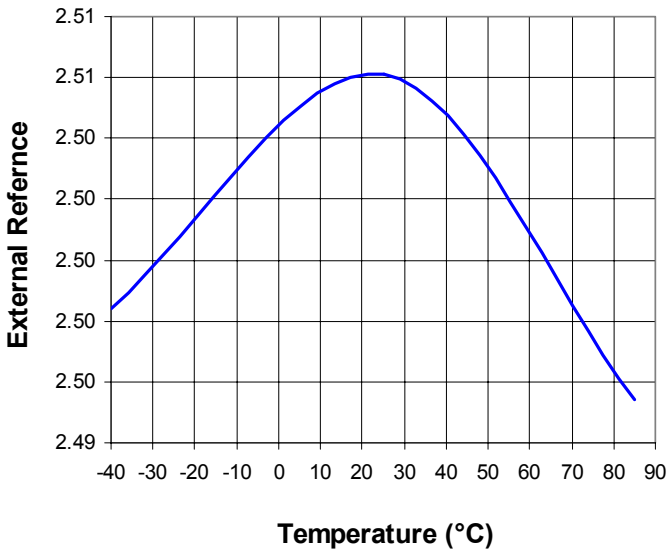
Current Amplifier Offset vs Temperature



Internal Reference vs Temperature



External Reference vs Temperature



Application Information

Introduction

The SC4901 is a voltage mode PWM controller for implementing secondary side synchronous rectification and simultaneous post regulation in forward convertors. Multiple outputs can be derived off the same transformer winding. Each output is independently regulated by modulating the on time of the forward MOSFET pair which acts as a bidirectional switch. An introduction to this unique Combi Sync topology is presented later in this section. The device takes the transformer secondary voltage as the clock input and generates an internal ramp. The switching frequency and maximum duty cycle are always determined by the transformer waveform.

The output current is sensed as a low level differential input signal. An amplified current signal is put out by the device for further use in current share and hot swap applications. Overload protection is achieved by peak current limiting followed by hiccup mode under short circuit. A buffered 2.5V reference is also put out for system monitoring and other purposes.

The controller implements the classical trailing edge modulation and the outputs are complementary PWM signals that drive the forward and rectifying MOSFETs. The high side outputs can source up to ± 2A peak current and can be easily configured for driving a pulse transformer with duty ratios greater than 50%.

Undervoltage, Soft Start and Enable

The SC4901 has an operating range of 4.5V to 18V with undervoltage lockout. Two conditions must be met before the controller is operational. The input supply should be above the undervoltage threshold of 4.5V and the SSEN pin should be above 0.65V typical. If not, the device is deactivated - the outputs are held active low, the SSEN and the VEA pins are also held low. The controller is in standby mode and draws only the quiescent current of 7 mA typical. Once the undervoltage threshold has been exceeded and the SSEN pin is released, the soft start capacitor at pin 5 is charged by a constant current of 10 µA. The VEA follows the SSEN voltage and the output gradually ramps up. Once the SSEN pin charges to 3.3V, the soft start cycle is complete and the device is fully operational.

ZCD and RCT

Since the SC4901 is specifically designed for secondary side control, the oscillator is always derived from the transformer winding. Special care must be taken to ensure that the transformer voltage, with all its variations in rise time, shape, magnitude and duty ratio is translated into a steady ramp on a cycle by cycle basis. SC4901 provides two pins, ZCD and RCT, for this purpose.

The transformer voltage is sensed at the Zero Crossover Detect or the ZCD pin. A limiting resistor, RZ in the Typical Application Circuit, from the winding to ZCD pin is required to limit the peak input current into the pin to 5 mA under all conditions. The ZCD pin has two comparators with hysteretic thresholds. One comparator has lower thresholds of 0.75/0.25V and the other has 3.5V/2.5V. Together they ensure proper turn on and turn off timings for the forward and the rectifying FETs. There is also an internal clamp which prevents the pin voltage from going below zero. Ensure that the ZCD pin is *not* forced into any negative voltage by external circuits. During the rise, ZCD pin voltage is also internally clamped to one diode drop above the 3.5V threshold.

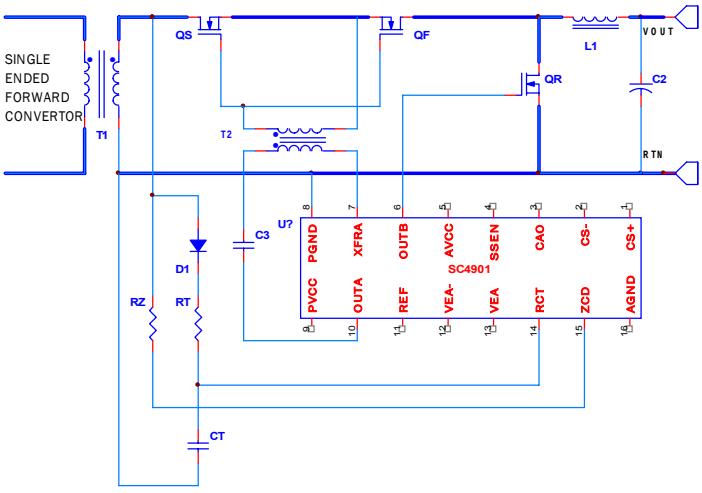


Fig 1. Generating the Zero Crossover Detect (ZCD) and the Timing Ramp (RCT) signals

The waveform at the ZCD pin should be held tightly in phase with the transformer secondary voltage. In some cases it may be useful to have a small capacitor in parallel with RZ to speed up the rise of ZCD input.

Application Information (Cont.)

The RCT pin has a timing capacitor CT connected to AGND and a charging resistor RT connected to the source, which is typically derived from the transformer voltage. The RCT pin is clamped to 3V peak internally and the ramp operates between 0V and 3V. The high side forward pulse is terminated whenever the RCT ramp hits the 3V peak.

Ensure that the ramp reaches this peak only after the negative transition of the transformer voltage, even under the worst case conditions of high line and maximum applicable duty ratio. Otherwise the available pulse width for post regulation will be limited. On the other hand, the timing capacitor should get charged fully to 3V prior to positive transition of the transformer voltage. This will ensure that the dead time between the rectifying and forward gate drives is consistently maintained. Ideally the ramp should be charged to its peak of 3V just after the falling edge of the transformer secondary voltage so that the voltage error amplifier output utilises the full range of 0 to 3V. This is shown in the idealised waveforms below.

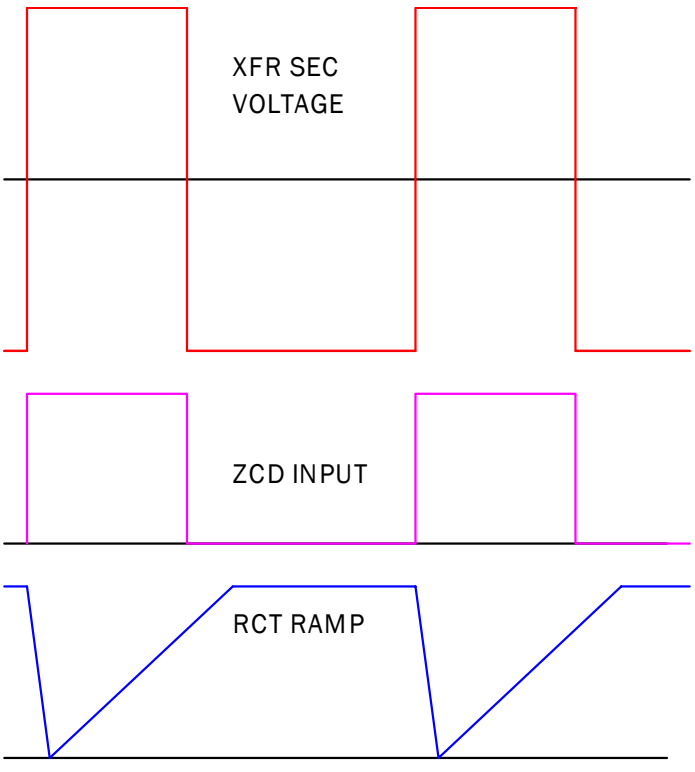


Fig 2. Idealised ZCD and RCT waveforms

The timings for the idealised waveforms above are easier to implement if the transformer has some form of constant volt-second operation or control; the secondary voltage can be directly used to charge the timing capacitor CT. The maximum input current into the RCT pin under clamped conditions should be limited to 2 mA.

Turn On Sequence

Prior to transformer voltage going positive, the ramp capacitor is at its maximum of 3.0V. On the rising edge of transformer secondary, 0.75V at the ZCD pin is detected first and OUTB gate drive goes low which turns off the low side rectifying FET QR (Fig. 1). Simultaneously a current sink of 10 mA is activated to discharge the timing capacitor CT to the lower threshold of 1V. This discharge time provides the delay between turn off of rectifying FET and turn on of the forward MOSFETs and is given by

$$DLon = CT \times 0.2$$

where CT is the ramp capacitor value in pF and DLon is the dead time in nS. The actual dead time is extended by the propagation delays internal to the controller, which should be taken into account while choosing CT. The propagation delays are typically in the range of a few tens of nanoseconds.

When the RCT pin goes down to 1V, OUTA is enabled to drive the high side pair of FETs. Meanwhile, on the rising edge of ZCD pin, a higher threshold of 3.5V is detected. Once both these conditions have been met, OUTA goes high, XFRA and the forward FETs QS and QF are turned on.

Setting the RCT Ramp

The CT capacitor is typically charged from the transformer secondary voltage through RT. The current through RT is given by $(V_{SEC} - V_{FWD} - V_{CT}) / RT$ where

V_{SEC} = Peak of the transformer secondary voltage
V_{FWD} = Forward drop of the signal diode (D1 in Fig 1)
V_{CT} = Instantaneous capacitor voltage

As a first approximation the average current can be assumed to be $(V_{SEC} - 2V) / RT$.

Application Information (Cont.)

Having chosen CT to meet dead time requirements, the resistor is chosen so that the ramp voltage is just below 3.0V peak at the end of the maximum ON time.

$$RT \cong \frac{300000 \times (Vsec - 2) \times D}{Fsw \times CT}$$

where

RT = Timing resistor in kΩ
Fsw = Switching frequency in kHz
D = Operating duty cycle at which Vsec is applied
CT = Timing capacitor in pF

If the primary side is PWM modulated in a feedback loop or has a volt second clamp, the product Vsec x D is fairly constant. If it is free running with a fixed duty cycle, use the maximum value of Vsec. The formula assumes that Vsec is much larger than the ramp voltage of 3.0V. For lower secondary voltages, use a smaller value of RT.

REF Output and Error Amplifier

The reference level for output voltage feedback is 0.75V bandgap. This is amplified, buffered and put out as a 2.5V REF output. The REF voltage can be used for external monitoring circuits or for regulating output voltages less than 0.75V. The output of the error amplifier can swing between 0.3V to 2.9V, just below the clamped peak of the timing ramp. The REF pin should be bypassed to AGND with a 0.1 uF ceramic capacitor. A maximum of 5 mA can be drawn from the REF output.

Delays and Turn Off Sequence

The delay between turn off of the rectifying MOSFET QR to the turn on of the forward MOSFETs QS and QF is determined by the discharge of the ramp capacitor CT through a 10 mA current. The other delay, between turn off of the forward MOSFETs and turn on of the rectifying MOSFET is fixed and typically 110 nS. This delay is valid when the output is in regulation and the forward FETs are turned off by the PWM comparator. During transients or if the output loses regulation, QS and QF will be turned off on the falling edge of the transformer voltage. First, the high comparator detects the 2.5V threshold and pulls down OUTA. This turns off the forward FETs. Further down, the lower comparator detects the 0.25V threshold and turns on OUTB. This ensures that the forward FET pair is off before transformer voltage goes negative.

Current Sense and Current Limit

Current sensing is done as the input of an uncommitted differential amplifier. The current limit threshold is 2.5V at the CAO pin. This allows the user considerable flexibility to design the current sensing circuit. A very low value sense resistor which results in a current signal of a few tens of millivolts or inductor drop sensing can be used for simple protection and maximum efficiency. The current amplifier gain has to be correspondingly higher. A larger current sense signal with lower gain may be preferred for better noise immunity and more precise current limit. Maximum recommended differential input is 200 mV and minimum differential gain for the current amplifier is 10, to ensure proper operation. The CAO output is typically 2V at full load. This signal can be brought out and used further for current sharing applications. The current sense pins have a maximum common mode range of AVCC - 2V.

When 2.5V limit is reached at CAO pin, the bidirectional forward switch QS/QF is turned off for the rest of the cycle. The rectifying FET is kept ON throughout to discharge the high inductor current. As the overload level is increased, the ON time continues to reduce and the output drops gradually. The output is continuously monitored for undervoltage and when it falls below 50% of the nominal voltage, an abnormal condition is detected and both the outputs are shut down. The soft start capacitor is discharged by a 2 uA current sink down to 0.8V at which point a soft start cycle is initiated to restart the convertor. This effectively provides hiccup mode of protection under short circuit.

Output Drivers

There are two complementary outputs designated A and B. Output A and XFRA are the PWM drives that control the bidirectional forward MOSFETs. The complementary output for driving the ground referenced rectifying MOSFET QR is designated as OUTB. This drive is capable of sourcing and sinking ±1A. OUTA is enabled when the transformer voltage turns on and ZCD voltage exceeds 3.5V. It is turned off on any one of the three conditions.

a) the ramp voltage on RCT exceeds the error amplifier output at VEA or
b) ZCD detects that the transformer voltage is turning off and gone below 2.5V or
c) overcurrent is detected at 2.5V on the CAO pin.

Application Information (Cont.)

In all these cases OUTA and XFRA are turned off and, after a fixed delay of 110 nS, the rectifier MOSFET is turned on. Both OUTA and XFRA can sink or source ± 2A peak current.

Since OUTA has to drive a level shifted MOSFET gate, it must be used with a pulse transformer. Note that the common source of the high side FETs presents a negative voltage to the return pin of any high side drive circuit and therefore a semiconductor driver is not recommended in this application. Another pin called XFRA is provided to simplify the gate drive design with a 1:1 transformer. The XFRA is configured as a high current open collector transistor and is turned on and off synchronously with OUTA. If the maximum duty cycle expected is less than 50%, the pulse transformer can be connected directly between OUTA and XFRA. This ensures that the gate is always driven with PVCC during both on and off periods. A 1A Schottky or ultrafast rectifier should be connected in reverse across the XFRA transistor. This is required to discharge the MOSFET gate rapidly during turn off. Refer to DTO in Fig. 3a) In addition, a smaller signal diode should be connected from XFRA to PVCC supply to reset the driver transformer. This diode may be rated to carry the magnetising current of the drive transformer. Refer DRES in Fig 3a) below.

If maximum duty ratio is more than 50% a ceramic capacitor C RES may be added in series to the transformer primary as shown in Fig 3b). The capacitor carries a small voltage only when duty ratio is more than 50% which correspondingly reduces the gate drive voltage during the ON time.

Alternately an additional zener Z RES may be used to reset the transformer during the OFF time as shown in Fig 3c). The zener voltage V_Z should be

$V_Z \geq$ PVCC x (2D -1) / (1-D) to reset the transformer

Note that in this arrangement the OFF voltage applied to the MOSFET gates increases to (PVCC + V_Z).

Inside the SC4901, the drive circuits are powered by a separate supply and ground pair, designated as PVCC and PGND. Adequate and independent noise bypassing of both AVCC and PVCC to the corresponding grounds is strongly recommended.

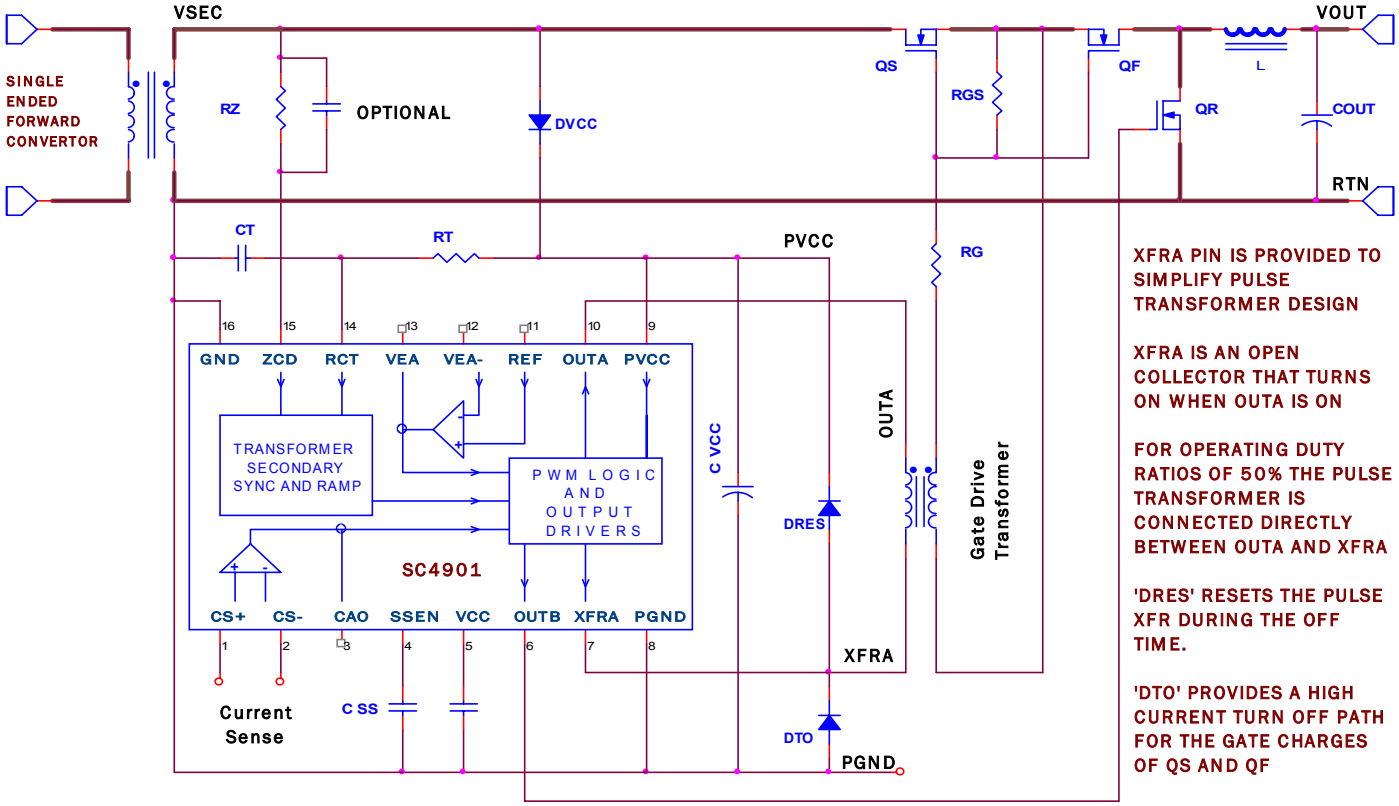


Fig 3a. Driving a Pulse Transformer using XFRA and OUTA with < 50% duty ratio

Application Information (Cont.)

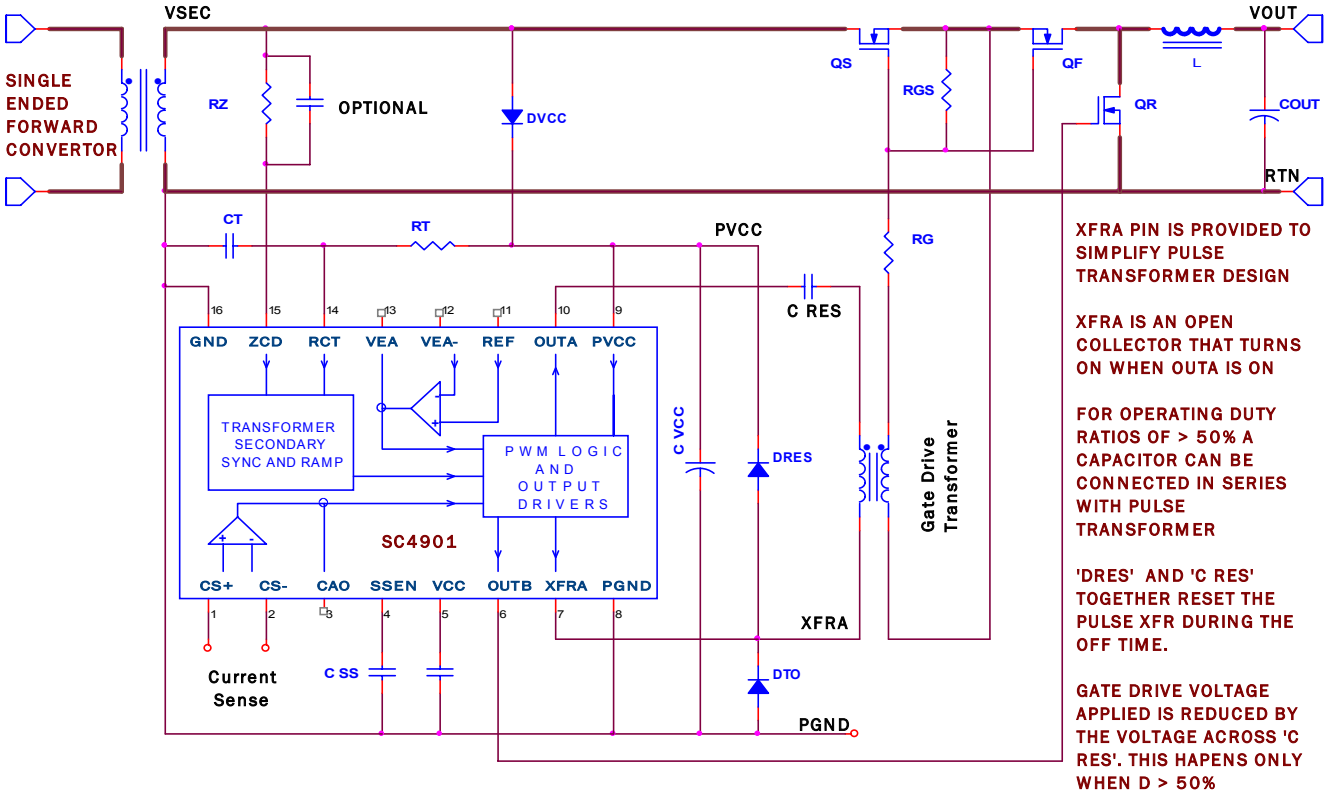


Fig 3b. Driving the Pulse Transformer with > 50% duty ratio using using a series capacitor

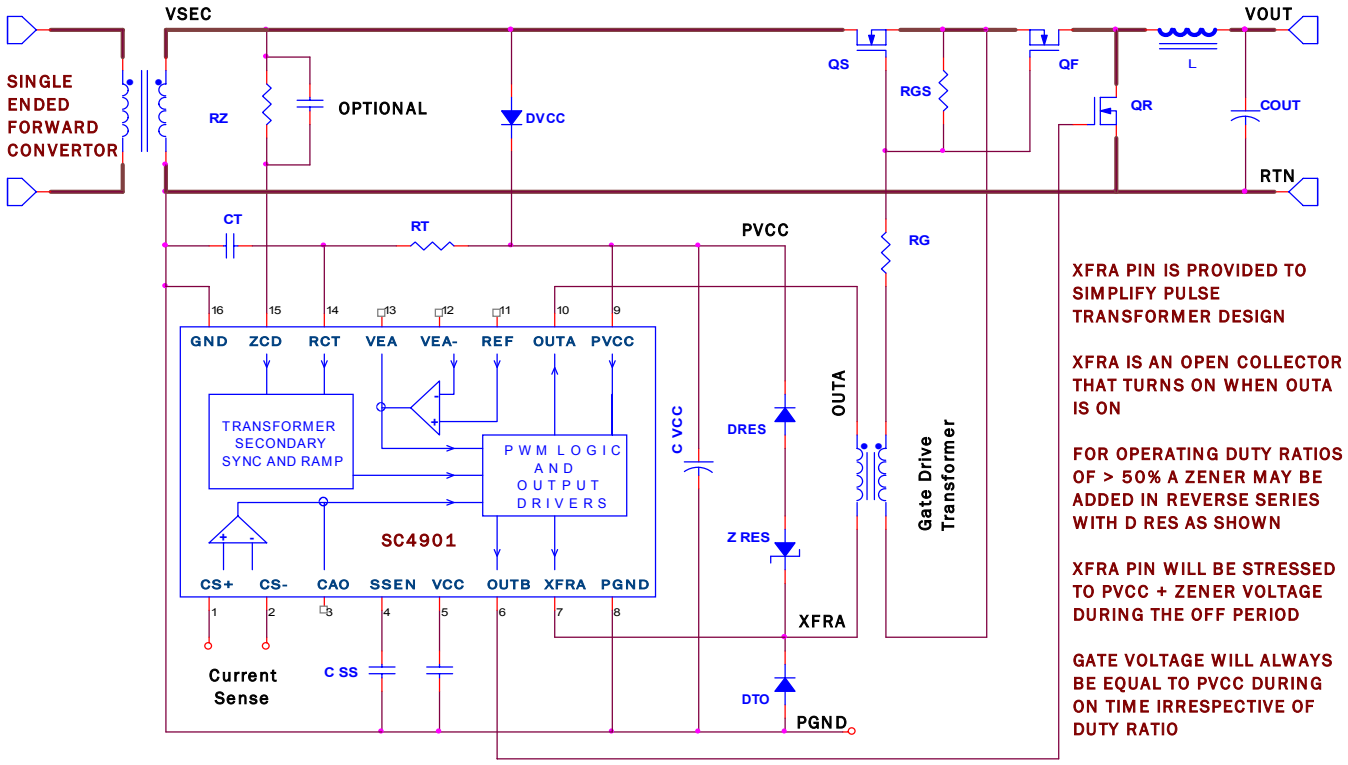


Fig 3c. Driving a Pulse Transformer with > 50% duty ratio using using a zener for reset

Application Information (Cont.)

Layout Guidelines

The Combi Sync topology and SC4901 are intended for use in multi output convertors and demand careful attention to good layout practices. The topology has an inherent advantage in that all switching circuits naturally operate at the same frequency set by the primary controller. But the operating duty ratio is different for different outputs and this may cause unexpected interferences. Make sure that the currents in the RTN path are kept separate and returned to a single node at the transformer end. High current returns from one output should be isolated from the signal current returns going into the AGND pins of other outputs. A dedicated ground plane is strongly recommended to improve noise immunity.

SC4901 requires a clean synchronising signal at the ZCD pin to ensure proper operation. There are several sources that may contribute to the noise at this pin. The traces from the transformer terminals to the corresponding QS drain and QR source pins must be kept to the absolute minimum. When the FETs are turned ON or OFF, the current in the transformer secondary winding is subjected to a rapid rate of di/dt. Long traces that encompass wide areas have higher parasitic lead inductances. The combination of a rapid di/dt and large parasitic inductance is a dip or spike in the transformer waveform which can confuse the ZCD pin and lead to random transitions at the output. The series resistor RZ shown in the Typical Application Circuit should have a separate connection to the transformer secondary terminal where the source waveform is relatively free of distortions.

The primary side layout also requires special attention. Excessive ringing or spikes on the primary side will be reflected to the secondary and interfere with the controller operation. It is important to physically separate the primary and secondary circuits and use separate ground planes to minimise interference.

The drive transformer for the forward FETs can contribute significantly to the overall performance. For fast rise and fall times and low switching losses, choose a driver with low inductances. The traces from the transformer to OUTA and XFRA pins must be kept short to minimise the overall inductance in the drive path.

Reference Design and Typical Waveforms

The complete schematic of a secondary channel delivering 3.3V/10A is shown in Fig 4). Typical waveforms are shown in Figs 5) to Fig 8) These waveforms were taken on a dual output convertor with 48V input and a transformer turns ratio of 6:1. Both outputs were generated off a single secondary winding. The primary topology was a free running, active reset, forward convertor operating at 225 kHz. Volt second control was implemented using input feedforward with a maximum duty ratio of 65% at 40V input. The two outputs were rated at 3.3V/13A and 2.5V/13A for a total of 75W power. Of special interest are the primary side waveforms shown in Fig 8). The zero current turn on can be clearly seen. During turn off, the current decreases as 2.5V forward FETs turn off first, followed by 3.3V output. The last small step at final turn off represents the magnetising current in transformer primary.

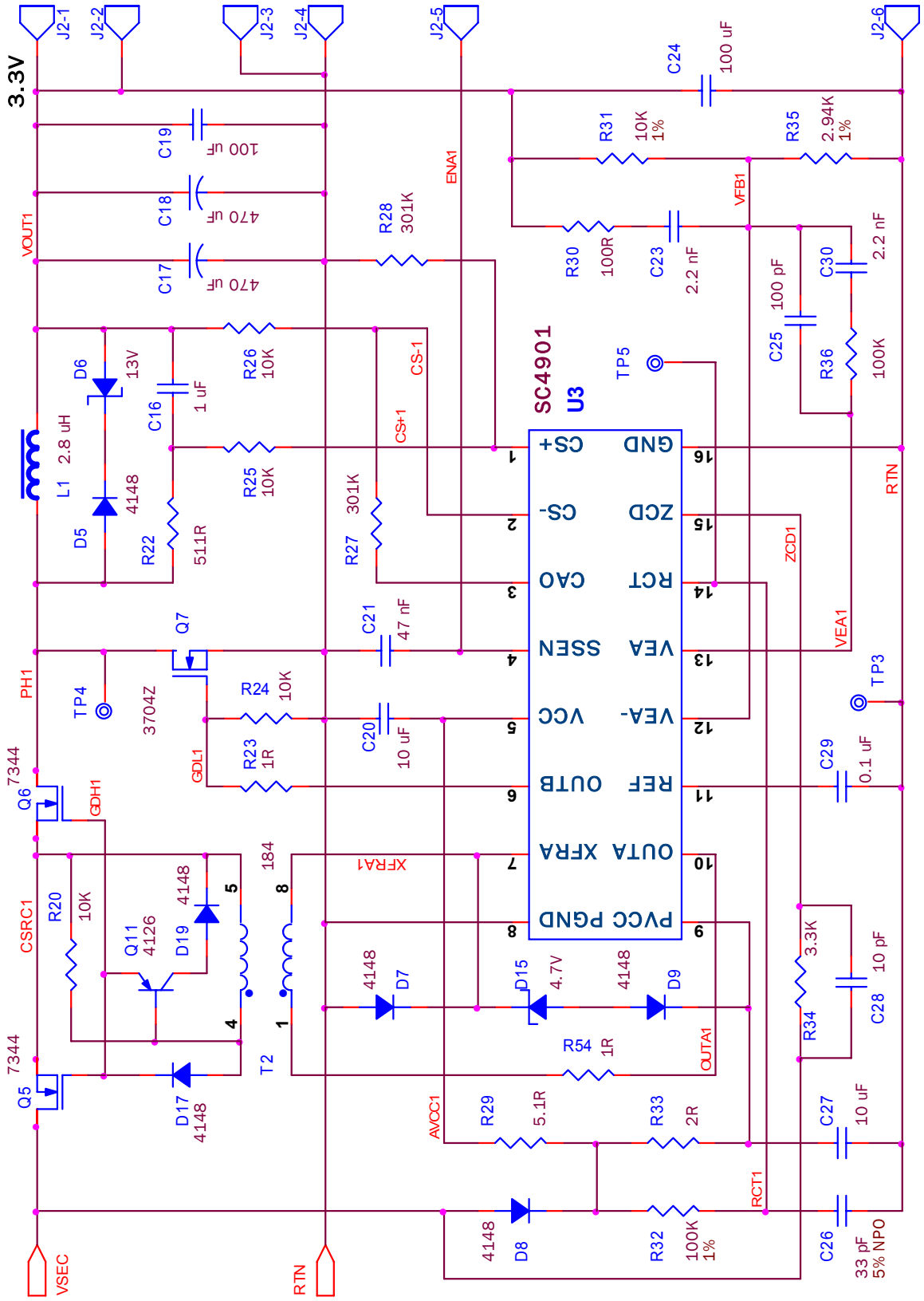


Fig 4) Complete secondary side schematic for a 3.3V/10A output.

Application Information (Cont.)

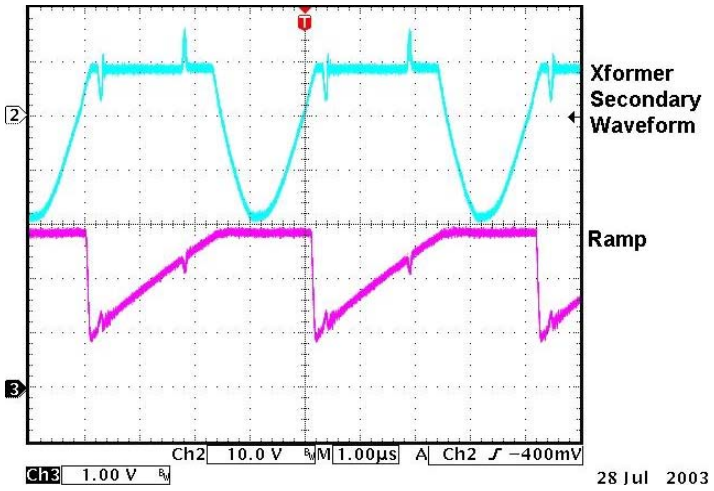


FIg 5) Transformer secondary voltage and ramp at RCT pin

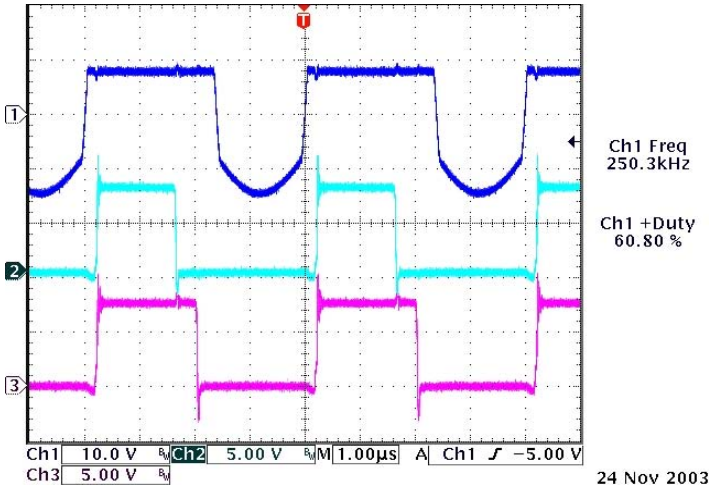


Fig 7) Transformer scondary voltage (top), rectified PWM output for 2.5V (center) and rectified PWM output for 3.3V (bottom)

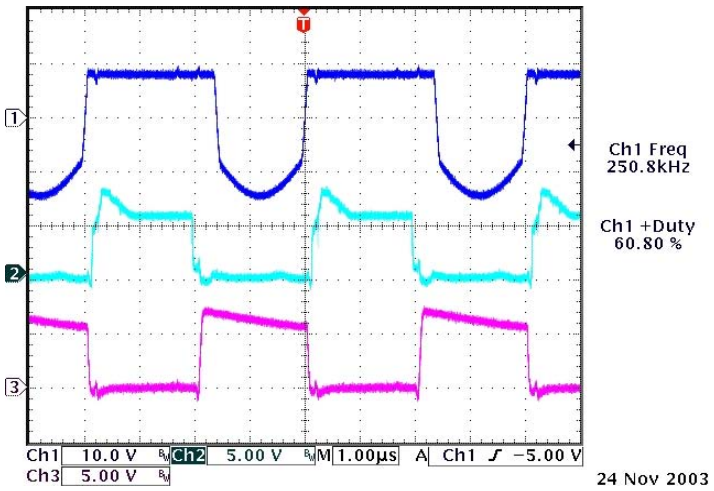


Fig 6) Transformer scondary voltage (top), OUTA gate drive for forward MOSFET pair (center) and OUTB gate drive for the rectifying FET (botom)

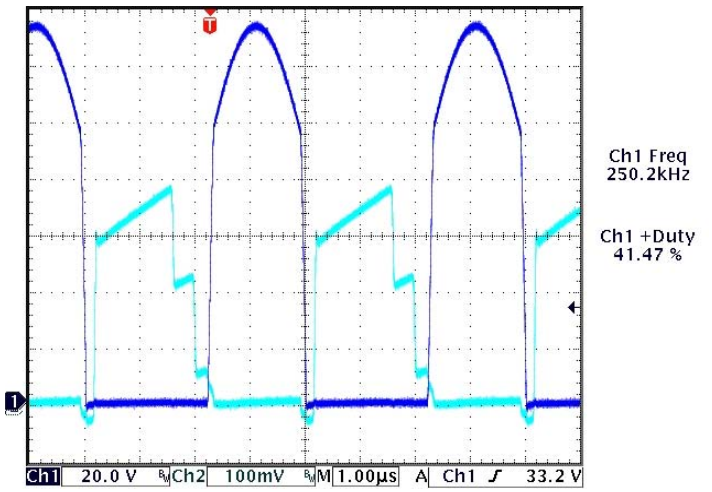


Fig 8) Primary MOSFET waveforms Drain to Source Voltage (Blue) and Current (green) .

Application Information (Cont.)

Combi-Sync Topology

Combi-Sync is a unique secondary side topology that overcomes most of the problems associated with synchronous rectification of isolated outputs. It also incorporates synchronous post regulation, making it the ideal solution for low voltage, high current outputs. Independently regulated multiple outputs can be derived from a common transformer winding. The output stage replaces the conventional rectifiers and regulators with three MOSFETs, two of which switch at zero voltage. The topology inherently eliminates turn on shoot through without complicated timing or look ahead circuits to maximise efficiency. All secondary switching circuits are naturally synchronised to primary which simplifies noise suppression. There are no separate synchronising, current sensing or gate driving signals crossing the isolation boundary. In most cases, there will be no need for a separate bias supply on the secondary side further simplifying the system design.

The primary side in a Combi-Sync circuit is a typical single ended forward convertor which may be regulated or free running. An additional benefit of the Combi-Sync topology is the zero current turn on and turn off for the primary MOSFET as well. The free running mode is preferred when there are multiple outputs without minimum load and cross regulation constraints. Input voltage feedforward is recommended to achieve volt-second clamp and minimise core losses in the free running mode.

Background on Synchronous Rectification and Post Regulation

The synchronous rectifier technology is widely used in non isolated DC-DC convertors but its use has been limited in isolated convertors because of various difficulties. An example of synchronous rectification on the secondary side of a forward convertor is shown in Fig 9. DF and DR are the parasitic body diodes of their respective FETs. The forward MOSFET QF is turned ON when the transformer secondary voltage goes positive and the rectifying MOSFET QR is turned ON when the transformer secondary is negative. Two approaches have been used to drive the MOSFETs. One is the self driven scheme where the transformer secondary itself provides the gate voltage for the appropriate FET. While the scheme is simple and has a very low cost, it has several limitations.

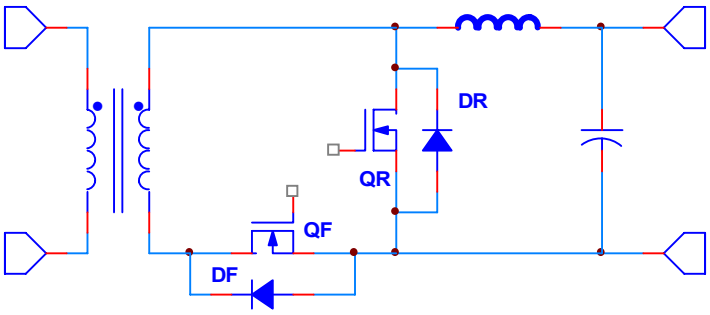


Fig 9) Isolated Synchronous Rectification

One is that QR can conduct synchronously only while the transformer is being reset. Thereafter there is no gate voltage to drive it and the circuit must employ diode. Secondly since the gate voltages, and the peak of transformer secondary, must be with 4.5V to 20V under all conditions, the scheme may fail at lower voltage and wide input ranges.

An alternative is to use a control driven approach where a synchronous controller provides the gate drive. This provides the low loss FET conduction over the entire cycle and is not limited by output or input ranges. However it is not without its own problems. At the instant transformer voltage turns positive the body diode of QF gets forward biased. At the same time, QR would also be fully conducting and the result is a shorted winding just when the primary switch is trying to turn ON. To prevent catastrophe it is necessary to turn QR OFF *prior to transformer voltage going positive*. This requires an advanced signal from the primary side crossing the isolation boundary. Attempts have been made to avoid this by complex timing or look ahead circuits on the secondary side itself and several patents have been issued for them.

It should be understood that all these techniques for isolated synchronous rectification have been restricted to a *single unregulated secondary output*. The existing circuits only rectify the output but do not synchronously regulate it any further. Nor is it possible to generate multiple outputs from the same winding. Post regulation of the isolated outputs has been implemented so far using either the saturable magnetic inductor or a power MOSFET in series with the forward diode. The saturable magnetic element is bulky and inefficient at high frequencies. The circuit with series MOSFET is widely known and well documented. Fig 10) shows a standard implementation.

Application Information (Cont.)

The series FET QS is turned ON and OFF in a controlled manner synchronously with the secondary waveform. The width of the ON time pulse is varied to regulate the output.

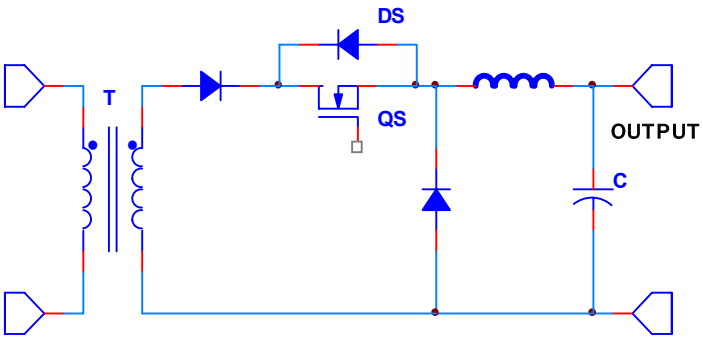


Fig 10) Synchronous Post Regulation

Again it should be understood that all previous attempts have used a *non synchronously rectified secondary*. That is, the transformer secondary was rectified using power diodes and the series MOSFET was added to synchronously regulate it further.

The Combi Sync Technique

The Combi Sync, as the name indicates is a unique secondary configuration that combines synchronous rectification and post regulation on transformer isolated multiple secondary voltages. The proposed implementation as well as typical waveforms are shown in Fig 11) on the next page. The highlights of its operation are as follows

a) Prior to the transformer voltage going positive, the rectifying MOSFET QR is conducting. When the voltage goes positive, QR is turned OFF.

b) After a delay, both QF and QS are turned ON. This delay prevents both high and low side FETs conducting at the same time and shorting the secondary winding.

c) The forward pair of QS and QF acts as a bidirectional switch and can be turned off in a controlled manner irrespective of the polarity of the transformer voltage. This is the key to the topology. With SC4901 the forward pair is turned off on any of the following conditions i) end of the active PWM duration ii) peak current crosses the overload limit or, iii) transformer secondary voltage begins to fall.

d) After the forward FETs QS and QF are turned OFF, the rectifying FET QR is turned after a short delay. QR continues to conduct until the beginning of the next cycle when transformer secondary voltage goes positive again. By modulating the ON time of the high side power MOSFETs output regulation is achieved.

This arrangement of MOSFETs and their control provides a highly efficient combination of synchronous rectification and simultaneous control of isolated secondary voltages.

Trailing Edge Modulation

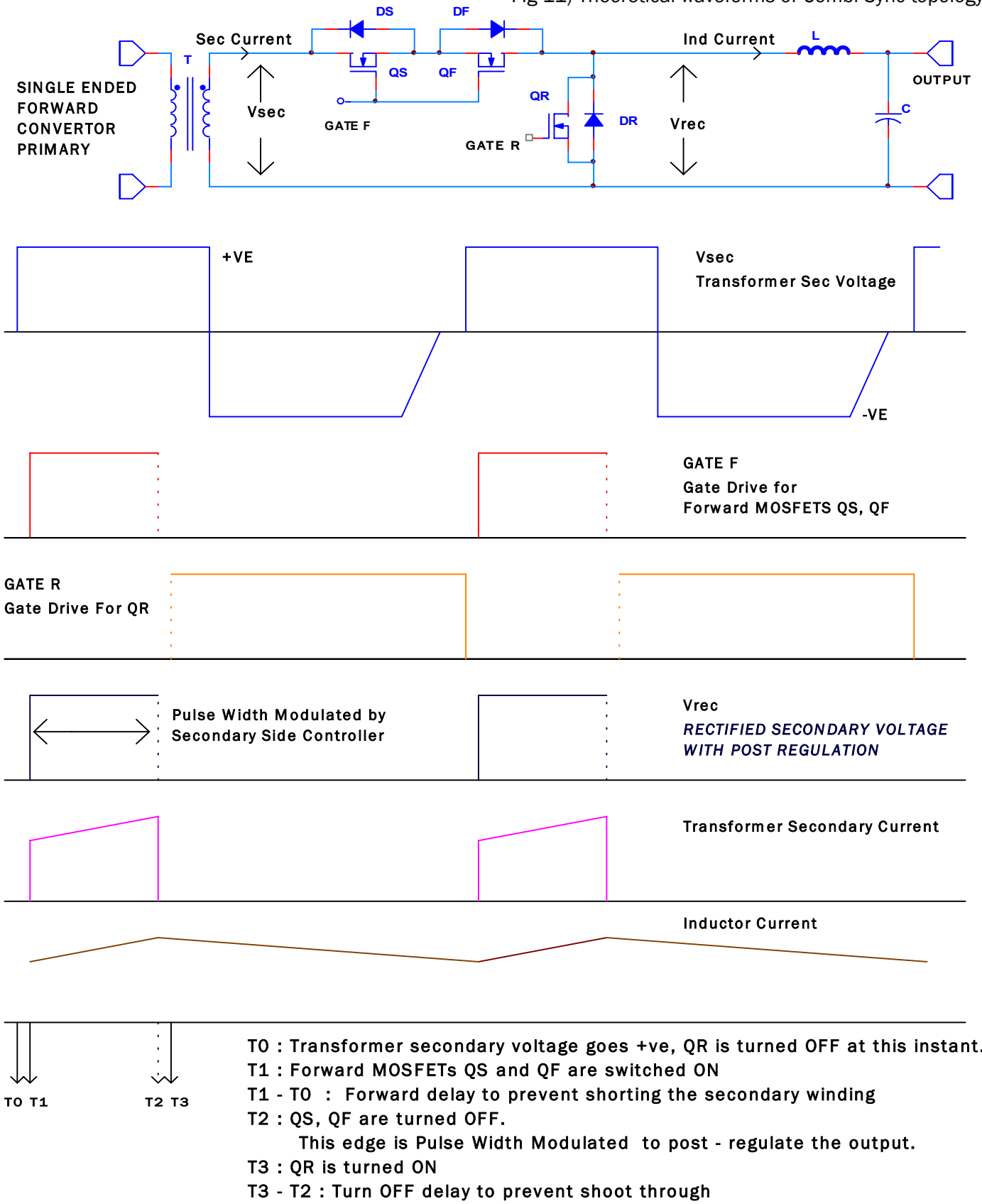
The Combi Sync topology offers the option of both leading and trailing edge modulations to achieve synchronous post regulation. With leading edge modulation, QS and QF are turned on during the forward mode, with a PWM dictated delay, but the turn off is synchronised to the falling edge of the transformer voltage. This results in zero current turn on for the primary switch but a hard turn off with full load. On the other hand, in conventional secondary side post regulation, the trailing edge modulation results in hard turn on and zero current turn off for the primary switch. However, the Combi Sync topology already has an inherent turn on delay for the forward FETs on the secondary side. This ensures zero current turn on for the primary switch, irrespective of the modulation scheme used. It is therefore advantageous to use trailing edge modulation which now results in both zero current turn on and turn off for the primary switch. If some form of ZVS is used in primary control, all of the switching losses may be eliminated on the primary side. Trailing edge modulation is the method employed in SC4901.

Switching Waveforms

Theoretical switching waveforms of the Combi Sync topology are shown on the next page. The first is the transformer secondary voltage which acts as the reference. Second and third are the gate drives for forward and rectifying FETs respectively. Rectified and pulse width modulated output that appears before the LC filter stage is shown next. Notice that this rectified output rises after a delay which is crucial to isolated synchronous rectification. In the simple isolated synchronous rectifiers, there is no QS, and QF begins to conduct (initially through its body diode) at the same instant as the transformer voltage going positive. Transformer secondary and inductor currents are also shown. The delay T1-T0 is set by the capacitor CT and the T3-T2 delay is fixed internally in SC4901

Application Information (Cont.)

Flg 11) Theoretical waveforms of Combi Sync topology



T0 : Transformer secondary voltage goes +ve, QR is turned OFF at this instant.
T1 : Forward MOSFETs QS and QF are switched ON
T1 - T0 : Forward delay to prevent shorting the secondary winding
T2 : QS, QF are turned OFF.
This edge is Pulse Width Modulated to post - regulate the output.
T3 : QR is turned ON
T3 - T2 : Turn OFF delay to prevent shoot through

Application Information (Cont.)

Features and Applications of the Combi Sync Circuit with SC4901

The Combi Sync topology is quite versatile and has a number of useful features

a) There is no connection between primary and secondary sides. No synchronising signals, drive pulses, voltage or current information needs to be exchanged across the isolation boundary. The bias supply for the controller is also generated on the secondary side, eliminating the additional burden of a low power bias supply. SC4901 is designed to operate over a range of 4.5V to 18V AVCC supply which is the typical range for MOSFET gate drives.

b) For multiple secondary windings, each winding can have its own set of synchronous MOSFETs and each set can be controlled by an individual SC4901 to generate independently regulated outputs. There is no cross regulation or minimum load requirement, each output can be turned ON or OFF independently of others. Placing the controller on the secondary side also helps to optimise the transient response.

c) It is possible to have multiple sets of synchronous FETs attached to the same transformer secondary and control them individually as shown in Fig 12. This way multiple secondary outputs with a common ground can be regulated off the same secondary winding.

d) All secondary switching is synchronised automatically with the transformer waveform. There is only one switching frequency in the convertor which simplifies EMI filter design. Zero current switching of the primary FET further reduces the switching noise generated on the primary side.

e) A number of options can be used to generate and control the transformer secondary voltage.

i) The primary may be free running, that is without being regulated by a feedback loop. It may further employ constant volt second operation to reduce magnetic stresses. In this mode the duty cycle is always at an optimum value to maximise the efficiency.

ii) The primary may be regulated in a feedback loop by one of the outputs; such regulation will typically employ voltage mode or average current mode control. Note that peak current mode control is not suitable with the trailing edge modulation.

f) It is necessary to drive the forward FETs through a transformer interface. The common source of the two devices is a floating return and will swing to the peak negative voltage appearing at the transformer secondary; see the Vsec waveform in Fig 11). This negative swing does not allow a semiconductor device to be used for driving the forward FET pair. An additional pin called XFRA is provided in SC4901 to simplify the design of driver transformer interface, particularly with duty ratios of >50%. XFRA is an open collector sink which turns on and off simultaneously with OUTA.

g) The no load condition at the output needs special consideration in this topology. Under light load, the inductor current is negative as in any synchronous rectifier. When the synchronous MOSFET QR is turned off, the current is interrupted and tends to charge the drain source capacitor of QR. The back to back connected forward FETs prevent this current being returned to the source. The resulting overshoot on QR can be clamped by connecting a zener and diode combination across the inductor as shown in Fig 4). The zener clamp conducts *only* during the dead time and also provides a small benefit of reducing the voltage across the forward FETs during turn on. The detailed application schematic in Fig 4) shows diode D1 and zener D2 connected across the output inductor L1 to reduce the no load spike.

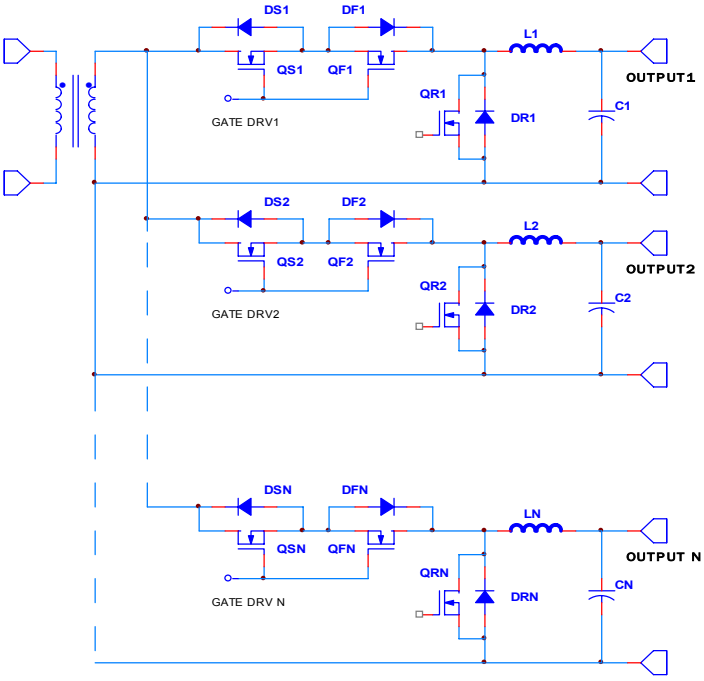
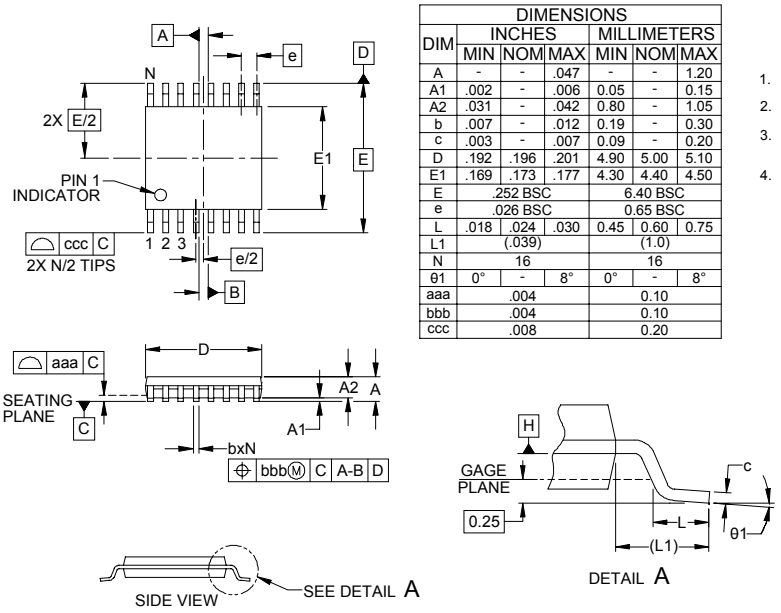


Fig 12) Generating Multiple Outputs from the same secondary winding using Combi Sync Topology

Outline Drawing - TSSOP-16

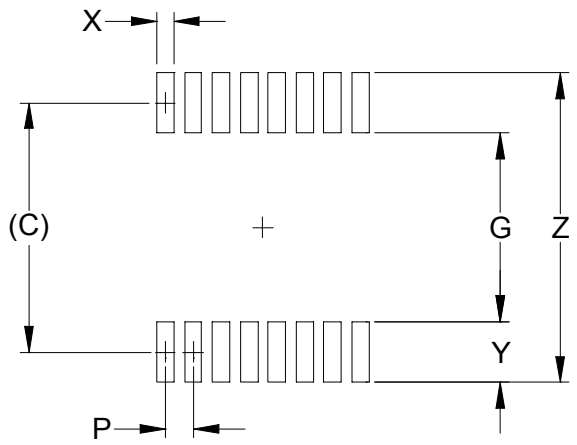


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.192	.196	.201	4.90	5.00	5.10
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	16			16		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AB.

Land Pattern - TSSOP-16



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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