

# SN54AS885, SN74AS885 8-BIT MAGNITUDE COMPARATORS

SDAS236A – DECEMBER 1982 – REVISED JANUARY 1995

- Latchable P-Input Ports With Power-Up Clear
- Choice of Logical or Arithmetic (Two's Complement) Comparison
- Data and PLE Inputs Utilize pnp Input Transistors to Reduce dc Loading Effects
- Approximately 35% Improvement in ac Performance Over Schottky TTL While Performing More Functions
- Cascadable to n Bits While Maintaining High Performance
- 10% Less Power Than STTL for an 8-Bit Comparison
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

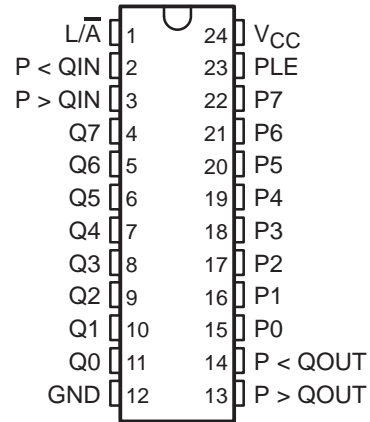
## description

These advanced Schottky devices are capable of performing high-speed arithmetic or logic comparisons on two 8-bit binary or two's complement words. Two fully decoded decisions about words P and Q are externally available at two outputs. These devices are fully expandable to any number of bits without external gates. To compare words of longer lengths, the P > QOUT and P < QOUT outputs of a stage handling less significant bits can be connected to the P > QIN and P < QIN inputs of the next stage handling more significant bits. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. Two alternative methods of cascading are shown in *application information*.

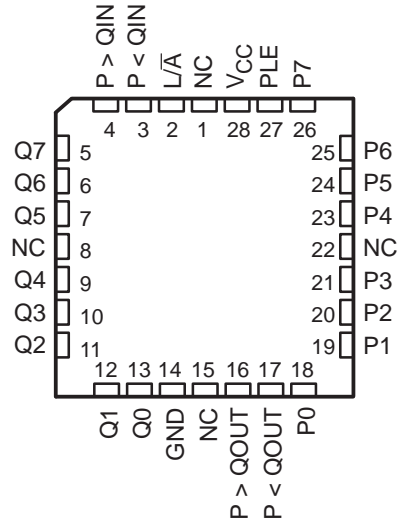
The latch is transparent when P latch-enable (PLE) input is high; the P-input port is latched when PLE is low. This provides the designer with temporary storage for the P-data word. The enable circuitry is implemented with minimal delay times to enhance performance when cascaded for longer words. The PLE, P, and Q data inputs utilize pnp input transistors to reduce the low-level current input requirement to typically -0.25 mA, which minimizes dc loading effects.

The SN54AS885 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS885 is characterized for operation from 0°C to 70°C.

SN54AS885 . . . JT PACKAGE  
SN74AS885 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54AS885 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

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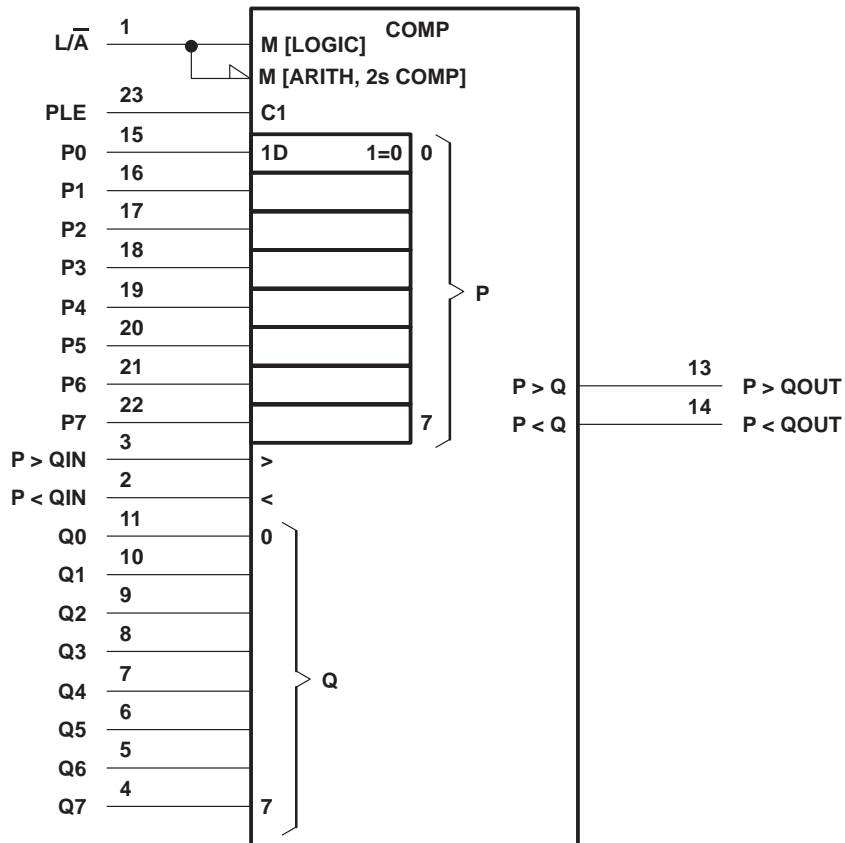
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FUNCTION TABLE

COMPARISON	INPUTS				OUTPUTS	
	$\overline{L/A}$	DATA P0–P7, Q0–Q7	P > QIN	P < QIN	P > QOUT	P < QOUT
Logical	H	P > Q	X	X	H	L
Logical	H	P < Q	X	X	L	H
Logical†	H	P = Q	H or L	H or L	H or L	H or L
Arithmetic	L	P AG Q	X	X	H	L
Arithmetic	L	Q AG P	X	X	L	H
Arithmetic†	L	P = Q	H or L	H or L	H or L	H or L

† In these cases, P > QOUT follows P > QIN and P < QOUT follows P < QIN.  
AG = arithmetically greater than

## logic symbol‡

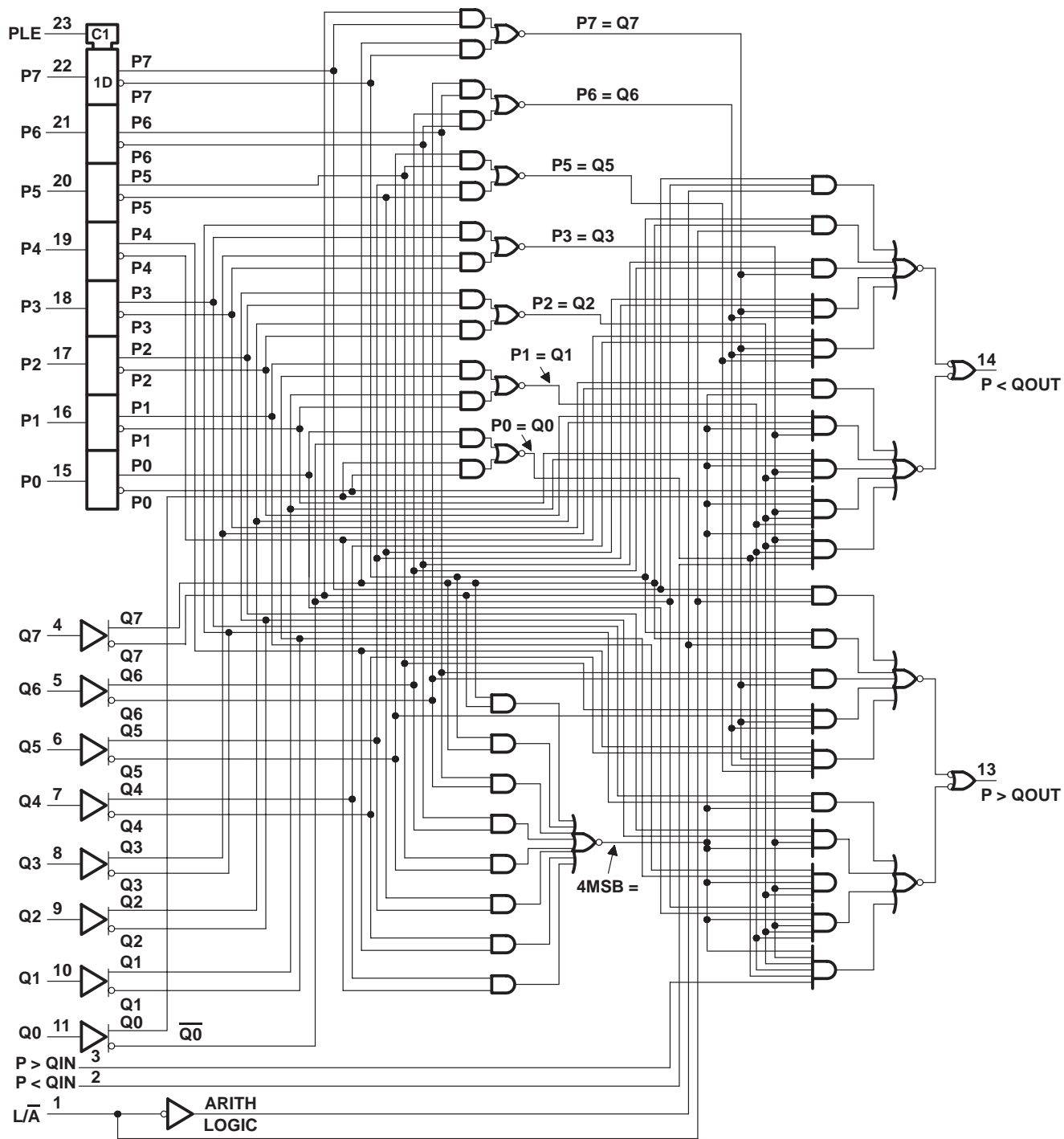


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the DW, JT, and NT packages.

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## logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54AS885	-55°C to 125°C
SN74AS885	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN54AS885			SN74AS885			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			-2			-2	mA
$I_{OL}$	Low-level output current			20			20	mA
$t_{su}^*$	Setup time, data before PLE↓	2			2			ns
$t_h^*$	Hold time, data after PLE↓	4.5			4			ns
$T_A$	Operating free-air temperature	-55		125	0		70	°C

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS885			SN74AS885			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5 V$ , $I_I = -18 mA$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 V$ to $5.5 V$ , $I_{OH} = -2 mA$	$V_{CC} - 2$			$V_{CC} - 2$			V
$V_{OL}$	$V_{CC} = 4.5 V$ , $I_{OL} = 20 mA$	0.35	0.5		0.35	0.5		V
$I_I$	$V_{CC} = 5.5 V$ , $V_I = 7 V$		0.1			0.1		mA
$I_{IH}$	$L/\bar{A}$		40			40		$\mu A$
	Others		20			20		
$I_{IL}$	$L/\bar{A}$		-4			-4		mA
	$P > QIN, P < QIN$		-2			-2		
	$P, Q, PLE$		-1			-1		
$I_{O}^{\S}$	$V_{CC} = 5.5 V$ , $V_O = 2.25 V$	-20		-112	-20		-112	mA
$I_{CC}$	$V_{CC} = 5.5 V$ , See Note 1		130	210		130	210	mA

‡ All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^\circ C$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with all inputs high except  $L/\bar{A}$ , which is low.



**switching characteristics (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX						UNIT
			SN54AS885			SN74AS885			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t <sub>PLH</sub>	L/ $\bar{A}$	P < QOUT, P > QOUT	2	8.5	14	1	8.5	13	ns
t <sub>PHL</sub>			2	7.5	14	1	7.5	13	
t <sub>PLH</sub>	P < QIN, P > QIN	P < QOUT, P > QOUT	2	5	10	1	5	8	ns
t <sub>PHL</sub>			2	5.5	10	1	5.5	8	
t <sub>PLH</sub>	Any P or Q data input	P < QOUT, P > QOUT	2	13.5	21	1	13.5	17.5	ns
t <sub>PHL</sub>			2	10	17	1	10	15	

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

**APPLICATION INFORMATION**

The 'AS885 can be cascaded to compare words longer than eight bits. Figure 1 shows the comparison of two 32-bit words; however, the design is expandable to n bits. Figure 1 shows the optimum cascading arrangement for comparing words of 32 bits or greater. Typical delay times shown are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C and use the standard advanced Schottky load of R<sub>L</sub> = 500 Ω, C<sub>L</sub> = 50 pF.

Figure 2 shows the fastest cascading arrangement for comparing 16-bit or 24-bit words. Typical delay times shown are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C and use the standard advanced Schottky load of R<sub>L</sub> = 500 Ω, C<sub>L</sub> = 50 pF.

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## APPLICATION INFORMATION

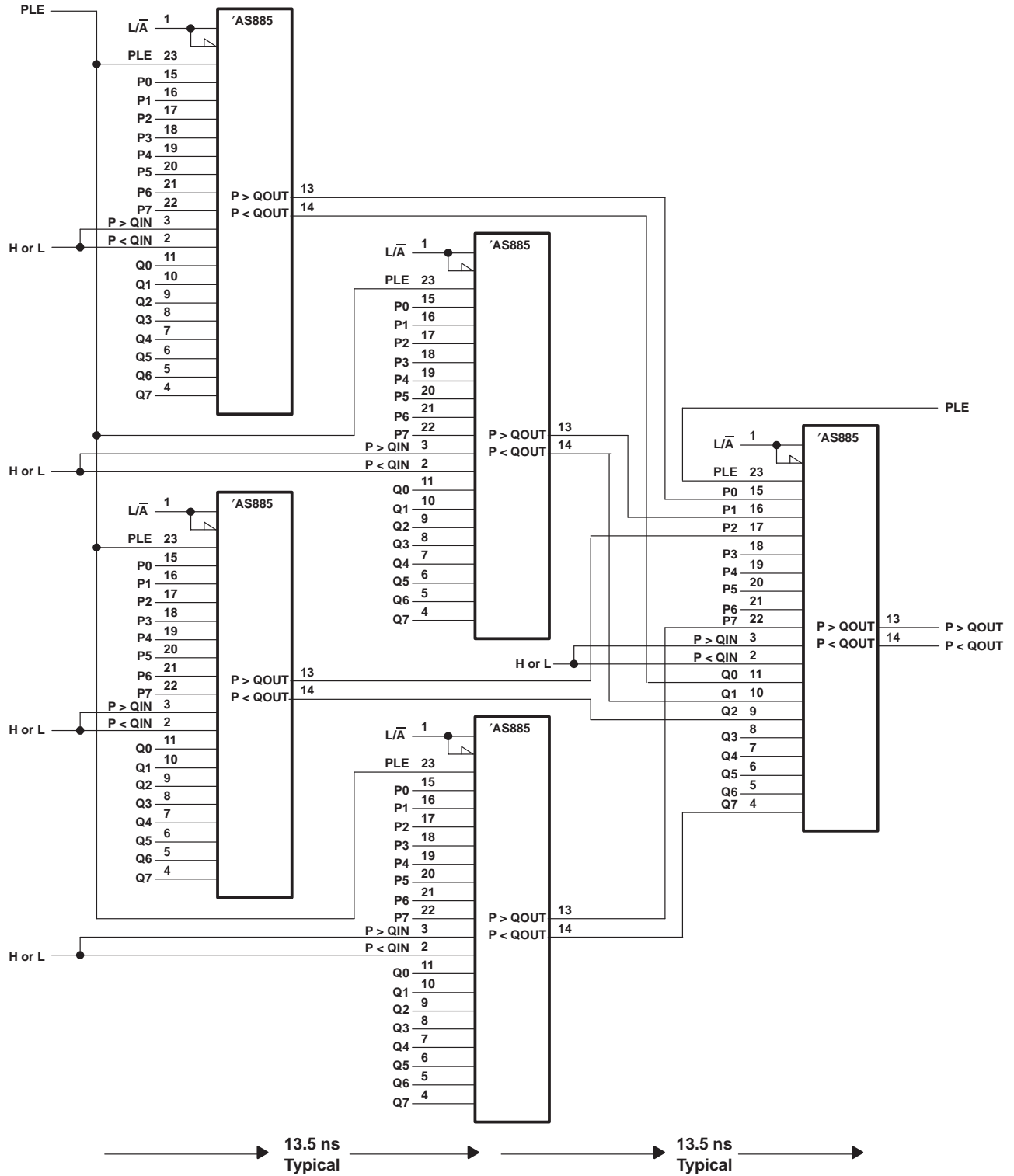


Figure 1. 32-Bit to 72 (n)-Bit Magnitude Comparator

APPLICATION INFORMATION

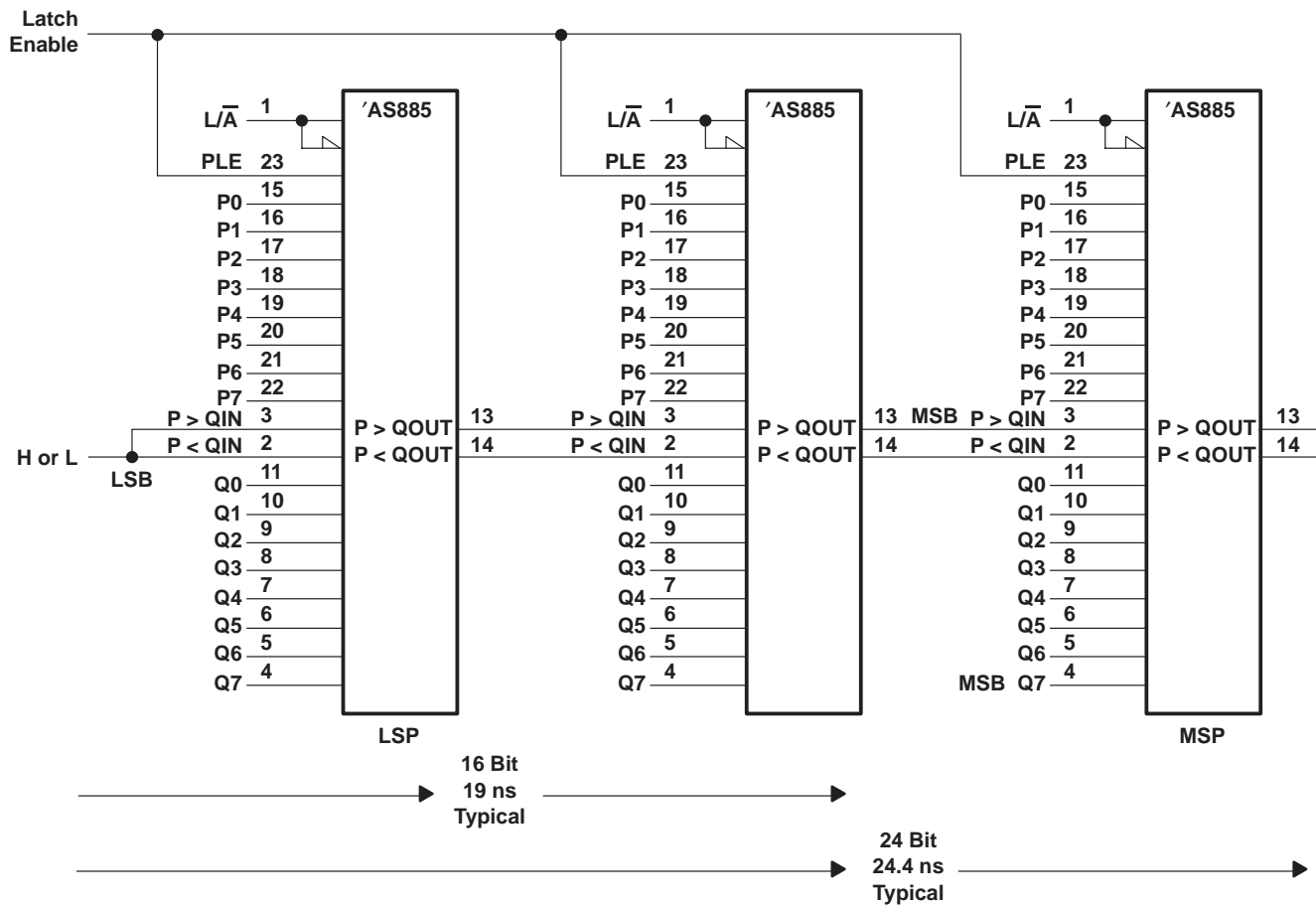
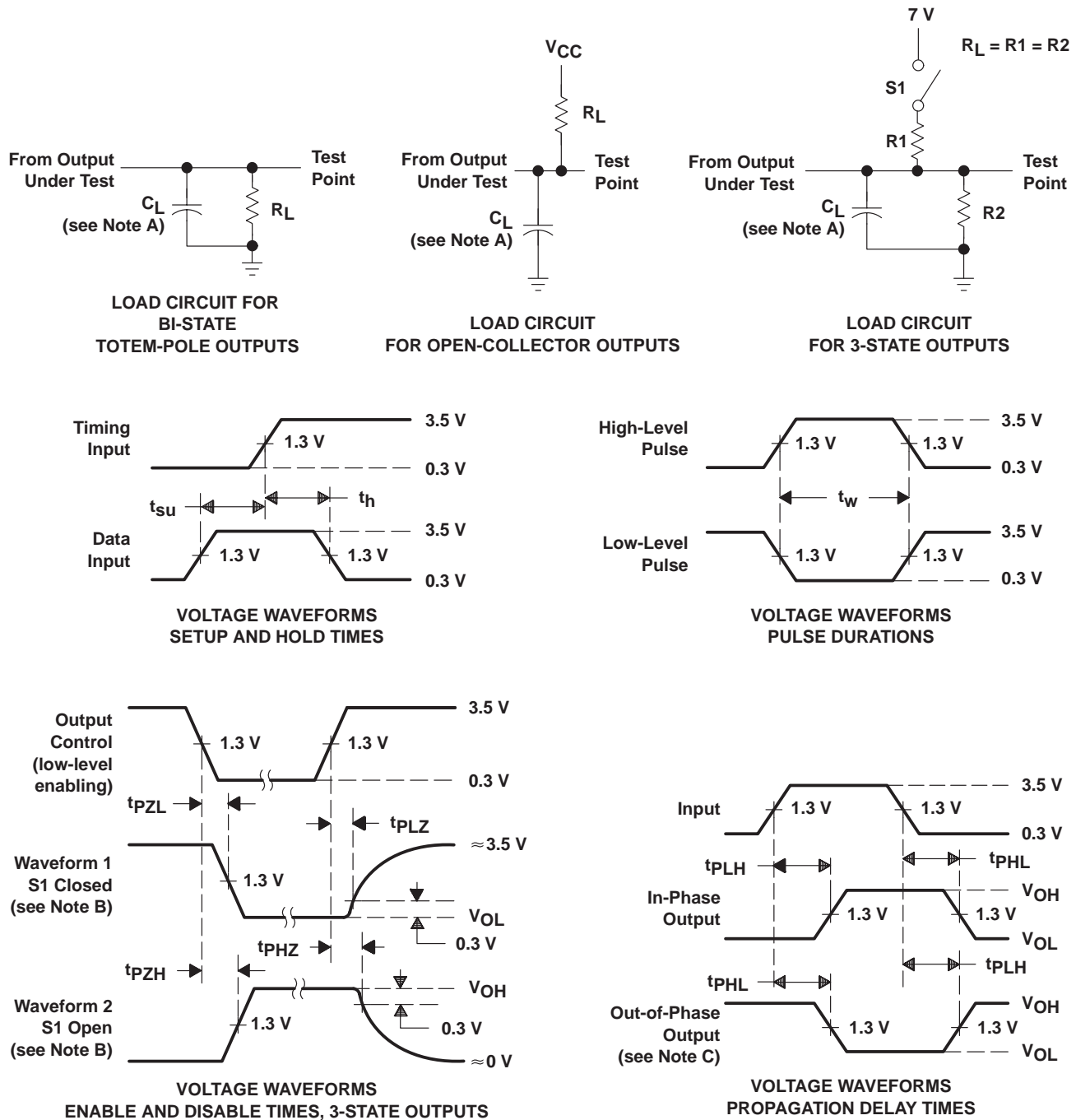


Figure 2. Fastest Cascading Arrangement for Comparing 16-Bit or 24-Bit Words

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-89757013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8975701KA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
5962-8975701LA	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SN54AS885JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SN74AS885DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS885DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS885DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS885DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS885DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS885DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS885NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS885NT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
SN74AS885NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54AS885FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54AS885JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54AS885W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

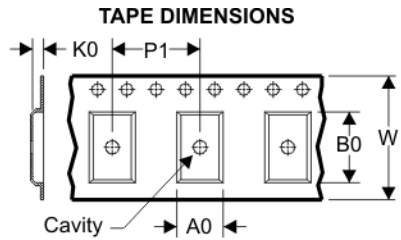
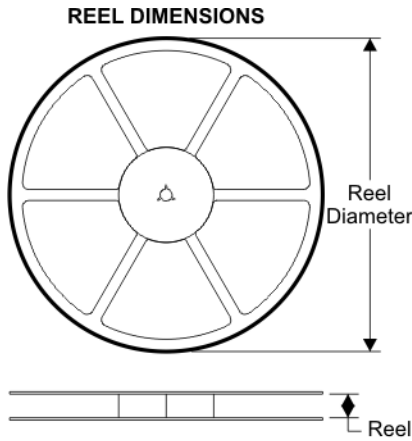
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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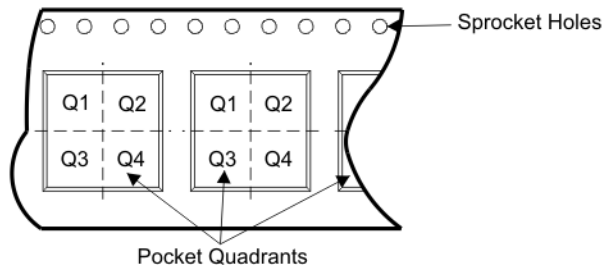
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**TAPE AND REEL BOX INFORMATION**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AS885DWR	DW	24	SITE 60	330	24	10.75	15.7	2.7	12	24	Q1

**TAPE AND REEL BOX DIMENSIONS**



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74AS885DWR	DW	24	SITE 60	346.0	346.0	0.0

JT (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN

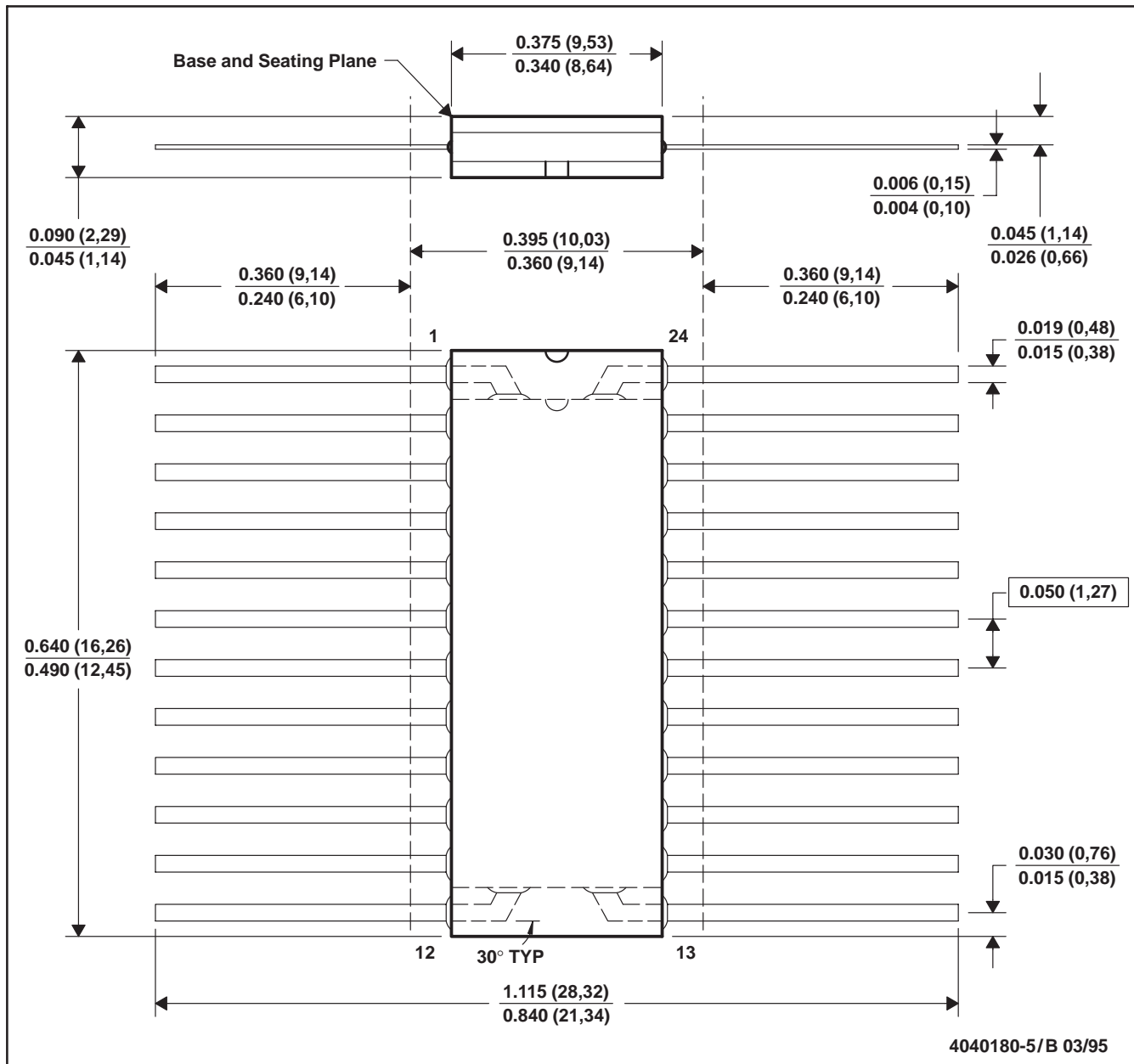


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- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK

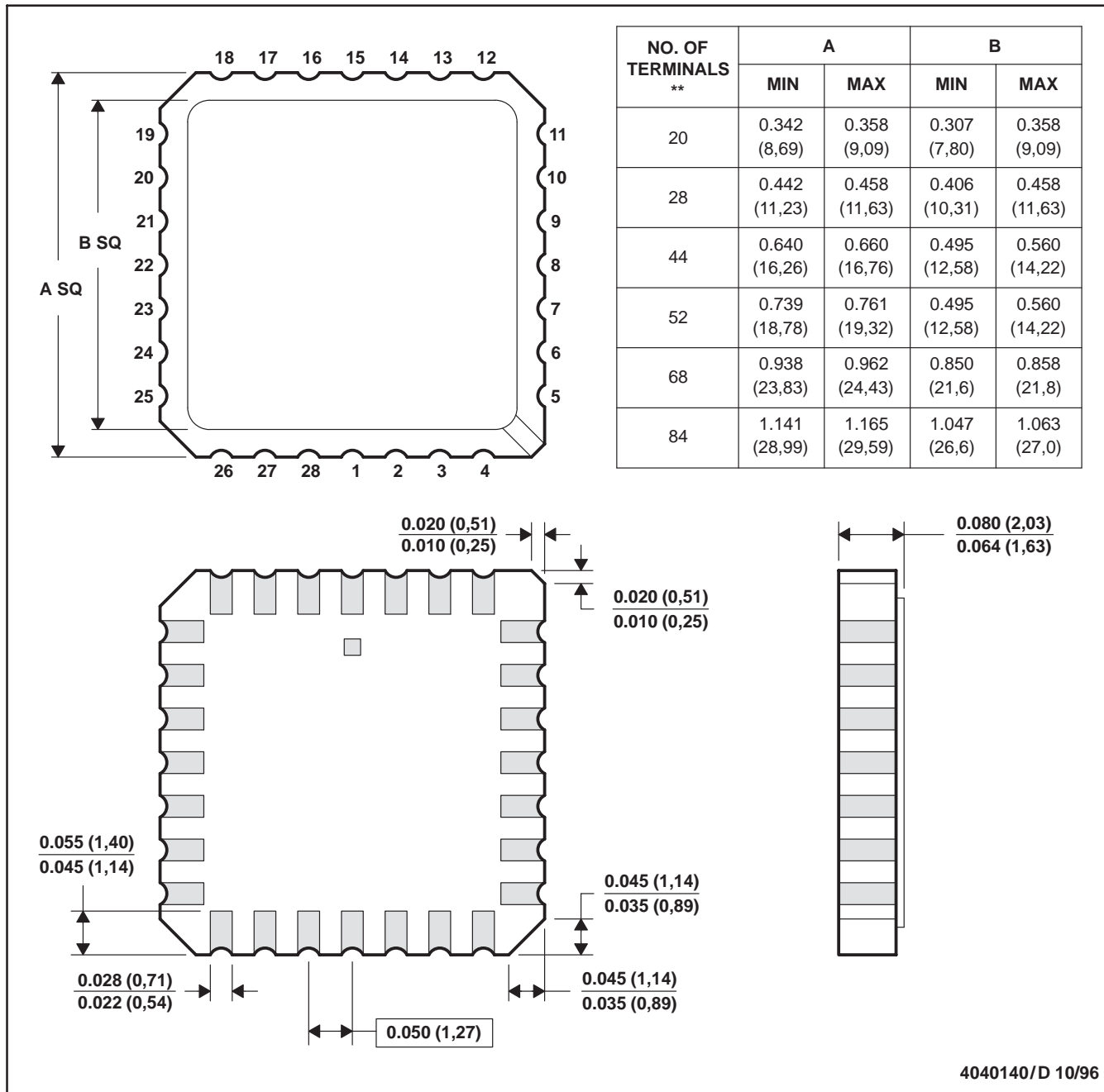


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  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
  - E. Index point is provided on cap for terminal identification only.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

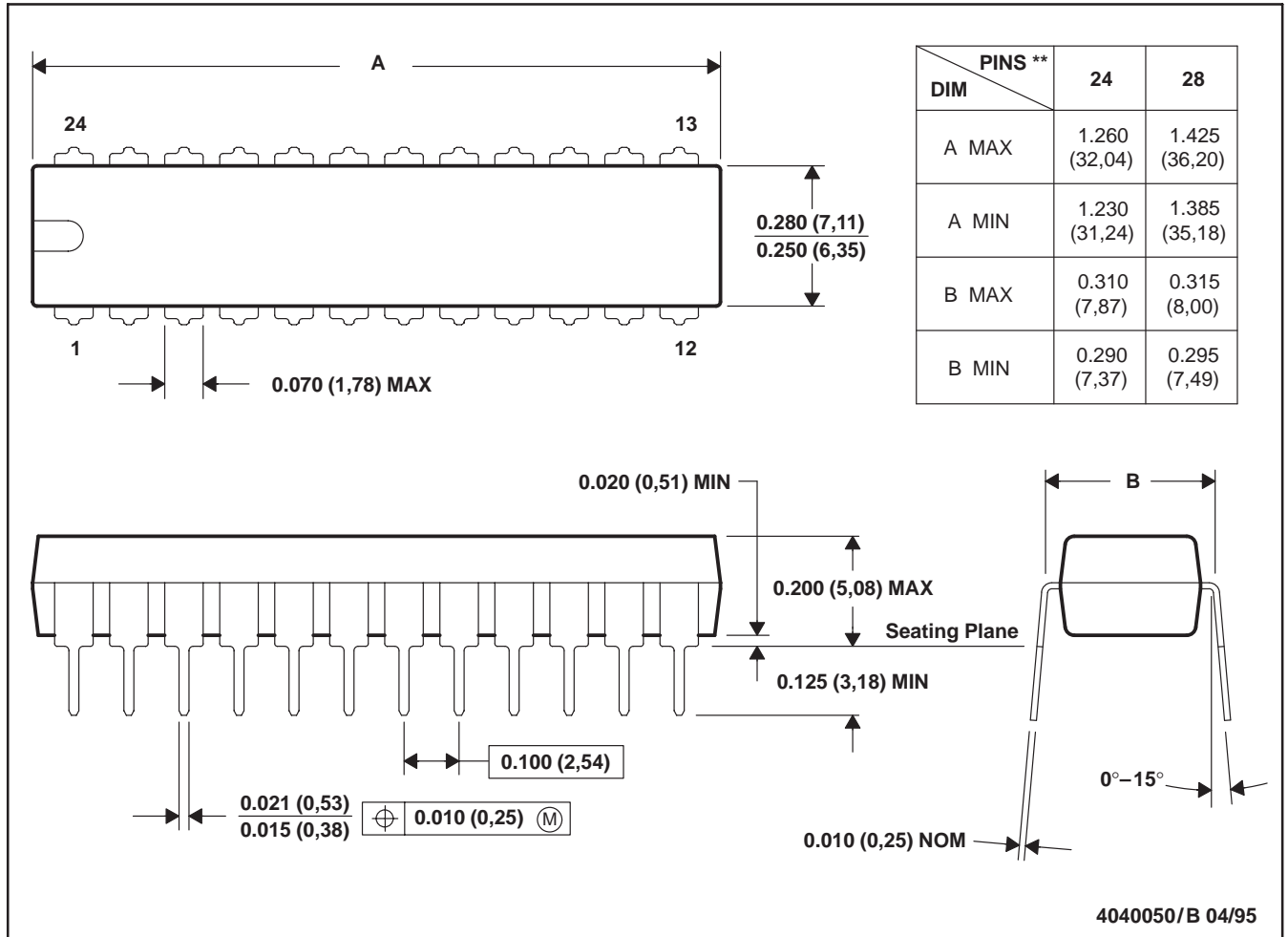


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

NT (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
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Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
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Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>	Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
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