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PHASE CONTROL THYRISTOR

AT706LT

Repetitive voltage up to **800 V**
Mean forward current **4767 A**
Surge current **70 kA**

FINAL SPECIFICATION

Feb. 17 - Issue: 1

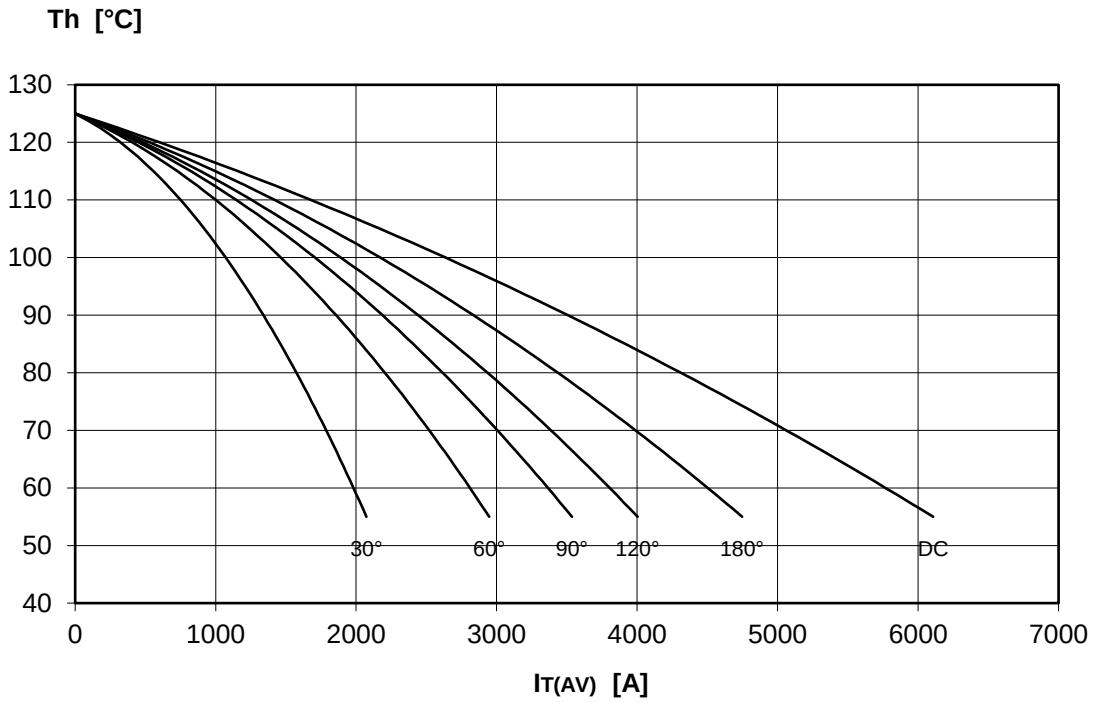
Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{RRM}	Repetitive peak reverse voltage		125	800	V
V_{RSM}	Non-repetitive peak reverse voltage		125	900	V
V_{DRM}	Repetitive peak off-state voltage		125	800	V
I_{RRM}	Repetitive peak reverse current	V=VRRM	125	200	mA
I_{DRM}	Repetitive peak off-state current	V=VDRM	125	200	mA
CONDUCTING					
$I_{T(AV)}$	Mean forward current	180° sin, 50 Hz, Th=55°C, double side cooled		4767	A
$I_{T(AV)}$	Mean forward current	180° sin, 50 Hz, Tc=85°C, double side cooled		3802	A
I_{TSM}	Surge forward current	Sine wave, 10 ms without reverse voltage	125	70	kA
I^2t	I^2t			24500 x 10^3	A^2s
V_T	On-state voltage	On-state current = 10000 A	125	1,44	V
$V_{T(TO)}$	Threshold voltage		125	0,84	V
r_T	On-state slope resistance		125	0,060	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% VDRM up to 3100 A; gate 10V, 5Ω	125	320	A/µs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of VDRM	125	500	V/µs
t_d	Gate controlled delay time, typical	VD=100V; gate source 10V, 10Ω , tr=.5 µs	25	3	µs
t_q	Circuit commutated turn-off time, typical	dv/dt = 20 V/µs linear up to 75% VDRM	125	160	µs
Q_{rr}	Reverse recovery charge	di/dt = -20 A/µs, I= 2050 A			µC
I_{rr}	Peak reverse recovery current	VR= 50 V			A
I_H	Holding current, typical	VD=5V, gate open circuit	25	300	mA
I_L	Latching current, typical	VD=5V, tp=30µs	25	700	mA
GATE					
V_{GT}	Gate trigger voltage	VD=5V	25	3,50	V
I_{GT}	Gate trigger current	VD=5V	25	250	mA
V_{GD}	Non-trigger gate voltage, min.	VD=VDRM	125	0,25	V
V_{FGM}	Peak gate voltage (forward)			30	V
I_{FGM}	Peak gate current			10	A
V_{RGM}	Peak gate voltage (reverse)			5	V
P_{GM}	Peak gate power dissipation	Pulse width 100 µs		150	W
P_G	Average gate power dissipation			2	W
MOUNTING					
$R_{th(j-h)}$	Thermal impedance, DC	Junction to heatsink, double side cooled		9,5	°C/kW
$R_{th(c-h)}$	Thermal impedance	Case to heatsink, double side cooled		2	°C/kW
T_j	Operating junction temperature			-30 / 125	°C
F	Mounting force			40,0 / 50,0	kN
	Mass			1150	g

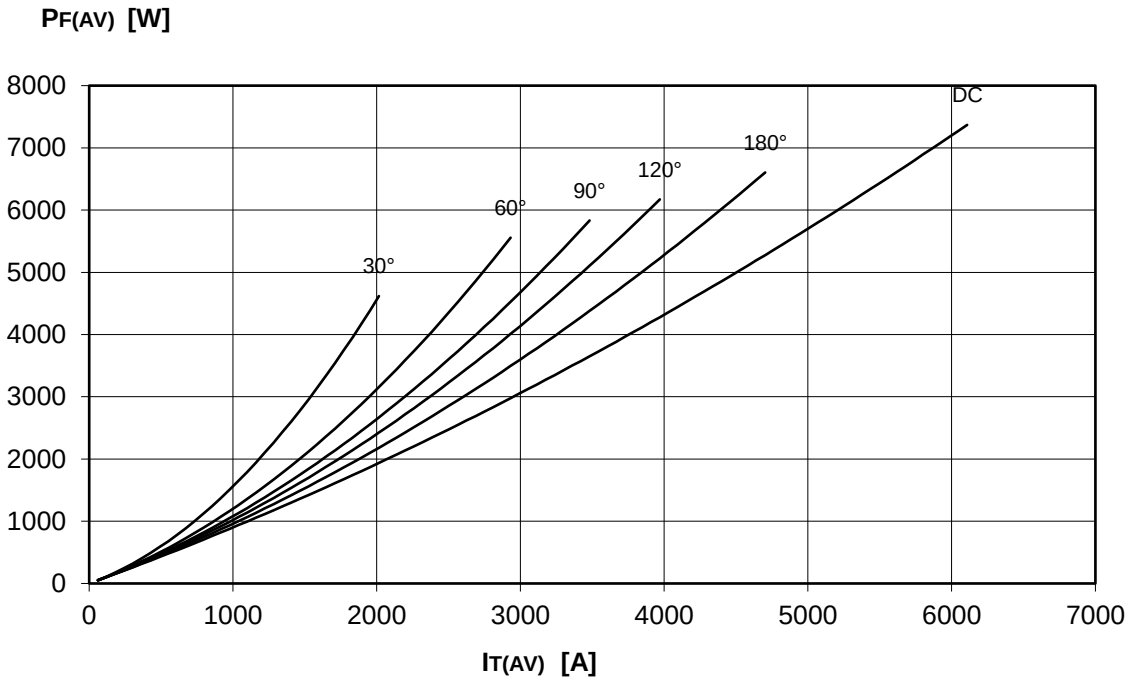
ORDERING INFORMATION : AT706LT S 08

standard specification — VRRM/100

DISSIPATION CHARACTERISTICS

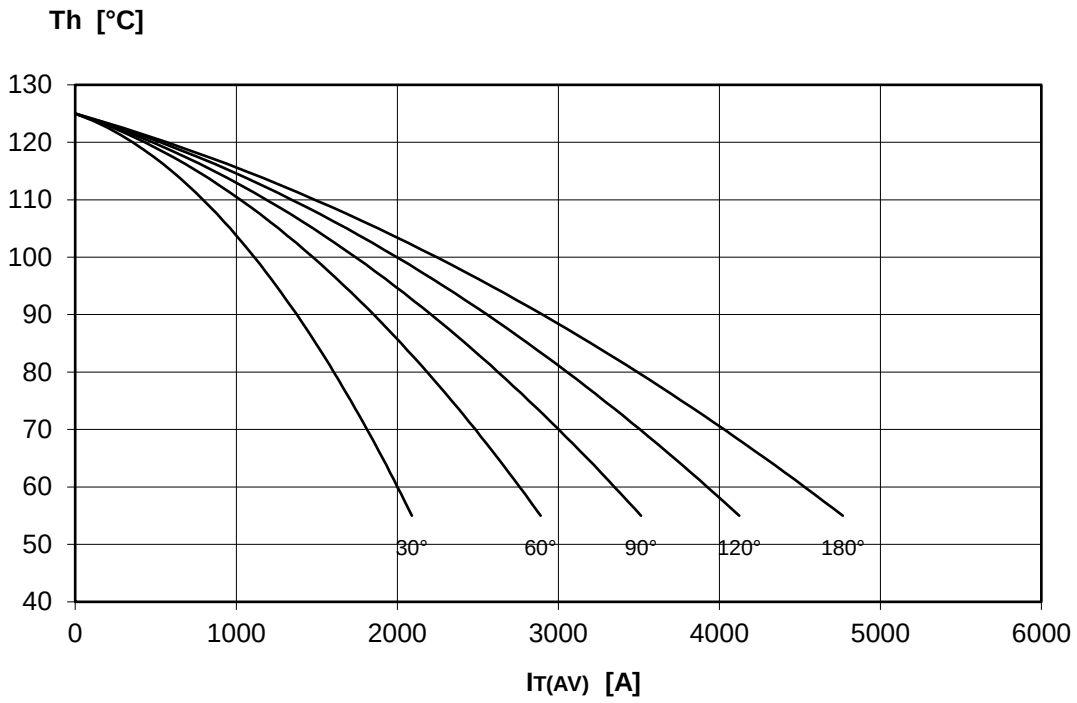
SQUARE WAVE

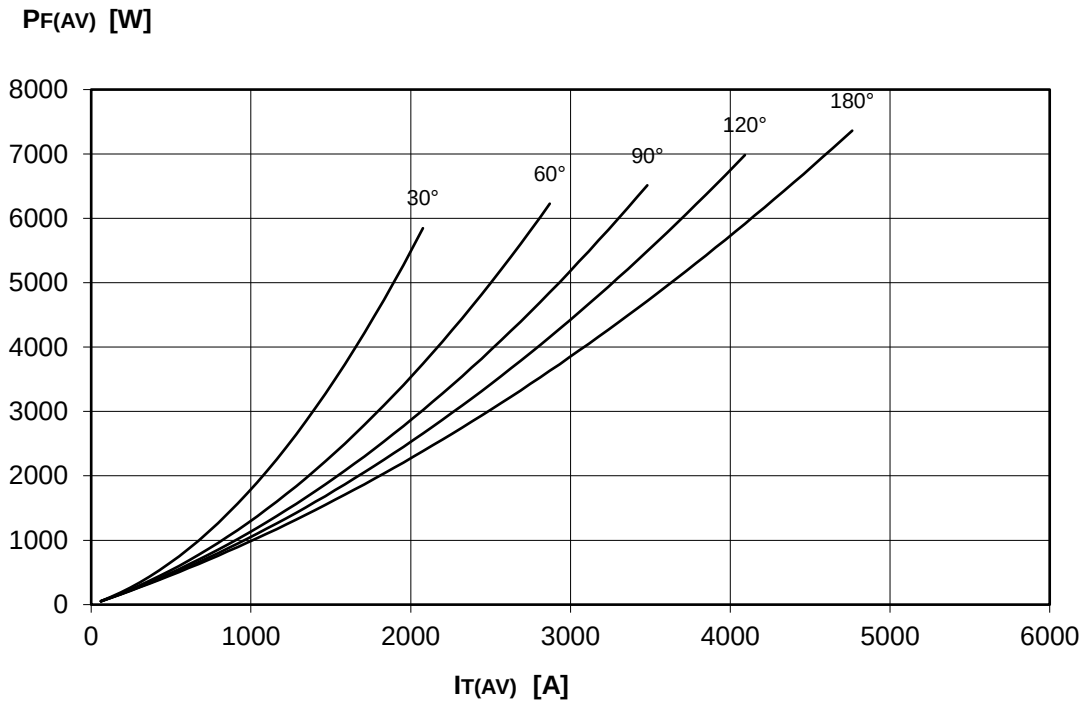




DISSIPATION CHARACTERISTICS

SINE WAVE



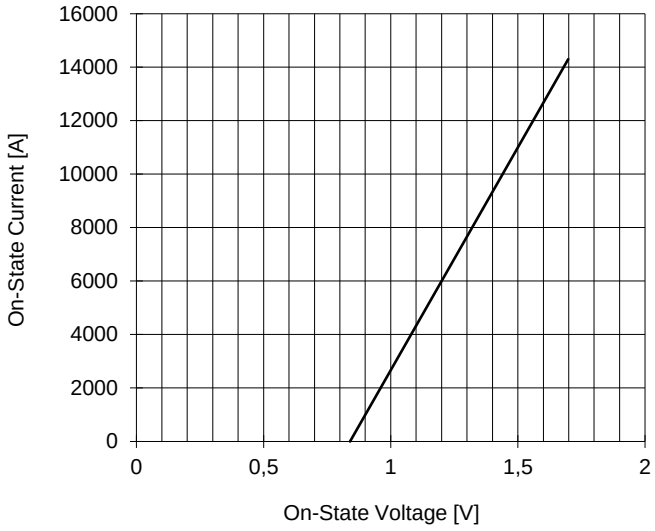


AT706LT PHASE CONTROL THYRISTOR

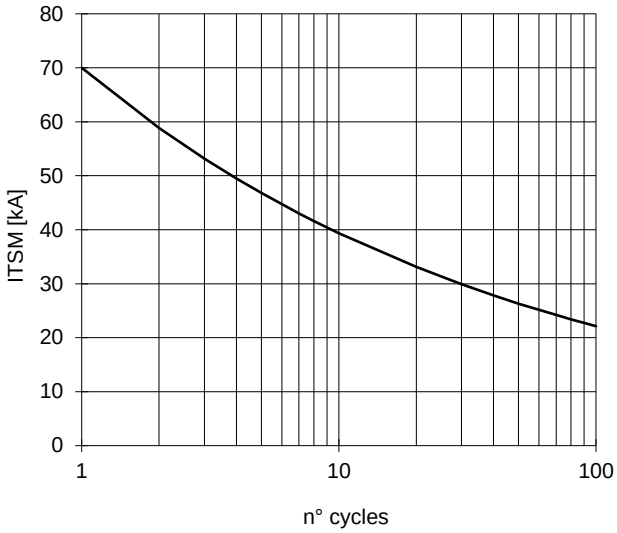
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FINAL SPECIFICATION Feb. 17 - Issue: 1

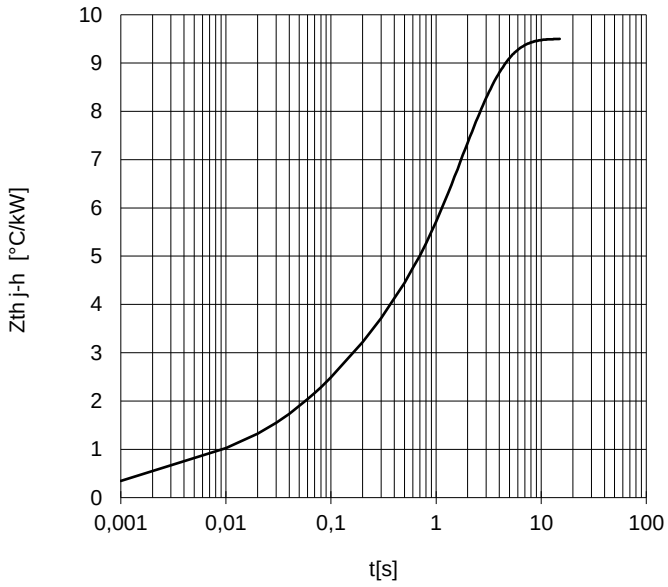
ON-STATE CHARACTERISTIC
Tj = 125 °C

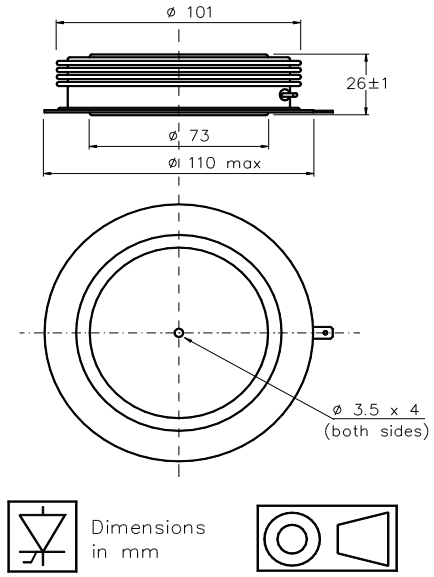


SURGE CHARACTERISTIC
Tj = 125 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED





Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.
In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

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