# Automotive IPD 1ch Low Side Switch with Output Diagnostic Function

## BV1LE080EFJ-C

### Features

- Built-in Dual TSD*1
- AEC-Q100 Qualified*2
- Built-in Over Current Protection Function(OCP)
- Built-in Active Clamp Function
- Direct Control Enabled from CMOS Logic IC, etc.
- On Resistance $R_{DS(ON)}$ = 80 mΩ (Typ) (when $V_{IN}$ = 5 V, $I_{OUT}$ = 1.5 A, Tj = 25 °C)
- Monolithic Power Management IC with the Control Block (CMOS) and Power MOS FET Mounted on a Single Chip

*1 This IC has thermal shutdown (Junction temperature detect) and ΔTj Protection (Power-MOS steep temperature rising detect).

*2 Grade1

### Key Specifications

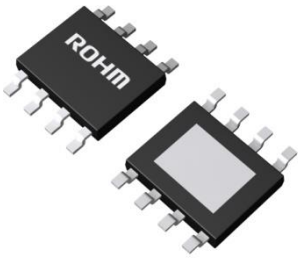
| | |
|---|---|
| On-state Resistance (Tj = 25 °C, Typ) | 80 mΩ |
| Over Current Limitation Level (Tj = 25 °C, Typ) | 13 A |
| Output Clamp Voltage (Min) | 40 V |
| Active Clamp Energy ($Tj_{(START)}$ = 25 °C) | 200 mJ |

### Package

HTSOP-J8

**W (Typ) x D (Typ) x H (Max)**

4.9 mm x 6.0 mm x 1.0 mm



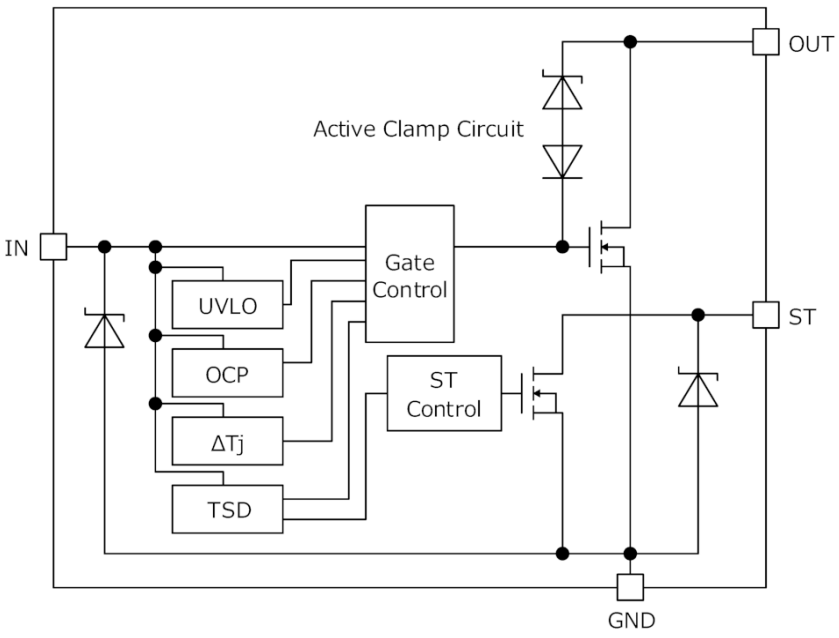

### General Description

BV1LE080EFJ-C is 1ch low side switch IC for 12 V automotive applications. It has built-in OCP, Dual TSD and Active Clamp function. It is equipped with output diagnostic function for TSD.

### Application

- Driving Resistive, Inductive and Capacitive Load

### Block Diagram




○ Product structure : Silicon integrated circuit ○ This product has no designed protection against radioactive rays.


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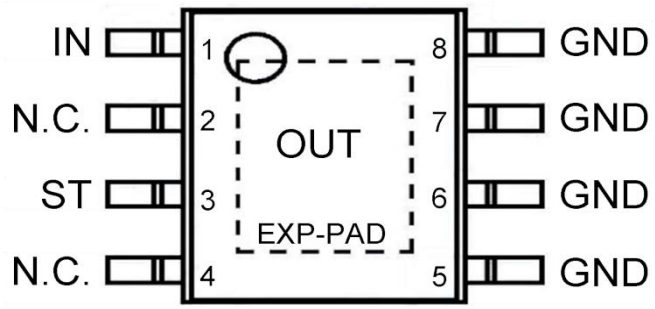
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### Pin Configuration

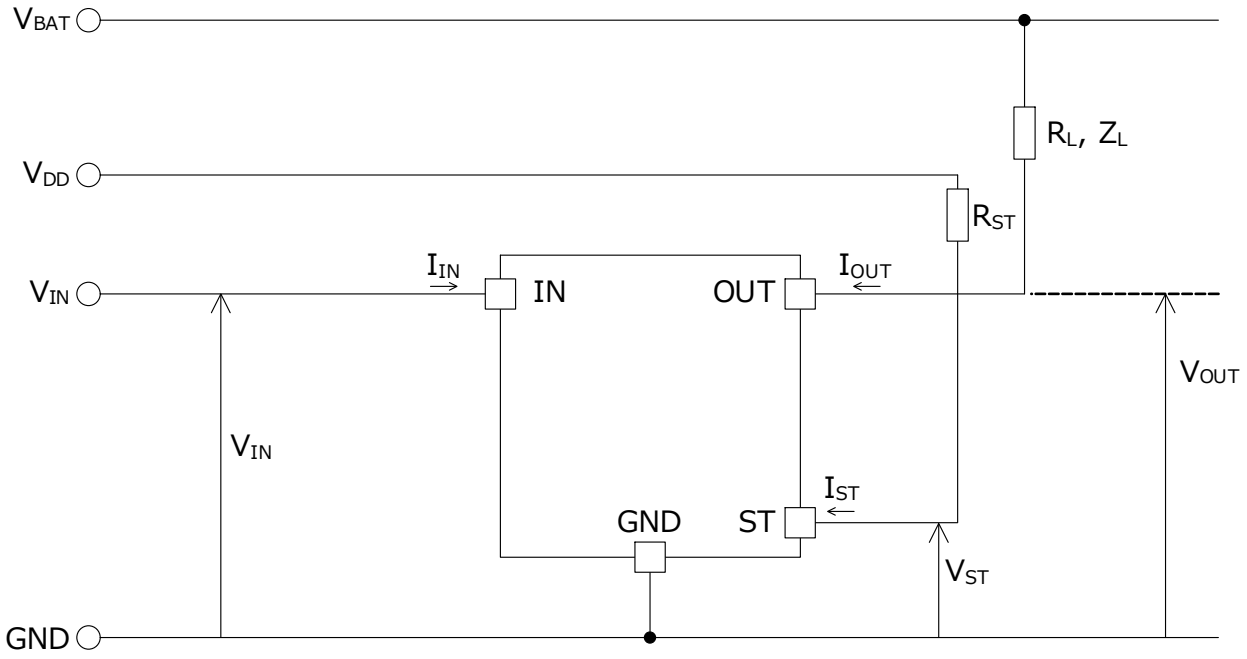
HTSOP-J8
(TOP VIEW)




### Pin Description

| Pin No. | Pin Name | Function |
|---|---|---|
| 1 | IN | Input pin, with internal pull-down resistor. |
| 2 | N.C. | Not connected to internal circuit. Be open, connected to GND. |
| 3 | ST | Self-diagnostic output pin. |
| 4 | N.C. | Not connected to internal circuit. Be open, connected to GND. |
| 5 | GND | GND pin. |
| 6 | GND | GND pin. |
| 7 | GND | GND pin. |
| 8 | GND | GND pin. |
| EXP-PAD | OUT | Output pin. When output pin shorted to battery and output current exceeding the over current detection value, output current will be limited to protect IC. |

### Definition





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## Absolute Maximum Ratings (Tj = 25°C)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Output Voltage | $V_{OUT}$ | -0.3～+40 | V |
| Input Voltage | $V_{IN}$ | -0.3 to +7 | V |
| Output Current | $I_{OUT}$ | 9 (inside limited)*1 | A |
| Diagnostic Output Voltage | $V_{ST}$ | -0.3 to +7 | V |
| Diagnostic Output Current | $I_{ST}$ | 10 | mA |
| Active Clamp Energy (Single Pulse) $Tj_{(START)}$ = 25 °C, $I_{OUT(START)}$ = 1.5 A | $E_{AS(25\ °C)}$ | 200 | mJ |
| Active Clamp Energy (Single Pulse) $Tj_{(START)}$ = 150 °C, $I_{OUT(START)}$ = 1.5 A *2 | $E_{AS(150\ °C)}$ | 55 | |
| Storage Temperature Range | Tstg | -55 to +150 | °C |
| Maximum Junction Temperature | Tjmax | 150 | °C |

*1 Internally limited by over current protection function.
*2 Not 100 % tested.

***Caution 1:*** *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

***Caution 2:*** *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

***Caution 3:*** *When IC turns off with an inductive load, reverse energy has to be dissipated in the IC. This energy can be calculated by the following equation:*

$$E_L = \frac{1}{2} L I_{OUT(START)}{}^2 \times \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CL)}}\right)$$

*Where:*
*L is the inductance of the inductive load.*
*$I_{OUT(START)}$ is the output current at the time of turning off.*
*$V_{OUT(CL)}$ is the output clamp voltage.*

*The IC integrates the active clamp function to internally absorb the reverse energy $E_L$ which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy $E_L$ is active clamp tolerance $E_{AS}$ (refer to Figure 1.) or under when inductive load is used.*

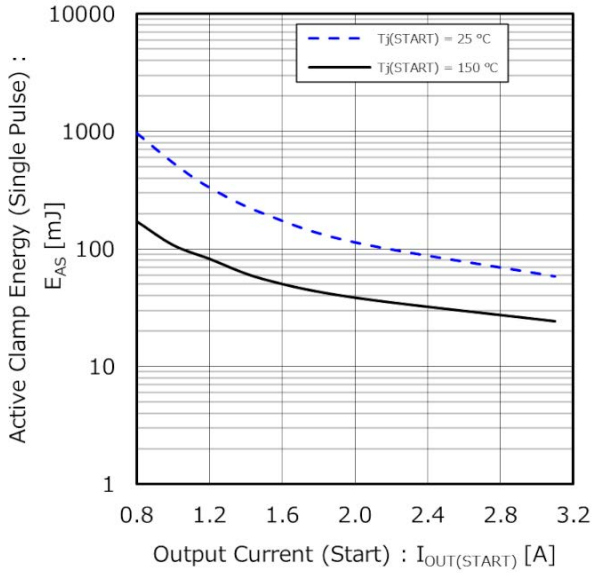



Figure 1. Active Clamp Energy (Single Pulse) vs Output Current (Start)

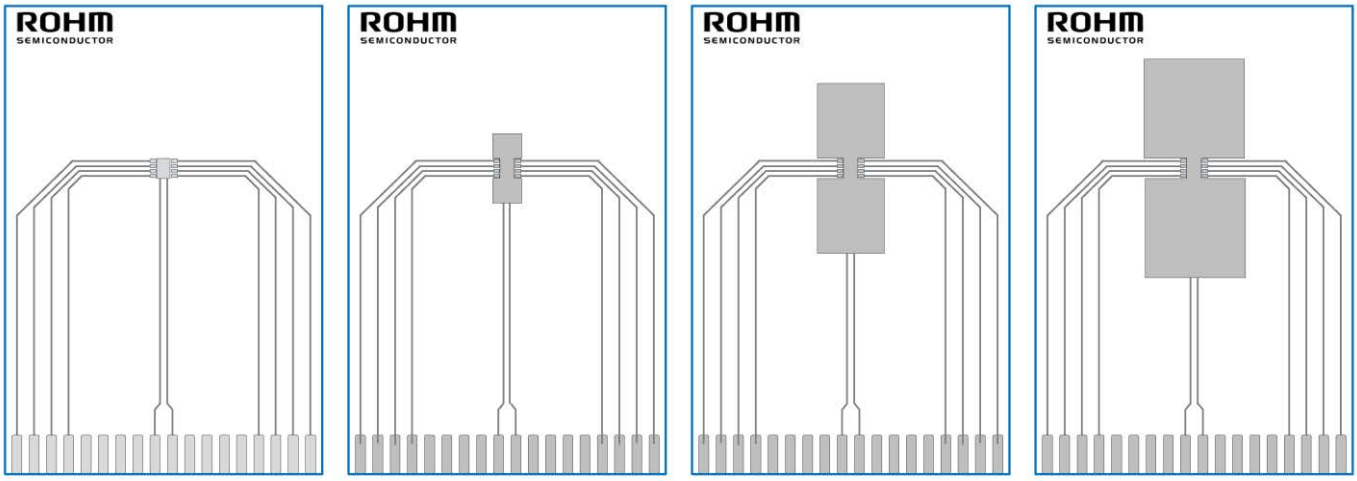

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## Thermal Resistance*1

| 項 目 | 記号 | 標準 | 単位 | 条件 |
|---|---|---|---|---|
| HTSOP-J8 | | | | |
| Between Junction and Surroundings Temperature Thermal Resistance | $\theta_{JA}$ | 131.2 | °C/W | 1s *2 |
| | | 39.8 | °C/W | 2s *3 |
| | | 28.1 | °C/W | 2s2p *4 |

*1 The thermal impedance is based on JESD51-2A (Still-Air) standard. It is used the chip of BV1LE080EFJ-C.
*2 JESD51-3 standard FR4 114.3 mm x 76.2 mm x 1.57 mm 1-layer (1s)
(Top copper foil: ROHM recommended Footprint + wiring to measure, 2 oz. copper.)
*3 JESD51-5 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 2-layers (2s)
(Top copper foil: ROHM recommended Footprint + wiring to measure/
Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm,
copper (top & reverse side) 2 oz.)
*4 JESD51-5, 7 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 4-layers (2s2p)
(Top copper foil: ROHM recommended Footprint + wiring to measure/
2 inner layers and copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm,
copper (top & reverse side/inner layers) 2 oz./1 oz.)

■ PCB Layout 1 layer (1s)

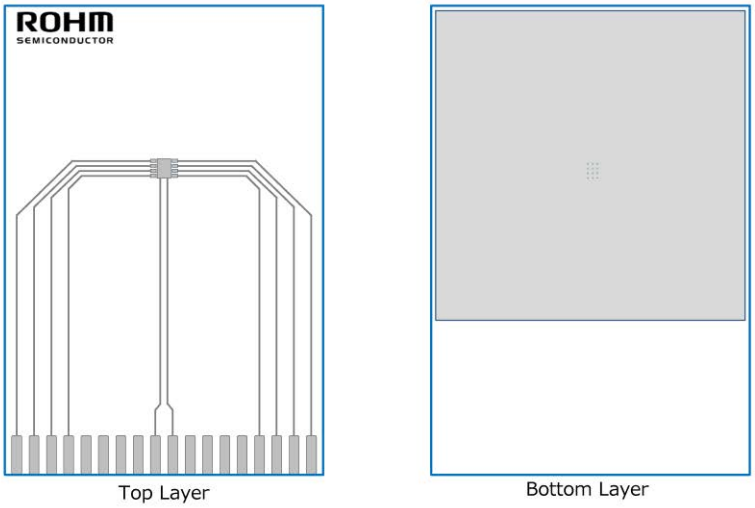


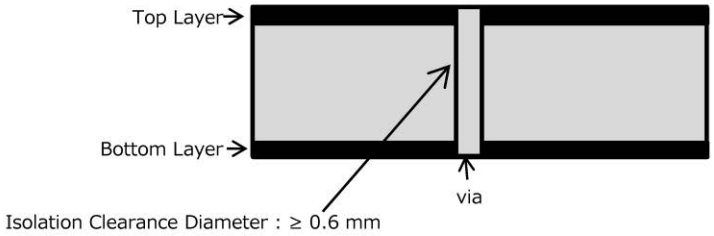

| Dimension | Value |
|---|---|
| Board Finish Thickness | 1.57 mm ± 10 % |
| Board Dimension | 76.2 mm x 114.3 mm |
| Board Material | FR4 |
| Copper Thickness (Top Layer) | 0.070 mm (Cu:2 oz) |
| Copper Foil Area Dimension | Footprint / 100 mm² / 600 mm² / 1200 mm² |


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### Thermal Resistance – continued

- PCB Layout 2 layers (2s)



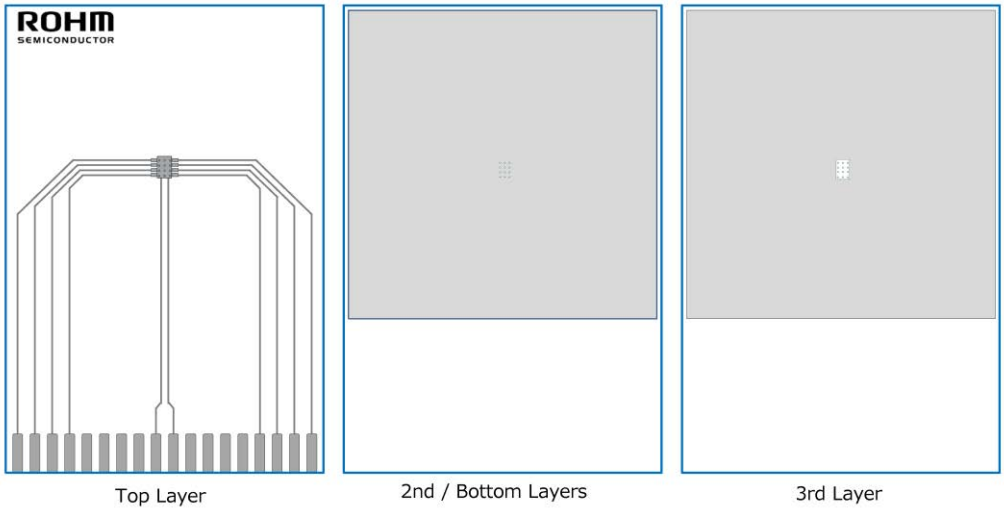

Cross Section

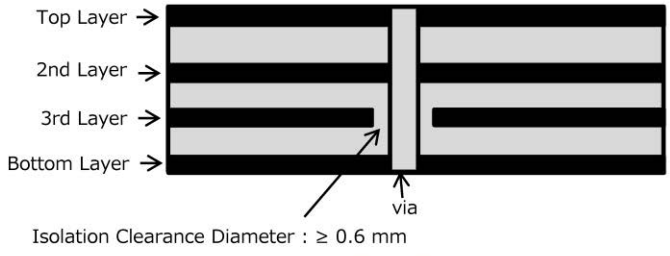
| Dimension | Value |
|---|---|
| Board Finish Thickness | 1.60 mm ± 10 % |
| Board Dimension | 76.2 mm x 114.3 mm |
| Board Material | FR4 |
| Copper Thickness (Top/Bottom Layers) | 0.070 mm (Cu + Plating) |
| Thermal Vias Separation/Diameter | 1.2 mm / 0.3 mm |


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## Thermal Resistance – continued

■ PCB Layout 4 layers (2s2p)



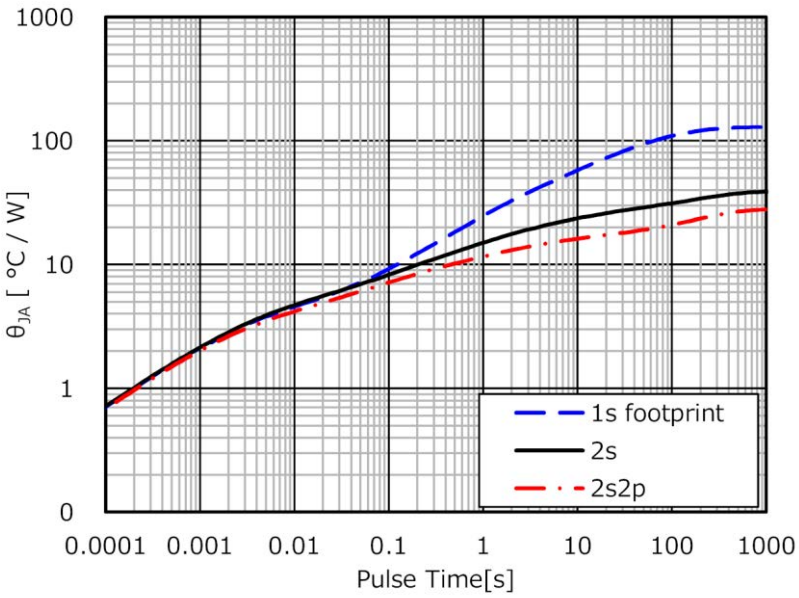

Cross Section

| Dimension | Value |
|---|---|
| Board Finish Thickness | 1.60 mm ± 10 % |
| Board Dimension | 76.2 mm x 114.3 mm |
| Board Material | FR4 |
| Copper Thickness (Top/Bottom Layers) | 0.070 mm (Cu + Plating) |
| Thermal Vias Separation/Diameter | 1.2 mm / 0.3 mm |

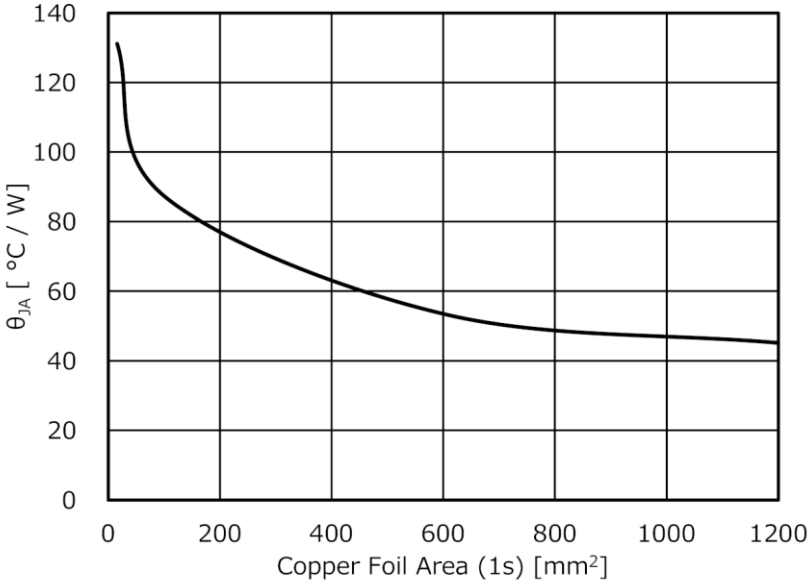

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## Thermal Resistance – continued

■ Transient Thermal Resistance (Single Pulse)




■ Thermal Resistance ($\theta_{JA}$ vs Copper foil area (1s))





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### Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | 3.0 | 5.0 | 5.5 | V |
| Operating Temperature | Tj | -40 | +25 | +150 | °C |

### Electrical Characteristics
### (Unless otherwise specified, –40 °C ≤ Tj ≤ +150 °C)

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Input (IN) | | | | | | |
| Input Threshold Voltage | $V_{IN(TH)}$ | 1.5 | - | 3.0 | V | - |
| High Level Input Current 1 | $I_{IN(H1)}$ | - | 100 | 200 | µA | $V_{IN}$ = 5 V, in Normal Operation |
| High Level Input Current 2*1 *2 | $I_{IN(H2)}$ | - | - | 300 | µA | $V_{IN}$ = 5 V, in Abnormal Operation |
| Low Level Input Current | $I_{IN(L)}$ | -10 | 0 | +10 | µA | $V_{IN}$ = 0 V |
| Power MOS Output | | | | | | |
| On-state Resistance | $R_{DS(ON)}$ | - | 80 | 105 | mΩ | $V_{IN}$ = 5 V, $I_{OUT}$ = 1.5 A, Tj = 25 °C |
| | $R_{DS(ON)}$ | - | - | 200 | mΩ | $V_{IN}$ = 5 V, $I_{OUT}$ = 1.5 A, Tj = 150 °C |
| Leak Current | $I_{OUT(L)}$ | - | 0.0 | 0.5 | µA | $V_{IN}$ = 0 V, $V_{OUT}$ = 18 V, Tj = 25 °C |
| | $I_{OUT(L)}$ | - | - | 2.9 | µA | $V_{IN}$ = 0 V, $V_{OUT}$ = 18 V, Tj = 150 °C |
| Output Clamp Voltage | $V_{OUT(CL)}$ | 40 | 43 | 46 | V | $V_{IN}$ = 0 V, $I_{OUT}$ = 1 mA |
| Turn-ON Time | $t_{ON}$ | 24 | 48 | 96 | µs | $V_{IN}$ = 0 V to 5 V, $R_L$ = 10 Ω, $V_{BAT}$ = 12 V, Tj = 25 °C |
| Turn-OFF Time | $t_{OFF}$ | 30 | 60 | 120 | µs | $V_{IN}$ = 5 V to 0 V, $R_L$ = 10 Ω, $V_{BAT}$ = 12 V, Tj = 25 °C |
| Slew Rate On | $SR_{ON}$ | 0.15 | 0.27 | 0.60 | V/µs | $V_{IN}$ = 0 V to 5 V, $R_L$ = 10 Ω, $V_{BAT}$ = 12 V, Tj = 25 °C |
| Slew Rate Off | $SR_{OFF}$ | 0.15 | 0.27 | 0.60 | V/µs | $V_{IN}$ = 5 V to 0 V, $R_L$ = 10 Ω, $V_{BAT}$ = 12 V, Tj = 25 °C |
| DC Output Current*2 | $I_{OUT(DC)}$ | - | 3.1 | - | A | JEDEC 2s2p PCB, Tj < 150 °C, Ta < 85 °C, $R_{DS(ON)}$ = 200 mΩ |

*1 When thermal shutdown function or over current protection function is ON.
*2 Not 100 % tested.


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**Electrical Characteristics – continued**
**(Unless otherwise specified, –40 °C ≤ Tj ≤ +150 °C)**

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Diagnostic Output | | | | | | |
| ST Low Voltage*2 | $V_{ST(L)}$ | - | - | 0.5 | V | $V_{IN}$ = 5 V, $I_{ST}$ = 1 mA |
| ST Leak Current | $I_{ST(L)}$ | - | - | 1 | µA | $V_{IN}$ = 5 V, $V_{ST}$ = 5 V |
| ST Detection Delay Time*2 | $t_{STDET}$ | - | - | 65 | µs | $V_{IN}$ = 5 V |
| ST Release Delay Time*2 | $t_{STREL}$ | - | - | 10 | µs | $V_{IN}$ = 5 V to 0 V |
| Protection Function | | | | | | |
| Over Current Limitation Level | $I_{OUT(LIM)}$ | 9.0 | 13.0 | 17.0 | A | $V_{IN}$ = 5 V, Tj = 25 °C, $V_{OUT}$= 12 V |
| Thermal Shutdown Detected Temperature*2 | $T_{TSDD}$ | 150 | 175 | - | °C | $V_{IN}$ = 5 V |
| Thermal Shutdown Released Temperature*2 | $T_{TSDR}$ | 130 | 155 | - | °C | $V_{IN}$ = 5 V |
| Thermal Shutdown Hysteresis Temperature*2 | $T_{TSDHYS}$ | - | 20 | - | °C | $V_{IN}$ = 5 V |
| ΔTj Protection Detected Temperature*2 | $T_{DTJD}$ | - | 80 | - | °C | $V_{IN}$ = 5 V |
| ΔTj Protection Released Temperature*2 | $T_{DTJR}$ | - | 45 | - | °C | $V_{IN}$ = 5 V |
| ΔTj Protection Hysteresis Temperature*2 | $T_{DTJHYS}$ | - | 35 | - | °C | $V_{IN}$ = 5 V |

*2 Not 100 % tested.


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## Typical Performance Curves
## (Unless otherwise specified, Tj = 25 °C, $V_{IN}$ = 5 V)

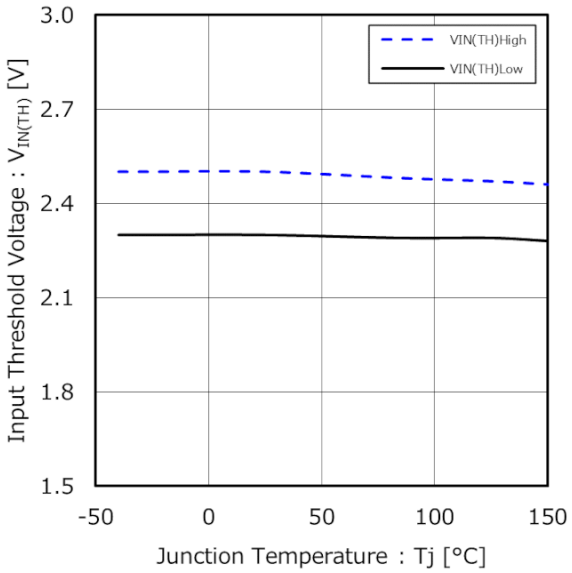



Figure 2. Input Threshold Voltage vs Junction Temperature

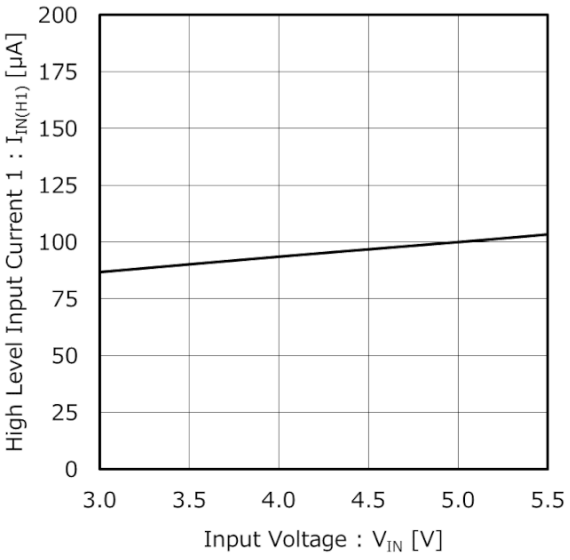



Figure 3. High Level Input Current 1 vs Input Voltage

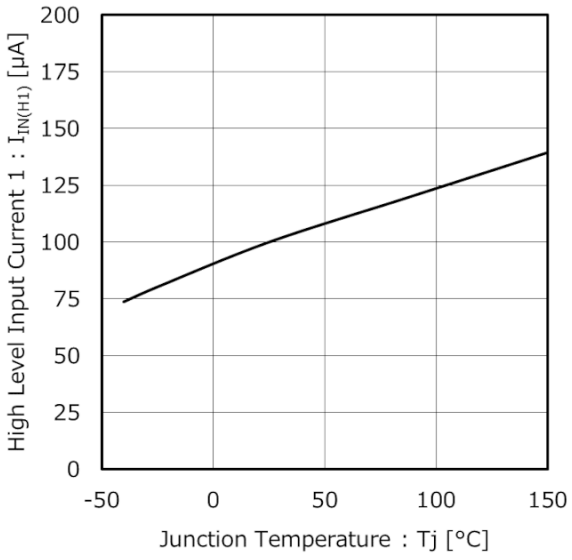



Figure 4. High Level Input Current 1 vs Junction Temperature

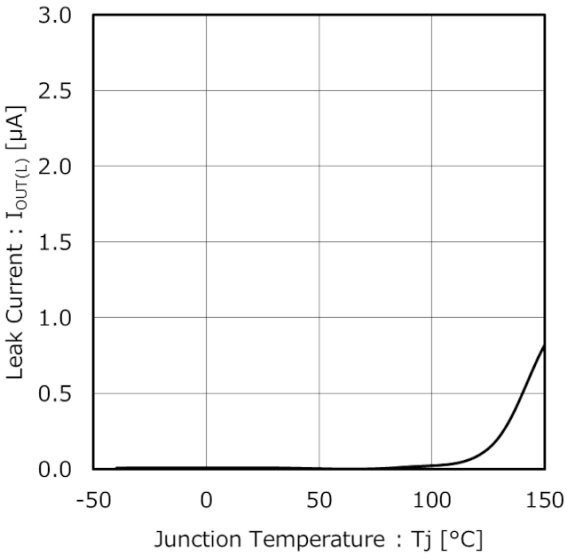



Figure 5. Leak Current vs Junction Temperature


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**Typical Performance Curves – continued**
**(Unless otherwise specified, Tj = 25 °C, $V_{IN}$ = 5 V)**

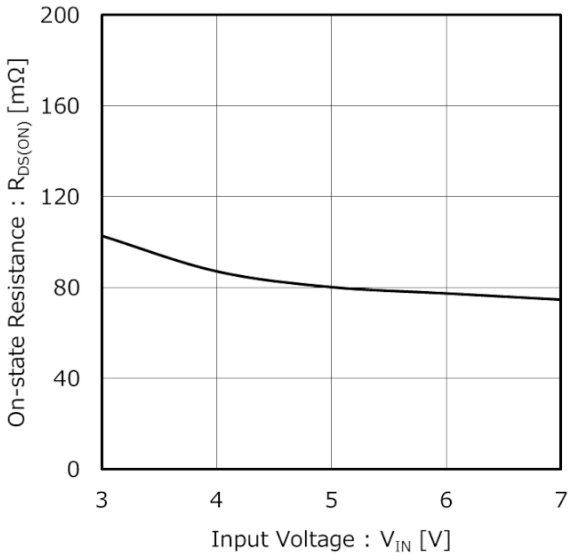



Figure 6. On-state Resistance vs Input Voltage

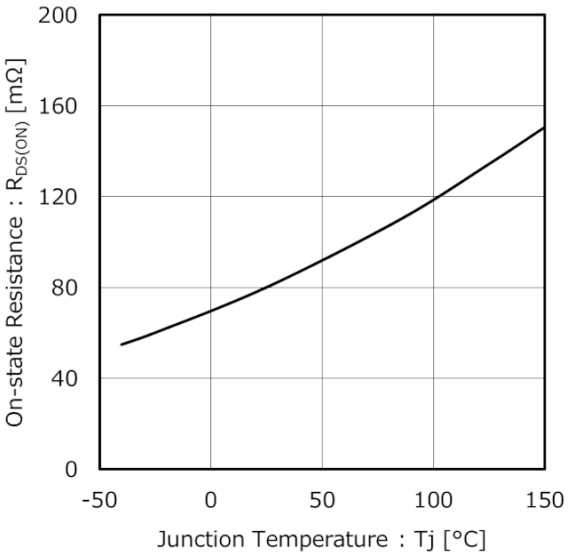



Figure 7. On-state Resistance vs Junction Temperature

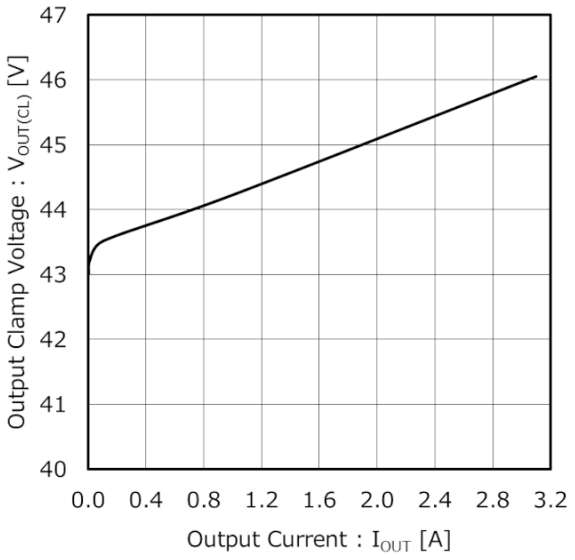



Figure 8. Output Clamp Voltage vs Output Current

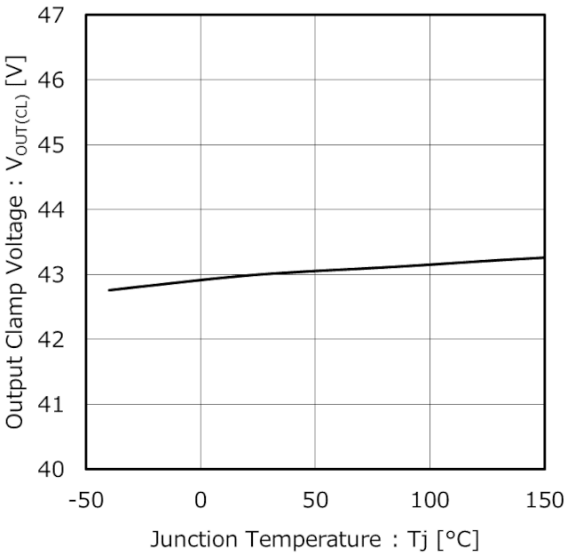



Figure 9. Output Clamp Voltage vs Junction Temperature
($I_{OUT}$ = 1 mA)


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**Typical Performance Curves – continued**
**(Unless otherwise specified, Tj = 25 °C, $V_{IN}$ = 5 V)**

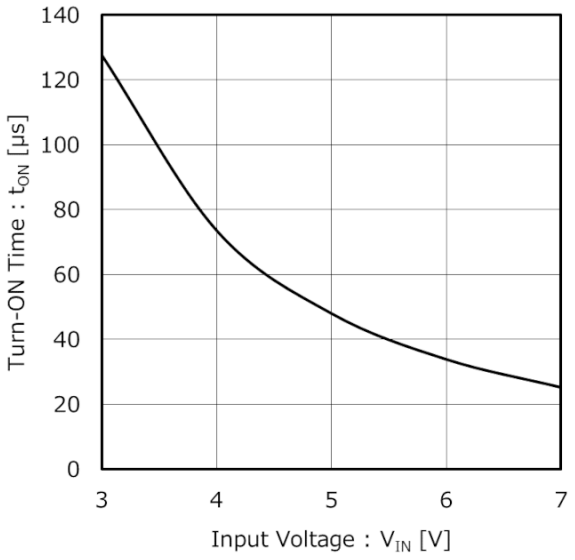



Figure 10. Turn-ON Time vs Input Voltage

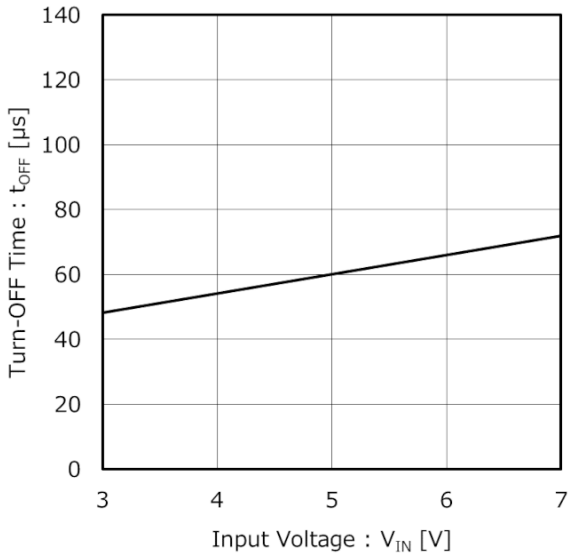



Figure 11. Turn-OFF Time vs Input Voltage

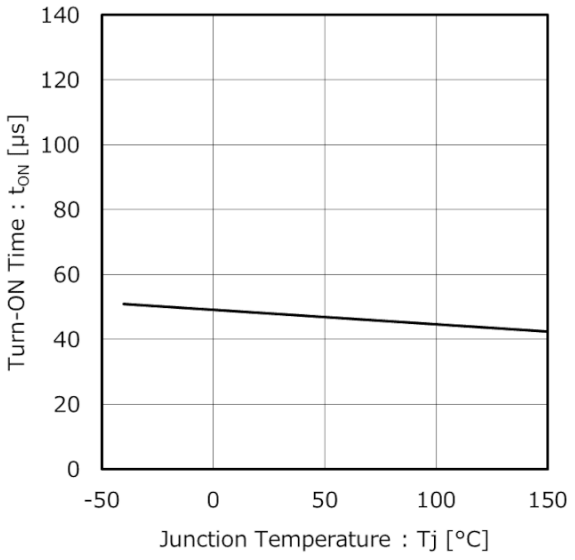



Figure 12. Turn-ON Time vs Junction Temperature

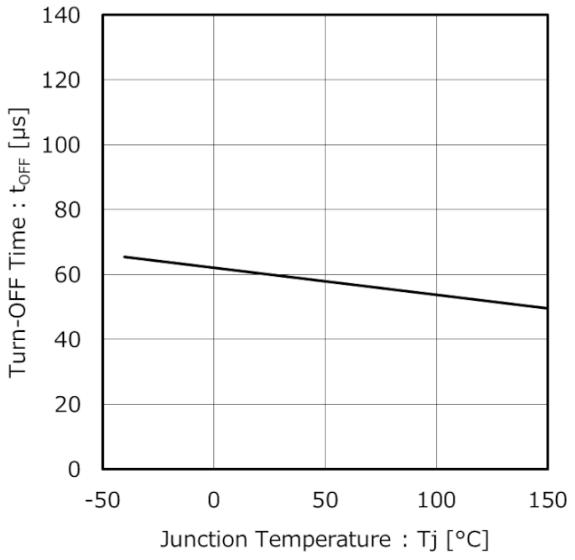



Figure 13. Turn-OFF Time vs Junction Temperature


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**Typical Performance Curves – continued**
**(Unless otherwise specified, Tj = 25 °C, $V_{IN}$ = 5 V)**

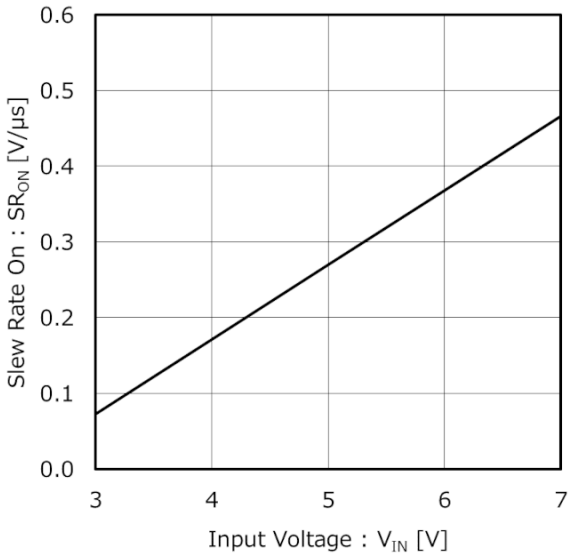



Figure 14. Slew Rate On vs Input Voltage

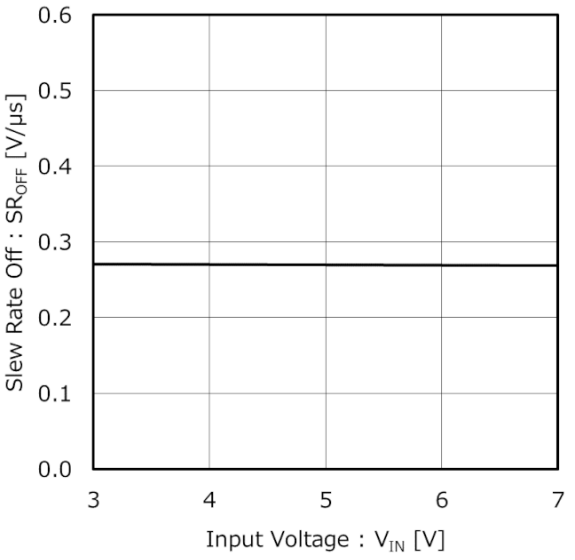



Figure 15. Slew Rate Off vs Input Voltage

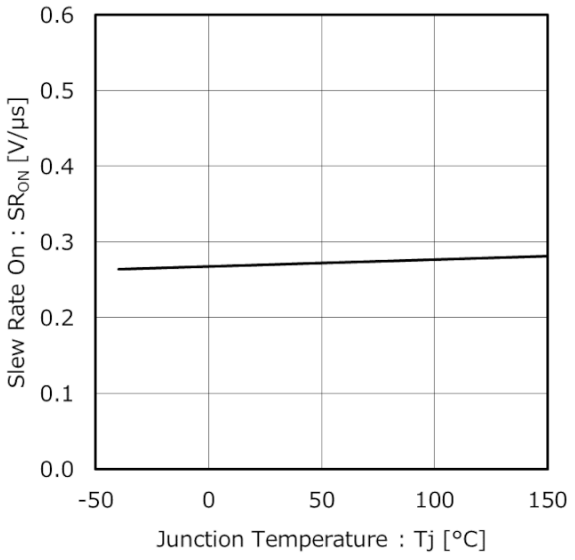



Figure 16. Slew Rate On vs Junction Temperature

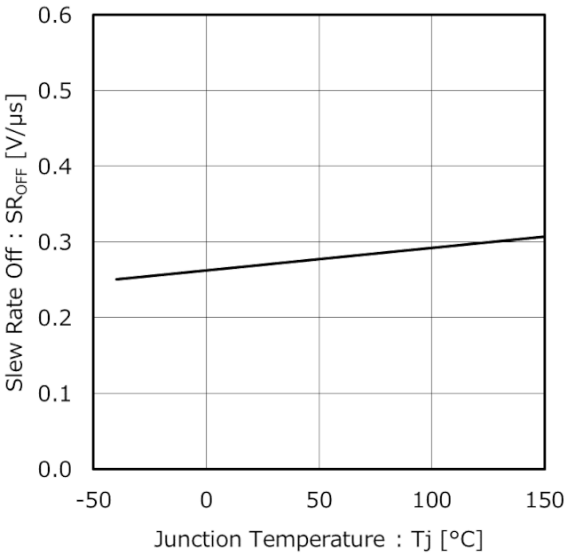



Figure 17. Slew Rate Off vs Junction Temperature


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**Typical Performance Curves – continued**
**(Unless otherwise specified, Tj = 25 °C, $V_{IN}$ = 5 V)**

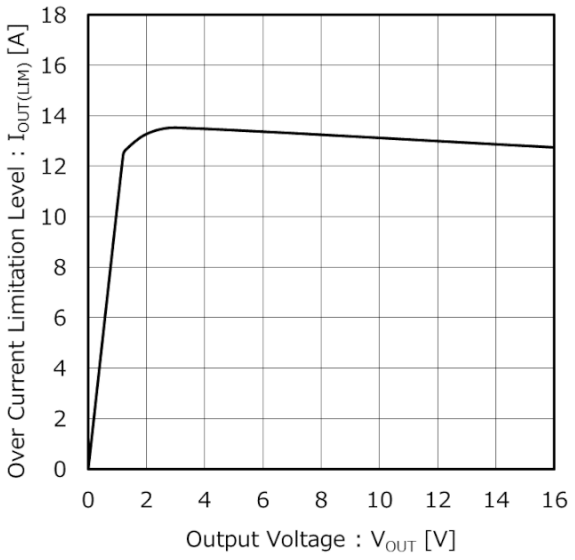



Figure 18. Over Current Limitation Level vs Output Voltage

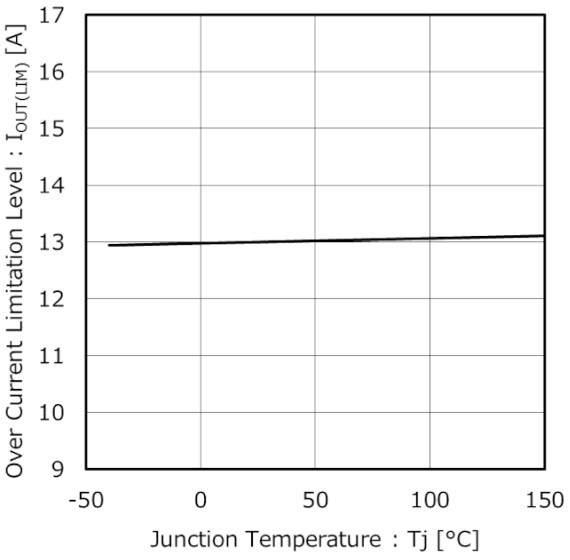



Figure 19. Over Current Limitation Level vs Junction Temperature ($V_{OUT}$ = 12 V)

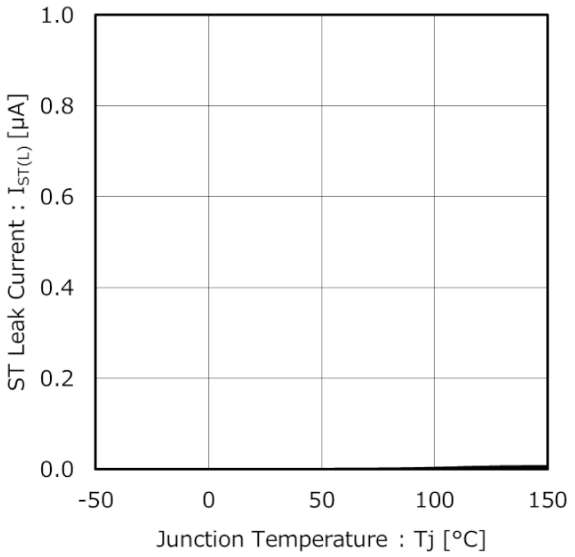
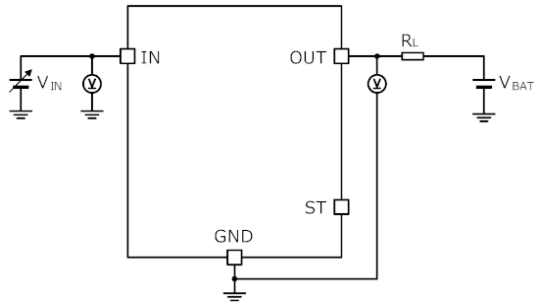


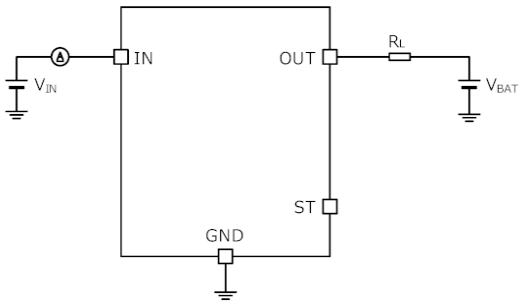

Figure 20. ST Leak Current vs Junction Temperature


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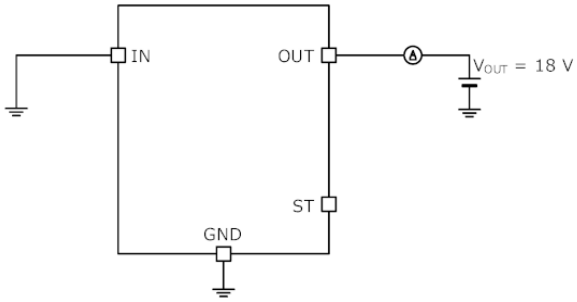
## Measurement Circuit for Typical Performance Curves



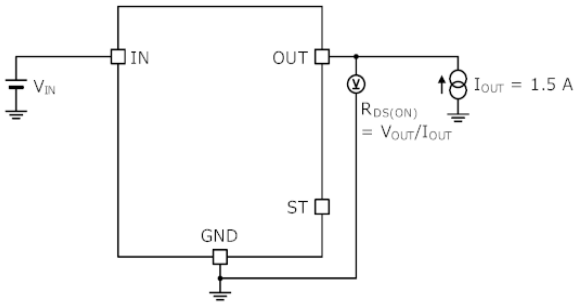

Measurement Circuit for Figure 2



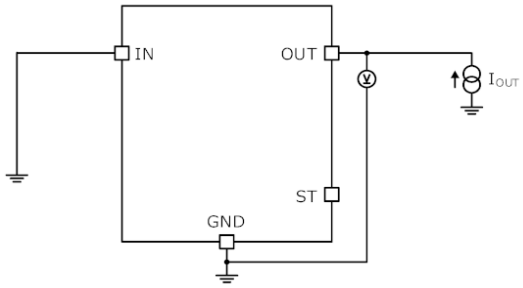

Measurement Circuit for Figure 3、Figure 4



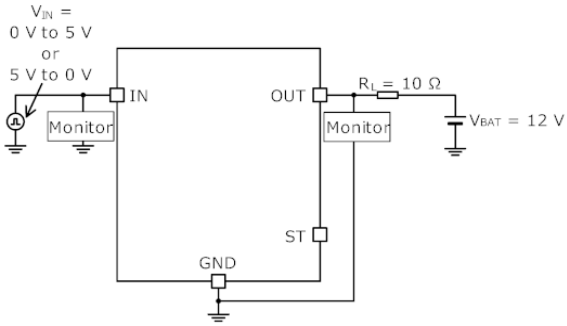

Measurement Circuit for Figure 5




Measurement Circuit for Figure 6、Figure 7



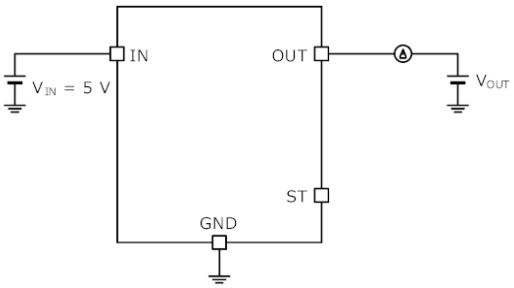

Measurement Circuit for Figure 8、Figure 9



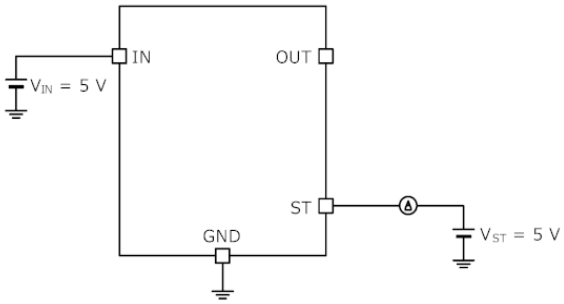

Measurement Circuit for Figure 10、Figure 11、Figure 12、Figure 13、Figure 14、Figure 15、Figure 16、Figure 17


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**Measurement Circuit for Typical Performance Curves – continued**




Measurement Circuit for Figure 18、Figure 19




Measurement Circuit for Figure 20


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### I/O Pin Truth Table

| $V_{IN}$ | State of Protection Function | State of Output | |
|---|---|---|---|
| | | $V_{OUT}$ | $V_{ST}$ *1 |
| Low | - | High | High |
| High | Normal | Low | High |
| | OCP | Current Limitation | High |
| | ΔTj | High | High |
| | TSD | High | Low*2 |

*1 ST pin is pulled up to $V_{DD}$.
*2 Once Thermal Shutdown is detected, ST pin is latched. Low. ST pin Low latch is released by setting IN pin to Low.


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### Timing Chart

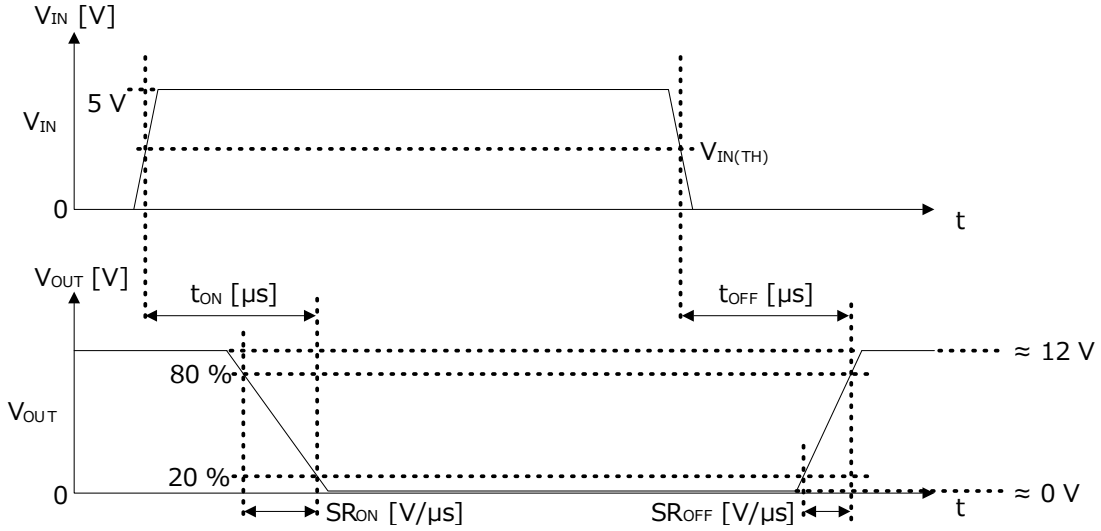



Figure 21. Definition of Turn-ON Time, Turn-OFF Time, and Slew Rate

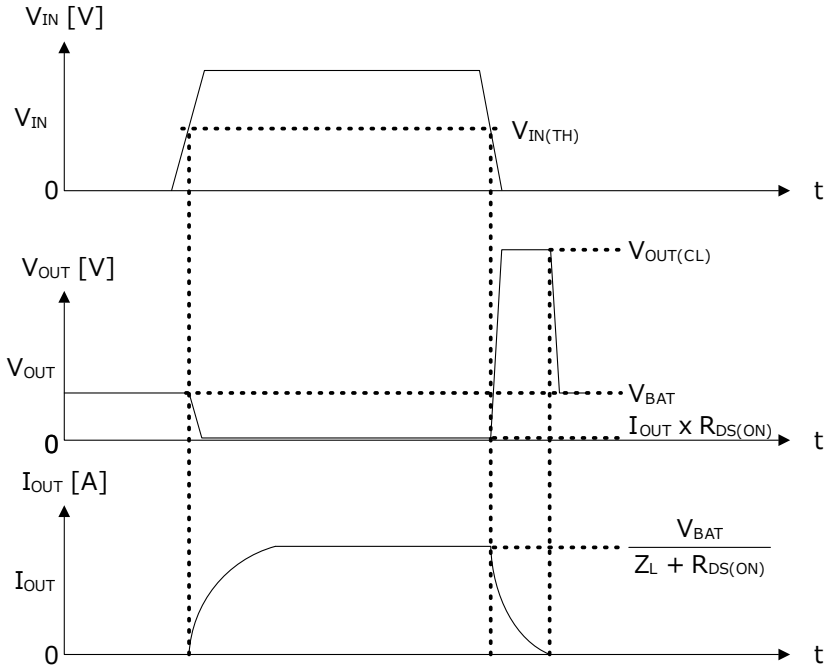



Figure 22. Inductive Load Operation


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## Function Description

■ Over Current Protection Function and Dual TSD Function

This IC has OCP function and Dual TSD function. Following shows the behavior when the OUT pin short circuit.

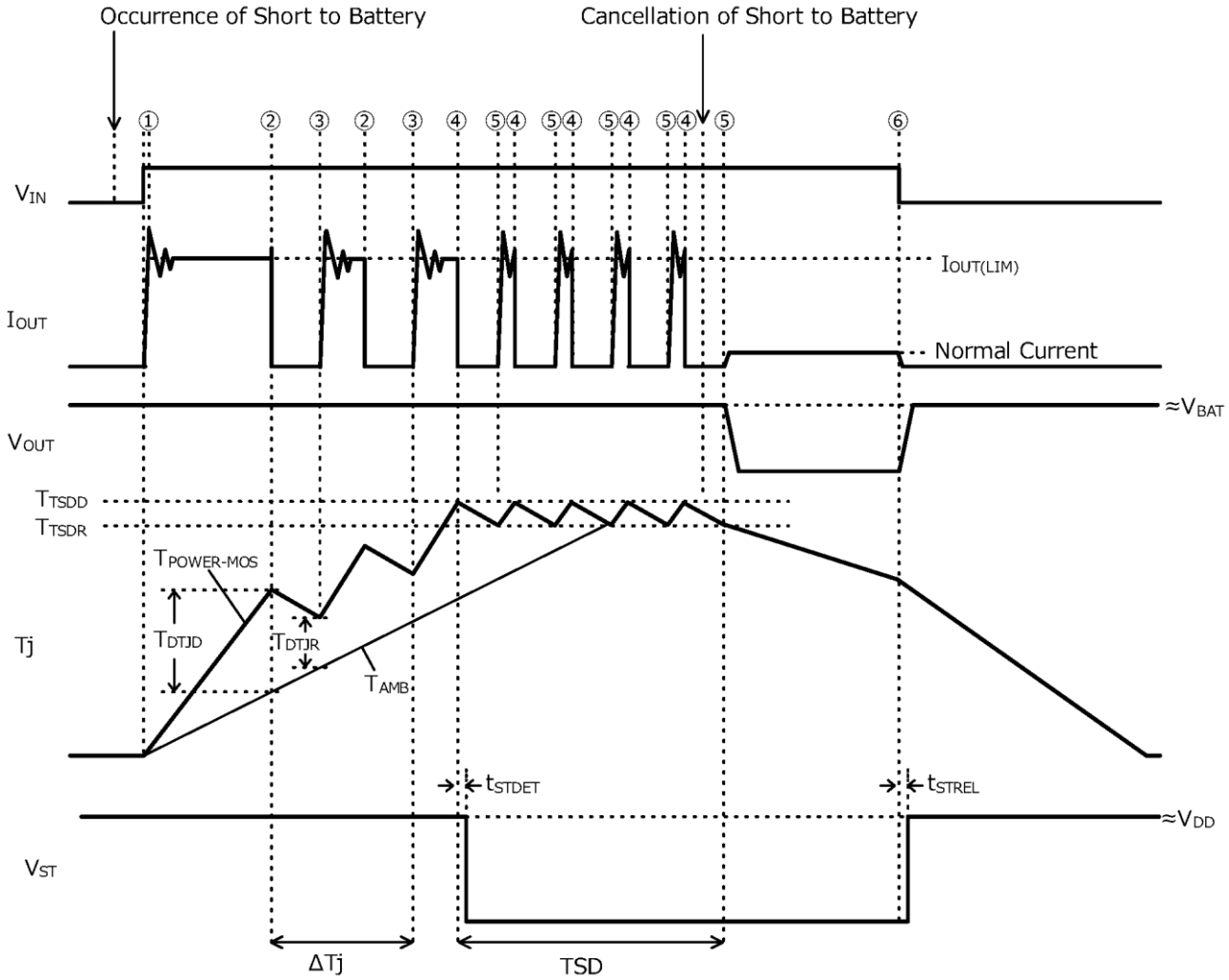



Figure 23. The Behavior when the OUT Pin Short Circuit

① $I_{OUT}$ is limited at Over Current Limitation Level ($I_{OUT(LIM)}$) = 13.0 A (Typ) when over current is occurred.

② The temperature of Power MOS FET part and the control part in this IC is each $T_{POWER-MOS}$, $T_{AMB}$. When the temperature difference becomes 80 °C (Typ) or more, the output turns OFF. This temperature defines as ΔTj Protection Detected Temperature ($T_{DTJD}$).

③ When the temperature difference of $T_{POWER-MOS}$ and $T_{AMB}$ becomes 45 °C (Typ) or less, the output turns automatically ON. This temperature defines as ΔTj Protection Released Temperature ($T_{DTJR}$).

④ The output is turned off when the temperature of the IC reaches Thermal Shutdown Detected Temperature ($T_{TSDD}$) = 175 °C (Typ) or more. At this time, $V_{ST}$ latches Low.

⑤ The output returns to its normal state when the temperature of the IC becomes Thermal Shutdown Released Temperature ($T_{TSDR}$) = 155 °C (Typ) or less. $V_{ST}$ keeps latching Low.

⑥ $V_{ST}$ becomes High after $t_{STREL}$ when $V_{IN}$ becomes Low.


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## Operational Notes

1. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

2. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

3. **GND Pin Connection**
   Connect all ground pins to ground.

4. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

5. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

6. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

7. **Ceramic Capacitor**
   When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

8. **Thermal Shutdown Function (TSD)**
   This IC has a built-in thermal shutdown function that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD function that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
   Note that the TSD function operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD function be used in a set design or for any purpose other than protecting the IC from heat damage.

9. **Over Current Protection Function (OCP)**
   This IC incorporates an integrated overcurrent protection function that is activated when the load is shorted. This protection function is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection function.

10. **Active Clamp Operation**
    The IC integrates the active clamp function to internally absorb the reverse energy $E_L$ which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy $E_L$ is active clamp energy $E_{AS}$ (refer to Figure 1.) or under when inductive load is used.


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## Operational Notes – continued

### 11. Negative Current of Output

When the OUT pin (DRAIN) becomes lower than the GND pin (SOURCE), a current flow from the in pin (the IN pin) to the OUT pin (DRAIN) through a parasitic transistor. As shown in Figure 24 when the input pin is High, a current flow from a power supply of the connection (MCU, and so on) of the input pin to the OUT pin (DRAIN). As shown in Figure 25 when the input pin is Low, a current flow from the GND of parts (MCU, and so on) that connected to the input pin to the OUT pin (DRAIN).

Therefore, set the OUT pin (DRAIN) is -0.3 V or higher. When the OUT pin becomes lower than -0.3V, add a restriction resistance 330 Ω or higher to the IN pin. However, set the value of restriction resistance in consideration of the voltage descent caused by power supply pin and input pins currents.

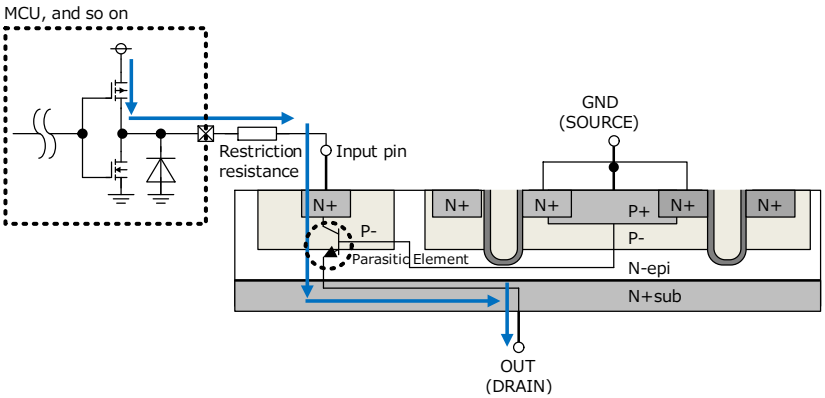



Figure 24. Negative Current Path (when the input pins are High)

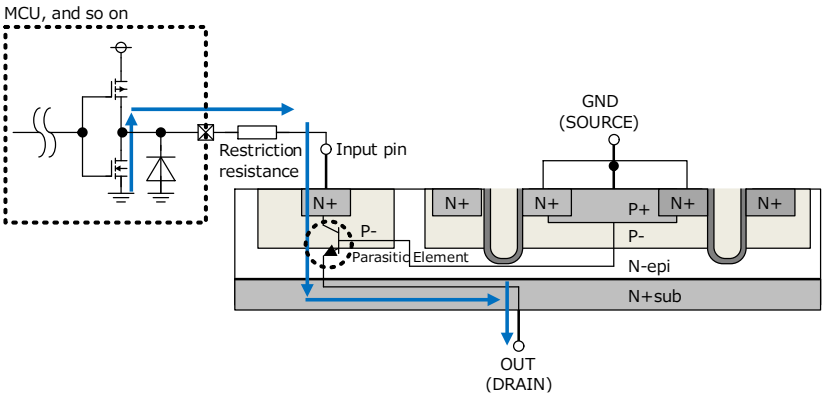



Figure 25. Negative Current Path (when the input pins are Low)


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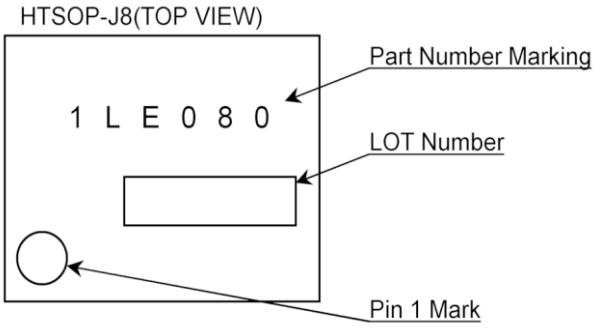
## Ordering Information

| B V 1 L E 0 8 0 EFJ | - | C E 2 |
|---|---|---|

パッケージ
EFJ：HTSOP-J8

Product Rank
C: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

## Marking Diagram

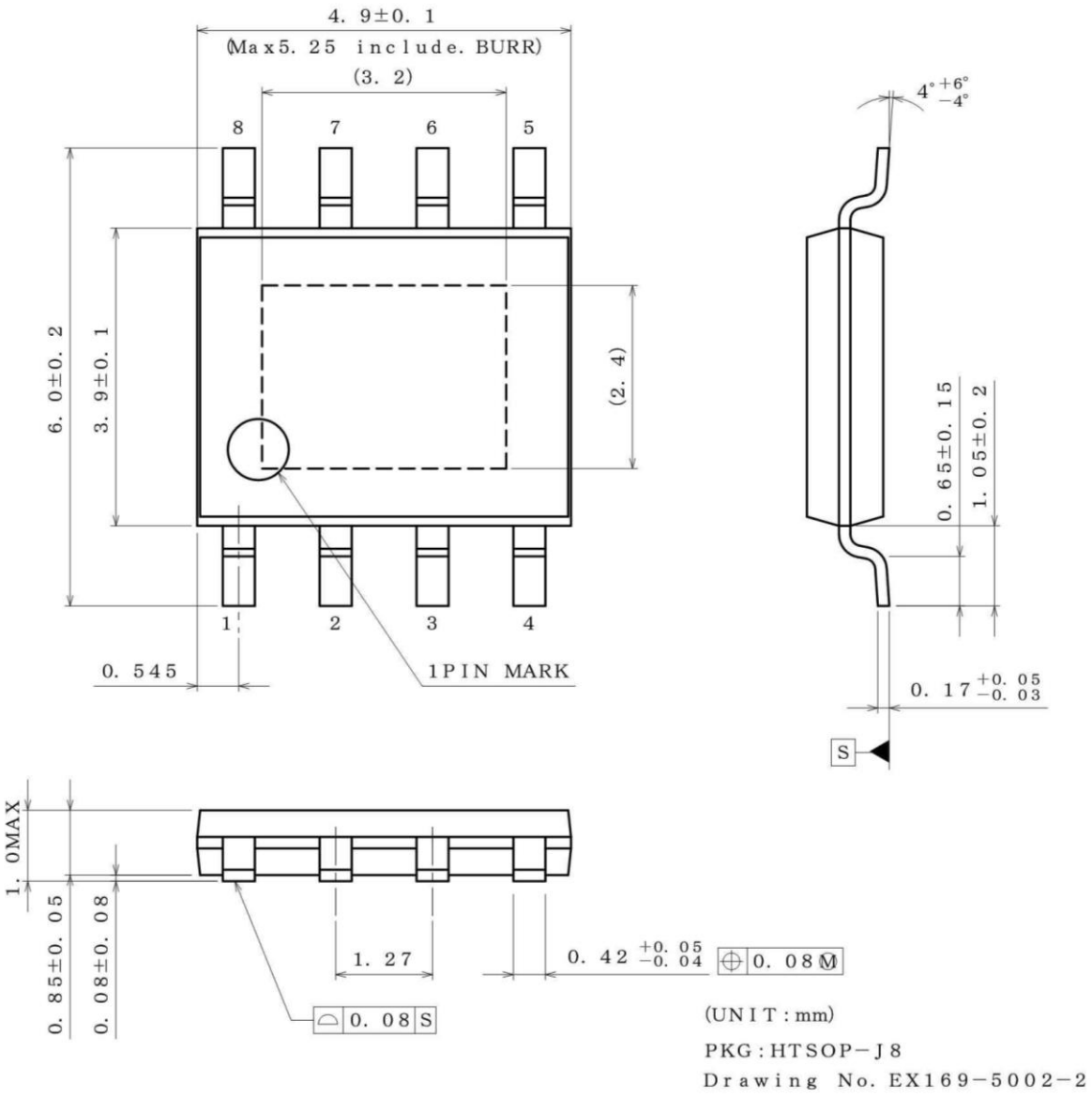




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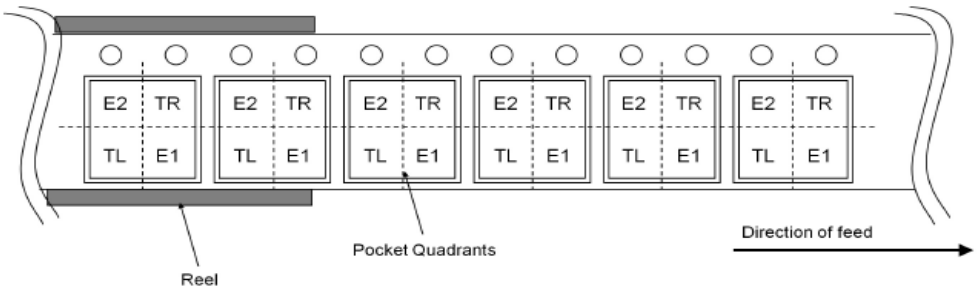
**Physical Dimension and Packing Information**

| Package Name | HTSOP-J8 |
|---|---|




< Tape and Reel Information >

| | |
|---|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2<br>The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand |





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**Revision History**

| Date | Revision | Changes |
|---|---|---|
| 08.Feb.2022 | 001 | New Release |


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# Notice

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| JAPAN | USA | EU | CHINA |
|---|---|---|---|
| CLASSⅢ | CLASSⅢ | CLASSⅡb | CLASSⅢ |
| CLASSⅣ | | CLASSⅢ | |

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification


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## Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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