512Kx32 SRAM 3.3V MODULE

*PRELIMINARY**

FEATURES

- Access Times of 15, 17, 20ns
- Low Voltage Operation
- Packaging
  - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400)
  - 68 lead, 22.4mm (0.88") CQFP, 4.6mm (0.180") high, (Package 509)
  - 68 lead, 23.9mm (0.940" sq.) Low Profile CQFP (G1U), 3.56mm (0.140") high, (Package 519)
- Organized as 512Kx32; User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- Low Voltage Operation:
  - 3.3V ±10% Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
  - No clock or refresh required.
- Three State Output.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS512K32V-XG2TX - 8 grams typical
  WS512K32V-XG1UX - 5 grams typical
  WS512K32NV-XH1X - 13 grams typical

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

PIN CONFIGURATION FOR WS512K32NV-XH1X

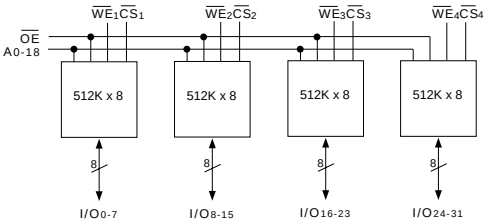
TOP VIEW

1	12	23	34	45	56
I/O8	$\overline{WE}_2$	I/O15	I/O24	VCC	I/O31
I/O9	$\overline{CS}_2$	I/O14	I/O25	$\overline{CS}_4$	I/O30
I/O10	GND	I/O13	I/O26	$\overline{WE}_4$	I/O29
A13	I/O11	I/O12	A6	I/O27	I/O28
A14	A10	$\overline{OE}$	A7	A3	A0
A15	A11	A18	NC	A4	A1
A16	A12	$\overline{WE}_1$	A8	A5	A2
A17	VCC	I/O7	A9	$\overline{WE}_3$	I/O23
I/O0	$\overline{CS}_1$	I/O6	I/O16	$\overline{CS}_3$	I/O22
I/O1	NC	I/O5	I/O17	GND	I/O21
I/O2	I/O3	I/O4	I/O18	I/O19	I/O20
11	22	33	44	55	66

PIN DESCRIPTION

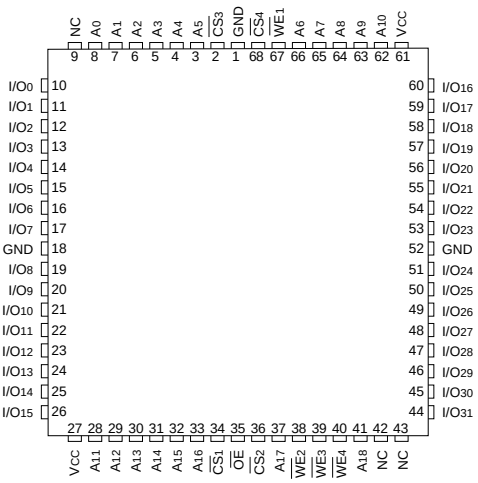
I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



PIN CONFIGURATION FOR WS512K32V-XG2TX AND WS512K32V-XG1UX

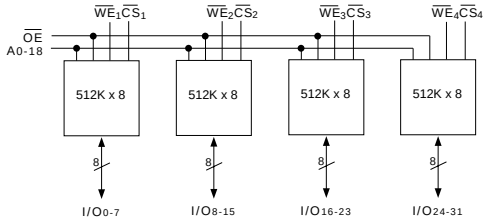
TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}$1-4	Write Enables
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	4.6	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	4.6	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance HIP (PGA)	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
CQFP G2T/G1U			20	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current (x 32 Mode)	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 3.6V		400	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 3.6V		200	mA
Output Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V.
NOTE: Contact factory for low power option.

AC CHARACTERISTICS
(V_{CC} = 3.3V, T_A = -55°C to +125°C)

Parameter Read Cycle	Symbol	-15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	Units
Read Cycle Time	t_{RC}	15		17		20		ns
Address Access Time	t_{AA}		15		17		20	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20	ns
Output Enable to Output Valid	t_{OE}		8		8		10	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	1		1		1		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		8		8		10	ns
Output Disable to Output in High Z	t_{OHZ}[1]		8		8		10	ns

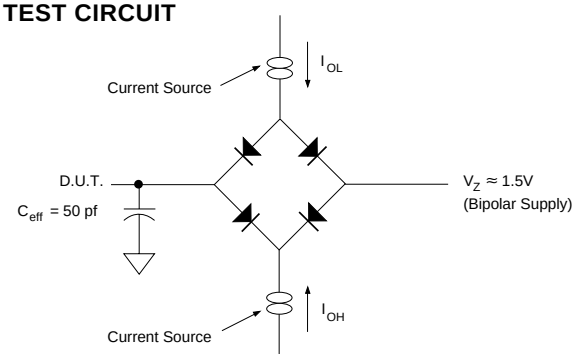
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(V_{CC} = 3.3V, T_A = -55°C to +125°C)

Parameter Write Cycle	Symbol	-15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	Units
Write Cycle Time	t_{WC}	15		17		20		ns
Chip Select to End of Write	t_{CW}	12		12		14		ns
Address Valid to End of Write	t_{AW}	12		12		14		ns
Data Valid to End of Write	t_{DW}	9		9		10		ns
Write Pulse Width	t_{WP}	12		14		14		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Output Active from End of Write	t_{OW}[1]	2		3		3		ns
Write Enable to Output in High Z	t_{WHZ}[1]		8		8		9	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

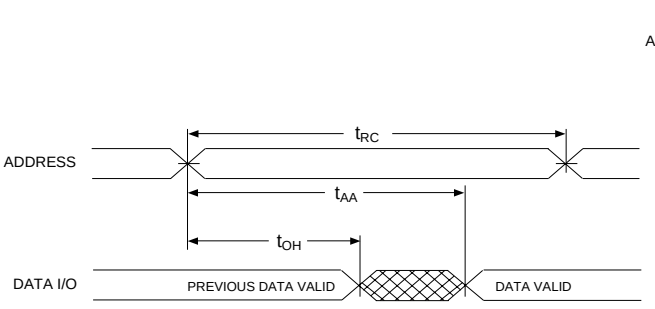


AC TEST CONDITIONS

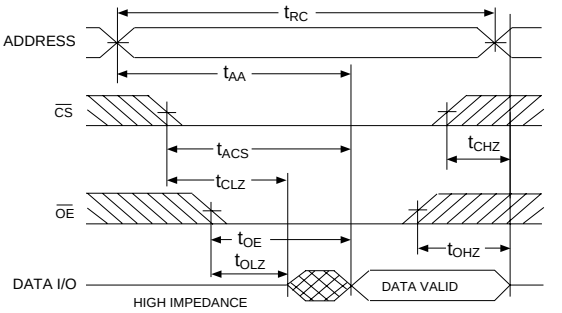
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TIMING WAVEFORM - READ CYCLE

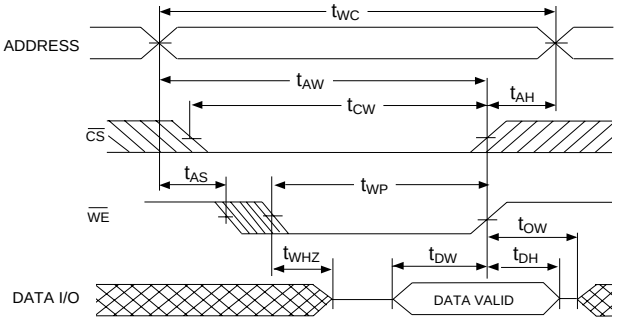


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



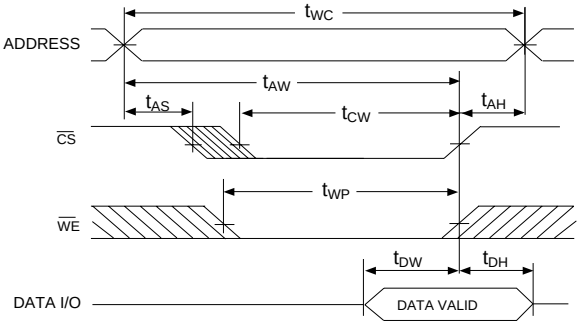
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE - $\overline{WE}$ CONTROLLED



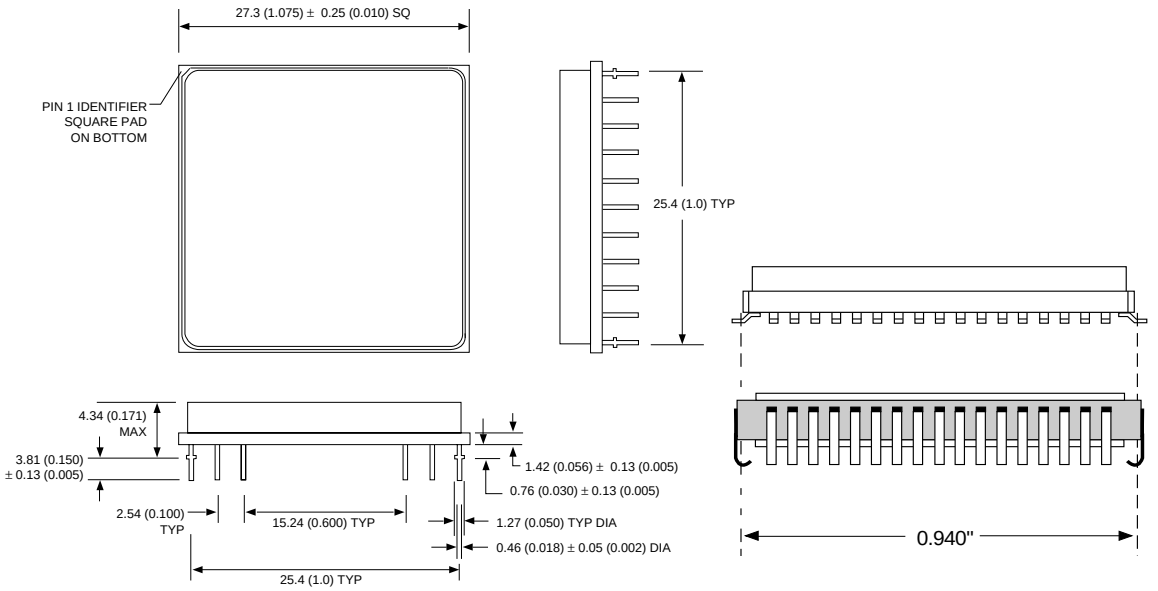
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED



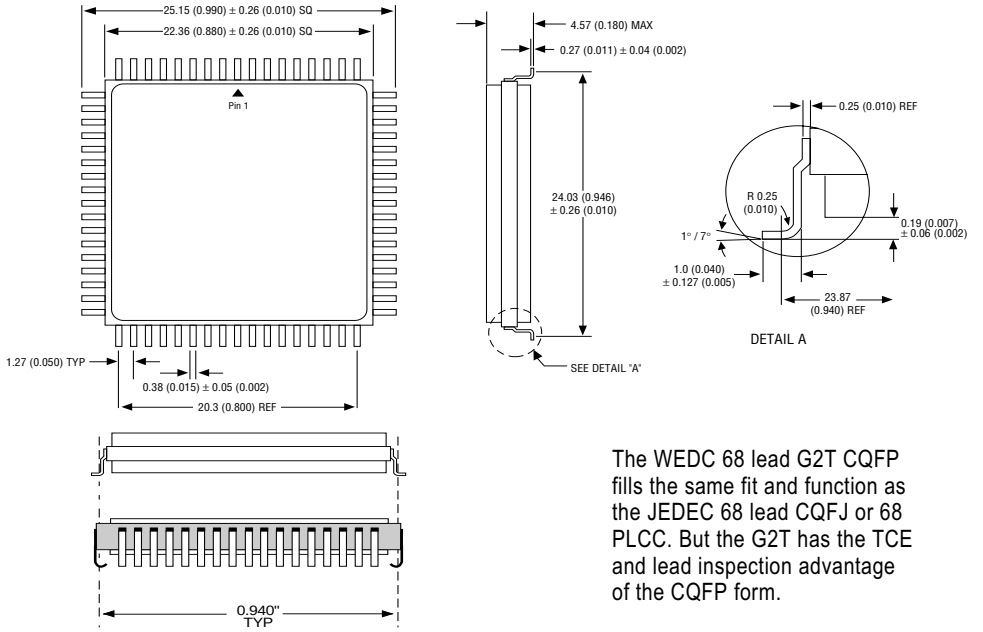
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

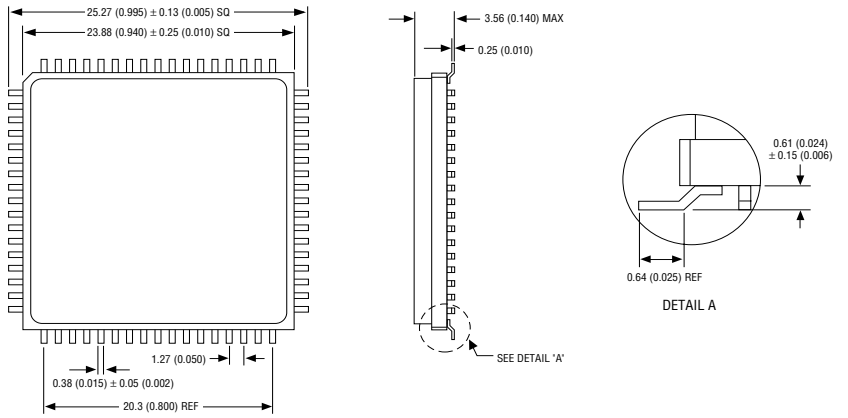
PACKAGE 509: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G2T)



The WEDC 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

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PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1U)



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ORDERING INFORMATION

