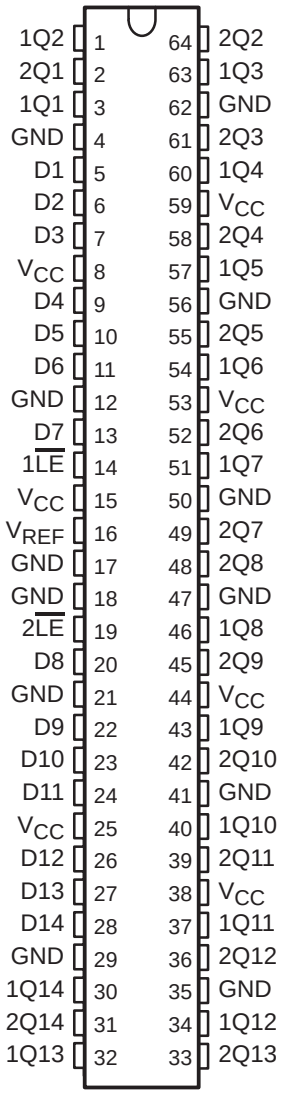
SCES091A – DECEMBER 1996 – REVISED APRIL 1997

- **Member of the Texas Instruments Widebus™ Family**
- **Inputs Meet JEDEC HSTL Standard JESD8-6**
- **All Outputs Have Equivalent 25-Ω Series Resistors**
- **Packaged in Plastic Thin Shrink Small-Outline Package**

DGG PACKAGE
(TOP VIEW)



description

This 14-bit to 28-bit D-type latch is designed for 3.15-V to 3.45-V V_{CC} operation. HSTL levels are expected on the inputs. LVTTL levels are driven on the Q outputs.

All outputs are designed to sink up to 12 mA and include 25-Ω series resistors to reduce overshoot and undershoot.

The SN74HSTL162822 is particularly suitable for driving an address bus to two banks of memory. Each bank of 14 outputs is controlled with its own latch-enable ($\overline{LE}$) input.

Each of the 14 data (D) inputs is tied to the inputs of two D-type latches, which provide true data at the outputs. While $\overline{LE}$ is low, the outputs (Q) of the corresponding 14 latches follow the D inputs. When $\overline{LE}$ is taken high, the Q outputs are latched at the levels set up at the D inputs.

The SN74HSTL162822 is characterized for operation from –40°C to 90°C.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{LE}$	D	Q
L	H	H
L	L	L
H	X	Q_0†

† Output level before the indicated steady-state input conditions were established

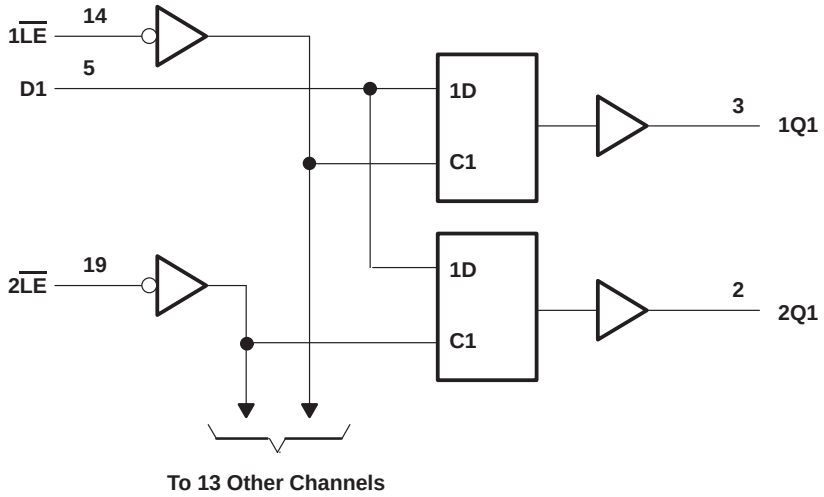
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 2) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 74°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and V_O > V_{CC}.
3. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15		3.45	V
V_{REF}	Reference voltage		0.68	0.75	0.9	V
V_I	Input voltage		0		1.5	V
V_{IH}	High-level input voltage	All pins	V_{REF}+100 mV			V
V_{IL}	Low-level input voltage	All pins			V_{REF}–100 mV	V
I_{OH}	High-level output current				–12	mA
I_{OL}	Low-level output current				12	
T_A	Operating free-air temperature		–40		90	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}		V_{CC} = 3.15 V,	I_{OH} = –12 mA	2.2			V
V_{OL}		V_{CC} = 3.15 V,	I_{OL} = 12 mA			0.8	V
I_I	Control inputs	V_{CC} = 3.45 V	V_I = 0 or 1.5 V			5	μA
	Data inputs		V_I = 0 or 1.5 V			5	
	V_{REF}		V_{REF} = 0.68 V or 0.9 V			90	
I_{CC}		V_{CC} = 3.45 V,	V_I = 0 or 1.5 V		50	100	mA
C_i	Control inputs	V_{CC} = 0 or 3.3 V,	V_I = 0 or 3.3 V		2		pF
	Data inputs	V_{CC} = 0 or 3.3 V,	V_I = 0 or 3.3 V		2		
C_o	Outputs	V_{CC} = 0,	V_O = 0		4		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

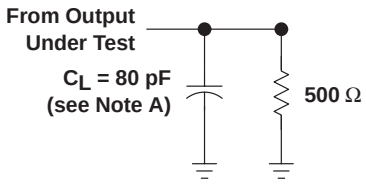
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V_{CC} = 3.3 V ± 0.15 V		UNIT
		MIN	MAX	
t_w	Pulse duration, $\overline{LE}$ low	3		ns
t_{su}	Setup time, D before $\overline{LE}\uparrow$	2		ns
t_h	Hold time, D after $\overline{LE}\uparrow$	1		ns

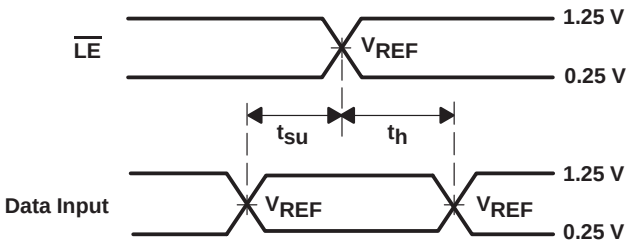
switching characteristics over recommended operating free-air temperature range, V_{REF} = 0.75 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t_{pd}	D	Q	1.6	5	ns
	$\overline{LE}$		1.7	5.7	

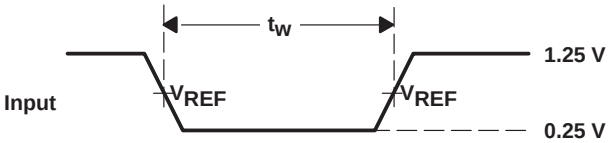
PARAMETER MEASUREMENT INFORMATION



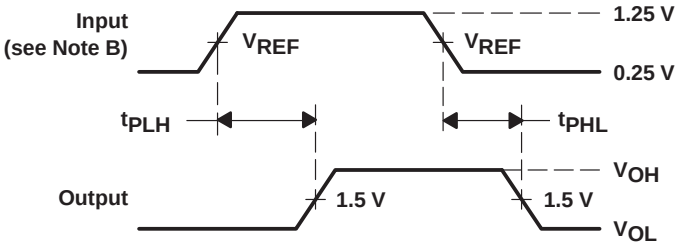
LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, t_f ≤ 1 ns.
C. The outputs are measured one at a time with one transition per measurement.
D. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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