

M62366GP

3V TYPE 8-BIT 12CH D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62366GP is a CMOS semiconductor IC, containing 12 channels of 8-bit D-A converters, with a high-performance buffer operational amplifier provided in the output of each channel. It is operable with a low supply voltage between 2.7~3.6V, and is easy to use due to serial data input, and 3-pin(DI,CLK,LD)connection with microcomputer.

The IC also contains Do pin terminal, enabling cascade connection. The built-in buffer operational amplifiers are of full-swing design with a wide operating supply voltage range for input/output voltage. In addition, this IC provides improved stability against a capacitive load, and therefore is suitable for application to electronic volume(VCA)control, substitute for adjustment semi-fixed resistor, etc.

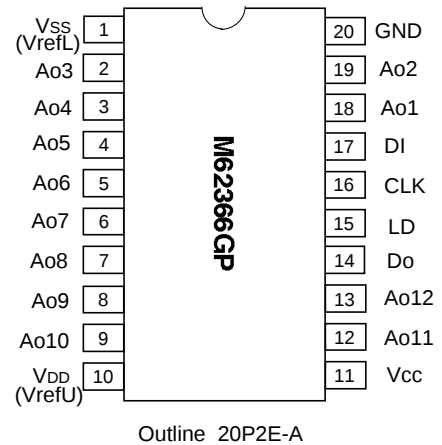
FEATURES

- Operable with a low voltage between 2.7~3.6V
- 12-bit serial data input (connected via 3 pins: DI, CLK, LD)
- 12 channels of R-2R and segment type high-performance 8-bit D-A converters
- 12 buffer operational amplifiers with full swing of output voltage between Vcc and GND.
- High oscillation stability against the capacitive load of buffer operational amplifiers.

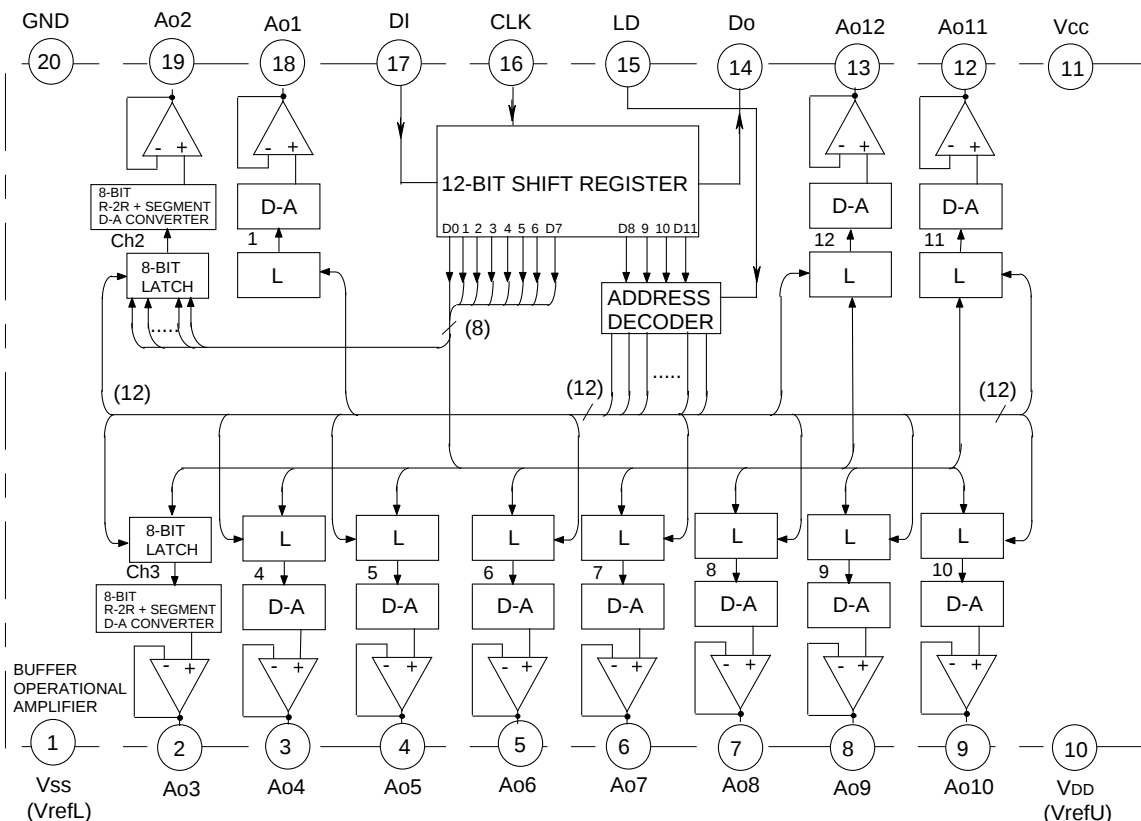
APPLICATION

Adjustment/control of industrial or home-use electric equipment, such as VTR camera, VTR set, TV, and CRT display.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



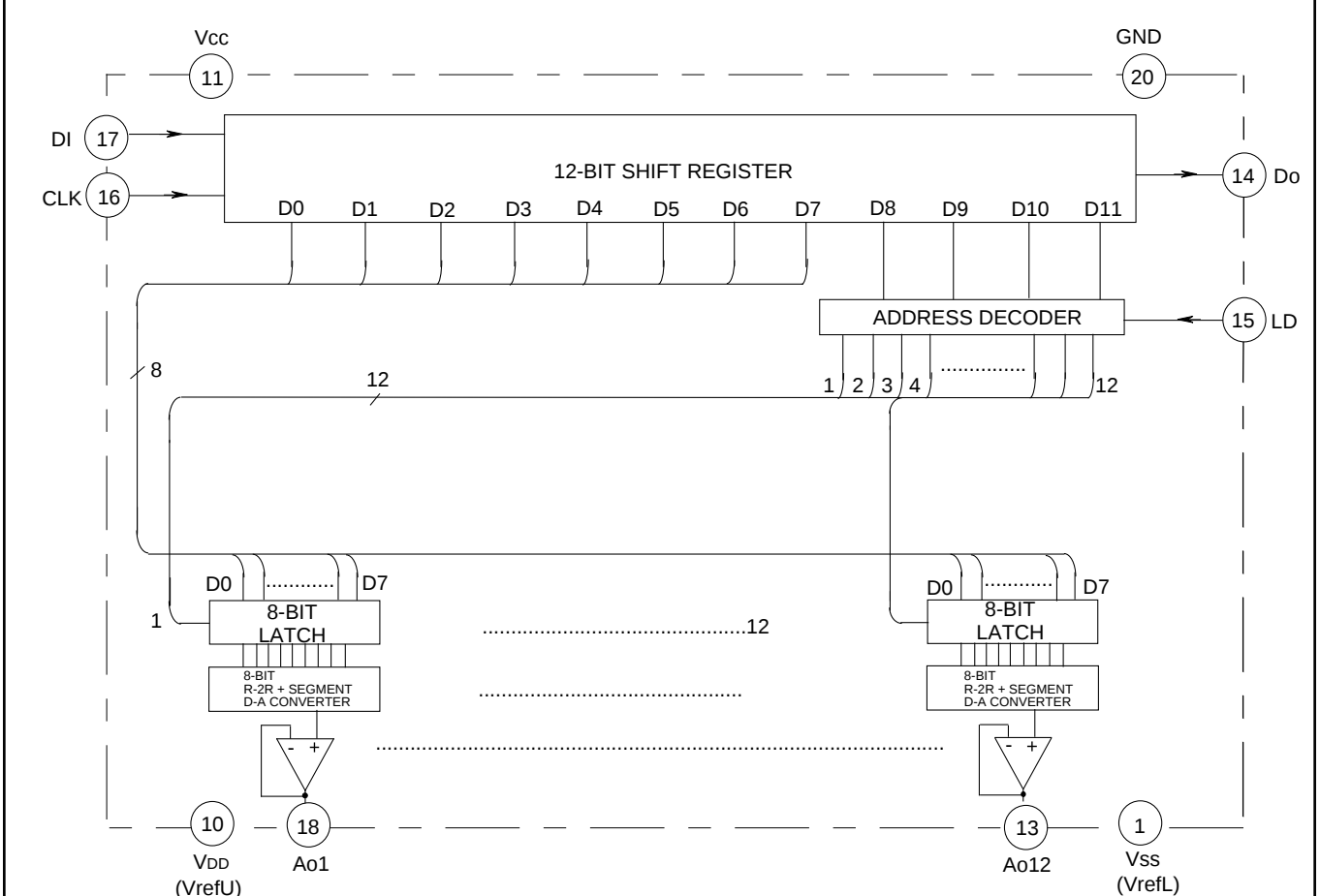
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EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
⑰	DI	Serial data input terminal to input 12-bit long serial data
⑭	Do	Terminal to output MSB data of 12-bit shift register
⑯	CLK	Shift clock input terminal. Input signal at DI pin is input to 12-bit shift register at rise of shift clock pulse
⑮	LD	When H-level signal is input to this terminal, the value stored in 12-bit shift register is loaded in decoder and D-A converter output register
⑱	Ao1	8-bit D-A converter output terminal
⑲	Ao2	
②	Ao3	
③	Ao4	
④	Ao5	
⑤	Ao6	
⑥	Ao7	
⑦	Ao8	
⑧	Ao9	
⑨	Ao10	
⑫	Ao11	
⑬	Ao12	
⑪	Vcc	Power supply terminal
⑳	GND	GND terminal
⑩	VDD	D-A converter upper reference voltage input terminal
①	VSS	D-A converter lower reference voltage input terminal

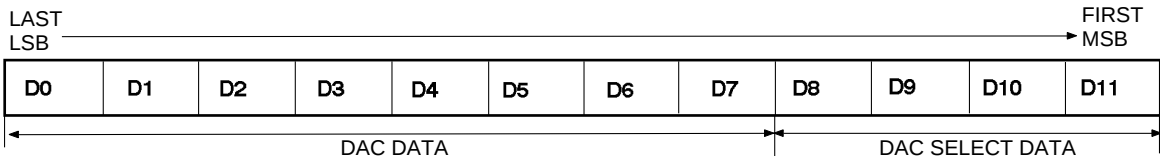
BLOCK DIAGRAM FOR EXPLANATION OF TERMINALS



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DIGITAL DATA FORMAT

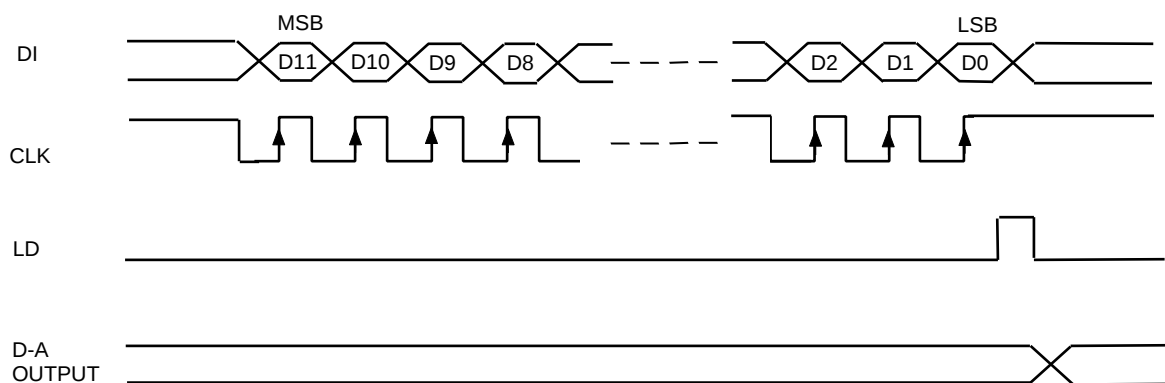


D0	D1	D2	D3	D4	D5	D6	D7	D-A output
0	0	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refU}-V_{refL}) / 256 \times 4 + V_{refL}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	$(V_{refU}-V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	V_{refU}

D8	D9	D10	D11	DAC selection
0	0	0	0	Don't care
0	0	0	1	Ao1 selection
0	0	1	0	Ao2
0	0	1	1	Ao3
0	1	0	0	Ao4
0	1	0	1	Ao5
0	1	1	0	Ao6
0	1	1	1	Ao7
1	0	0	0	Ao8
1	0	0	1	Ao9
1	0	1	0	Ao10
1	0	1	1	Ao11
1	1	0	0	Ao12
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

* $V_{refU}=V_{DD}$
 $V_{refL}=V_{SS}$

TIMING CHART (MODEL)



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3~+7.0	V
V _{DD}	Upper reference voltage of D-A converter		-0.3~+7.0	V
V _{IN}	Input voltage		-0.3-V _{CC} +0.3	V
V _O	Output voltage		-0.3-V _{CC} +0.3	V
P _d	Power dissipation		150	mW
T _{opr}	Operating temperature		-20~+85	°C
T _{stg}	Storage temperature		-55~+150	°C

ELECTRICAL CHARACTERISTICS

Digital part(V_{CC},V_{refU}=+3V±10%, V_{CC}≥V_{refU},GND,V_{refL}=0V,Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage		2.7	3.0	3.6	V
I _{CC}	Circuit current	CLK=1MHz operation,V _{CC} =3V,I _{AO} =0μA			3.5	mA
I _{ILK}	Input leak current	V _{IN} =0~V _{CC}	-10		10	μA
V _{IL}	Input low voltage				0.2V _{CC}	V
V _{IH}	Input high voltage		0.8V _{CC}			V
V _{OL}	Output low voltage	I _{OL} =2.5mA			0.4	V
V _{OH}	Output high voltage	I _{OH} =-400μA	V _{CC} -0.4			V

Note:The standard values are obtained at Ta=25°C

Analog part(V_{CC},V_{refU}=+3V±10%, V_{CC}≥V_{refU},Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{refU}	Current dissipation	V _{refU} =3V,V _{refL} =0V Data condition:maximum current		1.4	2.5	mA
V _{refU}	D-A converter upper reference voltage range	Reference voltage can not always be set to any value in this range,because it is restricted to the buffer amplifier output voltage range	0.7V _{CC}		V _{CC}	V
V _{refL}	D-A converter lower reference voltage range		GND		0.3V _{CC}	V
V _{AO}	Buffer amplifier output driver voltage range	I _{AO} =±100μA	0.1		V _{CC} -0.1	V
		I _{AO} =+500μA -200μA	0.2		V _{CC} -0.2	
I _{AO}	Buffer amplifier output voltage range	Upper saturation voltage=0.4V Lower saturation voltage=0.4V	-0.3		1	mA
SDL	Differential nonlinearity error	V _{CC} =2.760V	-1.0		1.0	LSB
SL	Nonlinearity error	V _{refU} =2.610V	-1.5		1.5	LSB
SZERO	Zero code error	V _{refL} =0.050V(10mV/LSB)	-2		2	LSB
SFULL	Full scale error	Without load(I _{AO} =±0)	-2		2	LSB
C _O	Output capacitive load				0.1	μF
R _O	Buffer amplifier output impedance			5		W

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AC CHARACTERISTICS($V_{CC}, V_{refU}=+5V\pm10\%$, $V_{CC}\geq V_{refU}, GND, V_{refL}=0V, T_a=-20\sim+85^{\circ}C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
tCKL	Clock "L" pulse width		200			ns
tCKH	Clock "H" pulse width		200			ns
tCR	Clock rise time				200	ns
tCF	Clock fall time				200	ns
tDCH	Data set up time		30			ns
tCHD	Data hold time		60			ns
tCHL	LD set up time		200			ns
tLDC	LD hold time		100			ns
tLDH	LD "H" pulse duration		100			ns
tDo	Data output delay time	$C_L=100pF$	70		350	ns
tLDD	D-A output setting time	$C_L\geq100pF, V_{AO}:0.1\rightarrow2.6V$ The time until the output becomes the final value of 1/2 LSB			300	μs

TIMING CHART

