8-BIT FM+ I²C BUS LED DRIVER

FEATURES

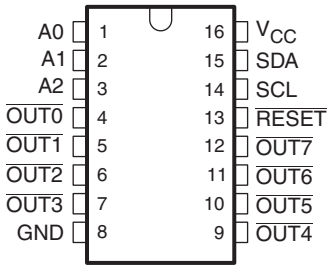
- Eight LED Drivers (Each Output Programmable at OFF, ON, Programmable LED Brightness, Programmable Group Dimming/Blinking Mixed With Individual LED Brightness)
- Eight Open-Drain Output Channels
- 256-Step (8-Bit) Linear Programmable Brightness Per LED Output Varying From Fully Off (Default) to Maximum Brightness Using a 97-kHz PWM Signal
- 256-Step Group Brightness Control Allows General Dimming [Using a 190-Hz PWM Signal From Fully Off to Maximum Brightness (Default)]
- 256-Step Group Blinking With Frequency Programmable From 24 Hz to 10.73 s and Duty Cycle From 0% to 99.6%
- 64 Programmable Slave Addresses Using Three Hardware Address Pins
- Four Software Programmable I²C Bus Addresses (One LED Group Call Address and Three LED Sub Call Addresses) Allow Groups of Devices to be Simultaneously Addressed Any Combination (For Example, One Register Used for 'All Call' so That All the TLC59208Fs on the I²C Bus Can be Simultaneously Addressed and the Second Register Used for Three Different Addresses so That One Third of All Devices on the Bus Can be Simultaneously Addressed)
- Software Enable and Disable for I²C Bus Address
- Software Reset Feature (SWRST Call) Allows the Device to be Reset Through the I²C Bus
- Up to 14 Possible Hardware Adjustable Individual I²C Bus Addresses Per Device so That Each Device Can be Programmed
- Up to 64 Possible Hardware Adjustable Individual I²C Bus Addresses Per Device so That Each Device Can be Programmed Individually
- Output State Change Programmable on the Acknowledge or the STOP Command to Update Outputs Byte-by-Byte or All at the Same Time (Default to 'Change on STOP')
- Maximum Output Current: 50 mA
- Maximum Output Voltage: 17 V
- 25-MHz Internal Oscillator Requires no External Components
- 1-MHz Fast-Mode Plus (FM+) Compatible I²C Bus Interface With 30 mA High Drive Capability on SDA Output for Driving High Capacitive Buses
- Internal Power-On Reset
- Noise Filter on SCL/SDA Inputs
- No Glitch on Power Up
- Active-Low Reset ($\overline{\text{RESET}}$)
- Supports Hot Insertion
- Low Standby Current
- 3.3-V or 5-V Supply Voltage
- 5.5-V Tolerant Inputs
- Packages Offered: 16-Pin Thin Shrink Small-Outline Package [TSSOP (PW)], 16-Pin Quad Flatpack No Lead [QFN (RGY)]
- –40°C to 85°C Operation

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

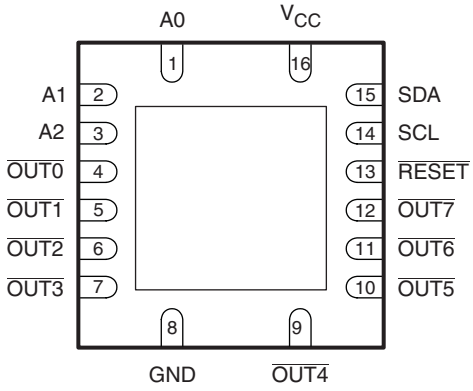
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PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



DESCRIPTION

The TLC59208F is an I^2C bus controlled 8-bit LED driver optimized for red/green/blue/amber (RGBA) color mixing applications. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 97 kHz with a duty cycle that is adjustable from 0% to 99.6% to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds with a duty cycle that is adjustable from 0% to 99.6% that is used to either dim or blink all LEDs with the same value.

Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The TLC59208F operates with a supply voltage range of 3 V to 5.5 V and the outputs are 17 V tolerant. LEDs can be directly connected to the TLC59208F device outputs.

Software programmable LED Group and three Sub Call I^2C bus addresses allow all or defined groups of TLC59208F devices to respond to a common I^2C bus address, allowing for example, all the same color LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I^2C bus commands.

Three hardware address pins allow up to 64 devices on the same bus (see Table 1).

The software reset (SWRST) Call allows the master to perform a reset of the TLC59208F through the I^2C bus, identical to the power-on reset (POR) that initializes the registers to their default state causing the outputs to be set high (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

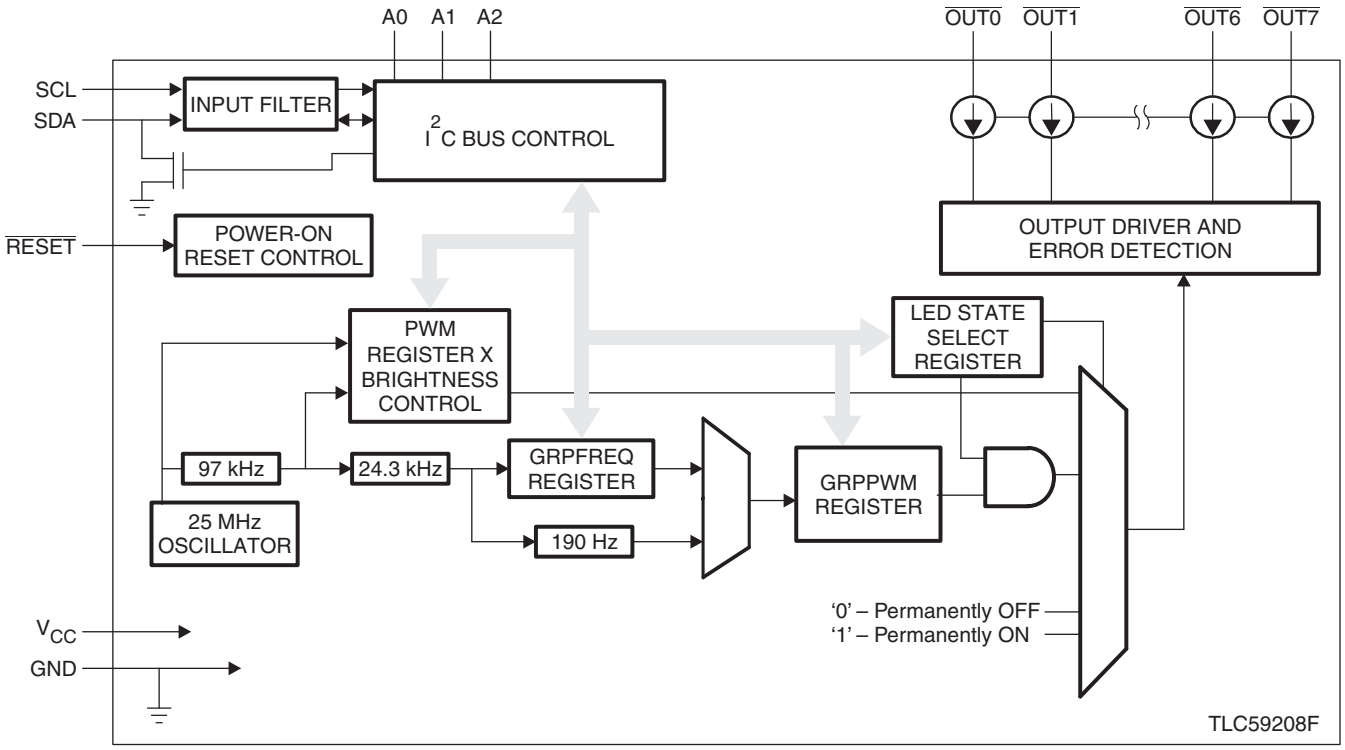
ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 2500	TLC59208FIRGYR	Y59208F
	TSSOP – PW	Reel of 2000	TLC59208FIPWR	Y59208F

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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BLOCK DIAGRAM



NOTE: Only one PWM shown for clarity.

TERMINAL FUNCTIONS

TERMINAL		I/O(1)	DESCRIPTION
NAME	NO.		
A0	1	I	Address input 0
A1	2	I	Address input 1
A2	3	I	Address input 2
$\overline{OUT0}$, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{OUT3}$, $\overline{OUT4}$, $\overline{OUT6}$, $\overline{OUT6}$, $\overline{OUT7}$	4, 5, 6, 7, 9, 10, 11, 12	O	Open-drain output 0 to 7, LED ON at low
GND	8	–	Ground
$\overline{RESET}$	13	I	Active-low reset input
SCL	14	I	Serial clock input
SDA	15	I/O	Serial data input/output
V_{CC}	16	–	Power supply

(1) I = input, O = output

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		0	7	V
V_I	Input voltage range		–0.4	7	V
V_O	Output voltage range		–0.5	20	V
I_O	Continuous output current			50	mA
θ_{JA}	Package thermal impedance	PW package(2)		108	°C/W
		RGY package(3)		39	
P_D	Power Dissipation, T_A = 25 °C, JESD 51-7	PW package		0.90	W
		RGY package		2.08	
T_J	Junction temperature range		–40	150	°C
T_{stg}	Storage temperature range		–55	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.
(3) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS(1)

		TEST CONDITIONS		MIN	MAX	UNIT
V_{CC}	Supply voltage			3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA, $\overline{RESET}$, A0, A1, A2		0.7 × V_{CC}	5.5	V
V_{IL}	Low-level input voltage	SCL, SDA, $\overline{RESET}$, A0, A1, A2		0	0.3 × V_{CC}	V
V_O	Output voltage	$\overline{OUT0}$ to $\overline{OUT7}$			17	V
I_{OL}	Low-level output current	SDA	V_{CC} = 3 V		20	mA
			V_{CC} = 4.5 V		30	
I_O	Output current	$\overline{OUT0}$ to $\overline{OUT7}$			50	mA
T_A	Operating free-air temperature			–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 3 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_I	Input/output leakage current	SCL, SDA, A0, A1, A2, $\overline{\text{RESET}}$	V_I = V_{CC} or GND			±0.3	µA
	Output leakage current	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$	V_O = 17 V, T_J = 25°C			0.5	µA
V_{POR}	Power-on reset voltage				2.5		V
I_{OL}	Low-level output current	SDA	V_{CC} = 3 V, V_{OL} = 0.4 V	20			mA
			V_{CC} = 4.5 V, V_{OL} = 0.4 V	30			
V_{OL}	Low-level output voltage	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$	V_{CC} = 3 V, I_{OL} = 50 mA		108	185	mV
			V_{CC} = 4.5 V, I_{OL} = 50 mA		90	165	
r_{ON}	ON-state resistance	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$	V_{CC} = 3 V, I_{OL} = 50 mA		2	3.75	Ω
			V_{CC} = 4.5 V, I_{OL} = 50 mA		1.8	3.3	
T_{SD}	Thermal shutdown temperature(2)			150	175	200	°C
T_{HYS}	Restart hysteresis				15		°C
C_i	Input capacitance	SCL, A0, A1, A2, $\overline{\text{RESET}}$	V_I = V_{CC} or GND		6		pF
C_{io}	Input/output capacitance	SDA	V_I = V_{CC} or GND		8		pF
I_{CC}	Supply current		V_{CC} = 3.3 V, $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ = OFF			5	mA
			V_{CC} = 5.5 V, $\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ = OFF			8	

(1) All typical values are at T_J = 25°C.
(2) Specified by design, not production tested.

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I²C INTERFACE TIMING REQUIREMENTS

T_A = –40°C to 85°C

		STANDARD-MODE I²C BUS		FAST-MODE I²C BUS		FAST-MODE PLUS I²C BUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I²C Interface								
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
t_{BUF}	I²C bus free time between stop and start	4.7		1.3		0.5		µs
$t_{HD;STA}$	Hold time (repeated) Start condition	4		0.6		0.26		µs
$t_{SU;STA}$	Set-up time for a repeated Start condition	4.7		0.6		0.26		µs
$t_{SU;STO}$	Set-up time for Stop condition	4		0.6		0.26		µs
$t_{HD;DAT}$	Data hold time	0		0		0		ns
$t_{VD;ACK}$	Data valid acknowledge time(1)	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{VD;DAT}$	Data valid time(2)	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{SU;DAT}$	Data set-up time	250		100		50		ns
t_{LOW}	Low period of the SCL clock	4.7		1.3		0.5		µs
t_{HIGH}	High period of the SCL clock	4		0.6		0.26		µs
t_f	Fall time of both SDA and SCL signals(3)(4)		300	20+0.1C_b(5)	300		120	ns
t_r	Rise time of both SDA and SCL signals		1000	20+0.1C_b(5)	300		120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter(6)		50		50		50	ns
Reset								
t_W	Reset pulse width	10		10		10		ns
t_{REC}	Reset recovery time	0		0		0		ns
t_{RESET}	Time to reset(7)(8)	400		400		400		ns

(1) $t_{VD;ACK}$ = time for Acknowledgement signal from SCL low to SDA (out) low.
(2) $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL low.
(3) A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the VIL of the SCL signal) in order to bridge the undefined region of SCLs falling edge.
(4) The maximum tf for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t_f) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
(5) C_b = total capacitance of one bus line in pF.
(6) Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns
(7) Resetting the device while actively communicating on the bus may cause glitches or errant Stop conditions.
(8) Upon reset, the full delay will be the sum of t_{RESET} and the RC time constant of the SDA bus.

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PARAMETER MEASUREMENT INFORMATION

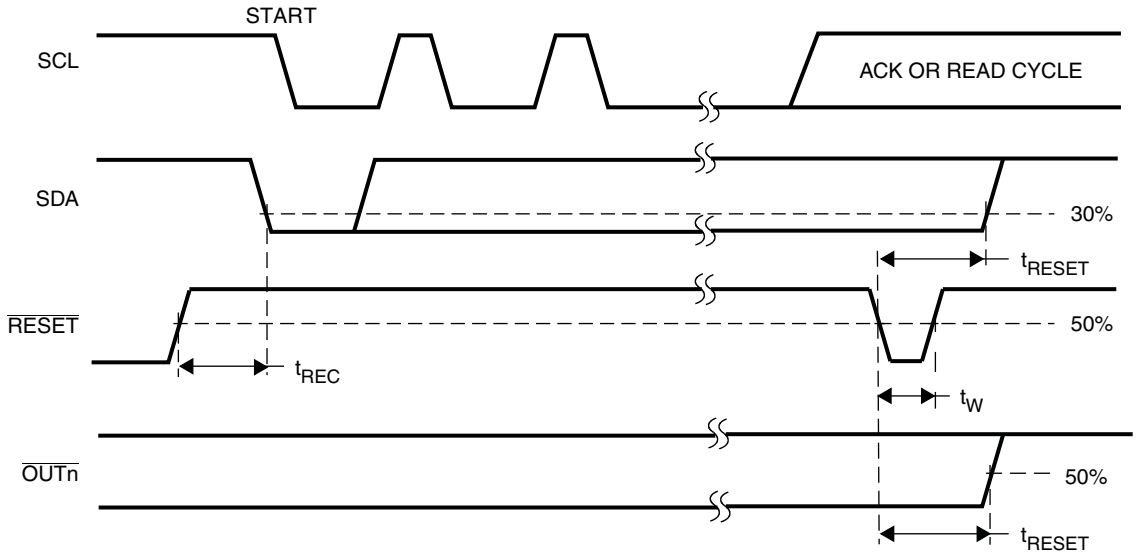


Figure 1. Definition of RESET Timing

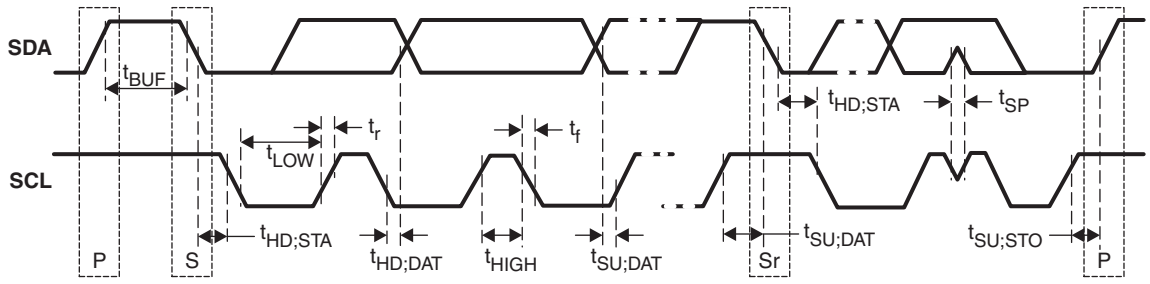
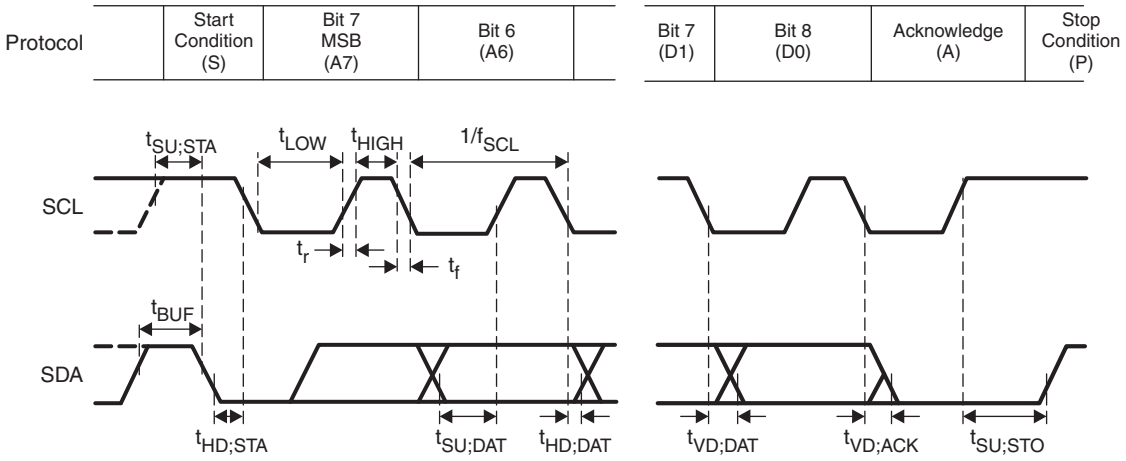


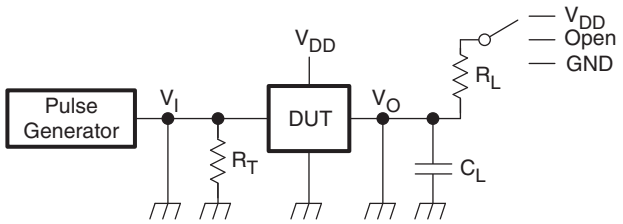
Figure 2. Definition of Timing



NOTE: Rise and fall times refer to V_{IL} and V_{IH}.

Figure 3. I²C Bus Timing

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: R_L = Load resistance for SDA and SCL; should be >1 kΩ at 3-mA or lower current.
C_L = Load capacitance; includes jig and probe capacitance.
R_T = Termination resistance; should be equal to the output impedance (Z_O) of the pulse generator.

Figure 4. Test Circuit for Switching Characteristics

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APPLICATION INFORMATION

Functional Description

Device Address

Following a Start condition, the bus master must output the address of the slave it is accessing.

Regular I^2C Bus Slave Address

The I^2C bus slave address of the TLC59208F is shown in Figure 5. Slave address pins A0, A1, and A2 choose 1 of 64 slave addresses. To conserve power, no internal pullup resistors are incorporated on A0, A1, or A2. Address values, depending on A0, A1, and A2, can be found in Table 1.

NOTE:

When using the TLC59208F, reserved I^2C bus addresses must be used with caution since they can interfere with the following:

- "Reserved for future use" I^2C bus addresses (0000 011, 1111 101, 1111 110, 1111 111)
- Slave devices that use the 10-bit addressing scheme (1111 0xx)
- High-speed mode master code (0000 1xx)

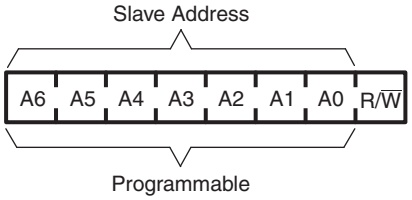


Figure 5. Slave Address

The last bit of the address byte defines the operation to be performed. When set to logic 1, a read operation is selected. When set to logic 0, a write operation is selected.

Regular I^2C Bus Slave Address

Table 1. TLC59208F Address Map

ADDRESS INPUT			SLAVE ADDRESS							
A2	A1	A0	A6	A5	A4	A3	A2	A1	A0	ADDRESS
GND	SCL	GND	0	0	1	0	0	0	0	20h
GND	SCL	V_{CC}	0	0	1	0	0	0	1	22h
GND	SDA	GND	0	0	1	0	0	1	0	24h
GND	SDA	V_{CC}	0	0	1	0	0	1	1	26h
V_{CC}	SCL	GND	0	0	1	0	1	0	0	28h
V_{CC}	SCL	V_{CC}	0	0	1	0	1	0	1	2Ah
V_{CC}	SDA	GND	0	0	1	0	1	1	0	2Ch
V_{CC}	SDA	V_{CC}	0	0	1	0	1	1	1	2Eh
GND	SCL	SCL	0	0	1	1	0	0	0	30h
GND	SCL	SDA	0	0	1	1	0	0	1	32h
GND	SDA	SCL	0	0	1	1	0	1	0	34h
GND	SDA	SDA	0	0	1	1	0	1	1	36h
V_{CC}	SCL	SCL	0	0	1	1	1	0	0	38h
V_{CC}	SCL	SDA	0	0	1	1	1	0	1	3Ah
V_{CC}	SDA	SCL	0	0	1	1	1	1	0	3Ch

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Table 1. TLC59208F Address Map (continued)

ADDRESS INPUT			SLAVE ADDRESS							
A2	A1	A0	A6	A5	A4	A3	A2	A1	A0	ADDRESS
V_{CC}	SDA	SDA	0	0	1	1	1	1	1	3Eh
GND	GND	GND	0	1	0	0	0	0	0	40h
GND	GND	V_{CC}	0	1	0	0	0	0	1	42h
GND	V_{CC}	GND	0	1	0	0	0	1	0	44h
GND	V_{CC}	V_{CC}	0	1	0	0	0	1	1	46h
V_{CC}	GND	GND	0	1	0	0	1	0	0	48h
V_{CC}	GND	V_{CC}	0	1	0	0	1	0	1	4Ah
V_{CC}	V_{CC}	GND	0	1	0	0	1	1	0	4Ch
V_{CC}	V_{CC}	V_{CC}	0	1	0	0	1	1	1	4Eh
GND	GND	SCL	0	1	0	1	0	0	0	50h
GND	GND	SDA	0	1	0	1	0	0	1	52h
GND	V_{CC}	SCL	0	1	0	1	0	1	0	54h
GND	V_{CC}	SDA	0	1	0	1	0	1	1	56h
V_{CC}	GND	SCL	0	1	0	1	1	0	0	58h
V_{CC}	GND	SDA	0	1	0	1	1	0	1	5Ah
V_{CC}	V_{CC}	SCL	0	1	0	1	1	1	0	5Ch
V_{CC}	V_{CC}	SDA	0	1	0	1	1	1	1	5Eh
SCL	SCL	GND	1	0	1	0	0	0	0	A0h
SCL	SCL	V_{CC}	1	0	1	0	0	0	1	A2h
SCL	SDA	GND	1	0	1	0	0	1	0	A4h
SCL	SDA	V_{CC}	1	0	1	0	0	1	1	A6h
SDA	SCL	GND	1	0	1	0	1	0	0	A8h
SDA	SCL	V_{CC}	1	0	1	0	1	0	1	AAh
SDA	SDA	GND	1	0	1	0	1	1	0	ACh
SDA	SDA	V_{CC}	1	0	1	0	1	1	1	AEh
SCL	SCL	SCL	1	0	1	1	0	0	0	B0h
SCL	SCL	SDA	1	0	1	1	0	0	1	B2h
SCL	SDA	SCL	1	0	1	1	0	1	0	B4h
SCL	SDA	SDA	1	0	1	1	0	1	1	B6h
SDA	SCL	SCL	1	0	1	1	1	0	0	B8h
SDA	SCL	SDA	1	0	1	1	1	0	1	BAh
SDA	SDA	SCL	1	0	1	1	1	1	0	BCh
SDA	SDA	SDA	1	0	1	1	1	1	1	BEh
SCL	GND	GND	1	1	0	0	0	0	0	C0h
SCL	GND	V_{CC}	1	1	0	0	0	0	1	C2h
SCL	V_{CC}	GND	1	1	0	0	0	1	0	C4h
SCL	V_{CC}	V_{CC}	1	1	0	0	0	1	1	C6h
SDA	GND	GND	1	1	0	0	1	0	0	C8h
SDA	GND	V_{CC}	1	1	0	0	1	0	1	CAh
SDA	V_{CC}	GND	1	1	0	0	1	1	0	CCh
SDA	V_{CC}	V_{CC}	1	1	0	0	1	1	1	CEh
SCL	GND	SCL	1	1	1	0	0	0	0	E0h
SCL	GND	SDA	1	1	1	0	0	0	1	E2h
SCL	V_{CC}	SCL	1	1	1	0	0	1	0	E4h
SCL	V_{CC}	SDA	1	1	1	0	0	1	1	E6h
SDA	GND	SCL	1	1	1	0	1	0	0	E8h

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Table 1. TLC59208F Address Map (continued)

ADDRESS INPUT			SLAVE ADDRESS							
A2	A1	A0	A6	A5	A4	A3	A2	A1	A0	ADDRESS
SDA	GND	SDA	1	1	1	0	1	0	1	EAh
SDA	V_{CC}	SCL	1	1	1	0	1	1	0	ECh
SDA	V_{CC}	SDA	1	1	1	0	1	1	1	EEh

LED All Call I²C Bus Address

- Default power-up value (ALLCALLADR address register): 90h or 1001 000
- Programmable through I²C bus (volatile programming)
- At power-up, LED All Call I²C bus address is enabled. TLC59208F sends an ACK when 90h (R/$\overline{W}$ = 0) or 91h (R/$\overline{W}$ = 1) is sent by the master.

NOTE:

The default LED All Call I²C bus address (90h or 1001 000) must not be used as a regular I²C bus slave address since this address is enabled at power-up. All the TLC59208Fs on the I²C bus will acknowledge the address if sent by the I²C bus master.

LED Sub Call I²C Bus Address

- Three different I²C bus addresses can be used
- Default power-up values:
  - SUBADR1 register: 92h or 1001 001
  - SUBADR2 register: 94h or 1001 010
  - SUBADR3 register: 98h or 1001 100
- Programmable through I²C bus (volatile programming)
- At power-up, Sub Call I²C bus address is disabled. TLC59208F does not send an ACK when 92h (R/$\overline{W}$ = 0) or 93h (R/$\overline{W}$ = 1) or 94h (R/$\overline{W}$ = 0) or 95h (R/$\overline{W}$ = 1) or 98h (R/$\overline{W}$ = 0) or 99h (R/$\overline{W}$ = 1) is sent by the master.

NOTE:

The default LED Sub Call I²C bus address may be used as a regular I²C bus slave address as long as the SUBADRx bits are disabled.

Software Reset I²C Bus Address

The address shown in Figure 6 is used when a reset of the TLC59208F needs to be performed by the master. The software reset address (SWRST Call) must be used with R/$\overline{W}$ = 0. If R/$\overline{W}$ = 1, the TLC59208F does not acknowledge the SWRST. See Software Reset for more detail.



Figure 6. Software Reset Address

NOTE:

The Software Reset I²C bus address is a reserved address and cannot be use as a regular I²C bus slave address or as an LED All Call or LED Sub Call address.

Control Register

Following the successful acknowledgement of the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the TLC59208F, which will be stored in the Control register. The lowest 5 bits are used as a pointer to determine which register will be accessed (D[4:0]). The highest 3 bits are used as Auto-Increment flag and Auto-Increment options (AI[2:0]).

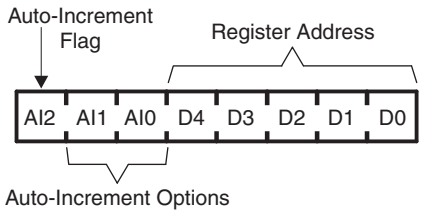


Figure 7. Control Register

When the Auto-Increment flag is set (AI2 = logic 1), the five low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values.

Table 2. Auto-Increment Options(1)

AI2	AI1	AI0	DESCRIPTION
0	0	0	No auto-increment
1	0	0	Auto-increment for all registers. D[4:0] roll over to '0 0000' after the last register ('1 0001') is accessed.
1	0	1	Auto-increment for individual brightness registers only. D[4:0] roll over to '0 0010' after the last register ('0 1001') is accessed.
1	1	0	Auto-increment for global control registers only. D[4:0] roll over to '0 1010' after the last register ('0 1011') is accessed.
1	1	1	Auto-increment for individual and global control registers only. D[4:0] roll over to '0 0010' after the last register ('0 1011') is accessed.

(1) Other combinations not shown in Table 2 (A1[2:0] = 001, 010, and 011) are reserved and must not be used for proper device operation.

AI[2:0] = 000 is used when the same register must be accessed several times during a single I^2C bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AI[2:0] = 100 is used when all the registers must be sequentially accessed, for example, power-up programming.

AI[2:0] = 101 is used when the four LED drivers must be individually programmed with different values during the same I^2C bus communication, for example, changing color setting to another color setting.

AI[2:0] = 110 is used when the LED drivers must be globally programmed with different settings during the same I^2C bus communication, for example, global brightness or blinking change.

AI[2:0] = 111 is used when individually and global changes must be performed during the same I^2C bus communication, for example, changing color and global brightness at the same time.

Only the 5 least significant bits D[4:0] are affected by the AI[2:0] bits.

When Control register is written, the register entry point determined by D[4:0] is the first register that will be addressed (read or write operation), and can be anywhere between 0 0000 and 1 0001 (as defined in LINKTOTABLE3). When AI[2] = 1, the Auto-Increment flag is set and the rollover value at which the point where the register increment stops and goes to the next one is determined by AI[2:0]. See for rollover values. For example, if the Control register = 1110 1100 (ECh), then the register addressing sequence will be (in hex):

04 →… → 11 → 02 →… → 11 → 02 →… → 11 as long as the master keeps sending or reading data.

Register Descriptions

Table 3 describes the registers in the TLC59208F.

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Table 3. Register Descriptions

REGISTER NUMBER (HEX)	NAME	ACCESS(1)	DESCRIPTION
00	MODE1	R/W	Mode register 1
01	MODE2	R/W	Mode register 2
02	PWM0	R/W	Brightness control LED0
03	PWM1	R/W	Brightness control LED1
04	PWM2	R/W	Brightness control LED2
05	PWM3	R/W	Brightness control LED3
06	PWM4	R/W	Brightness control LED4
07	PWM5	R/W	Brightness control LED5
08	PWM6	R/W	Brightness control LED6
09	PWM7	R/W	Brightness control LED7
0A	GRPPWM	R/W	Group duty cycle control
0B	GRPFREQ	R/W	Group frequency
0C	LEDOUT0	R/W	LED output state 0
0D	LEDOUT1	R/W	LED output state 1
0E	SUBADR1	R/W	I^2C bus sub-address 1
0F	SUBADR2	R/W	I^2C bus sub-address 2
10	SUBADR3	R/W	I^2C bus sub-address 3
11	ALLCALLADR	R/W	LED all call I^2C bus address

(1) R = read, W = write

Mode Register 1 (MODE1)

Table 4 describes Mode Register 1.

Table 4. MODE1 – Mode Register 1 (Address 00h) Bit Description

BIT	SYMBOL	ACCESS(1)	VALUE	DESCRIPTION
7	AI2	R	0(2)	Register auto-increment disabled
			1	Register auto-increment enabled
6	AI1	R	0(2)	Auto-increment bit 1 = 0
			1	Auto-increment bit 1 = 1
5	AI0	R	0(2)	Auto-increment bit 0 = 0
			1	Auto-increment bit 0 = 1
4	SLEEP	R/W	0	Normal mode(3)
			1(2)	Low power mode. Oscillator off(4).
3	SUB1	R/W	0(2)	Device does not respond to I^2C bus sub-address 1.
			1	Device responds to I^2C bus sub-address 1.
2	SUB2	R/W	0(2)	Device does not respond to I^2C bus sub-address 2.
			1	Device responds to I^2C bus sub-address 2.
1	SUB3	R/W	0(2)	Device does not respond to I^2C bus sub-address 3.
			1	Device responds to I^2C bus sub-address 3.
0	ALLCALL	R/W	0	Device does not respond to LED All Call I^2C bus address.
			1(2)	Device responds to LED All Call I^2C bus address.

(1) R = read, W = write
(2) Default value
(3) It takes 500 µs max. for the oscillator to be up and running once SLEEP bit has been set from logic 1 to 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM, or GRPFREQ registers are accessed within the 500 µs window.
(4) No LED control (on, off, blinking, or dimming) is possible when the oscillator is off. Write to a register cannot be accepted during SLEEP mode. When you change the LED condition, SLEEP bit must be set to logic 0.

Mode Register 2 (MODE2)

Table 5 describes Mode Register 2.

Table 5. MODE2 – Mode Register 2 (Address 01h) Bit Description

BIT	SYMBOL	ACCESS(1)	VALUE	DESCRIPTION
7:6		R	00(2)	Reserved
5	DMBLNK	R/W	0(3)	Group control = dimming
			1	Group control = blinking
4		R	0(2)	Reserved
3	OCH	R/W	0(2)	Outputs change on Stop command(4).
			1	Outputs change on ACK.
2	WDT ENABLE	R/W	0(2)	Disable WDT
			1	Enable WDT
1:0	WDT PERIOD	R/W	00	5 ms
			01	15 ms
			10	25 ms
			11(2)	35 ms

(1) R = read, W = write
(2) Default value
(3) Default value
(4) Change of the outputs at the STOP command allows synchronizing outputs of more than one TLC59208F. Applicable to registers from 02h (PWM0) to 0Dh (LEDOUT) only.

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Individual Brightness Control Registers (PWM0–PWM7)

Table 6 describes the Individual Brightness Control Registers.

Table 6. PWM0–PWM7 – Individual Brightness Control Registers (Addresses 02h–09h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS(1)	VALUE	DESCRIPTION
02h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000(2)	PWM0 individual duty cycle
03h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000(2)	PWM1 individual duty cycle
04h	PWM2	7:0	IDC2[7:0]	R/W	0000 0000(2)	PWM2 individual duty cycle
05h	PWM3	7:0	IDC3[7:0]	R/W	0000 0000(2)	PWM3 individual duty cycle
06h	PWM4	7:0	IDC4[7:0]	R/W	0000 0000(2)	PWM4 individual duty cycle
07h	PWM5	7:0	IDC5[7:0]	R/W	0000 0000(2)	PWM5 individual duty cycle
08h	PWM6	7:0	IDC6[7:0]	R/W	0000 0000(2)	PWM6 individual duty cycle
09h	PWM7	7:0	IDC7[7:0]	R/W	0000 0000(2)	PWM7 individual duty cycle

(1) R = read, W = write
(2) Default value

A 97-kHz fixed-frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = LED output at maximum brightness). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 and LEDOUT1 registers).

$$\text{duty cycle} = \frac{\text{IDCx[7:0]}}{256}$$

Group Duty Cycle Control Register (GRPPWM)

Table 7 describes the Group Duty Cycle Control Register .

Table 7. GRPPWM – Group Duty Cycle Control Register (Address 0Ah) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS(1)	VALUE	DESCRIPTION
0Ah	GRPPWM	7:0	GDC0[7:0]	R/W	1111 1111(2)	GRPPWM register

(1) R = read, W = write
(2) Default value

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 190 Hz fixed frequency signal is superimposed with the 97 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a ‘Don’t care’.

General brightness for the 8 outputs is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 and LEDOUT1 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 24 Hz to 10.73 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$\text{duty cycle} = \frac{\text{GDC[7:0]}}{256}$$

Group Frequency Register (GRPFREQ)

Table 7 describes the Group Frequency Register.

Table 8. GRPFREQ – Group Frequency Register (Address 0Bh) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS(1)	VALUE	DESCRIPTION
0Bh	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000(2)	GRPFREQ register

(1) R = read, W = write
(2) Default value

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GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a 'Don't care' when DMBLNK = 0. Applicable to LED output programmed with LDRx = 11 (LEDOUT0 and LEDOUT1 registers).

Blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 s).

$$\text{globalblinkingperiod} = \frac{\text{GFRQ[7:0]} + 1}{24}(\text{s})$$

LED Driver Output State Registers (LEDOUT0, LEDOUT1)

Table 9 describes the LED Driver Output State Registers.

Table 9. LEDOUT0 and LEDOUT1 – LED Driver Output State Registers (Address 0Ch and 0Dh) Bit Descriptions

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS(1)	VALUE	DESCRIPTION
0Ch	LEDOUT0	7:6	LDR3[1:0]	R/W	00(2)	LED3 output state control
		5:4	LDR2[1:0]		00(2)	LED2 output state control
		3:2	LDR1[1:0]		00(2)	LED1 output state control
		1:0	LDR0[1:0]		00(2)	LED0 output state control
0Dh	LEDOUT1	7:6	LDR7[1:0]	R/W	00(2)	LED7 output state control
		5:4	LDR6[1:0]		00(2)	LED6 output state control
		3:2	LDR4[1:0]		00(2)	LED5 output state control
		1:0	LDR4[1:0]		00(2)	LED4 output state control

(1) R = read, W = write
(2) Default value

LDRx = 00 : LED driver x is off (default power-up state).

LDRx = 01 : LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10 : LED driver x is individual brightness can be controlled through its PWMx register.

LDRx = 11 : LED driver x is individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

I^2C Bus Sub-Address Registers 1 to 3 (SUBADR1–SUBADR3)

Table 10 describes the Output Gain Control Register.

Table 10. SUBADR1–SUBADR3 – I^2C Bus Sub-Address Registers 1 to 3 (Addresses 0Eh–10h) Bit Descriptions

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS(1)	VALUE	DESCRIPTION
0Eh	SUBADR1	7:1	A1[7:1]	R/W	1001 001(2)	I^2C bus sub-address 1
		0	A1[0]	R	0(2)	Reserved
0Fh	SUBADR2	7:1	A2[7:1]	R/W	1001 010(2)	I^2C bus sub-address 2
		0	A2[0]	R	0(2)	Reserved
10h	SUBADR3	7:1	A3[7:1]	R/W	1001 100(2)	I^2C bus sub-address 3
		0	A3[0]	R	0(2)	Reserved

(1) R = read, W = write
(2) Default value

Sub-addresses are programmable through the I^2C bus. Default power-up values are 92h, 94h, 98h and the device(s) will not acknowledge these addresses right after power-up (the corresponding SUBx bit in MODE1 register is equal to 0).

Once sub-addresses have been programmed to their right values, SUBx bits need to be set to 1 in order to have the device acknowledging these addresses (MODE1 register).

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Only the 7 MSBs representing the I^2C bus sub-address are valid. The LSB in SUBADRx register is a read-only bit (0).

When SUBx is set to 1, the corresponding I^2C bus sub-address can be used during either an I^2C bus read or write sequence.

LED All Call I^2C Bus Address Register (ALLCALLADR)

Table 11 describes the LED All Call I^2C Bus Address Register.

Table 11. ALLCALLADR – LED All Call I^2C Bus Address Register Addresses 11h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS(1)	VALUE	DESCRIPTION
11h	ALLCALLADR	7:1	AC[7:1]	R/W	1101 000(2)	ALLCALL I^2C bus address
		0	AC[0]	R	0(2)	Reserved

(1) R = read, W = write
(2) Default value

The LED All Call I^2C bus address allows all the TLC59208Fs in the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to 1 (power-up default state)). This address is programmable through the I^2C-bus and can be used during either an I^2C bus read or write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I^2C bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0, the device does not acknowledge the address programmed in register ALLCALLADR.

Power-On Reset

When power is applied to V_{CC}, an internal power-on reset holds the TLC59208F in a reset condition until V_{CC} has reached V_{POR}. At this point, the reset condition is released and the TLC59208F registers and I^2C bus state machine are initialized to their default states causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below 0.2 V to reset the device.

External Reset

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of tW. The TLC59208F registers and I^2C state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again high.

This input requires a pull-up resistor to V_{CC} if no active connection is used.

Software Reset

The Software Reset Call (SWRST Call) allows all the devices in the I^2C bus to be reset to the power-up state value through a specific I^2C bus command. To be performed correctly, the I^2C bus must be functional and there must be no device hanging the bus.

The SWRST Call function is defined as the following:

1. A Start command is sent by the I^2C bus master.
2. The reserved SWRST I^2C bus address 1001 111 with the R/$\overline{W}$ bit set to 0 (write) is sent by the I^2C bus master.
3. The TLC59208F device(s) acknowledge(s) after seeing the SWRST Call address 1001 0110 (9Eh) only. If the R/$\overline{W}$ bit is set to 1 (read), no acknowledge is returned to the I^2C bus master.
4. Once the SWRST Call address has been sent and acknowledged, the master sends two bytes with two specific values (SWRST data byte 1 and byte 2):
   a. Byte1 = A5h: the TLC59208F acknowledges this value only. If byte 1 is not equal to A5h, the TLC59208F does not acknowledge it.
   b. Byte 2 = 5Ah: the TLC59208F acknowledges this value only. If byte 2 is not equal to 5Ah, the TLC59208F does not acknowledge it.

   If more than two bytes of data are sent, the TLC59208F does not acknowledge any more.

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5. Once the correct two bytes (SWRST data byte 1 and byte 2 only) have been sent and correctly acknowledged, the master sends a Stop command to end the SWRST Call. The TLC59208F then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

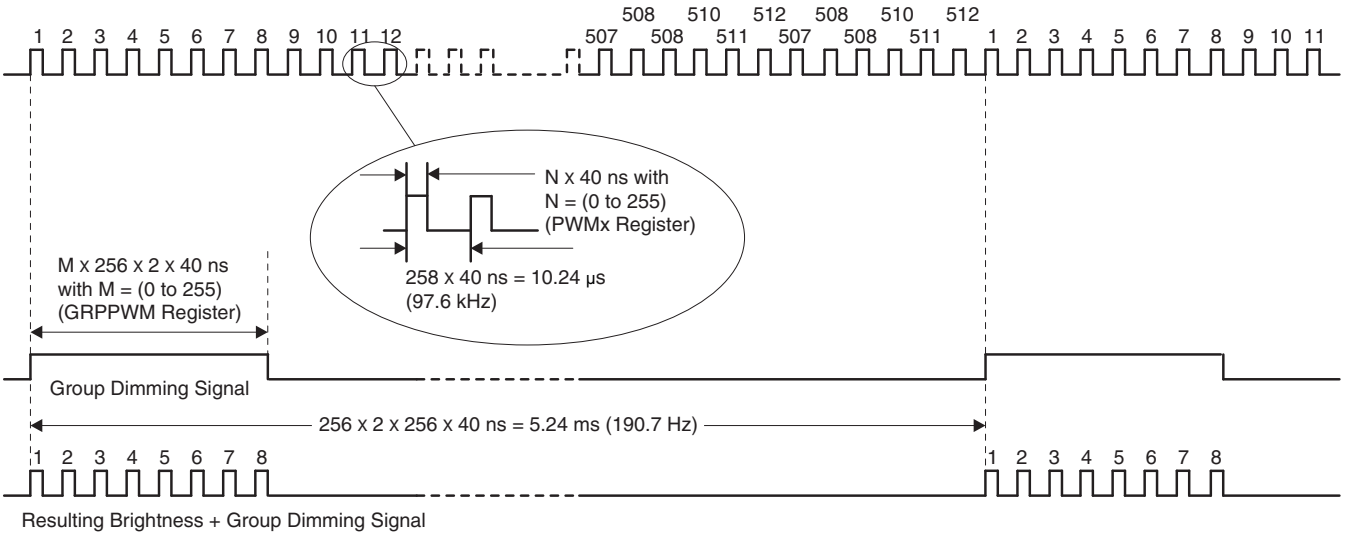
The I^2C bus master may interpret a non-acknowledge from the TLC59208F (at any time) as a SWRST Call Abort. The TLC59208F does not initiate a reset of its registers. This happens only when the format of the Start Call sequence is not correct.

Individual Brightness Control With Group Dimming/Blinking

A 97 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 4 LED outputs):

- A lower 190 Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 24 Hz to 1/10.73 s (8 bits, 256 steps) is used to provide a global blinking control.



A. Minimum pulse width for LEDn brightness control is 40 ns.

B. Minimum pulse width for group dimming is 20.48 µs.

C. When M = 1 (GRPPWM register value), the resulting LEDn brightness control and group dimming signal will have two pulses of the LED brightness control signal (pulse width = N × 40 ns,w ith N defined in the PWMx register).

D. The resulting brightness plus group dimming signal shown above demonstrate a resulting control signal with M = 4 (8 pulses).

Figure 8. Brightness + Group Dimming Signals

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Characteristics of the I²C Bus

The I²C bus is for two-way two-line communication between different devices or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 9).

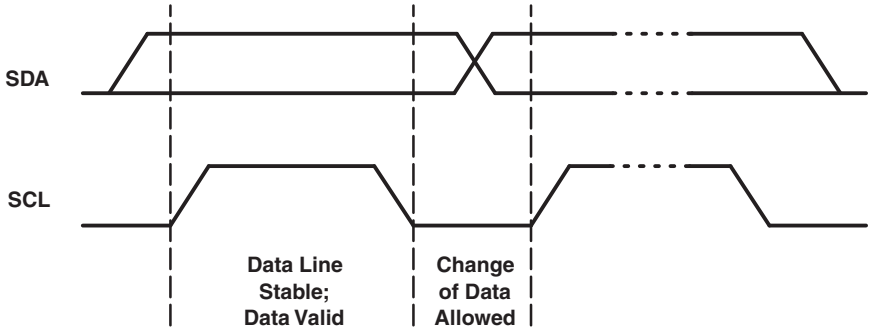


Figure 9. Bit Transfer

Start and Stop Conditions

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the Start condition (S). A low-to-high transition of the data line while the clock is high is defined as the Stop condition (P) (see Figure 10).

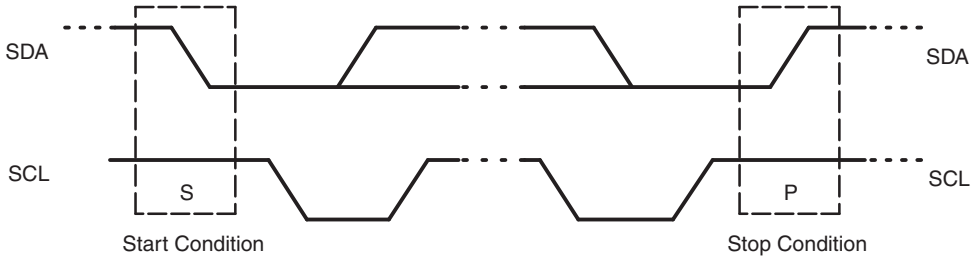


Figure 10. Start and Stop Conditions

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System Configuration

A device generating a message is a transmitter; a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 11).

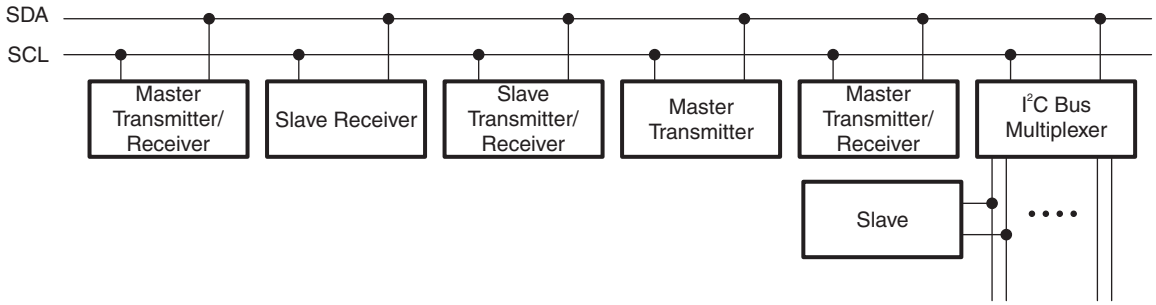


Figure 11. System Configuration

Acknowledge

The number of data bytes transferred between the Start and the Stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a high level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line high to enable the master to generate a Stop condition.

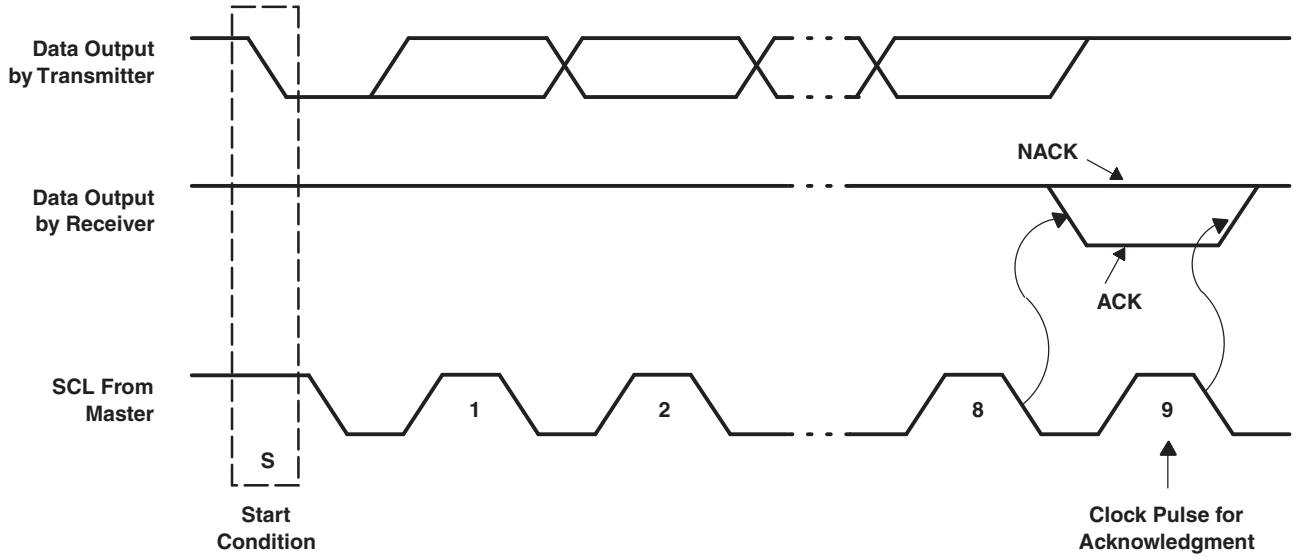


Figure 12. Acknowledge on I²C Bus

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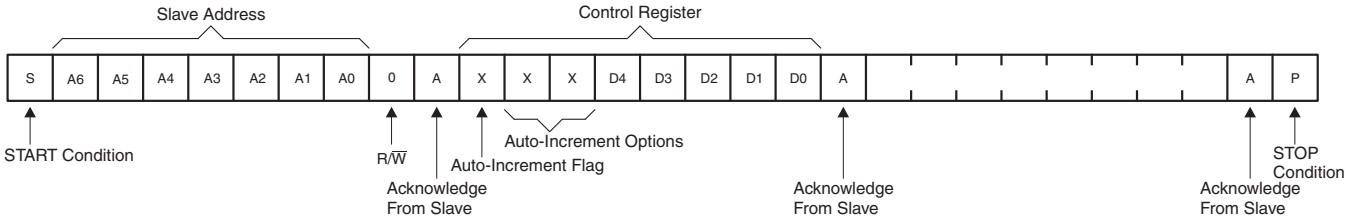


Figure 13. Write to a Specific Register

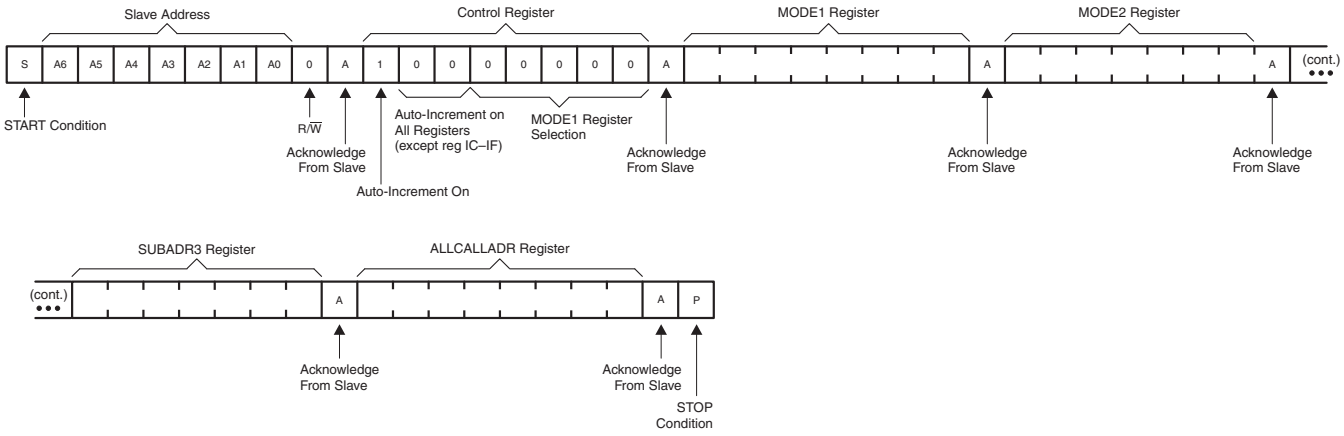


Figure 14. Write to All Registers Using Auto-Increment

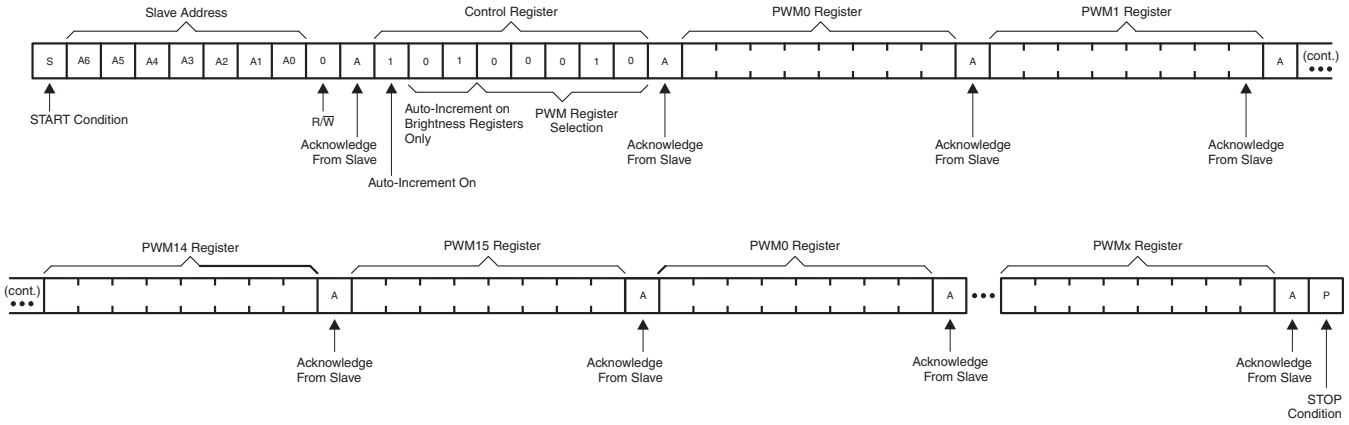


Figure 15. Multiple Writes to Individual Brightness Registers Only Using the Auto-Increment Feature

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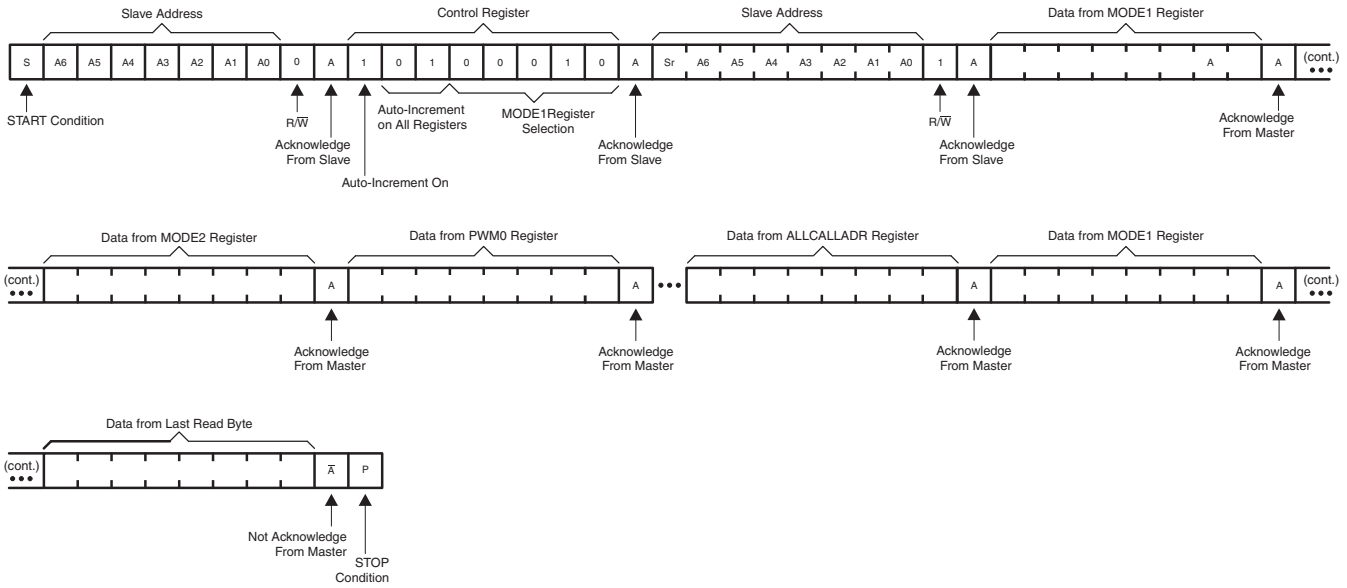
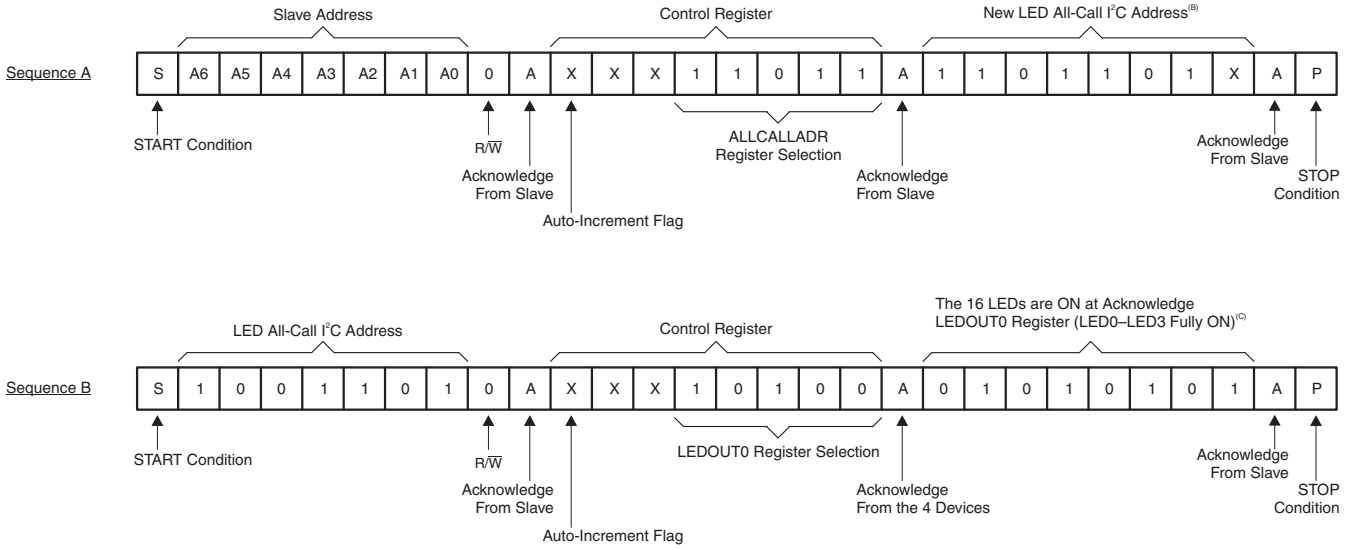


Figure 16. Read All Registers With the Auto-Increment Feature



A. In this example, several TLC59208Fs are used with the same sequence sent to each.

B. ALLCALL bit in MODE1 register is equal to 1 for this example.

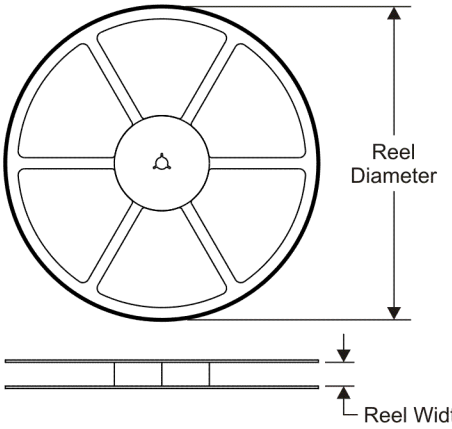
C. OCH bit in MODE2 register is equal to 1 for this example.

Figure 17. LED All-Call I²C Bus Address Programming and LED All-Call Sequence Example

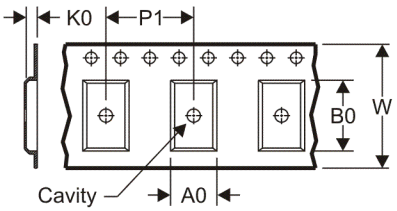
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

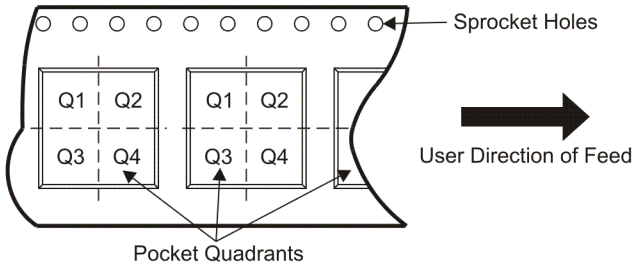


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

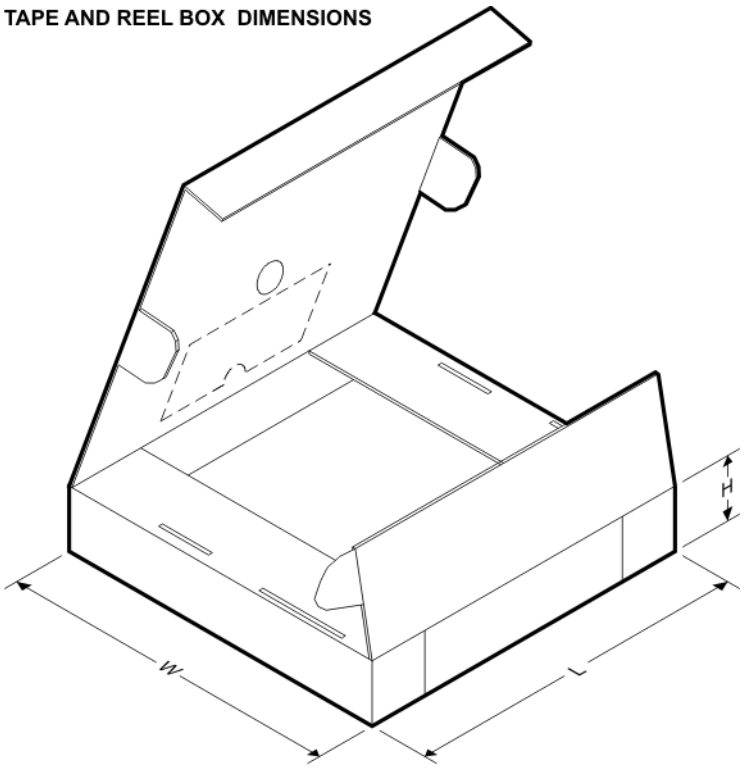
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59208FIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC59208FIRGYR	VQFN	RGY	16	2500	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

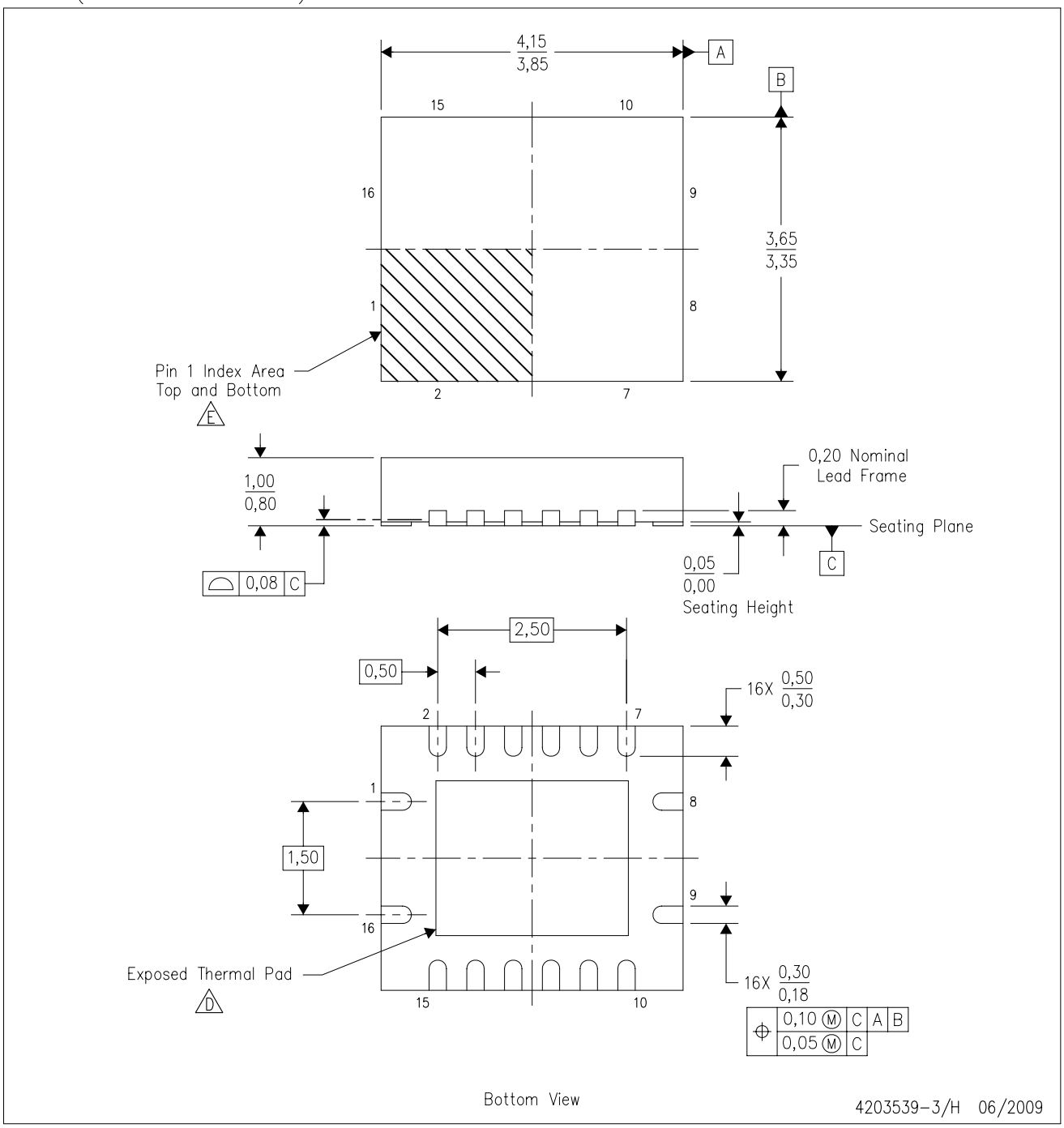
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59208FIPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
TLC59208FIRGYR	VQFN	RGY	16	2500	346.0	346.0	29.0

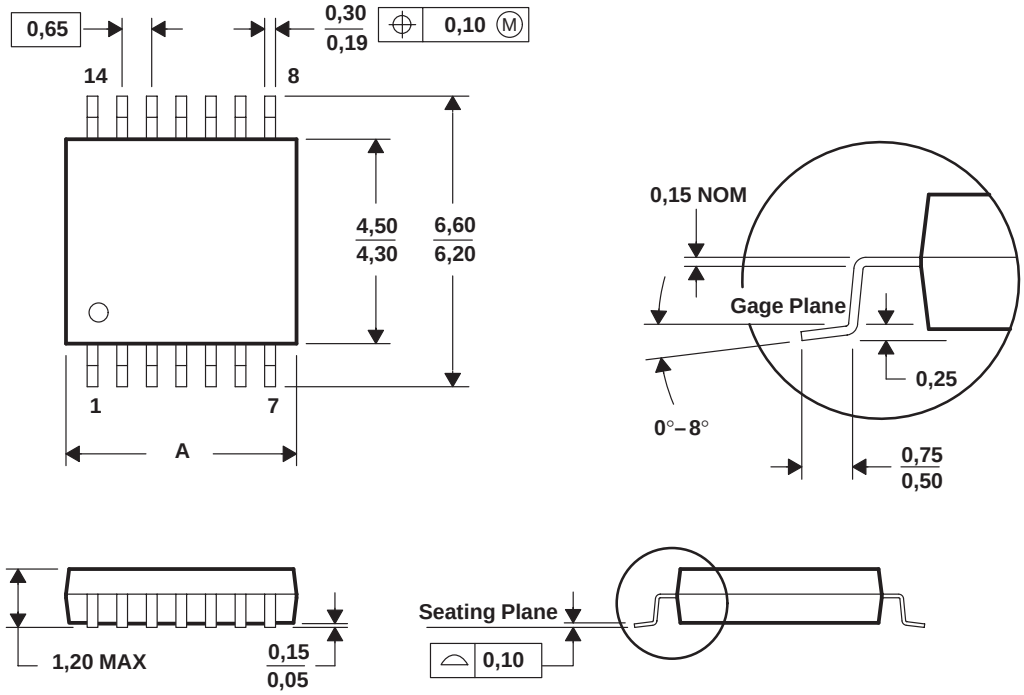
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BB.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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