FLU17ZM

L-Band Medium & High Power GaAs FET

FEATURES

- High Output Power: P1dB=32.5dBm(typ.)
- High Gain: G1dB=12.5dB(typ.)
- Low Cost Plastic(SMT) Package
- Tape and Reel Available



DESCRIPTION

The FLU17ZM is a GaAs FET designed for base station and CPE applications. This is a new product series using a plastic surface mount package that has been optimized for high volume cost driven applications. Fujitsu's stringent Quality Assurance Program assures the highest reliability and consistent performance.

ABSOLUTE MAXIMUM RATINGS (Case Temperature Tc=25℃)

Item	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	15	V
Gate-Soutce Voltage	V_{GS}	-5	V
Total Power Dissipation	P_T	8.3	W
Storage Temperature	T_{stg}	-55 to +150	℃
Channel Temperature	T_{ch}	150	℃

Recommended Operating Condition (Case Temperature Tc=25℃)

Item	Symbol	Condition	Unit
DC Input Voltage	V_{DS}	≤ 10	V
Channel Temperature	T_{ch}	≤ 145	℃
Forward Gate Current	I_{gsf}	≤ 9..6	mA
Reverse Gate Current	I_{gsr}	≥-1.0	mA
Gate Resistance	R_g	200	Ω

ELECTRICAL CHARACTERISTICS (Case Temperature Tc=25℃)

Item	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Drain Current	I_{DSS}	V_{DS}=5V, V_{GS}=0V	-	600	900	mA
Transconductance	gm	V_{DS}=5V, I_{DS}=400mA	-	300	-	mS
Pinch-off Voltage	V_p	V_{DS}=5V, I_{DS}=30mA	-1.0	-2.0	-3.5	V
Gate-Source Breakdown Voltage	V_{GSO}	I_{GS}=-30uA	-5	-	-	V
Output Power at 1dB G.C.P.	P_{1dB}	V_{DS}=10V, f=2.0GHz, I_{DS}=0.6I_{DSS}(Typ.)	31.5	32.5	-	dBm
Power Gain at 1dB G.C.P.	G_{1dB}		11.5	12.5	-	dB
Thermal Resistance	R_{th}	Channel to Case	-	12	15	℃/W

CASE STYLE: ZM

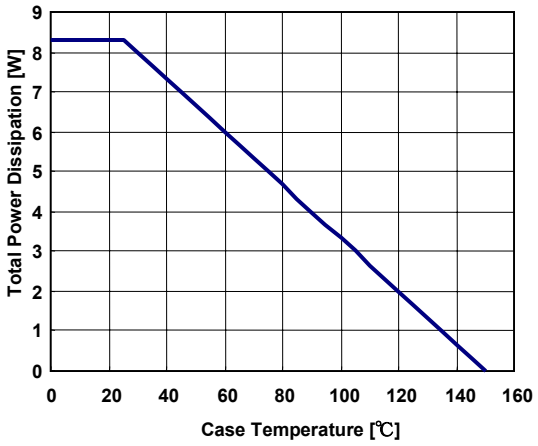
G.C.P.:Gain Compression Point

Note 1: Product supplied to this specification are 100% DC performance tested.
Note 2: The RF parameters are measured on a lot basis by sample testing 10 pcs/lot.
Acceptance Criteria:(accept/reject)=(0/1). Any lot failure shall be 100% retested.

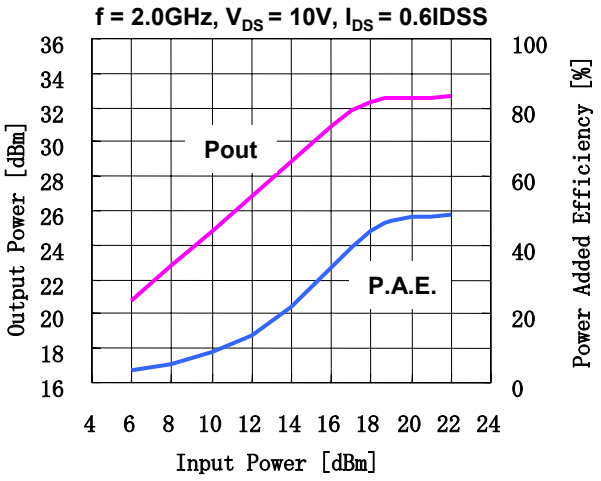
ESD	Class Ⅱ	500 ～ 1999 V

Note : Based on EIAJ ED-4701 C-111A (C=100pF,R=1.5kΩ)

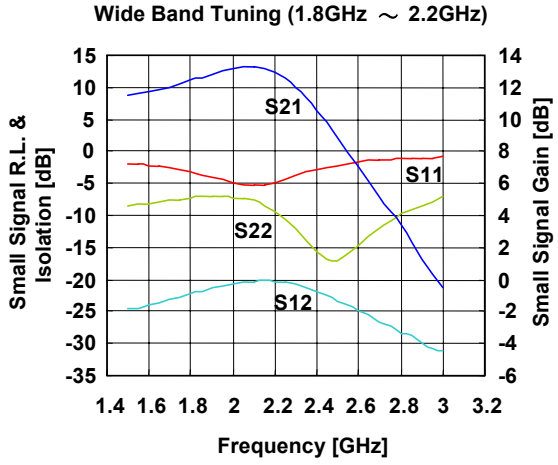
POWER DERATING CURVE



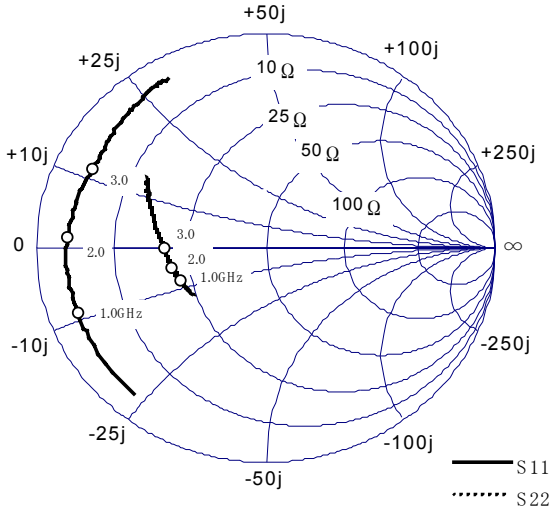
OUTPUT POWER & POWER ADDED EFFICIENCY vs. INPUT POWER

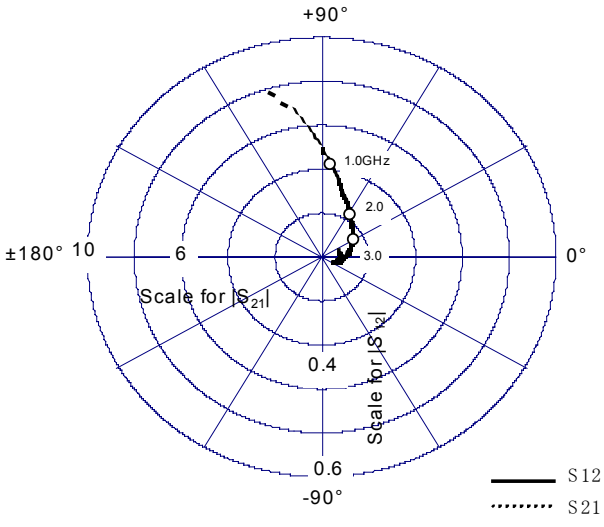


SMALL SINGLE R.L. vs FREQUENCY



■ S-PARAMETER



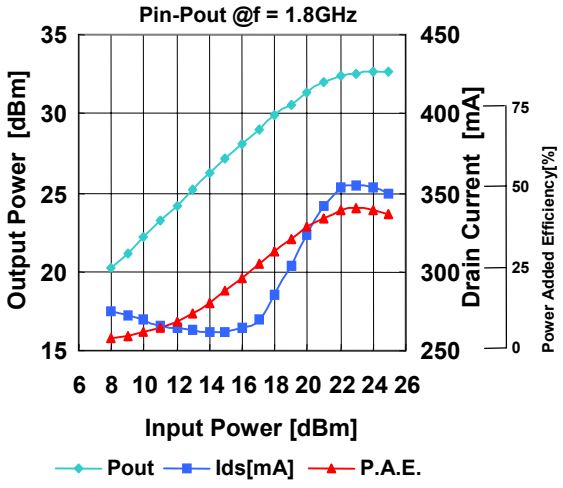


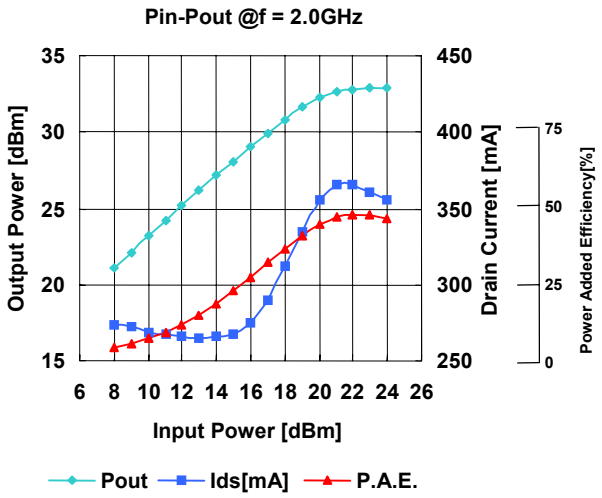
V_{DS} = 10V, I_{DS} = 360mA

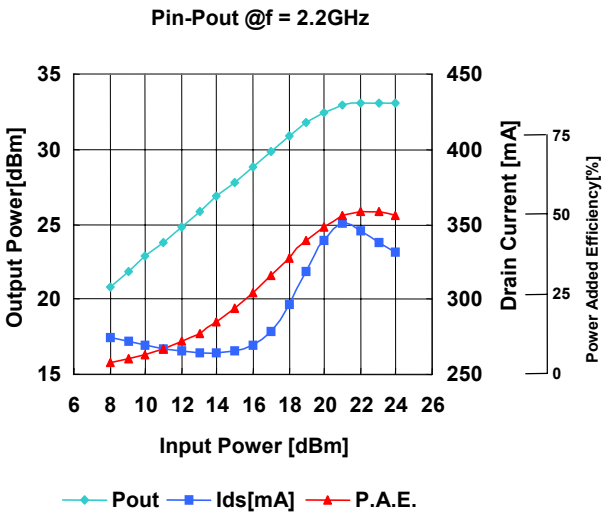
Freq	S11		S21		S12		S22	
[GHz]	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
0.5	0.89	-130.40	7.82	106.20	0.05	22.81	0.38	-144.06
1	0.87	-159.47	4.26	84.91	0.05	10.25	0.40	-157.62
1.5	0.87	-172.30	2.95	71.11	0.05	3.23	0.41	-162.28
2	0.87	176.73	2.31	58.41	0.05	-2.81	0.42	-166.91
2.5	0.85	166.01	1.89	45.71	0.05	-10.38	0.43	-172.98
3	0.84	153.61	1.58	31.88	0.04	-11.34	0.44	179.73
3.5	0.85	142.11	1.33	18.68	0.04	-15.81	0.48	170.94
4	0.87	131.82	1.12	5.71	0.04	-20.61	0.52	162.31
4.5	0.89	124.40	0.94	-5.77	0.04	-22.32	0.57	154.52
5	0.90	118.39	0.79	-16.59	0.03	-26.62	0.61	147.78

OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER

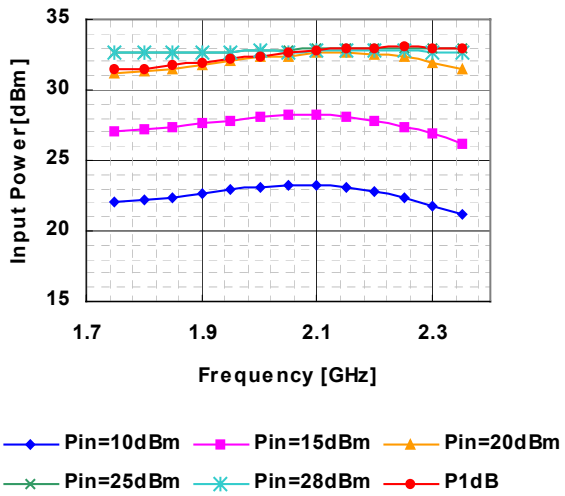
@ V_{DS} = 10V, I_{DS} = 0.6IDSS





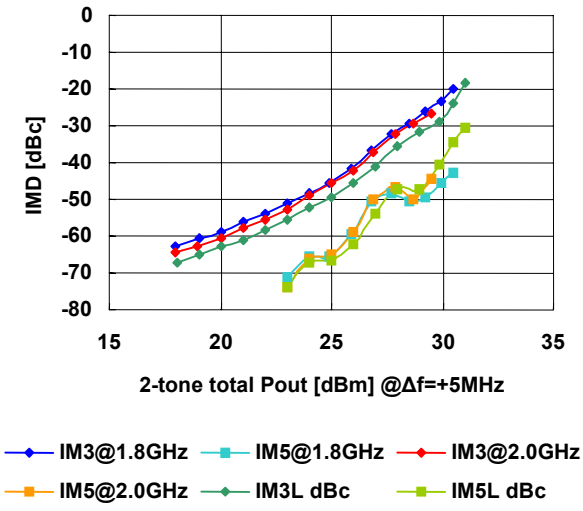


OUTPUT POWER vs. FREQUENCY

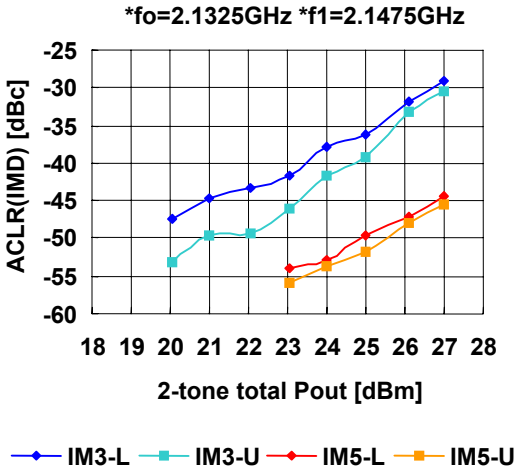


@ V_{DS} = 10V, I_{DS} = 0.6IDSS

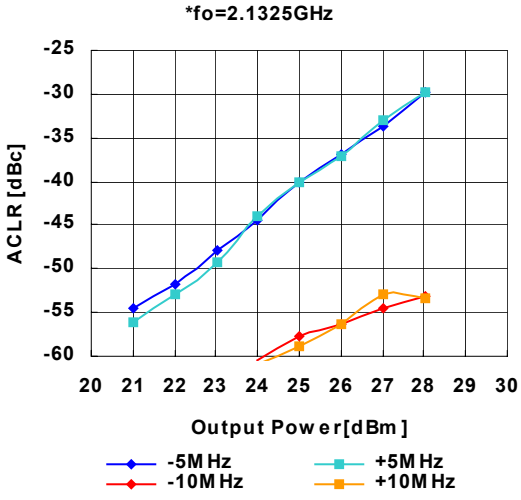
IMD vs OUTPUT POWER(2-tone)



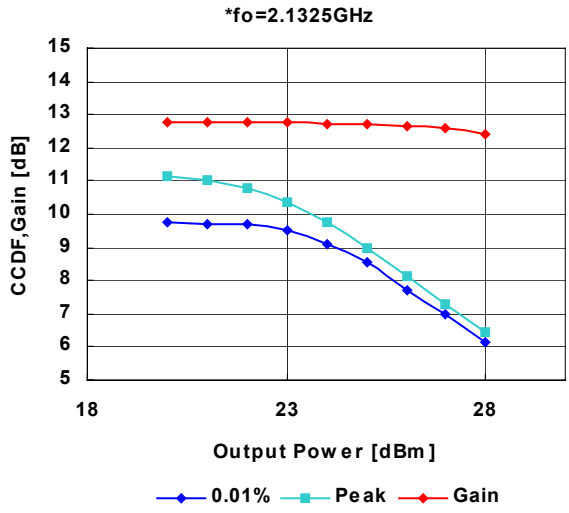
W-CDMA, 2-CARRIER IMD(ACLR)



W-CDMA SINGLE CARRIER ACLR

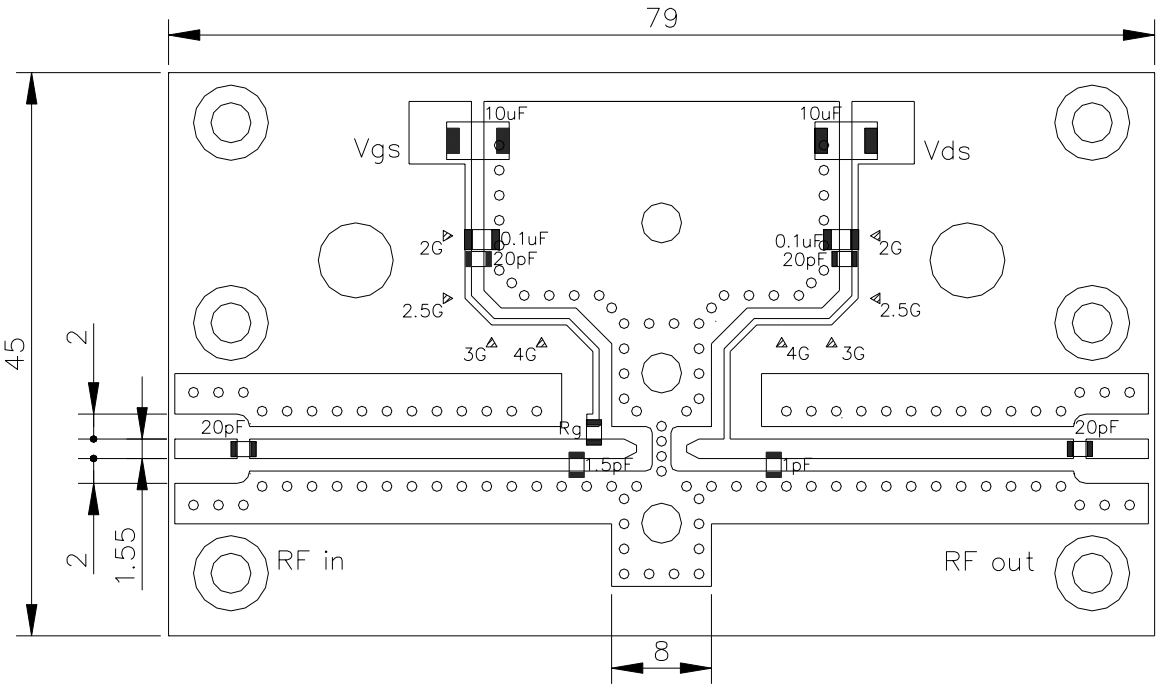


W-CDMA SINGLE CARRIER CCDF AND GAIN



Note : *All signals are W-CDMA modulated at 3GPP3.4.12-00 BS-1 64ch non clipping.

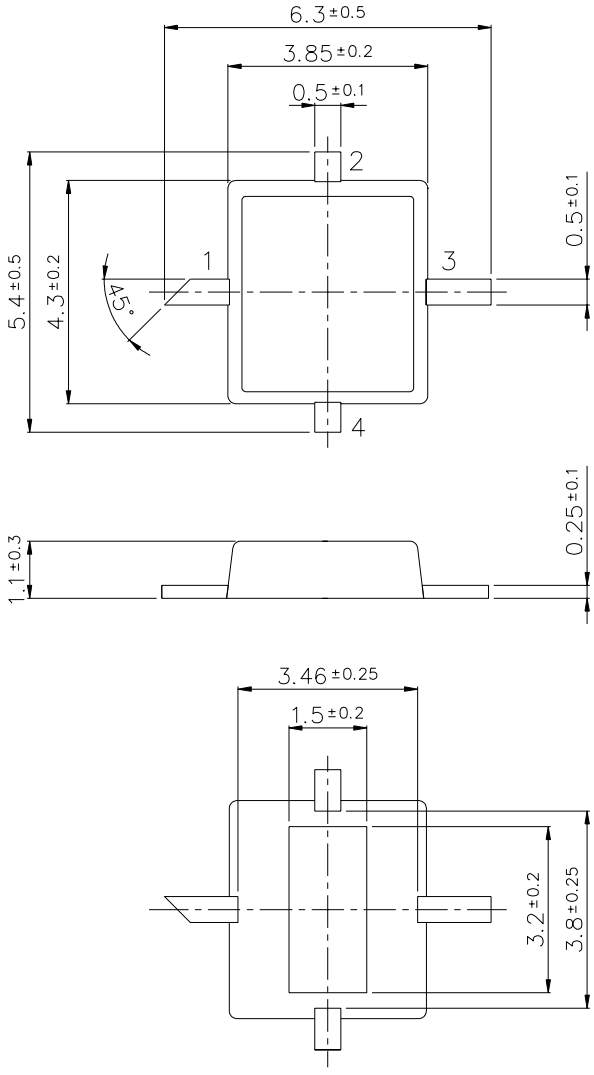
■ Recommended Bias Circuit and Internal Block Diagram



<Board information>
ε r=3.5, t=0.8

* Board was tuned for wide band performance with data shown on pages 4 and 5.

■ Package Outline



1 : Gate

2. Source

3. Drain

4. Source

Unit : mm

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