

Description

The S4560 is dual operational amplifiers which achieve approximately twice the high output current of the S4560, as well as featuring a higher slew rate of 4V/us, a gain band width of 10MHz, and an improved frequency characteristic.

Features

- Built-in output short-circuit protection circuit.
- Internal phase correction.
- No latch-up
- Wide same phase mode and differential voltage ranges
- High gain. low noise

Applications

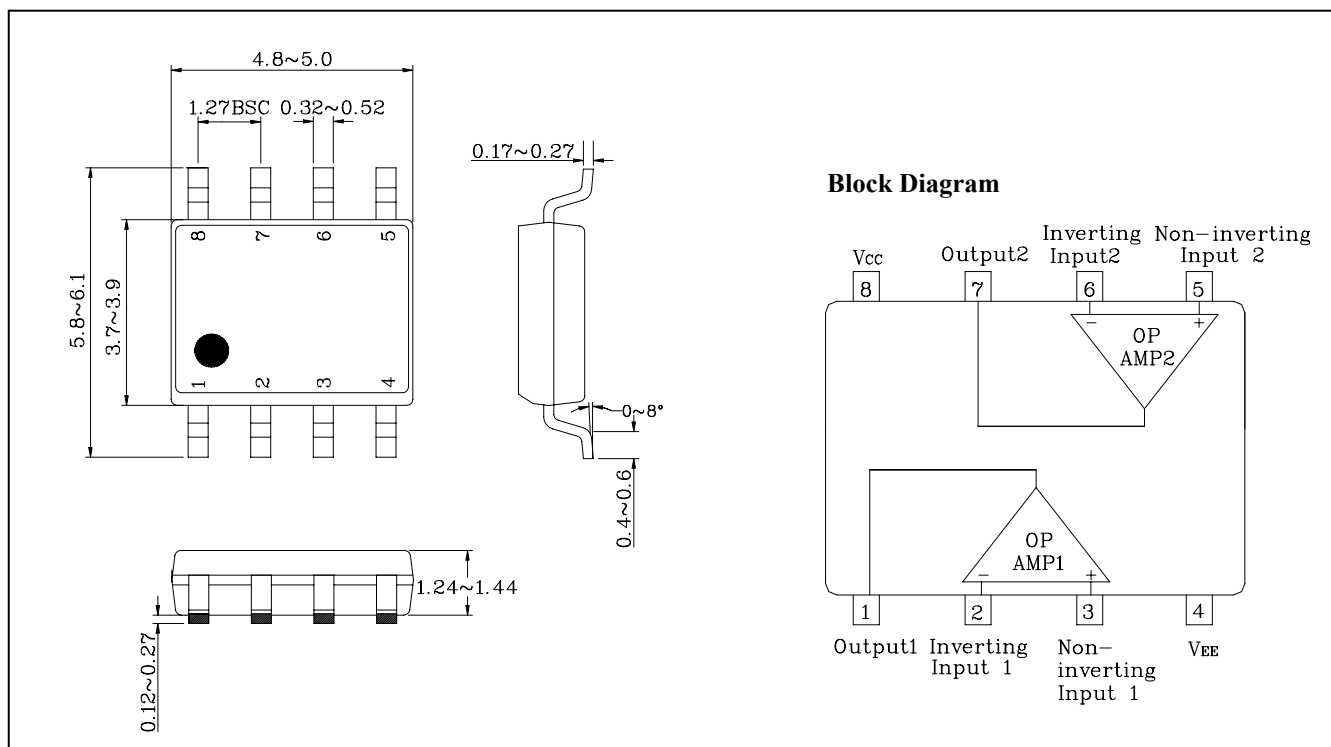
- Active filters
- Audio amplifiers
- VCOs
- Other electronic circuits

Ordering Information

Type NO.	Marking	Package Code
S4560	S4560	SOP-8

Outline Dimensions

unit : mm



Absolute maximum ratings

(Ta = 25 °C)

Characteristic	Symbol	Ratings	Unit
Supply voltage	V _{CC}	±18	V
Differential input voltage	V _{ID}	±30	V
Input voltage	V _{IC}	-V _{CC} ~V _{CC}	V
Power Dissipation	P _D *	550	mW
Operating temperature	T _{opr}	-40 ~ +85	°C
Storage temperature	T _{stg}	-55 ~ +125	°C

* Refer to Pd characteristics diagram. The values for the S4560 are those when it is mounted on a glass epoxy PCB(50 mm×50 mm×1.6 mm).

Electrical Characteristics(Unless otherwise specified. V_{CC} = +15V, V_{EE} = -15V and Ta = 25 °C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input offset voltage	V _{IOS}	R _g ≤ 10 kΩ	-	0.5	6	mV
Input offset current	I _{IOS}	-	-	5	200	nA
Input bias current	I _{IB}	-	-	50	500	nA
Input common mode Voltage Range	V _{ICR}	-	±12	±14	-	V
Maximum Output Voltage	V _{OM}	R _L ≥ 10 kΩ	±12	±14	-	V
		R _L ≥ 2 kΩ	±10	±13	-	V
Large signal Voltage Gain	G _V	V _{out} = ±10V, R _L ≥ 2 kΩ	86	100	-	dB
Common mode rejection ratio	CMRR	R _g ≤ 10 kΩ	70	90	-	dB
Power supply rejection ratio	PSRR	R _g ≤ 10 kΩ	-	30	150	uV/V
Slew Rate	SR	G _V = 1, R _L ≥ 2 kΩ	-	4.0	-	V/us
Input conversion noise voltage	V _n	-	-	-	2.2	uV
Gain band width product	GBW	f = 10kHz	-	10	-	MHz

Electrical Characteristic Curves

Fig. 1 $G_V - f$

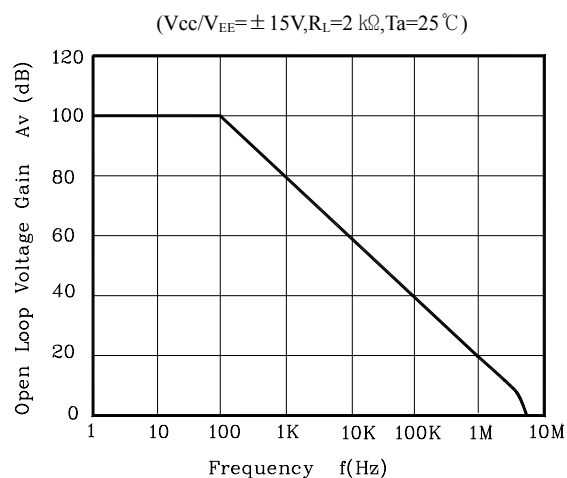


Fig. 2 $V_{OP-P} - f$

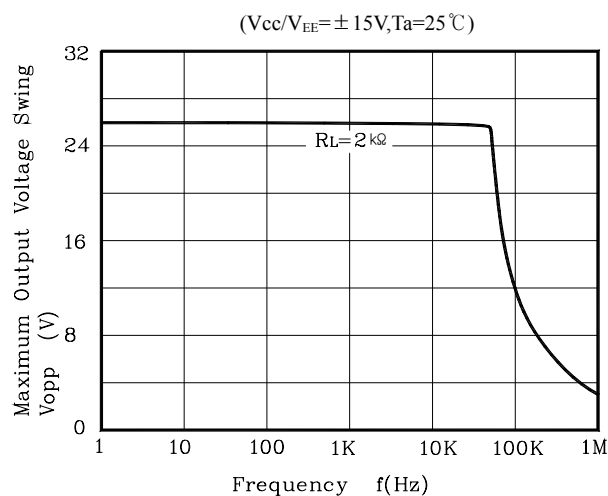


Fig. 3 $I_{IB} - T_a$

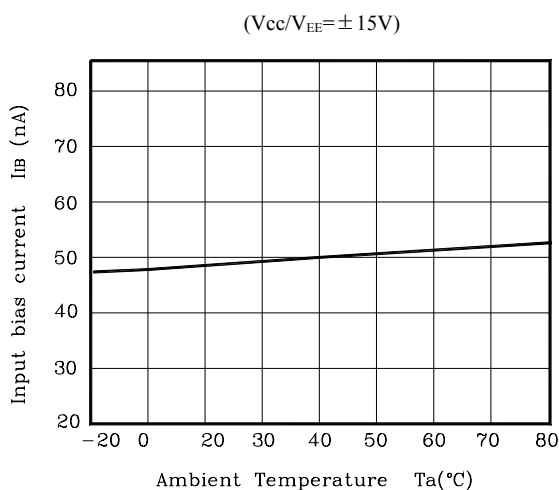


Fig. 4 $V_{ICR} - V_{CC} / V_{EE}$

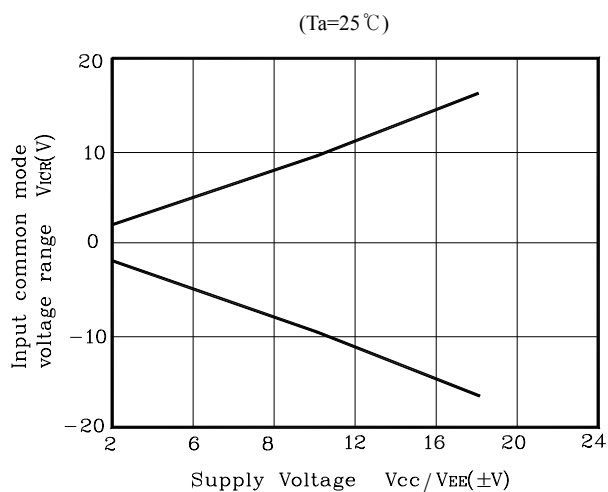


Fig. 5 $I_Q - V_{CC} / V_{EE}$

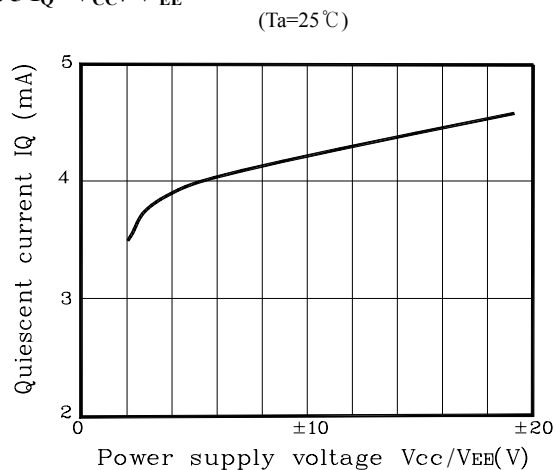
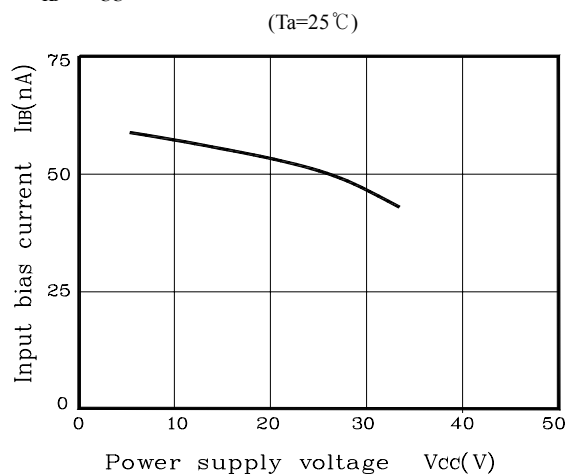


Fig. 6 $I_{IB} - V_{CC}$



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