

- Complete Discrete Multitone (DMT)-Based Asymmetric Digital Subscriber Line (ADSL) Coder/Decoder (CODEC) Solution
- Complies With ANSI T1.413 Issue II and ITU G.992.1
- Supports up to 8 MBPS Downstream and 800 KBPS Upstream Duplex
- Integrated 14-Bit Converters for Transmitter/Echo-Canceller/Receiver (TX/EC/RX)
- Integrated 12-Bit DAC for VCXO Control
- Integrated TX/EC/RX Channel Filters
- Integrated TX/EC/RX Attenuation/Gain
- Integrated Voltage Reference
- High-Speed Parallel Interface
- 16-bit 2s Complement Data Format
- Selectable 2.2 MSPS or 4.4 MSPS Parallel Data Transfer Rate
- Serial Configuration Port
- Eight General-Purpose Output Pins
- Single 3.3-V Supply
- Hardware/Software Power Down
- 100-Pin PQFP (PZ) Package
- –40°C to 85°C Operation

## description

The TLV320AD11A is a high-speed codec for remote terminal-side (RT) modems that support the ANSI T1.413 [Issue 2 discrete multi-tone (DMT) asymmetric digital subscriber line (ADSL) access] and ITU G.992.1 standards. It is a low-power device that includes five major functional blocks: transmitter, receiver, clock, reference, and host interface. It is designed to work with the Texas Instruments TLV320AD12 central office-side (CO) codec.

The device's transmit channel consists of the following functional blocks: 138 kHz digital low-pass filter, bypassable 25.875 kHz digital high-pass filter, 14-bit high speed DAC, 138 kHz analog low-pass filter, transmit attenuator, and an echo cancellation channel. The receiver channel consists of two programmable-gain amplifiers, a frequency equalizer, a 1.104-MHz low-pass analog filter, a 14-bit high speed ADC, and a 1.104-MHz low-pass digital filter. The clock circuit divides a 35.328-MHz frequency from an external VCXO down to the necessary frequencies used throughout the device. The frequency of the external VCXO is controlled by a 12-bit onboard voltage output DAC. An onboard reference circuit generates a 1.5-V reference for the converters.

The device has a parallel port for data transfer and a serial port for control. The parallel port is 16 bits wide and is reserved for moving data between the codec and a DSP such as the Texas Instruments TMS320C6XX. Configuration is done via a serial port. The device can be powered down via a dedicated pin, or through software control, to reduce heat dissipation. Additionally, there is a general-purpose (GP) port consisting of eight output terminals for control of external circuitry.

The TLV320AD11A codec is available in a 100-pin PZ PQFP package and is characterized for operation in the temperature range of –40°C to 85°C.



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 **TEXAS  
INSTRUMENTS**

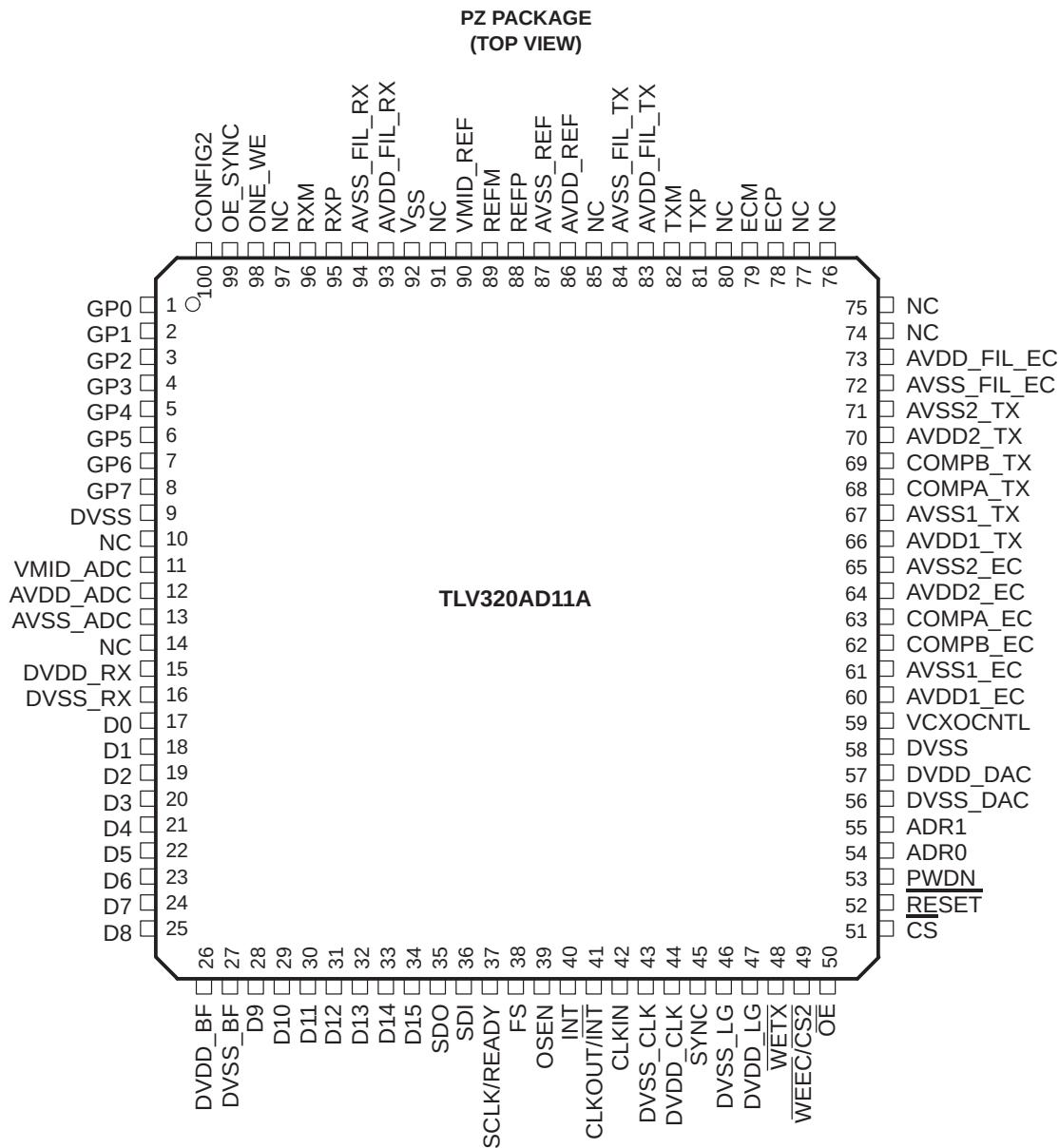
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# TLV320AD11A

## 3.3 V INTEGRATED ADSL OVER POTS CODEC

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### Terminal Functions

| TERMINAL<br>NAME NO.                                                                               |                                                                                                          | I/O | DESCRIPTION                                                                                                                                                    |
|----------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADR0<br>ADR1                                                                                       | 54<br>55                                                                                                 | I   | Serial port chip ID address bits, ADR0 is the least significant bit.                                                                                           |
| AVDD1_EC                                                                                           | 60                                                                                                       | I   | EC channel analog power supply #1                                                                                                                              |
| AVDD2_EC                                                                                           | 64                                                                                                       | I   | EC channel analog power supply #2                                                                                                                              |
| AVDD1_TX                                                                                           | 66                                                                                                       | I   | TX channel analog power supply #1                                                                                                                              |
| AVDD2_TX                                                                                           | 70                                                                                                       | I   | TX channel analog power supply #2                                                                                                                              |
| AVDD_ADC                                                                                           | 12                                                                                                       | I   | Receive channel analog power supply                                                                                                                            |
| AVDD_FIL_EC                                                                                        | 73                                                                                                       | I   | EC channel filter analog power supply                                                                                                                          |
| AVDD_FIL_RX                                                                                        | 93                                                                                                       | I   | Receive channel filter analog power supply                                                                                                                     |
| AVDD_FIL_TX                                                                                        | 83                                                                                                       | I   | Transmit channel filter analog power supply                                                                                                                    |
| AVDD_REF                                                                                           | 86                                                                                                       | I   | Reference analog power supply                                                                                                                                  |
| AVSS1_EC                                                                                           | 61                                                                                                       | I   | EC channel analog ground # 1                                                                                                                                   |
| AVSS2_EC                                                                                           | 65                                                                                                       | I   | EC channel analog ground #2                                                                                                                                    |
| AVSS1_TX                                                                                           | 67                                                                                                       | I   | TX channel analog ground #1                                                                                                                                    |
| AVSS2_TX                                                                                           | 71                                                                                                       | I   | TX channel analog ground #2                                                                                                                                    |
| AVSS_ADC                                                                                           | 13                                                                                                       | I   | Receive channel analog ground                                                                                                                                  |
| AVSS_FIL_EC                                                                                        | 72                                                                                                       | I   | EC channel filter analog ground                                                                                                                                |
| AVSS_FIL_RX                                                                                        | 94                                                                                                       | I   | Receive channel filter analog ground                                                                                                                           |
| AVSS_FIL_TX                                                                                        | 84                                                                                                       | I   | Transmit channel filter analog ground                                                                                                                          |
| AVSS_REF                                                                                           | 87                                                                                                       | I   | Reference analog ground                                                                                                                                        |
| CLKIN                                                                                              | 42                                                                                                       | I   | 35.328 MHz VCXO clock input                                                                                                                                    |
| CLKOUT/ $\overline{\text{INT}}$                                                                    | 41                                                                                                       | O   | If CONFIG2 (pin 100) is low, this pin is 4.416 MHz clock output. If CONFIG2 is high, this pin functions as $\overline{\text{INT}}$ .                           |
| COMP_A_EC                                                                                          | 63                                                                                                       | O   | EC channel cap input A. Add 500 pF X7R ceramic capacitor to AVDD1_EC.                                                                                          |
| COMP_B_EC                                                                                          | 62                                                                                                       | O   | EC channel cap input B. Add 1 $\mu\text{F}$ X7R ceramic capacitor to AVDD1_EC.                                                                                 |
| COMP_A_TX                                                                                          | 68                                                                                                       | O   | TX channel decoupling cap input A. Add 500 pF ceramic capacitor to AVDD1_TX.                                                                                   |
| COMP_B_TX                                                                                          | 69                                                                                                       | O   | TX channel decoupling cap input B. Add 1 $\mu\text{F}$ ceramic capacitor to AVDD1_TX.                                                                          |
| CONFIG2                                                                                            | 100                                                                                                      | I   | I/O configuration input pin. A high on this pin redefines the function of pins 37 and 41. The default state of this pin is low. Refer to Figure 3 for details. |
| $\overline{\text{CS}}$                                                                             | 51                                                                                                       | I   | Parallel port chip select                                                                                                                                      |
| D15<br>D14<br>D13<br>D12<br>D11<br>D10<br>D9<br>D8<br>D7<br>D6<br>D5<br>D4<br>D3<br>D2<br>D1<br>D0 | 34 (MSB)<br>33<br>32<br>31<br>30<br>29<br>28<br>25<br>24<br>23<br>22<br>21<br>20<br>19<br>18<br>17 (LSB) | I/O | Parallel port data bits D0=LSB                                                                                                                                 |

# TLV320AD11A

## 3.3 V INTEGRATED ADSL OVER POTS CODEC

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### Terminal Functions(Continued)

| TERMINAL<br>NAME                                     | NO.                                             | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                             |
|------------------------------------------------------|-------------------------------------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DVDD_BF                                              | 26                                              | I   | Digital I/O buffer supply                                                                                                                                                                                                                                                                                                                                                               |
| DVDD_CLK                                             | 44                                              | I   | Digital clock supply                                                                                                                                                                                                                                                                                                                                                                    |
| DVDD_LG                                              | 47                                              | I   | Digital logic supply                                                                                                                                                                                                                                                                                                                                                                    |
| DVDD_RX                                              | 15                                              | I   | Receive channel digital power supply                                                                                                                                                                                                                                                                                                                                                    |
| DVDD_DAC                                             | 57                                              | I   | Digital power supply for DAC                                                                                                                                                                                                                                                                                                                                                            |
| DVSS                                                 | 9, 58                                           | I   | Digital ground                                                                                                                                                                                                                                                                                                                                                                          |
| DVSS_BF                                              | 27                                              | I   | Digital I/O buffer ground                                                                                                                                                                                                                                                                                                                                                               |
| DVSS_CLK                                             | 43                                              | I   | Digital clock ground                                                                                                                                                                                                                                                                                                                                                                    |
| DVSS_LG                                              | 46                                              | I   | Digital logic ground                                                                                                                                                                                                                                                                                                                                                                    |
| DVSS_RX                                              | 16                                              | I   | Receive channel ground                                                                                                                                                                                                                                                                                                                                                                  |
| DVSS_DAC                                             | 56                                              | I   | DAC ground                                                                                                                                                                                                                                                                                                                                                                              |
| ECM                                                  | 79                                              | O   | EC output minus                                                                                                                                                                                                                                                                                                                                                                         |
| ECP                                                  | 78                                              | O   | EC output plus                                                                                                                                                                                                                                                                                                                                                                          |
| FS                                                   | 38                                              | I   | Frame sync input                                                                                                                                                                                                                                                                                                                                                                        |
| GP7<br>GP6<br>GP5<br>GP4<br>GP3<br>GP2<br>GP1<br>GP0 | 8<br>7<br>6<br>5<br>4<br>3<br>2<br>1            | O   | General-purpose output port                                                                                                                                                                                                                                                                                                                                                             |
| INT                                                  | 40                                              | O   | Data rate clock (INT is 4.4 MHz when OSEN=1, 2.2 MHz when OSEN=0)                                                                                                                                                                                                                                                                                                                       |
| NC                                                   | 10, 14, 74,<br>75, 76, 77,<br>80, 85, 91,<br>97 |     | No connection. All the NC pins should be left open.                                                                                                                                                                                                                                                                                                                                     |
| $\overline{\text{OE}}$                               | 50                                              | I   | Parallel port output enable from host processor                                                                                                                                                                                                                                                                                                                                         |
| OE_SYNC                                              | 99                                              | I   | $\overline{\text{OE}}$ synchronized input. A high input will optimize the read operation from keep-out zone. The default state of this pin is low. See Figure 5 for details.                                                                                                                                                                                                            |
| ONE_WE                                               | 98                                              | I   | TX and EC write combined input. A high on this pin allows pin 48, $\overline{\text{WETX}}$ , to be used to write to both the EC and TX channels. In this case, after a hardware reset or write to SCR14[0], the first low-going pulse of $\overline{\text{WETX}}$ will be a write to TX channel and the second one will be a write to EC channel. The default state of this pin is low. |
| OSEN                                                 | 39                                              | I   | Over-sampling enable input. OSEN=1 enables over-sampling mode (INT = 4.4 MHz).                                                                                                                                                                                                                                                                                                          |
| PWDN                                                 | 53                                              | I   | Power-down input. When PWDN=0, device is in normal operating mode. When PWDN=1, device is in power-down mode.                                                                                                                                                                                                                                                                           |
| REFM                                                 | 89                                              | O   | Decoupling reference REF voltage minus. Add 10 $\mu\text{F}$ tantalum and 0.1 $\mu\text{F}$ ceramic capacitors to AVSS_REFP. The nominal dc voltage at this terminal is 0.5 V. See figure 9 for detail.                                                                                                                                                                                 |
| REFP                                                 | 88                                              | O   | Decoupling reference REF voltage plus. Add 10 $\mu\text{F}$ tantalum and 0.1 $\mu\text{F}$ ceramic capacitors to AVSS_REFM. The nominal dc voltage at this terminal is 2.5 V.. See figure 9 for detail.                                                                                                                                                                                 |
| $\overline{\text{RESET}}$                            | 52                                              | I   | H/W system reset. An low level will reset the device.                                                                                                                                                                                                                                                                                                                                   |
| RXM                                                  | 96                                              | I   | Receive RX input minus. RXM is self-biased to AVDD_FIL_RX/2.                                                                                                                                                                                                                                                                                                                            |
| RXP                                                  | 95                                              | I   | Receive RX input plus. RXP is self-biased to AVDD_FIL_RX/2.                                                                                                                                                                                                                                                                                                                             |
| SCLK/READY                                           | 37                                              | O   | If CONFIG2 (pin 100) is low, this pin is serial clock output. If CONFIG2 is high, it indicates the period in which parallel data can be transferred.                                                                                                                                                                                                                                    |
| SDI                                                  | 36                                              | I   | Serial data input                                                                                                                                                                                                                                                                                                                                                                       |

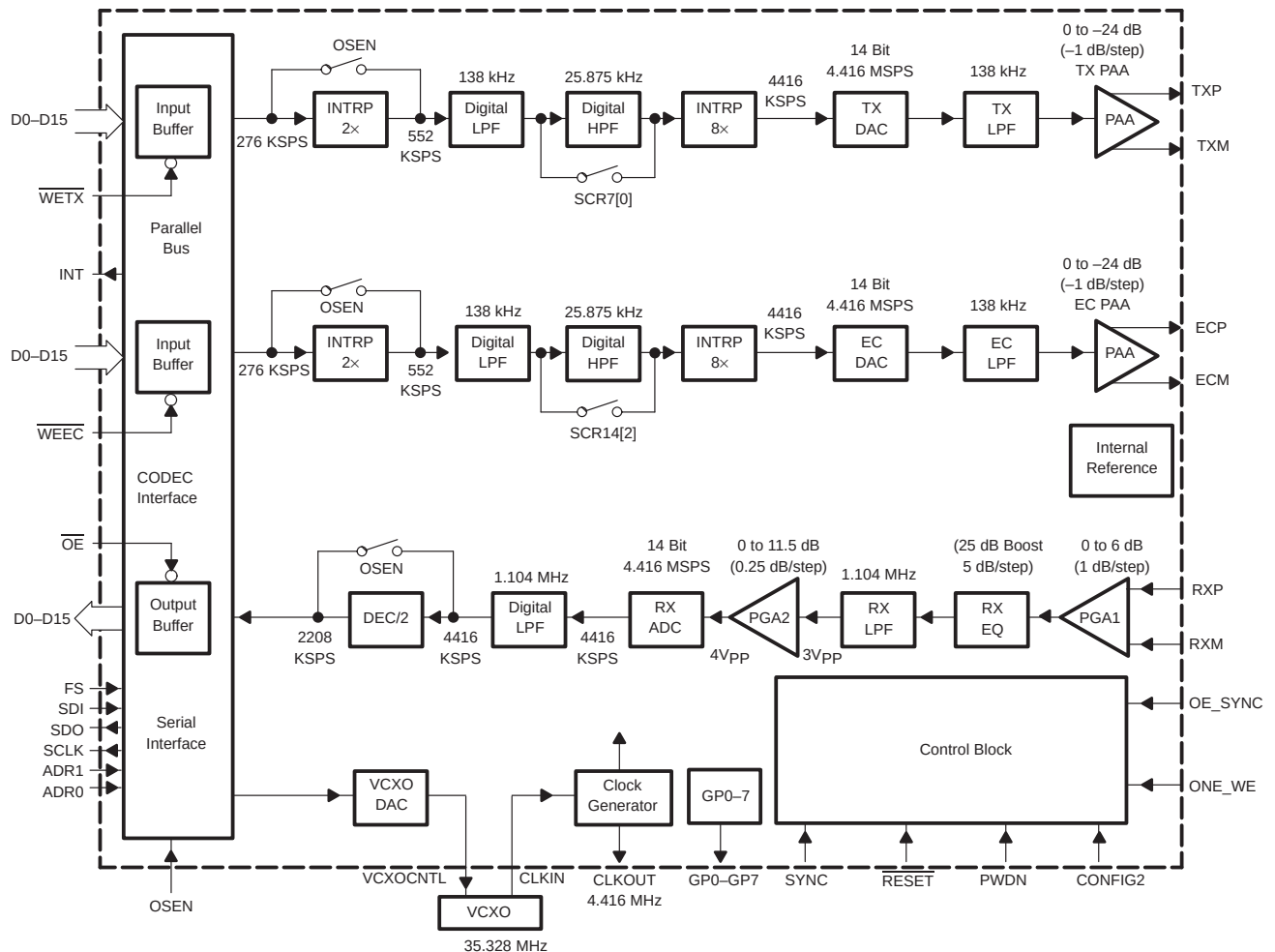


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### Terminal Functions(Continued)

| TERMINAL<br>NAME | NO. | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                    |
|------------------|-----|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SDO              | 35  | O   | Serial data output                                                                                                                                                                                                                                                                             |
| SYNC             | 45  | I   | SYNC pulse for clock synchronization. A high pulse to the pin synchronizes the clock operation. The default state of the pin is low. Refer to Figure 4 for detail.                                                                                                                             |
| TXM              | 82  | O   | Transmit output minus                                                                                                                                                                                                                                                                          |
| TXP              | 81  | O   | Transmit output plus                                                                                                                                                                                                                                                                           |
| VCXOCTL          | 59  | O   | VCXO DAC output                                                                                                                                                                                                                                                                                |
| VMID_ADC         | 11  | O   | Decoupling 1.5 V for ADC. Add 10 $\mu$ F tantalum and 0.1 $\mu$ F ceramic capacitors to AVSS_ADC.                                                                                                                                                                                              |
| VMID_REF         | 90  | O   | Decoupling 1.5 V reference voltage. Add 10 $\mu$ F tantalum and 0.1 $\mu$ F ceramic capacitors to AVSS_REF.                                                                                                                                                                                    |
| V <sub>SS</sub>  | 92  | I   | Substrate. V <sub>SS</sub> needs to connect to analog ground.                                                                                                                                                                                                                                  |
| WEEC/CS2         | 49  | I   | Write enable to EC channel from host processor, when ONE_WE (pin 98) is low. If ONE_WE is high, it functions as second chip select, CS2, and both CS and CS2 need to be low in order to have WETX access data on the parallel bus.                                                             |
| WETX             | 48  | I   | Write enable for TX channel from host processor. If ONE_WE is high, it functions as write enable for both TX and EC after hardware reset or write to SCR14[0]. In this case, the first low-going pulse of WETX will be a write to TX channel, and the second one will be a write to EC channel |

### functional block diagram



# TLV320AD11A

## 3.3 V INTEGRATED ADSL OVER POTS CODEC

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### PRINCIPLES OF OPERATION

#### communication channels

##### transmitter channel/echo-cancellation channel

The transmitter channel is powered by a high performance DAC. This is a 4.416-MHz, 14-bit DAC that provides a 16X over-sampling to reduce DAC noise. The input buffer is sampled at either 276 KSPS (pin OSEN = low, default), or 552 KSPS (pin OSEN = high). A low-pass filter limits its output to 138 kHz. A programmable attenuator, with a range between 0 and –24 dB in –1-dB steps, drives the output into the external ADSL line driver.

A second transmitter is used to perform pre-echo cancellation. This analog echo cancellation helps reduce the dynamic range requirements of the RT receiver. It has the same function as the first transmitter channel. It drives a separate external line driver to perform the cancellation.

##### receiver channel

The receiver channel has two PGAs and an equalizer to match the loop loss and flatten the spectrum. This results in a reduction in dynamic range requirement for the high resolution ADC. The receiver channel also has a 1.104-MHz low-pass filter with a 4.416 MSPS and a 14-bit ADC to provide a 2X over-sampling. The output buffer is updated at either 2208 KSPS (pin OSEN = low, default), or 4416 KSPS (pin OSEN = high).

##### VCXO-control DAC

A 12-bit DAC is used to control the external 35.328-MHz VCXO (voltage control oscillator) that provides the system clock to the codec. In a typical application, the typical update rate of the DAC is about 4 kHz, depending on the ADSL frame rate. The host DSP initiates the update through the serial interface. The two 8-bit registers SCR4 and SCR5 (each 2s complement) are used to generate the 12-bit code for the DAC. This requires the use of 16 bits to obtain a 12-bit number. So the lower 4 bits of the MSB register (SCR5[3:0]) are added (2s complement) to the higher 4 bits of the LSB register (SCR4[7:4]). Refer to Figure 1 for code generation. The updated code is sent to the DAC two SCLKs after the SCR4 register is received. Notice that if SCR5 does not need to be updated, only one write cycle to SCR4 is needed to update the VCXO DAC. In this case, the lower 8 bits of the 12-bit word will be updated.

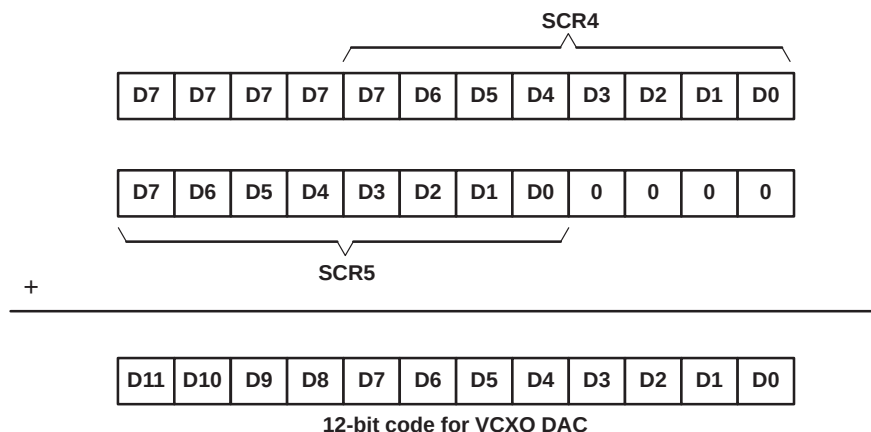


Figure 1. 12-Bit Code Generation for VCXO DAC

## PRINCIPLES OF OPERATION

### communication channels (continued)

#### clock generation

The clock generation block provides the necessary clock signals for the device, with minimum skew and jitter. This is closely dependent on the performance of the external VCXO. The external VCXO specifications are:

- 3.3 V supply
- 35.328 MHz  $\pm$  50 PPM
- Minimum duty cycle is 60/40 (50/50 is optimum)

The major clocks generated internally are shown in Table 1.

**Table 1. Clock Description**

| CLOCK  | FREQUENCY<br>(MHz) |        |
|--------|--------------------|--------|
|        | OSEN=0             | OSEN=1 |
| INT    | 2.208              | 4.416  |
| CLKOUT | 4.416              | 4.416  |
| SCLK   | 4.416              | 4.416  |

#### INT

The interrupt (INT) to the host processor is 4.416 MHz when OSEN = 1 and 2.208 MHz when OSEN = 0.

#### SCLK

The serial clock used in the serial codec interface has a fixed frequency of 4.416 MHz and is synchronous with the master clock (35.328 MHz).

#### CLKOUT

CLKOUT is a 4.416-MHz clock output, and is synchronous with the master clock (35.328 MHz).

### interface

#### parallel interface

The device has a 16-bit parallel interface for transmitter and receiver data. Strobes  $\overline{OE}$ ,  $\overline{WETX}$ , and  $\overline{CS}$  from the host DSP are edge-triggered signals. An incoming signal is registered on the rising edge of  $\overline{WETX}/\overline{WEEC}$ . When ONE\_WE is enabled, only  $\overline{WETX}$  is needed for both the transmit channel and the echo-cancellation channel write operation. After D0 of register SCR14 is programmed, the data from the first pulse of  $\overline{WETX}$  goes to the transmit channel, while the data from the second pulse of  $\overline{WETX}$  goes to the echo-cancellation channel. Output data from the codec is enabled after the falling edge of the  $\overline{OE}$  strobe, and disabled after the rising edge of the  $\overline{OE}$  strobe. The INT cycle time is hardware-configurable to 4.416 MHz (2X over-sampling mode, OSEN=1), or to 2.208 MHz (1X over-sampling mode, OSEN=0). SYNC is used to synchronize the operation between the codec and the host transceiver. SCLK/READY is used to indicate the parallel data transfer period in configuration mode 2. See Figure 3 for details.

OE\_SYNC is used to synchronize the codec timing to  $\overline{OE}$ . See Figure 5 for details.

For the 16-bit parallel data, D0 is the LSB and D15 is the MSB. The parallel TX and RX data contains 16 valid bits. All 16 bits are used in the digital filtering.

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### PRINCIPLES OF OPERATION

#### interface (continued)

##### keep-out zones

The last CLKIN cycle before a transition of CLKOUT is defined as a keep-out zone. These zones are reserved for the sampling of analog signals. All digital I/O (except for CLKIN) should be quiet during these keep-out zones.

##### over-sampling mode

The OSEN pin selects 2X over-sampling mode (INT running at 4.416 MHz), or 1X over-sampling mode (INT running at 2.208 MHz).

##### serial interface

The serial port is used for codec configuration and register reading. The word length is 16-bit. Two hardware configuration terminals, ADR[1:0], are used to configure the device ID. Up to four codecs can be identified for each common serial port. Refer to figure 6 for timing and format.

The master codec (ADR[1:0] = [0,0]) provides the SCLK to the host processor. The SCLK terminals on the other codecs are left unconnected. All the codecs in a multi-codec system should be synchronized so that their SCLK signals are in phase, even though the signals themselves are not being used. This ensures that, even though the individual SCLK signals of each codec are not being used, the data is being latched into the codec properly.

The SCLK is a continuously running 4.416-MHz fixed-frequency clock, synchronized to the codec internal events and CLKOUT (to the host) so that the keep-out zones may be monitored. A host DSP can drive the FS (synchronized to the CLKOUT from the codec) into the codec to initiate a 16-bit serial I/O frame.

If SCR5 needs to be updated, the host controller (DSP) must first write the SCR5 of the VCXO DAC data, and then the SCR4 of the VCXO DAC data. The VCXO DAC only gets updated after the SCR4 is written.

##### GP port

The general-purpose port provides eight outputs, each capable of delivering 0.5 mA, for control of external circuitry such as LEDs, gain control, and power down.

##### voltage reference

The built-in reference provides the required reference voltage and current to individual analog blocks. It is also brought out to external terminals for noise decoupling.



## PRINCIPLES OF OPERATION

register programming (see Figure 6 for timing and format details)

**Table 2. System Control Registers (SCR)**

| REGISTER |                        | MODE | DEFAULT VALUE | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                               |
|----------|------------------------|------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME     | ADDRESS S3, S2, S1, S0 |      |               |                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| SCR0     | 0000                   | R    | 00000000      |                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|          |                        | W    |               | D0: S/W RESET (self clearing)                                                                                                                                                                                                                                                                                                                                                                                                          |
| SCR1     | 0001                   | R/W  | 00000000      | D[4:0]=TX channel PAA gain select. D[4:0]=00000 for 0 dB<br>D[4:0]=11000 for –24 dB                                                                                                                                                                                                                                                                                                                                                    |
| SCR2     | 0010                   | R/W  | 00000000      | D[5:0]=RX PGA2. D[5:0]=0000000 for 0 dB. D[5:0]=101110 for 11.5 dB.                                                                                                                                                                                                                                                                                                                                                                    |
| SCR3     | 0011                   | R/W  | 00000000      | D[2:0]= RX EQ slope select. D[2:0]=000 for 0dB/MHz, D[2:0]=001 for 5 dB/MHz,<br>D[2:0]=101 for 25 dB/MHz                                                                                                                                                                                                                                                                                                                               |
| SCR4     | 0100                   | R/W  | 00000000      | D[7:0]=VCXODAC (low 8 bits of 12-bit DAC code)                                                                                                                                                                                                                                                                                                                                                                                         |
| SCR5     | 0101                   | R/W  | 00000000      | D[7:0]=VCXODAC (high 8 bits of 12-bit DAC code)                                                                                                                                                                                                                                                                                                                                                                                        |
| SCR6     | 0110                   | R/W  | 00000000      | D[7:0]=GP[7:0]                                                                                                                                                                                                                                                                                                                                                                                                                         |
| SCR7     | 0111                   | R/W  | 00000000      | MISC control (set to 1 to enable)<br>D0: bypass TX DHPF (25.875 kHz)<br>D1: S/W power-down RX channel<br>D2: S/W power-down TX channel<br>D3: analog loop-back (TX channel)<br>D4: digital loop-back (TX and EC channel)<br>D5: TX parallel interface (read-back) test mode enable<br>D6: EC channel power down<br>D7: EC analog loop-back                                                                                             |
| SCR8     | 1000                   | R/W  | 00000000      | D[4:0]=EC channel PAA gain select. D[4:0]=00000 for 0 dB.<br>D[4:0]=11000 for –24 dB.                                                                                                                                                                                                                                                                                                                                                  |
| SCR9     | 1001                   | R/W  | 00000000      | D[7:0]=RX offset low                                                                                                                                                                                                                                                                                                                                                                                                                   |
| SCR10    | 1010                   | R/W  | 00000000      | D[7:0]=RX offset high                                                                                                                                                                                                                                                                                                                                                                                                                  |
| SCR11    | 1011                   | R/W  | 00000000      | D[4:0]=TX digital gain select. The gain range is –1dB to 1dB in 0.1 dB-steps.<br>D[4:0]=00000 for 0 dB. D[4:0]=00001 for +0.1 dB. D[4:0]=01010 for +1 dB.<br>D[4:0]=10000 for –1 dB. D[4:0]=11001 for –0.1 dB.                                                                                                                                                                                                                         |
| SCR12    | 1100                   | R/W  | 00000000      | D[2:0]=RX PGA1. D[2:0]=000 for 0 dB. D[2:0]=110 for 6 dB.                                                                                                                                                                                                                                                                                                                                                                              |
| SCR13    | 1101                   | R/W  | 00000000      | D[4:0]=EC digital gain select. The gain range is –1dB to 1dB in 0.1-dB steps.<br>D[4:0]=00000 for 0 dB. D[4:0]=00001 for +0.1 dB. D[4:0]=01010 for +1 dB.<br>D[4:0]=10000 for –1 dB. D[4:0]=11001 for –0.1 dB.                                                                                                                                                                                                                         |
| SCR14    | 1110                   | R/W  | 00000000      | D0: Sync the write operation when ONE_WE is selected. After D0 is set to 1, the first pulse of WETX goes to TX channel, and the second pulse goes to EC channel. The bit will be self-cleared to 0.<br>D1: enable FIFO (first-in, first-out). See Note 1.<br>D2: Bypass EC DHPF (25.875 kHz)<br>D3: ECNULL. When D3 is set to 1, ECP and ECM are connected to weakly driven mid supply. It can only be used during EC power-down mode. |

NOTE 1: It is a two-stage FIFO buffer, and can store up to two write-samples if asynchronous write operation is required.

### SCR0 – system control register

Address:0000b

Contents at reset: 00000000b

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REGISTER VALUE (HEX) | DESCRIPTION                                                                |
|----|----|----|----|----|----|----|----|----------------------|----------------------------------------------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 01                   | S/W reset (self clearing). All control registers are set to reset content. |

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### PRINCIPLES OF OPERATION

#### register programming (continued)

##### SCR1 – TX PAA control register

Address:0001b

Contents at reset: 00000000b

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REGISTER<br>VALUE (HEX) | DESCRIPTION          |
|----|----|----|----|----|----|----|----|-------------------------|----------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 00                      | TX PAA gain = 0 dB   |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 01                      | TX PAA gain = –1 dB  |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 02                      | TX PAA gain = –2 dB  |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 03                      | TX PAA gain = –3 dB  |
| 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 04                      | TX PAA gain = –4 dB  |
| 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 05                      | TX PAA gain = –5 dB  |
| 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 06                      | TX PAA gain = –6 dB  |
| 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 07                      | TX PAA gain = –7 dB  |
| 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 08                      | TX PAA gain = –8 dB  |
| 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 09                      | TX PAA gain = –9 dB  |
| 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0A                      | TX PAA gain = –10 dB |
| 0  | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 0B                      | TX PAA gain = –11 dB |
| 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0C                      | TX PAA gain = –12 dB |
| 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0D                      | TX PAA gain = –13 dB |
| 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0E                      | TX PAA gain = –14 dB |
| 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 0F                      | TX PAA gain = –15 dB |
| 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 10                      | TX PAA gain = –16 dB |
| 0  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 11                      | TX PAA gain = –17 dB |
| 0  | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 12                      | TX PAA gain = –18 dB |
| 0  | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 13                      | TX PAA gain = –19 dB |
| 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 14                      | TX PAA gain = –20 dB |
| 0  | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 15                      | TX PAA gain = –21 dB |
| 0  | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 16                      | TX PAA gain = –22 dB |
| 0  | 0  | 0  | 1  | 0  | 1  | 1  | 1  | 17                      | TX PAA gain = –23 dB |
| 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 18                      | TX PAA gain = –24 dB |
| –  | –  | –  | –  | –  | –  | –  | –  | 19–FF                   | TX PAA gain = –24 dB |



## PRINCIPLES OF OPERATION

### register programming (continued)

SCR2 – RX PGA2 control register

Address: 0010b

Contents at reset: 0000000b

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REGISTER<br>VALUE (HEX) | DESCRIPTION        |
|----|----|----|----|----|----|----|----|-------------------------|--------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 00                      | RX PGA2 = 0 dB     |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 01                      | RX PGA2 = 0.25 dB  |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 02                      | RX PGA2 = 0.5 dB   |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 03                      | RX PGA2 = 0.75 dB  |
| 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 05                      | RX PGA2 = 1 dB     |
| 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 06                      | RX PGA2 = 1.25 dB  |
| 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 07                      | RX PGA2 = 1.5 dB   |
| 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 08                      | RX PGA2 = 1.75 dB  |
| 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 09                      | RX PGA2 = 2 dB     |
| 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0A                      | RX PGA2 = 2.25 dB  |
| 0  | 0  | 0  | 0  | 1  | 0  | 1  | 1  | 0B                      | RX PGA2 = 2.5 dB   |
| 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0C                      | RX PGA2 = 2.75 dB  |
| 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0D                      | RX PGA2 = 3 dB     |
| 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0E                      | RX PGA2 = 3.25 dB  |
| 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 0F                      | RX PGA2 = 3.5 dB   |
| 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 10                      | RX PGA2 = 3.75 dB  |
| 0  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 11                      | RX PGA2 = 4 dB     |
| 0  | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 12                      | RX PGA2 = 4.25 dB  |
| 0  | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 13                      | RX PGA2 = 4.5 dB   |
| 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 14                      | RX PGA2 = 4.75 dB  |
| 0  | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 15                      | RX PGA2 = 5 dB     |
| 0  | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 16                      | RX PGA2 = 5.25 dB  |
| 0  | 0  | 0  | 1  | 0  | 1  | 1  | 1  | 17                      | RX PGA2 = 5.5 dB   |
| 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 18                      | RX PGA2 = 5.75 dB  |
| 0  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 19                      | RX PGA2 = 6 dB     |
| 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 1A                      | RX PGA2 = 6.25 dB  |
| 0  | 0  | 0  | 1  | 1  | 0  | 1  | 1  | 1B                      | RX PGA2 = 6.5 dB   |
| 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 1C                      | RX PGA2 = 6.75 dB  |
| 0  | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 1D                      | RX PGA2 = 7 dB     |
| 0  | 0  | 0  | 1  | 1  | 1  | 1  | 0  | 1E                      | RX PGA2 = 7.25 dB  |
| 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1F                      | RX PGA2 = 7.5 dB   |
| 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 20                      | RX PGA2 = 7.75 dB  |
| 0  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 21                      | RX PGA2 = 8 dB     |
| 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 22                      | RX PGA2 = 8.25 dB  |
| 0  | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 23                      | RX PGA2 = 8.5 dB   |
| 0  | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 24                      | RX PGA2 = 8.75 dB  |
| 0  | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 25                      | RX PGA2 = 9 dB     |
| 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 04                      | RX PGA2 = 9.25 dB  |
| 0  | 0  | 1  | 0  | 0  | 1  | 1  | 0  | 26                      | RX PGA2 = 9.5 dB   |
| 0  | 0  | 1  | 0  | 0  | 1  | 1  | 1  | 27                      | RX PGA2 = 9.75 dB  |
| 0  | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 28                      | RX PGA2 = 10 dB    |
| 0  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 29                      | RX PGA2 = 10.25 dB |

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### PRINCIPLES OF OPERATION

#### register programming (continued)

**SCR2 – RX PGA2 control register (continued)**      **Address:0010b**      **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REGISTER VALUE (HEX) | DESCRIPTION        |
|----|----|----|----|----|----|----|----|----------------------|--------------------|
| 0  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 2A                   | RX PGA2 = 10.5 dB  |
| 0  | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 2B                   | RX PGA2 = 10.75 dB |
| 0  | 0  | 1  | 0  | 1  | 1  | 0  | 0  | 2C                   | RX PGA2 = 11 dB    |
| 0  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 2D                   | RX PGA2 = 11.25 dB |
| 0  | 0  | 1  | 0  | 1  | 1  | 1  | 0  | 2E                   | RX PGA2 = 11.5 dB  |
| –  | –  | –  | –  | –  | –  | –  | –  | 2F–FF                | RX PGA2 = 11.5 dB  |

**SCR3 – RX EQ control register**      **Address:0011b**      **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REGISTER VALUE (HEX) | DESCRIPTION       |
|----|----|----|----|----|----|----|----|----------------------|-------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 00                   | RX EQ = 0 dB/MHz  |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 01                   | RX EQ = 5 dB/MHz  |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 02                   | RX EQ = 10 dB/MHz |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 03                   | RX EQ = 15 dB/MHz |
| 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 04                   | RX EQ = 20 dB/MHz |
| 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 05                   | RX EQ = 25 dB/MHz |
| –  | –  | –  | –  | –  | –  | –  | –  | 06–FF                | RX EQ = 25 dB/MHz |

**SCR4 – VCXO data register**      **Address:0100b**      **Contents at reset: 00000000b**

**SCR5 – VCXO data register**      **Address:0101b**      **Contents at reset: 00000000b**

The following table shows some representative analog outputs. Notice that the read-back values of SCR4 and SCR5 are different from the values written in.

**Table 3. VCXODAC Digital-Analog Mapping**

| OPERATION                                        | HEX RESULT | ANALOG OUTPUT (see Note 2 and 3) | COMMENTS       |
|--------------------------------------------------|------------|----------------------------------|----------------|
| $\text{SRC5}[7:0] \times 2^4 + \text{SCR4}[7:0]$ | 0x800      | 0 V                              | Min scale      |
|                                                  | 0x801      | $\Delta V$                       | Just above min |
|                                                  | ...        | ...                              | ...            |
|                                                  | 0xFFFF     | 2047 $\Delta V$                  | Just below mid |
|                                                  | 0x000      | 2048 $\Delta V$                  | Mid scale      |
|                                                  | 0x001      | 2049 $\Delta V$                  | Just above mid |
|                                                  | ...        | ...                              | ...            |
|                                                  | 0x7FE      | 4094 $\Delta V$                  | Just below max |
|                                                  | 0x7FF      | 4095 $\Delta V$                  | Max scale      |

NOTES: 2.  $\Delta = (3/4095) V$

3. The analog output is computed as follows:

$$((\text{SCR}\%[7:0] \times 2^4 + \text{SCR4}[7:0])) + 2048(\text{decimal}) \times \Delta$$

## PRINCIPLES OF OPERATION

### register programming (continued)

#### examples:

- Positive SCR5 + positive SCR4  
 $(0x24 \times 2^4 + 0x42) = 0x240 + 0x42 = 0x282 = 642$  decimal  
 Analog output =  $(642 + 2048) \Delta V = 2690 \Delta V = 1.971$  V  
 The read back values of SCR5 and SCR4 are 0x02 and 0x82
- Positive SCR5 + negative SCR4  
 $(0x24 \times 2^4 + 0xC2) = 0x240 + 0xFC2 = 0x202 = 514$  decimal  
 Analog output =  $(514 + 2048) \Delta V = 2562 \Delta V = 1.877$  V  
 The read back values of SCR5 and SCR4 are 0x02 and 0x02
- Negative SCR5 + positive SCR4  
 $(0xA2 \times 2^4 + 0x42) = 0xA20 + 0x42 = 0xA62 = -1438$  decimal  
 Analog output =  $(-1438 + 2048) \Delta V = 610 \Delta V = 0.447$  V  
 The read back values of SCR5 and SCR4 are 0x0A and 0x62
- Negative SCR5 + negative SCR4  
 $(0xA2 \times 2^4 + 0xC2) = 0xA20 + 0xFC2 = 0x9E2 = -1566$  decimal  
 Analog output =  $(-1566 + 2048) \Delta V = 482 \Delta V = 0.353$  V  
 The read back values of SCR5 and SCR4 are 0x09 and 0xE2

### SCR6 – general-purpose output data register    Address:0110b    Contents at reset: 00000000b

| D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  | REGISTER<br>VALUE (HEX) | DESCRIPTION          |
|-----|-----|-----|-----|-----|-----|-----|-----|-------------------------|----------------------|
| 0/1 | –   | –   | –   | –   | –   | –   | –   |                         | GP7 = low(0)/high(1) |
| –   | 0/1 | –   | –   | –   | –   | –   | –   |                         | GP6 = low(0)/high(1) |
| –   | –   | 0/1 | –   | –   | –   | –   | –   |                         | GP5 = low(0)/high(1) |
| –   | –   | –   | 0/1 | –   | –   | –   | –   |                         | GP4 = low(0)/high(1) |
| –   | –   | –   | –   | 0/1 | –   | –   | –   |                         | GP3 = low(0)/high(1) |
| –   | –   | –   | –   | –   | 0/1 | –   | –   |                         | GP2 = low(0)/high(1) |
| –   | –   | –   | –   | –   | –   | 0/1 | –   |                         | GP1 = low(0)/high(1) |
| –   | –   | –   | –   | –   | –   | –   | 0/1 |                         | GP0 = low(0)/high(1) |

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### PRINCIPLES OF OPERATION

#### register programming (continued)

**SCR7 – miscellaneous control register 1**      **Address:0111b**      **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REGISTER VALUE (HEX) | DESCRIPTION                                                     |
|----|----|----|----|----|----|----|----|----------------------|-----------------------------------------------------------------|
| –  | –  | –  | –  | –  | –  | –  | 1  |                      | Bypass TX DHPF (25.875 kHz)                                     |
| –  | –  | –  | –  | –  | –  | 1  | –  |                      | S/W power-down RX channel                                       |
| –  | –  | –  | –  | –  | 1  | –  | –  |                      | S/W power-down TX channel                                       |
| –  | –  | –  | –  | 1  | –  | –  | –  |                      | Analog loop-back (TX channel) (see Note 4)                      |
| –  | –  | –  | 1  | –  | –  | –  | –  |                      | Digital loop-back (TX and EC channel) (see Note 5)              |
| –  | –  | 1  | –  | –  | –  | –  | –  |                      | TX parallel interface (read back) test mode enable (see Note 6) |
| –  | 1  | –  | –  | –  | –  | –  | –  |                      | EC channel power down                                           |
| 1  | –  | –  | –  | –  | –  | –  | –  |                      | EC analog loop-back                                             |

NOTES: 4. Analog loop-back: Analog output pins (TXP/TXM or ECP/ECM) are internally connected to RXP/RXM.  
5. Digital loop-back: RX digital output buffer (16-bit word) is internally connected to the TX/EC digital input buffer.  
6. The input digital data is read back from RX output buffer without going through DAC converter.

**SCR8 – EC PAA control register**      **Address: 1000b**      **Contents at reset: 00000000b**

SCR8 shares the same format with SCR1. Check with SCR1 for detail

**SCR9 – RX offset control register[7:0]**      **Address:1001b**      **Contents at reset: 00000000b**

**SCR10 – RX offset control register [15:8]**      **Address:1010b**      **Contents at reset: 00000000b**

These two registers are concatenated to form a 16-bit word in 2s complement data format. The 16-bit word is used to adjust RX channel dc offset error. It adds to the 16-bit data from the RX digital filter before the data goes to the RX output buffer.



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## PRINCIPLES OF OPERATION

### register programming (continued)

**SCR11 – TX channel digital gain control register**    **Address: 1011b**    **Contents at reset: 00000000b**  
(see Note 7)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REGISTER VALUE (HEX) | DESCRIPTION               |
|----|----|----|----|----|----|----|----|----------------------|---------------------------|
| 0  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 19                   | TX digital gain = –0.1 dB |
| 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 18                   | TX digital gain = –0.2 dB |
| 0  | 0  | 0  | 1  | 0  | 1  | 1  | 1  | 17                   | TX digital gain = –0.3 dB |
| 0  | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 16                   | TX digital gain = –0.4 dB |
| 0  | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 15                   | TX digital gain = –0.5 dB |
| 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 14                   | TX digital gain = –0.6 dB |
| 0  | 0  | 0  | 1  | 0  | 0  | 1  | 1  | 13                   | TX digital gain = –0.7 dB |
| 0  | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 12                   | TX digital gain = –0.8 dB |
| 0  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 11                   | TX digital gain = –0.9 dB |
| 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 10                   | TX digital gain = –1 dB   |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 00                   | TX digital gain = 0 dB    |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 01                   | TX digital gain = 0.1 dB  |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 02                   | TX digital gain = 0.2 dB  |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 03                   | TX digital gain = 0.3 dB  |
| 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 04                   | TX digital gain = 0.4 dB  |
| 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 05                   | TX digital gain = 0.5 dB  |
| 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 06                   | TX digital gain = 0.6 dB  |
| 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 07                   | TX digital gain = 0.7 dB  |
| 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 08                   | TX digital gain = 0.8 dB  |
| 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 09                   | TX digital gain = 0.9 dB  |
| 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0A                   | TX digital gain = 1 dB    |
| –  | –  | –  | –  | –  | –  | –  | –  | All others           | Reserved (see Note 8)     |

NOTES: 7. Digital gain is used to compensate the TX channel gain error.

8. Performance of the codec for invalid combination of bits should not be used. The user should make no assumption that the code bits will saturate to a maximum or minimum value or wrap around to a valid combination.

**SCR12 – RX PGA1 control register**    **Address:1100b**    **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REGISTER VALUE (HEX) | DESCRIPTION    |
|----|----|----|----|----|----|----|----|----------------------|----------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 00                   | RX PGA1 = 0 dB |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 01                   | RX PGA1 = 1 dB |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 02                   | RX PGA1 = 2 dB |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 03                   | RX PGA1 = 3 dB |
| 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 04                   | RX PGA1 = 4 dB |
| 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 05                   | RX PGA1 = 5 dB |
| 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 06                   | RX PGA1 = 6 dB |
| –  | –  | –  | –  | –  | –  | –  | –  | 07–FF                | RX PGA1 = 6 dB |

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### PRINCIPLES OF OPERATION

#### register programming (continued)

**SCR13 – EC channel digital gain control register**    **Address:1101b**    **Contents at reset: 00000000b**

SCR13 has the same format as SCR11. Check with SCR11 for details.

**SCR14 – Miscellaneous control register 2**    **Address:1110b**    **Contents at reset: 00000000b**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REGISTER VALUE (HEX) | DESCRIPTION                                                                                           |
|----|----|----|----|----|----|----|----|----------------------|-------------------------------------------------------------------------------------------------------|
| 0  | 0  | 0  | 0  | –  | –  | –  | 1  |                      | One write operation reset. (see Note 9)                                                               |
| 0  | 0  | 0  | 0  | –  | –  | 1  | –  |                      | Enable FIFO                                                                                           |
| 0  | 0  | 0  | 0  | –  | 1  | –  | –  |                      | Bypass EC DHPF (25.875 kHz)                                                                           |
| 0  | 0  | 0  | 0  | 1  | –  | –  | –  |                      | ECP and ECM are connected to weakly driven mid-supply. It can only be used during EC power-down mode. |

NOTE 9: Write-synchronized operation: A 1 is written to bit D0 of SCR14 register after pin ONE\_WE is set to high. This sets the start point for the TX/EC operation. During the first WETX pulse, data is written to the TX channel. During the second WETX pulse, data is written to the EC channel. D0 of SCR14 is always self-cleared; therefore, the read-back value of bit D0 of SCR14 is always zero.

#### device initialization time

The TLV320AD11A completes all calibration and initialization in less than 1 second. This includes reference settling time ( $\approx 950 \mu\text{s}$ ), one rest after power up (1 serial frame), VCXODAC configuration (2 serial frames), TX/RX gain select (4 serial frames), and self-calibration of the DAC (256X113 ns). Each 16-bit frame requires up to 5  $\mu\text{s}$ . The host processor needs to initiate this process upon a successful power up.

#### power-down

Both hardware and software power-down modes are provided. The serial interface is operative when the codec is in power-down mode. By sending commands through serial interface, either the codec or part of the codec, can be software powered down. All the references are kept on in the software power-down mode. The codec can also be hardware powered down by setting PWDN pin to high. All the references are shut off in the hardware power-down mode. The contents of the registers will not change in either power-down modes.

#### power supply grouping recommendation

The following power supply grouping is recommended for best performance of this device. Ferrite beads are used to separate group1, group 2, and group 3 if the same 3.3-V analog power source is shared

- Group 1: AVDD\_FIL\_TX, AVDD\_FIL\_EC, AVDD1\_TX, AVDD2\_TX, AVDD1\_EC, AVDD2\_EC
- Group 2: AVDD\_FIL\_RX, AVDD\_ADC
- Group 3: AVDD\_REF
- Group 4: DVDD\_BF, DVDD\_CLK, DVDD\_LG, DVDD\_RX, DVDD\_DAC



**absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>**

|                                                              |                      |
|--------------------------------------------------------------|----------------------|
| Supply voltage, AVDD to AGND, DVDD to DGND                   | –0.3 V to 4.5 V      |
| Analog input voltage range to AGND                           | –0.3 V to AVDD+0.3 V |
| Digital input voltage range to DGND                          | –0.3 V to DVDD+0.3 V |
| Operating virtual junction temperature range, T <sub>J</sub> | –40°C to 150°C       |
| Operating free-air temperature range, T <sub>A</sub>         | –40°C to 85°C        |
| Storage temperature range, T <sub>Str</sub>                  | –65°C to 150°C       |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C                |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

**power supply**

|                |                                                                                                         | MIN | NOM | MAX | UNIT |
|----------------|---------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| Supply voltage | AVDD_FIL_TX, AVDD_FIL_EC, AVDD1_TX, AVDD2_TX, AVDD1_EC, AVDD2_EC;<br>AVDD_FIL_RX, AVDD_ADC;<br>AVDD_REF | 3   | 3.3 | 3.6 | V    |
|                | DVDD_BF, DVDD_CLK, DVDD_LG, DVDD_RX, DVDD_DAC                                                           | 3   | 3.3 | 3.6 |      |

**digital inputs**

|                                           |                           | MIN | NOM | MAX | UNIT |
|-------------------------------------------|---------------------------|-----|-----|-----|------|
| High-level input voltage, V <sub>IH</sub> | I <sub>I</sub> = 0.75 mA  | 2   |     |     | V    |
| Low-level input voltage, V <sub>IL</sub>  | I <sub>I</sub> = –0.75 mA |     |     | 0.8 |      |

**analog input**

|                           |                                                                   | MIN                | NOM | MAX | UNIT |
|---------------------------|-------------------------------------------------------------------|--------------------|-----|-----|------|
| Analog input signal range | AVDD_FIL_RX = 3.3 V. The input signal is measured single-ended.   | AVDD_FIL_RX/2±0.75 |     |     | V    |
|                           | AVDD_FIL_RX = 3.3 V. The input signal is measured differentially. | 3                  |     |     | Vp–p |

**clock inputs**

|                        |                | MIN | NOM    | MAX | UNIT |
|------------------------|----------------|-----|--------|-----|------|
| Input clock frequency  | DVDD_CLK=3.3 V |     | 35.328 |     | MHz  |
| Input clock duty cycle |                |     | 50%    |     |      |

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## 3.3 V INTEGRATED ADSL OVER POTS CODEC

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electrical characteristics over recommended operating free-air temperature range, typical at  $T_A = 25^\circ\text{C}$ ,  $f_{\text{CLKIN}} = 35.328\text{ MHz}$ , analog power supply = 3.3 V, digital power supply = 3.3 V (unless otherwise noted)

TX and EC channel (measured differentially unless otherwise noted)

| PARAMETER                                                         | TEST CONDITIONS                          | MIN   | TYP            | MAX  | UNIT |
|-------------------------------------------------------------------|------------------------------------------|-------|----------------|------|------|
| Signal bandwidth                                                  |                                          |       | 138            |      | kHz  |
| Conversion rate                                                   | OSEN pin high                            |       | 4.416          |      | MHz  |
|                                                                   | OSEN pin low                             |       | 2.208          |      |      |
| Channel gain error                                                | PAA = 0 dB, Input = 99.1875 kHz at 06 dB | −0.1  |                | 0.1  | dB   |
| PAA step gain error                                               |                                          | −0.2  |                | 0.2  | dB   |
| DC offset                                                         |                                          | −70   |                | 70   | mV   |
| Cross-talk                                                        | RX to TX channel (43.125 kHz at −1 dB)   |       | −65            |      | dB   |
| Group delay                                                       |                                          |       | 6              |      | μs   |
| Power supply reject ratio (PSRR)                                  | 200 mVpp at 99.1875 kHz                  |       | 50             |      | dB   |
| Full scale output voltage                                         | Load = 2000 Ω, single-ended measured     |       | AVDD_TX/2±0.75 |      | V    |
|                                                                   | Load = 4000 Ω, differentially measured   |       | 3              |      | Vp-p |
| <b>AC Performance</b>                                             |                                          |       |                |      |      |
| SNR Signal-to-noise ratio                                         | 43.125 kHz at −1 dB (see Note 10)        |       | 81             |      | dB   |
| THD Total harmonic distortion ratio                               |                                          |       | 86             |      | dB   |
| TSNR Signal-to-noise + harmonic distortion ratio                  |                                          |       | 80             |      | dB   |
| MT Missing-tone test (see Note 11)                                | 120.750 kHz (missing-tone)               |       | 76             |      | dB   |
| <b>Channel Frequency Response (refer to Figure 7)</b>             |                                          |       |                |      |      |
| Gain relative to gain at 99.1875<br>(25.875 kHz DHPF is bypassed) | 30 kHz                                   | −0.25 |                | 0.25 | dB   |
|                                                                   | 60 kHz                                   | −0.25 |                | 0.25 |      |
|                                                                   | 138 kHz                                  |       | −3             |      |      |
|                                                                   | 276 kHz                                  |       | −55            |      |      |

NOTES: 10. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential output with this input condition is 3 Vpp.

11. 27 tones, 25.875 to 138 kHz, 4.3125 kHz/step, −1 dB

reference outputs (see Note 12)

| PARAMETER                                  | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|--------------------------------------------|------------------|-----|-----|-----|------|
| REFP REF plus input voltage                | AVDD_REF = 3.3 V |     | 2.5 |     | V    |
| REFM REF minus input voltage               |                  |     | 0.5 |     |      |
| VMID_REF REF mid input voltage             |                  |     | 1.5 |     |      |
| VMID_ADC Receive channel mid-input voltage |                  |     | 1.5 |     |      |

NOTE 12: All the reference outputs should not be used as voltage source.

digital outputs

| PARAMETER                                 | TEST CONDITIONS           | MIN | TYP | MAX | UNIT |
|-------------------------------------------|---------------------------|-----|-----|-----|------|
| V <sub>OH</sub> High-level output voltage | I <sub>OH</sub> = 0.5 mA  | 2.4 |     |     | V    |
| V <sub>OL</sub> Low-level output voltage  | I <sub>OL</sub> = −0.5 mA |     |     | 0.6 |      |



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted), typical at  $T_A = 25^\circ\text{C}$ ,  $f_{\text{CLKIN}} = 35.328\text{ MHz}$ , analog power supply = 3.3 V, digital power supply = 3.3 V (unless otherwise noted) (continued)

**RX channel (measured differentially unless otherwise noted)**

| PARAMETER                                                           | TEST CONDITIONS                                             | MIN                        | TYP   | MAX  | UNIT |
|---------------------------------------------------------------------|-------------------------------------------------------------|----------------------------|-------|------|------|
| Signal bandwidth                                                    |                                                             |                            | 1104  |      | kHz  |
| Conversion rate                                                     |                                                             |                            | 4.416 |      | MHz  |
| Channel gain error                                                  | PGA1 = 0 dB, PGA2 = 2.5 dB,<br>Input = 99.1875 kHz at −1 dB | −1.5                       |       | 1.5  | dB   |
| PGA gain error                                                      | PGA1 (0 to 6 dB at 1 dB/step)                               | −0.2                       |       | 0.2  | dB   |
|                                                                     | PGA2 (2.5 to 14 dB at 0.25 dB/step)                         | −0.03                      |       | 0.03 |      |
| DC offset                                                           | PGA1 = 0 dB, PGA2 = 2.5 dB                                  |                            | 3     |      | mV   |
| Crosstalk                                                           | TX to RX channel (99.1875 kHz at −1 dB<br>see Note 13)      |                            | 63    |      | dB   |
| Group delay                                                         |                                                             |                            | 8     |      | μs   |
| Common mode reject ratio (CMRR)                                     | 99.1875 kHz at −1 dB                                        |                            | 70    |      | dB   |
| Power supply reject ratio (PSRR)                                    | 200 mVpp at 99.1875 kHz                                     |                            | 50    |      | dB   |
| Analog input self-bias dc voltage                                   |                                                             | AVDD_FIL_RX/2±0.75         |       |      | V    |
| Input impedance                                                     |                                                             |                            | 10    |      | kΩ   |
| AC Performance                                                      |                                                             |                            |       |      |      |
| SNR                                                                 | Signal-to-noise ratio                                       | 99.1875 kHz at 0 dB        | 68    |      | dB   |
| THD                                                                 | Total harmonic distortion ratio                             |                            | 77    |      |      |
| TSNR                                                                | Signal-to-noise + harmonic distortion ratio                 |                            | 68    |      |      |
| MT                                                                  | Missing-tone test (see Note 14)                             | 120.750 kHz (missing-tone) | 66    |      | dB   |
|                                                                     |                                                             | 750.375 kHz (missing-tone) | 66    |      |      |
| Channel Frequency Response (EQ[2:0] = 0 dB/MHz) (refer to Figure 8) |                                                             |                            |       |      |      |
| Gain relative to gain at 99.1875 kHz                                | 60 kHz                                                      | −0.25                      |       | 0.25 | dB   |
|                                                                     | 300 kHz                                                     | −0.25                      |       | 0.25 |      |
|                                                                     | 800 kHz                                                     | 1                          |       |      |      |
|                                                                     | 1000 kHz                                                    | 0.7                        |       |      |      |

NOTES: 13. The analog input test signal is a sine wave with 0 dB = 3 Vpp as the reference level.

14. 250 tones, 25.875 to 1104 kHz, 4.3125 kHz/step, 0 dB.

**VCXO DAC**

| PARAMETER                               | TEST CONDITIONS                                  | MIN | TYP     | MAX | UNIT |
|-----------------------------------------|--------------------------------------------------|-----|---------|-----|------|
| Resolution                              |                                                  |     | 12      |     | Bits |
| DNL Differential nonlinearity           |                                                  |     | $\pm 1$ |     | LSB  |
| INL Integral nonlinearity               |                                                  |     | $\pm 4$ |     | LSB  |
| Offset error                            |                                                  |     | 30      |     | mV   |
| Analog output Full scale output voltage | Load = 50 k $\Omega$ and $V_{DD} = 3.3\text{ V}$ |     | 3       |     | V    |

**power dissipation**

| PARAMETER         | TEST CONDITIONS | MIN                 | TYP | MAX | UNIT |
|-------------------|-----------------|---------------------|-----|-----|------|
| Power dissipation | Active mode     |                     | 800 | 850 | mW   |
|                   | Power-down mode | Hardware power down | 65  |     |      |
|                   |                 | Software power down | 70  |     |      |

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## 3.3 V INTEGRATED ADSL OVER POTS CODEC

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

parallel port (see Figures 2, 3, and 4)

| PARAMETER        |                                                                                                                                                                         | MIN    | TYP  | MAX | UNIT  |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------|-----|-------|
| t <sub>c1</sub>  | Period, CLKIN                                                                                                                                                           |        | 28.3 |     | ns    |
| t <sub>c2</sub>  | Cycle time, INT                                                                                                                                                         | OSEN=0 |      | 16  | CLKIN |
|                  |                                                                                                                                                                         | OSEN=1 |      | 8   |       |
| t <sub>c3</sub>  | Period, CLKOUT                                                                                                                                                          |        | 8    |     |       |
| t <sub>d1</sub>  | Delay time, keep-out zone end to $\overline{\text{INT}}\uparrow$                                                                                                        |        |      | 5   | ns    |
| t <sub>d2</sub>  | Delay time, keep-out zone end (CLKIN $\uparrow$ ) to $\overline{\text{OE}}\downarrow/\overline{\text{CS}}\downarrow$                                                    | 0      |      |     | ns    |
| t <sub>d3</sub>  | Delay time, keep-out zone end to $\overline{\text{WETX}}\downarrow/\overline{\text{CS}}\downarrow$ or $\overline{\text{WEEC}}\downarrow/\overline{\text{CS}}\downarrow$ | 0      |      |     | ns    |
| t <sub>d4</sub>  | Delay time, data valid after $\overline{\text{OE}}\downarrow/\overline{\text{CS}}\downarrow$                                                                            |        |      | 15  | ns    |
| t <sub>d5</sub>  | Delay time, data becomes Hi-Z after $\overline{\text{OE}}\uparrow/\overline{\text{CS}}\uparrow$                                                                         |        |      | 5   | ns    |
| t <sub>d6</sub>  | Delay time, keep-out zone end to SCLK/READY $\uparrow$                                                                                                                  |        | 14.2 |     | ns    |
| t <sub>d7</sub>  | Delay time, SCLK/READY $\downarrow$ to keep-out zone                                                                                                                    |        | 14.2 |     | ns    |
| t <sub>d9</sub>  | Delay time, time between the rising edge of $\overline{\text{WETX}}/\overline{\text{WEEC}}$ to the rising edge of $\overline{\text{CS}}$                                | 5      |      |     | ns    |
| t <sub>h1</sub>  | Hold time, data valid after $\overline{\text{WETX}}\uparrow$                                                                                                            | 5      |      |     | ns    |
| t <sub>h2</sub>  | Hold time, data valid after $\overline{\text{WEEC}}\uparrow$                                                                                                            | 5      |      |     | ns    |
| t <sub>h3</sub>  | Hold time, SYNC keep high after CLKIN $\uparrow$                                                                                                                        | 5      |      |     | ns    |
| t <sub>su1</sub> | Setup time, data valid before $\overline{\text{WETX}}\uparrow$                                                                                                          | 15     |      |     | ns    |
| t <sub>su2</sub> | Setup time, data valid before $\overline{\text{WEEC}}\uparrow$ or second $\overline{\text{WETX}}\uparrow$                                                               | 15     |      |     | ns    |
| t <sub>su3</sub> | Setup time, SYNC is high before CLKIN $\uparrow$                                                                                                                        | 10     |      |     | ns    |
| t <sub>w1</sub>  | Pulse width, keep-out zone time                                                                                                                                         |        | 1    |     | CLKIN |
| t <sub>w2</sub>  | Pulse width, $\overline{\text{OE}}$                                                                                                                                     | 20     |      |     | ns    |
| t <sub>w3</sub>  | Pulse width, $\overline{\text{WETX}}$ or $\overline{\text{WETX}}$ first pulse                                                                                           | 28     |      |     | ns    |
| t <sub>w4</sub>  | Pulse width, $\overline{\text{WEEC}}$ or $\overline{\text{WETX}}$ second pulse                                                                                          | 28     |      |     | ns    |
| t <sub>w5</sub>  | Pulse width, SYNC                                                                                                                                                       |        | 28   |     | ns    |

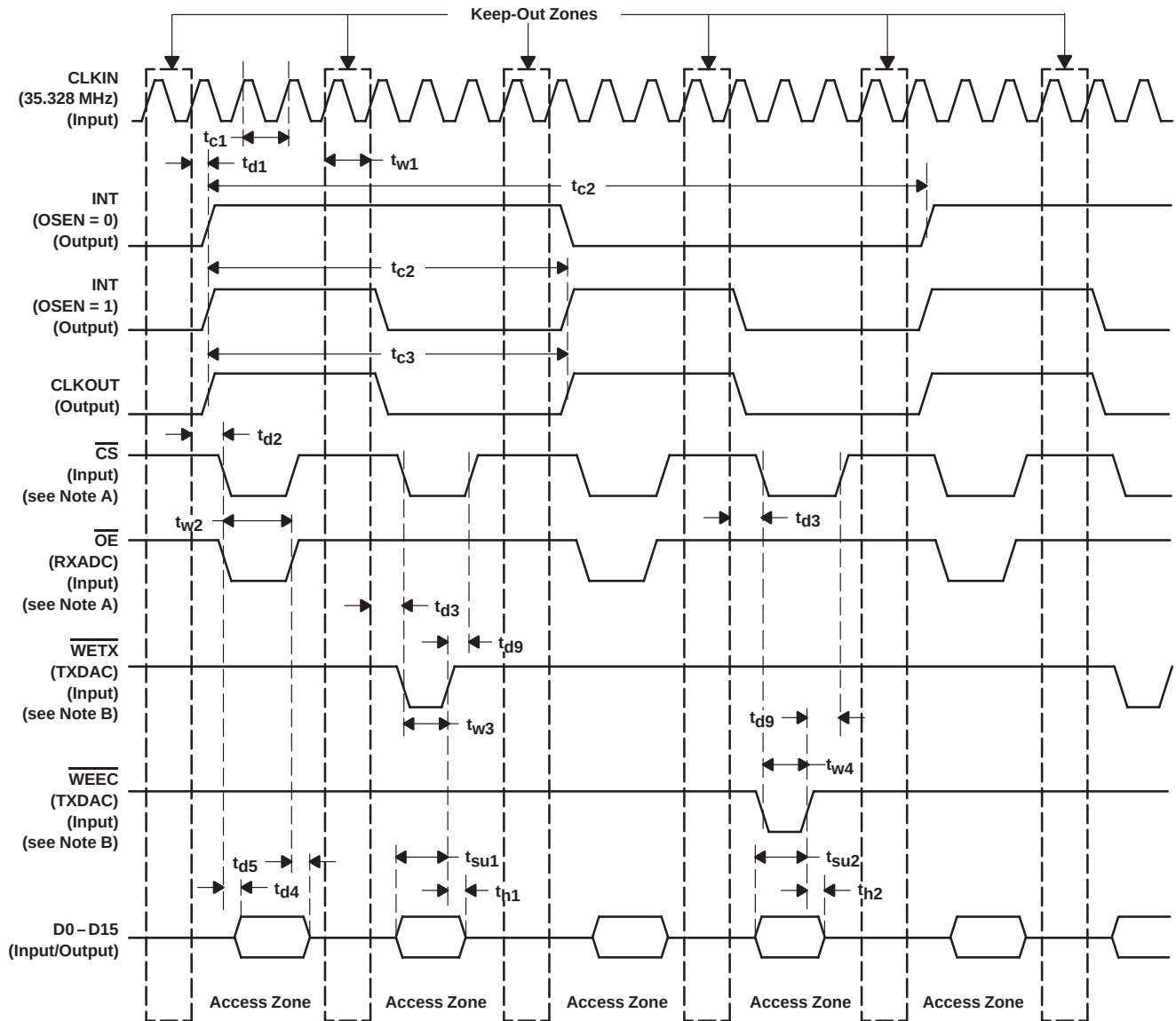
serial port (see Figure 6)

| PARAMETER        |                                                 | MIN | TYP | MAX | UNIT  |
|------------------|-------------------------------------------------|-----|-----|-----|-------|
| t <sub>c4</sub>  | Cycle time, SCLK                                |     | 8   |     | CLKIN |
| t <sub>d8</sub>  | Delay time, SCLK rising edge to SDO valid       |     |     | 15  | ns    |
| t <sub>h4</sub>  | Hold time, FS keep high after SCLK $\downarrow$ | 5   |     |     | ns    |
| t <sub>h5</sub>  | SDI valid after SCLK $\downarrow$               | 5   |     |     | ns    |
| t <sub>su4</sub> | Setup time, FS valid before SCLK $\downarrow$   | 20  |     |     | ns    |
| t <sub>su5</sub> | SDI valid before SCLK $\downarrow$              | 20  |     |     | ns    |
| t <sub>w6</sub>  | FS pulse width                                  |     | 28  |     | ns    |



## PARAMETER MEASUREMENT INFORMATION

CONFIG2=0 or floating



- NOTES: A.  $\overline{CS}$  AND  $\overline{OE}$  may fall/rise together or be skewed from each other. It does not matter which falls/rises first. However,  $t_{d4}$  is referenced from whichever falls last, and  $t_{d5}$  is referenced from whichever rises first.  $\overline{CS}$  can be connected to low if the parallel bus is not shared.
- B.  $\overline{CS}$  and  $\overline{WETX}/\overline{WEEC}$  may fall together or be skewed from each other. But the rising edge of  $\overline{WETX}$  and  $\overline{WEEC}$  should occur prior to the rising edge of  $\overline{CS}$ .
- C. The minimum update rate for TX and EC channel is 276 kHz in normal mode, and 552 kHz in over-sampling mode. The write operation for Tx and EC can occur at any time, if they do not conflict with each other or the Rx read cycle.

Figure 2. Parallel Timing Diagram

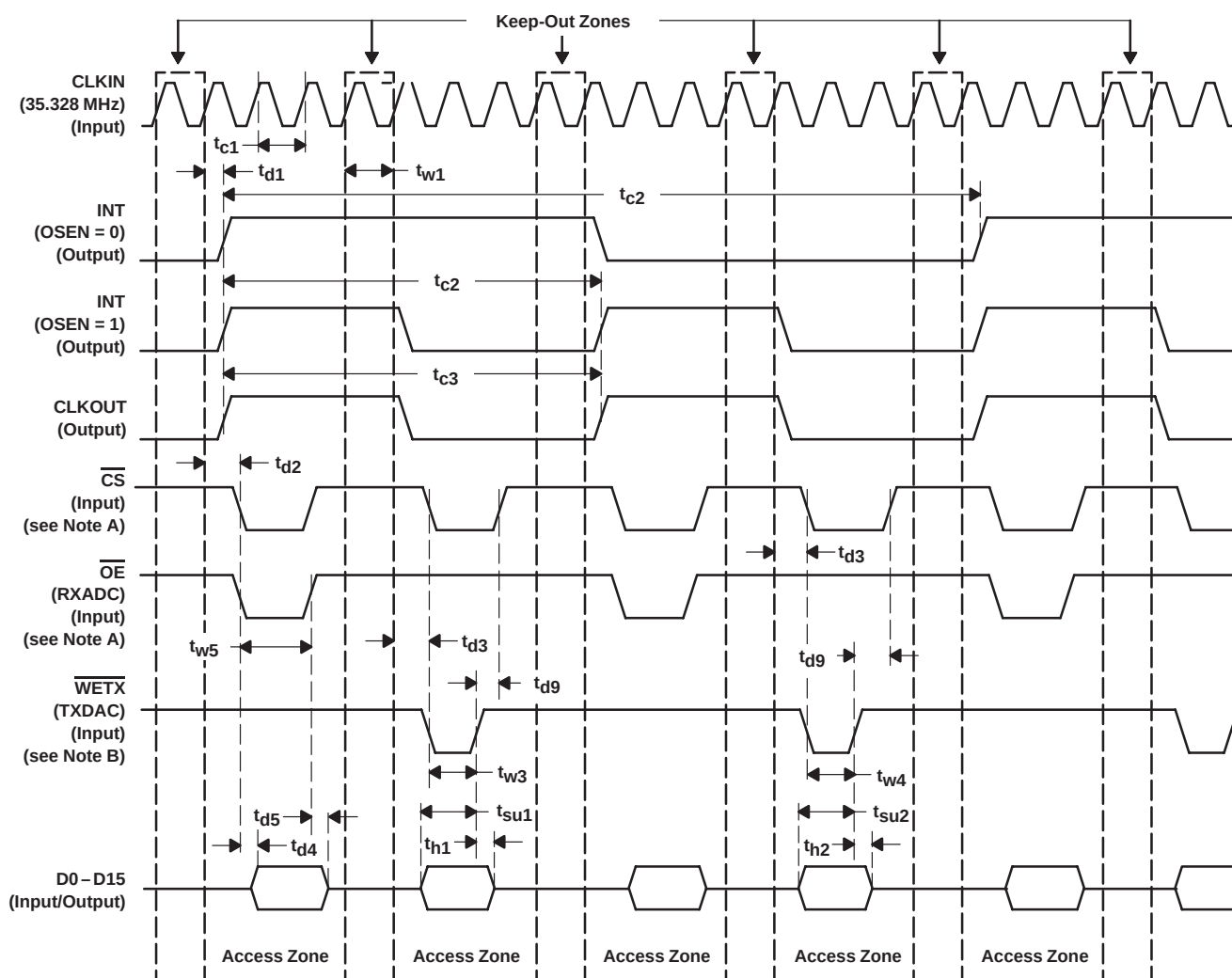
# TLV320AD11A

## 3.3 V INTEGRATED ADSL OVER POTS CODEC

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### PARAMETER MEASUREMENT INFORMATION

CONFIG2=1 and ONE\_WE selected



- NOTES:
- A.  $\overline{CS}$  AND  $\overline{OE}$  may fall/rise together or be skewed from each other. It does not matter which falls/rises first. However,  $t_{d4}$  is referenced from whichever falls last, and  $t_{d5}$  is referenced from whichever rises first.  $\overline{CS}$  can be connected to low if the parallel bus is not shared.
  - B.  $\overline{CS}$  and  $\overline{WETX}$  may fall together or be skewed from each other. But the rising edge of  $\overline{WETX}$  and  $\overline{WEEC}$  should occur prior to the rising edge of  $\overline{CS}$ .
  - C. The minimum update rate for TX and EC channel is 276 kHz in normal mode, and 552 kHz in over-sampling mode. The write operation for Tx and EC can occur at any time, if they do not conflict with each other or the Rx read cycle.

Figure 3. Parallel Timing Diagram

# PARAMETER MEASUREMENT INFORMATION

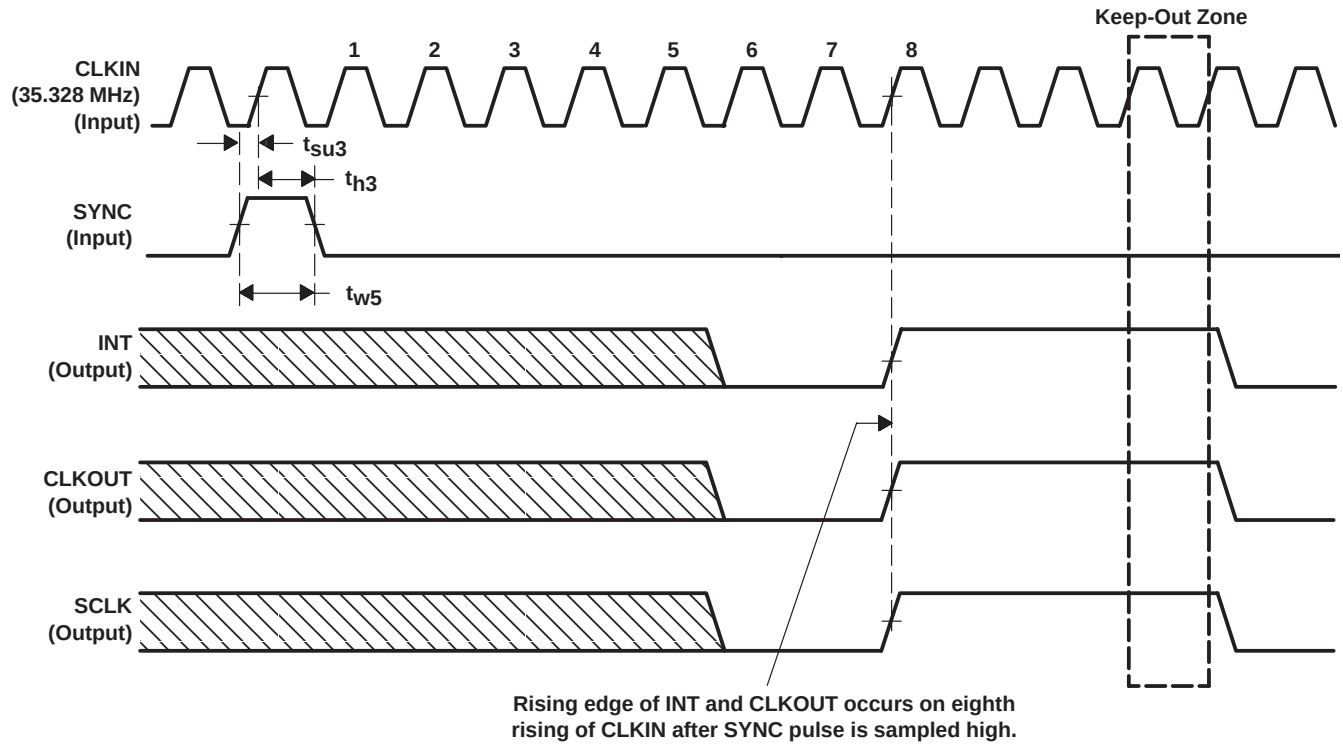
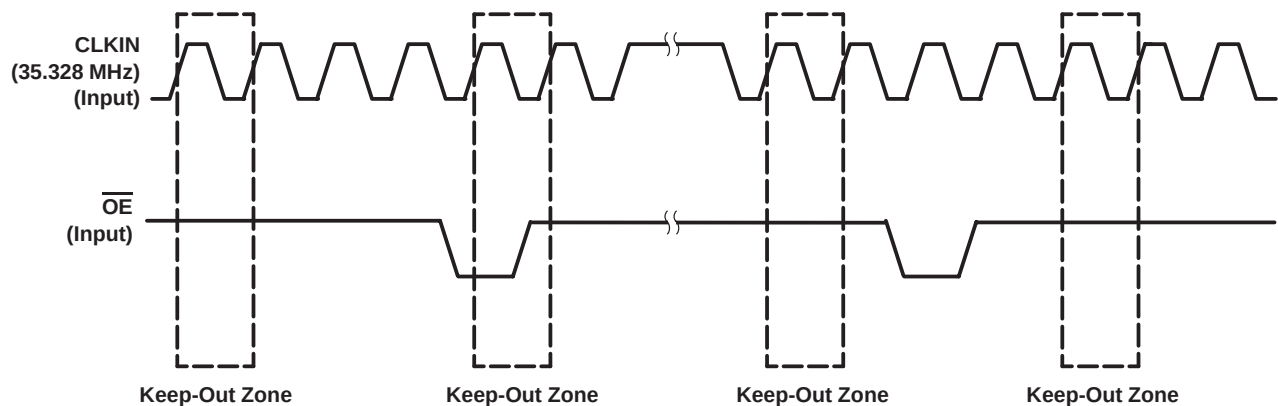


Figure 4. SYNC Pulse Timing



- NOTES: A. It takes about 16 CLKINs to shift the keep-out-zone out of the  $\overline{OE}$  pulse.  
B.  $\overline{OE}$  need to be periodic signal.

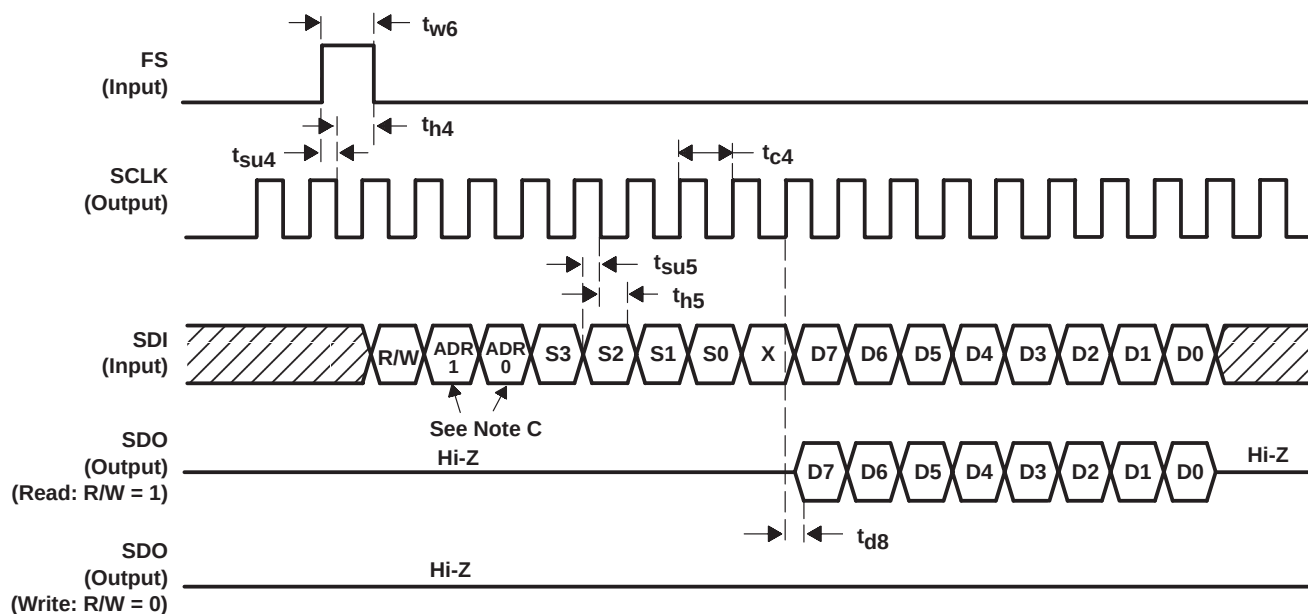
Figure 5. OE\_SYNC Pulse Timing (OE\_SYNC is set to high)

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### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Data on SDI is latched at the falling edge of SCLK.  
 B. Data is sent to SDO at the rising edge of SCLK.  
 C. ADR0 and ADR1 are the hardware configurable of ADR0 and ADR1 input pins.

Figure 6. Serial Port Timing

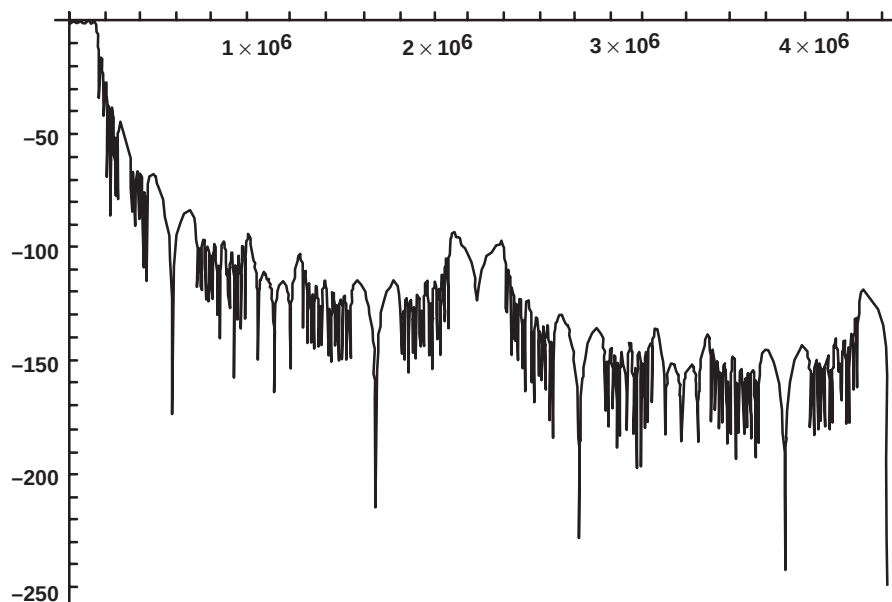


Figure 7. TX/EC Channel Filter Response (25.875 kHz DHPF is bypassed)

PARAMETER MEASUREMENT INFORMATION

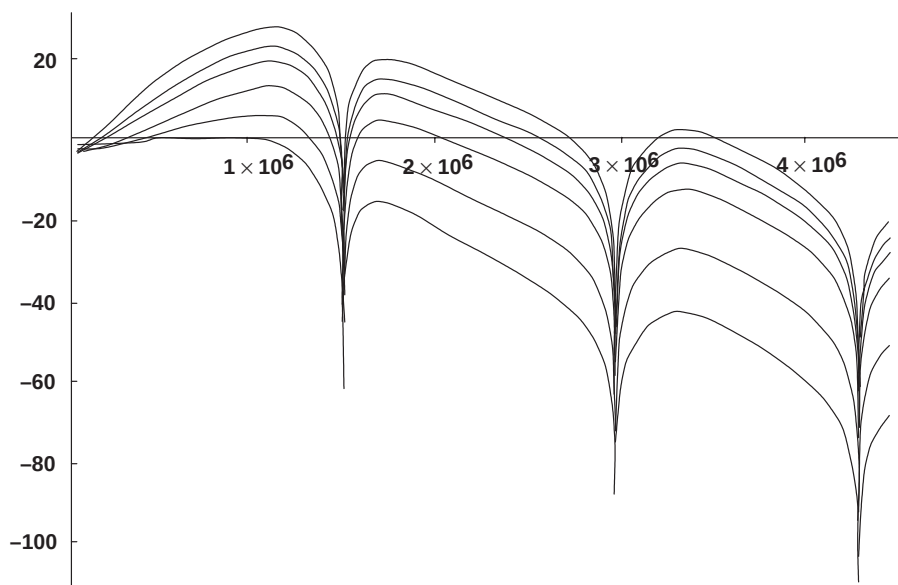


Figure 8. RX Channel Filter Response With Different Equalizer Setting

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### APPLICATION INFORMATION

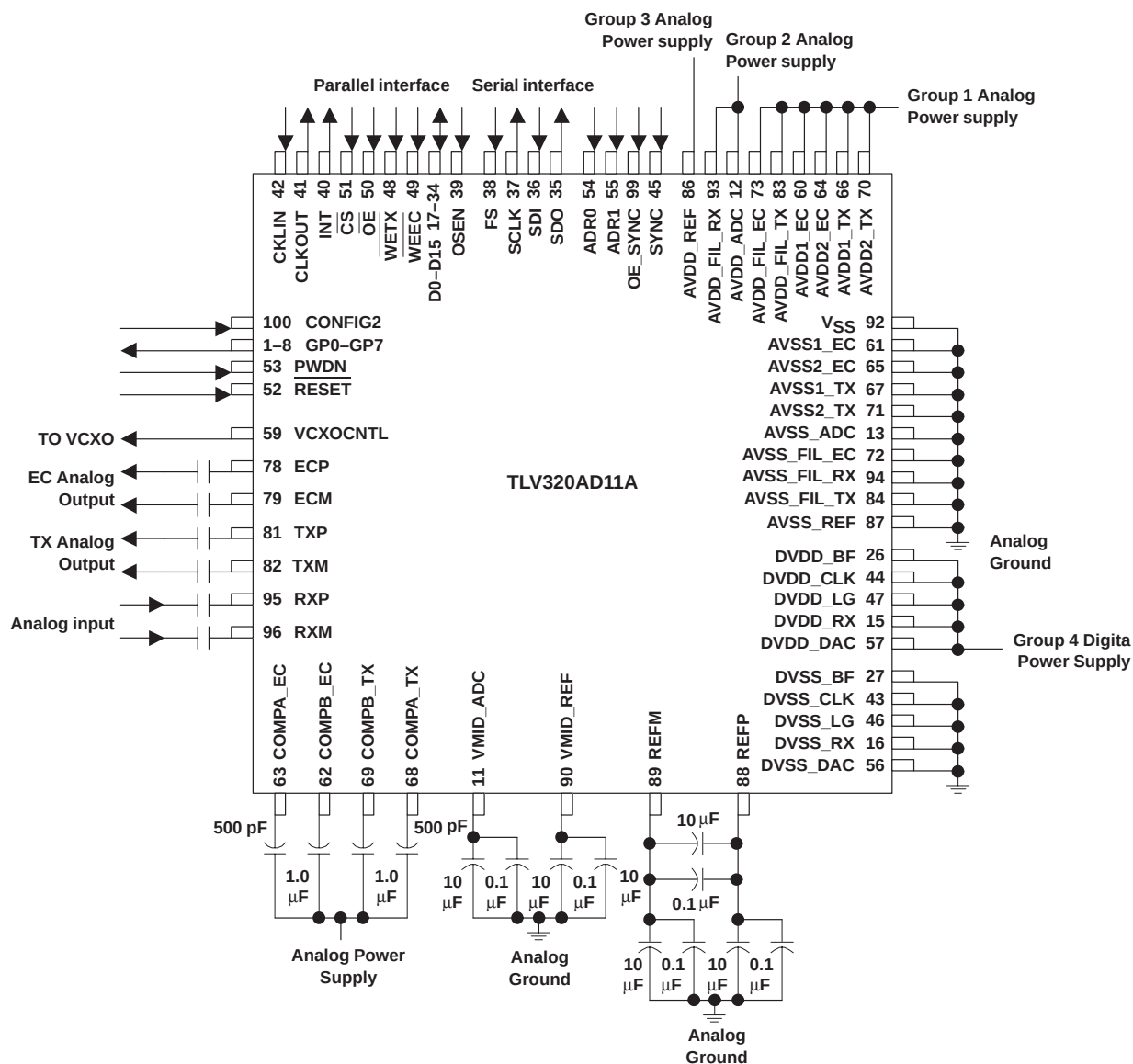
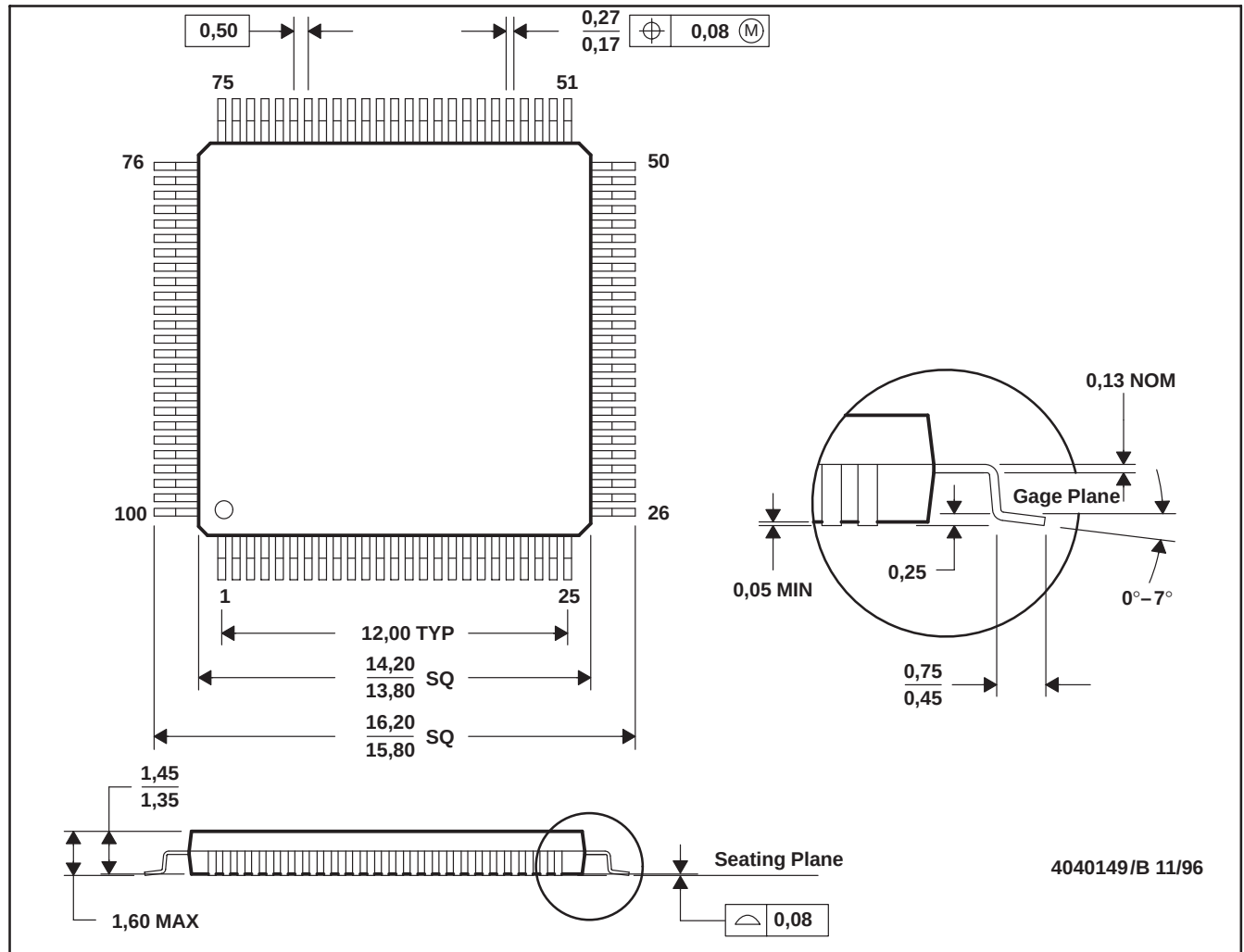


Figure 9. Typical Chip Configuration

MECHANICAL DATA

PZ (S-PQFP-G100)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Falls within JEDEC MS-026

thermal resistance characteristics (S-PQFP package)

| NO |                                       | °C/W | AIR FLOW<br>LFPM |
|----|---------------------------------------|------|------------------|
| 1  | R1 <sub>JC</sub> Junction-to-case     | 5.40 | N/A              |
| 2  | R1 <sub>JC</sub> Junction-to-free air | 30.4 | 0                |
| 3  | R1 <sub>JC</sub> Junction-to-free air | 24.2 | 100              |
| 4  | R1 <sub>JC</sub> Junction-to-free air | 22.3 | 250              |
| 5  | R1 <sub>JC</sub> Junction-to-free air | 20   | 500              |

† LFPM - Linear feet per minute

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