256MB DDR SDRAM MODULE

(32Mx64 based on 32Mx8 DDR SDRAM)

Unbuffered 184pin DIMM
64-bit Non-ECC/Parity

Revision 0.3

May. 2002

Revision History

Revision 0 (Oct 2001)

1. First release for internal usage

Version 0.1(November,2001)

- Revised "Absolute maximum rating" table in page 38.
  . Changed "Voltage on VDDQ supply relative to VSS" value from -0.5~3.6V to -1~3.6V
  . Changed "power dissipation" value from 8W to 12W.
- Revised AC parameter table

	From						To					
	DDR266A		DDR266B		DDR200		DDR266A		DDR266B		DDR200	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
tHZ	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8
tLZ	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8
tWPST (tCK)	0.25		0.25		0.25		0.4	0.6	0.4	0.6	0.4	0.6
tPDEX	10ns		10ns		10ns		7.5ns		7.5ns		10ns	

Revision 0.2 (Jan, 2002)

1. Added tRAP(Active to Read w/ autoprecharge command)

Revision 0.3 (May, 2002)

1. Change pin location of A13 from pin 103 to pin 167

M368L3223CTL DDR SDRAM 184pin DIMM

32Mx64 DDR SDRAM 184pin DIMM based on 32Mx8

GENERAL DESCRIPTION

The Samsung M368L3223CTL is 32M bit x 64 Double Data Rate SDRAM high density memory modules. The Samsung M368L3223CTL consists of eight CMOS 32M x 8 bit with 4banks Double Data Rate SDRAMs in 66pin TSOP-II(400mil) packages mounted on a 184pin glass-epoxy substrate. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The M368L3223CTL is Dual In-line Memory Modules and inten-ded for mounting into 184pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

• Performance range

Part No.	Max Freq.	Interface
M368L3223CTL-C(L)B3	167MHz(6.0ns@CL=2.5)	SSTL_2
M368L3223CTL-C(L)A2	133MHz(7.5ns@CL=2)	
M368L3223CTL-C(L)B0	133MHz(7.5ns@CL=2.5)	

• Power supply : Vdd: 2.5V ± 0.2V, Vddq: 2.5V ± 0.2V
• Double-data-rate architecture; two data transfers per clock cycle
• Bidirectional data strobe(DQS)
• Differential clock inputs(CK and $\overline{CK}$)
• DLL aligns DQ and DQS transition with CK transition
• Programmable Read latency 2, 2.5 (clock)
• Programmable Burst length (2, 4, 8)
• Programmable Burst type (sequential & interleave)
• Edge aligned data output, center aligned data input
• Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
• Serial presence detect with EEPROM
• PCB : **Height 1250 mil**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	*/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	*/CS2	102	NC	133	DQ31	163	*/CS3
11	VSS	42	VSS	72	DQ48	103	NC	134	*CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	*CB5	165	DQ52
13	DQ9	44	*CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	*CB1	75	/CK2	106	DQ13	137	CK0	167	*A13
15	VDDQ	46	VDD	76	CK2	107	DM1	138	/CK0	168	VDD
16	CK1	47	*DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	/CK1	48	A0	78	DQS6	109	DQ14	140	*DM8	170	DQ54
18	VSS	49	*CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	*CKE1	142	*CB6	172	VDDQ
20	DQ11	51	*CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	*BA2	144	*CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

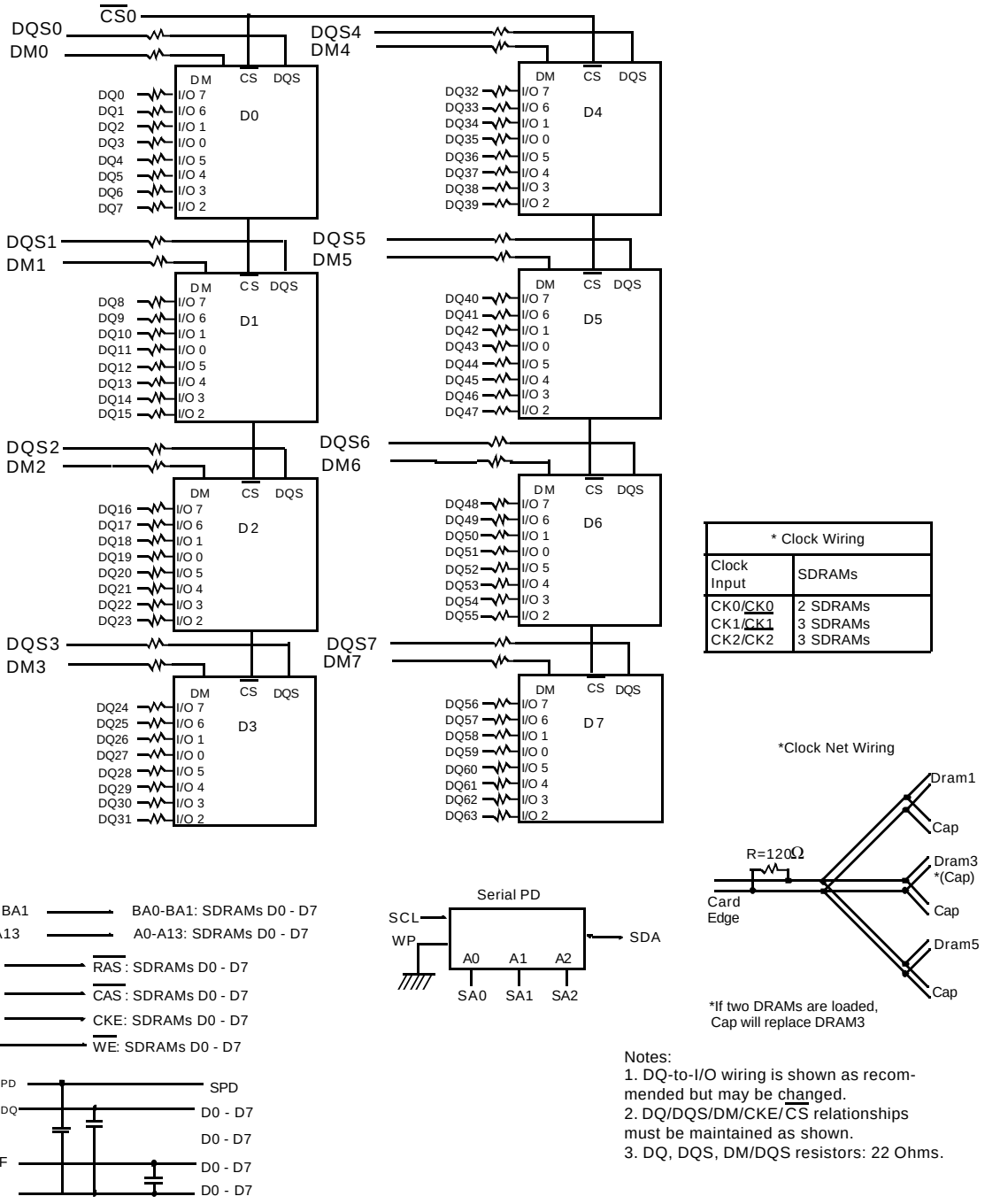
PIN DESCRIPTION

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Bank Select Address
DQ0 ~ DQ63	Data input/output
DQS0 ~ DQS7	Data Strobe input/output
CK0,$\overline{CK0}$ ~ CK2, $\overline{CK2}$	Clock input
CKE0	Clock enable input
$\overline{CS0}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DM0 ~ DM7	Data - in mask
VDD	Power supply (2.5V)
VDDQ	Power Supply for DQS(2.5V)
VSS	Ground
VREF	Power supply for reference
VDDSPD	Serial EEPROM Power Supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
VDDID	VDD identification flag
NC	No connection

* These pins are not used in this module.

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Functional Block Diagram



* Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	2 SDRAMs
CK1/CK1	3 SDRAMs
CK2/CK2	3 SDRAMs

*Clock Net Wiring

*If two DRAMs are loaded, Cap will replace DRAM3

BA0 - BA1 → BA0-BA1: SDRAMs D0 - D7
A0 - A13 → A0-A13: SDRAMs D0 - D7
$\overline{RAS}$ → $\overline{RAS}$: SDRAMs D0 - D7
$\overline{CAS}$ → $\overline{CAS}$: SDRAMs D0 - D7
CKE0 → CKE: SDRAMs D0 - D7
$\overline{WE}$ → $\overline{WE}$: SDRAMs D0 - D7

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/$\overline{CS}$ relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}	-1.0 ~ 3.6	V
Voltage on V_{DDQ} supply relative to Vss	V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	12	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS (SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{DD} of 2.5V)	V_{DD}	2.3	2.7		
I/O Supply voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	VDDQ/2-50mV	VDDQ/2+50mV	V	1
I/O Termination voltage(system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	4
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.15	V	4
Input Voltage Level, CK and $\overline{CK}$ inputs	V_{IN}(DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	V_{ID}(DC)	0.3	V_{DDQ}+0.6	V	3
Input crossing point voltage, CK and $\overline{CK}$ inputs	V_{IX}(DC)	1.15	1.35	V	5
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strengh driver) ;$V_{OUT} = V_{TT}$ + 0.84V	I_{OH}	-16.8		mA	
Output High Current(Normal strengh driver) ;$V_{OUT} = V_{TT}$ - 0.84V	I_{OL}	16.8		mA	
Output High Current(Half strengh driver) ;$V_{OUT} = V_{TT}$ + 0.45V	I_{OH}	-9		mA	
Output High Current(Half strengh driver) ;$V_{OUT} = V_{TT}$ - 0.45V	I_{OL}	9		mA	

Notes 1. Includes ± 25mV margin for DC offset on V_{REF}, and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤ 3nH.

2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}

3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.

5. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the dc level of the same.

6. These characterictics obey the SSTL-2 class II standards.

DDR SDRAM IDD spec table

Symbol		B3(DDR333@CL=2.5)	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	Unit	Notes
IDD0		920	760	760	mA	
IDD1		1120	960	960	mA	
IDD2P		24	24	24	mA	
IDD2F		240	216	216	mA	
IDD2Q		160	144	144	mA	
IDD3P		320	256	256	mA	
IDD3N		480	400	400	mA	
IDD4R		1480	1240	1240	mA	
IDD4W		1400	1160	1160	mA	
IDD5		1560	1440	1440	mA	
IDD6	Normal	24	24	24	mA	
	Low power	12	12	12	mA	Optional
IDD7A		2800	2280	2280	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

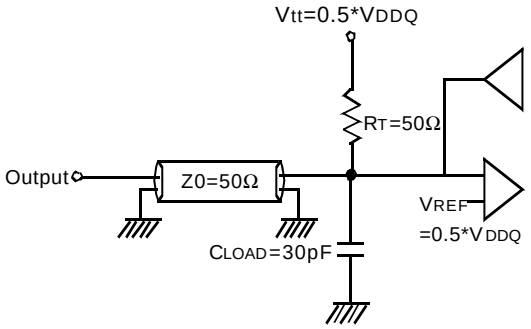
AC OPERATING CONDITIONS

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note 1. VID is the magnitude of the difference between the input level on CK and the input on $\overline{CK}$.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pim on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specificatims are refation to a Vref envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS (V_{DD}=2.5V, V_{DDQ}=2.5V, T_A= 0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * VDDQ	V	
Input signal maximum peak swing	1.5	V	
Input Levels(VIH/VIL)	VREF+0.31/VREF-0.31	V	
Input timing measurement reference level	VREF	V	
Output timing measurement reference level	Vtt	V	
Output load condition	See Load Circuit		



Output Load Circuit (SSTL_2)

Input/Output CAPACITANCE (V_{DD}=2.5V, V_{DDQ}=2.5V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A_0 ~ A_{12}, BA_0 ~ BA_1,$\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	C_{IN1}	49	57	pF
Input capacitance(CKE_0)	C_{IN2}	42	50	pF
Input capacitance($\overline{CS_0}$)	C_{IN3}	42	50	pF
Input capacitance(CLK_0, CLK_1,CLK_2)	C_{IN4}	22	25	pF
Data & DQS input/output capacitance(DQ_0~DQ_{63})	C_{OUT}	6	8	pF
Input capacitance(DM_0~DM_8)	C_{IN5}	6	8	pF

AC Timming Parameters & Specifications (These AC charicteristics were tested on the Component)

Parameter		Symbol	-TCB3 (DDR333)		-TCA2 (DDR266A)		-TCB0 (DDR266B)		Unit	Note
			Min	Max	Min	Max	Min	Max		
Row cycle time		tRC	60		65		65		ns	
Refresh row cycle time		tRFC	72		75		75		ns	
Row active time		tRAS	42	70K	45	120K	45	120K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD	18		20		20		ns	
Row precharge time		tRP	18		20		20		ns	
Row active to Row active delay		tRRD	12		15		15		ns	
Write recovery time		tWR	15		15		15		ns	
Last data in to Read command		tWTR	1		1		1		tCK	
Col. address to Col. address delay		tCCD	1		1		1		tCK	
Clock cycle time	CL=2.0	tCK	7.5	12	7.5	12	10	12	ns	5
	CL=2.5		6	12	7.5	12	7.5	12	ns	5
Clock high level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/$\overline{CK}$		tDQSCK	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns	
Output data access time from CK/$\overline{CK}$		tAC	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Data strobe edge to ouput data edge		tDQSQ	-	0.45	-	0.5	-	0.5	ns	5
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		0		ns	2
DQS-in hold time		tWPRE	0.25		0.25		0.25		tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		0.2		0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		0.2		0.2		tCK	
DQS-in high level width		tDQSH	0.35		0.35		0.35		tCK	
DQS-in low level width		tDQSL	0.35		0.35		0.35		tCK	
DQS-in cycle time		tDSC	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Address and Control Input setup time(fast)		tIS	0.75		0.9		0.9		ns	6
Address and Control Input hold time(fast)		tIH	0.75		0.9		0.9		ns	6
Address and Control Input setup time(slow)		tIS	0.8		1.0		1.0		ns	6
Address and Control Input hold time(slow)		tIH	0.8		1.0		1.0		ns	6
Data-out high impedence time from CK/$\overline{CK}$		tHZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Data-out low impedence time from CK/$\overline{CK}$		tLZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Input Slew Rate(for input only pins)		tSL(I)	0.5		0.5		0.5		V/ns	6
Input Slew Rate(for I/O pins)		tSL(IO)	0.5		0.5		0.5		V/ns	7
Output Slew Rate(x4,x8)		tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	10
Output Slew Rate Matching Ratio(rise to fall)		tSLMR	0.67	1.5	0.67	1.5	0.67	1.5		

Parameter	Symbol	-TCB3 (DDR333)		-TCA2 (DDR266A)		-TCB0 (DDR266B)		Unit	Note
		Min	Max	Min	Max	Min	Max		
Mode register set cycle time	tMRD	12		15		15		ns	
DQ & DM setup time to DQS	tDS	0.45		0.5		0.5		ns	7,8,9
DQ & DM hold time to DQS	tDH	0.45		0.5		0.5		ns	7,8,9
Control & Address input pulse width	tIPW	2.2		2.2		2.2		ns	
DQ & DM input pulse width	tDIPW	1.75		1.75		1.75		ns	
Power down exit time	tPDEX	6		7.5		7.5		ns	
Exit self refresh to non-Read command	tXSNR	75		75		75		ns	4
Exit self refresh to read command	tXSRD	200		200		200		tCK	
Refresh interval time	tREFI	7.8		7.8		7.8		us	1
Output DQS valid window	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	5
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	
Data hold skew factor	tQHS		0.55		0.75		0.75	ns	
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	3
Active to Read with Auto precharge command	tRAP	20		20		20			
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	11

1. Maximum burst refresh cycle : 8
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with t_{RCD} satisfied after this command.
5. For registered DIMMs, t_{CL} and t_{CH} are ≥ 45% of the period including both the half period jitter ($t_{JIT(HP)}$) of the PLL and the half period jitter due to crosstalk ($t_{JIT(crosstalk)}$) on the DIMM.
6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	ΔtIS	ΔtIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	ΔtDS	ΔtDH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating

I/O Input Level	ΔtDS	ΔtDH
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase tDS/tDH in the case where the input level is flat below VREF ± 310mV for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	ΔtDS	ΔtDH
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 =.4V/ns then the Delta Rise/Fall Rate =-0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guranteed by design.

11. For each of the terms, if not already an integer, round to the next highest integer. tCK is actual to the system clock cycle time.

<Reference>

The following table specifies derating values for the specifications listed if the single-ended clock skew rate is less than 1.0V/ns.

CK slew rate (Single ended)	ΔtIH/tIS (ps)	ΔtDSS/tDSH (ps)	ΔtAC/tDQSCK (ps)	ΔtLZ(min) (ps)	ΔtHZ(max) (ps)
1.0V/ns	0	0	0	0	0
0.75V/ns	+50	+50	+50	-50	+50
0.5V/ns	+100	+100	+100	-100	+100

Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

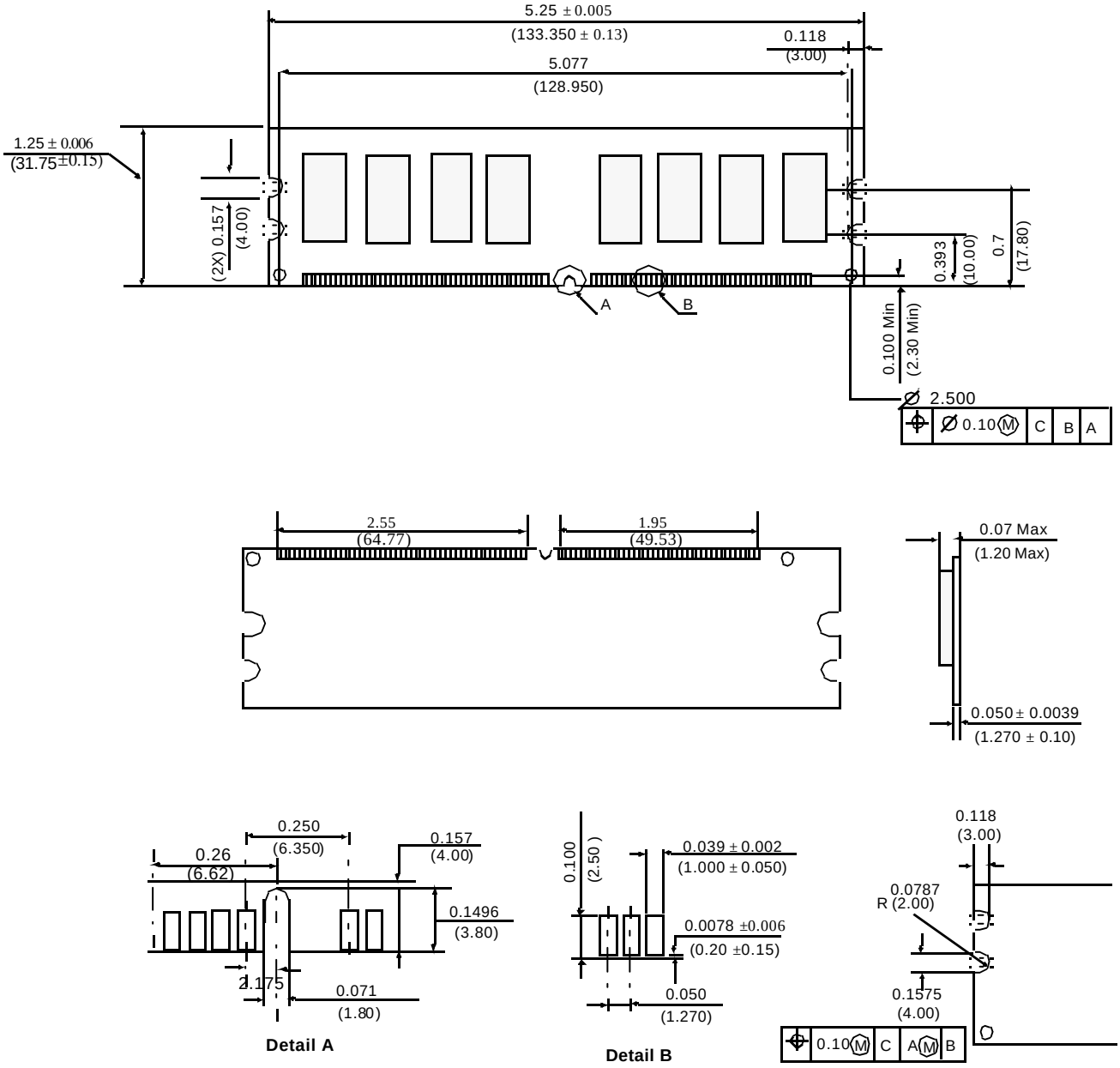
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A11, A12 A9 ~ A0	Note
Register	Extended MRS		H	X	L	L	L	L	OP CODE			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

Note : 1. OP Code : Operand Code. $A_0 \sim A_{12}$ & $BA_0 \sim BA_1$: Program keys. (@EMRS/MRS)

2. EMRS/ MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified.
The used device is 32Mx8 DDR SDRAM, TSOP.
SDRAM Part NO : K4H560838C.