NCN6024

Compact and Low Cost Smart Card Interface IC

The NCN6024 is a compact and low cost single smart card interface IC. It is dedicated for 3.0 V/5.0 V smart card reader/writer applications.

The device is fully compatible with the ISO 7816−3 and EMV standards as well as with standards specifying conditional access in Set−Top−Box (STB).

Features

- Single IC Card Interface
- Fully Compatible with ISO 7816−3, EMV and Related Standards Including STB Standards
- Three Protected Bidirectional Buffered I/O Lines (C4, C7 and C8 Card Pins)
- 3.0 V or 5.0 V ± 5% Regulated Card Power Supply such as ICC ≤ 65 mA at VDDP = 4.5 V to 5.5 V
- Independent Power Supply on Controller Interface ($2.7\ V < V_{DD} < 5.5\ V$)
- Thermal and Short Circuit Protection on all Card Pins
- Support up to 20 MHz Clock with Internal Division Ratio 1/1, 1/2, 1/4 and 1/8 through CLKDIV1 and CLKDIV2
- ESD Protection on Card Pins up to 8 kV+ (Human Body Model)
- Activation/Deactivation Sequences
- Fault Protection Mechanisms Enabling Automatic Device Deactivation in Case of Overload, Overheating, Card Take−off or Power Supply Drop−out
- Interrupt Signal $\overline{INT}$ for Card Presence and Faults
- External Undervoltage Lockout Threshold Adjustment on V_{DD} (PORADJ Pin)
- Available in 2 Package Formats: SOIC−28 and TSSOP−28
- These are Pb−Free Devices

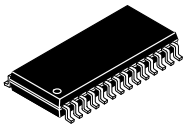
Typical Application

- Pay TV, Set Top Box Decoder with Conditional Access and Pay−per−View
- Conditional Access Module (CAM)
- Portable Systems
- Point Of Sales and Transaction Terminals
- Electronic Payment and Identification

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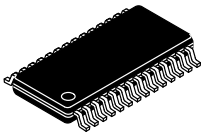
MARKING DIAGRAMS

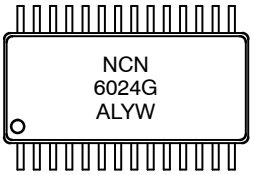




SOIC−28*
CASE 751F

*Consult Sales Office





TSSOP−28
CASE 948AA

NCN6024 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

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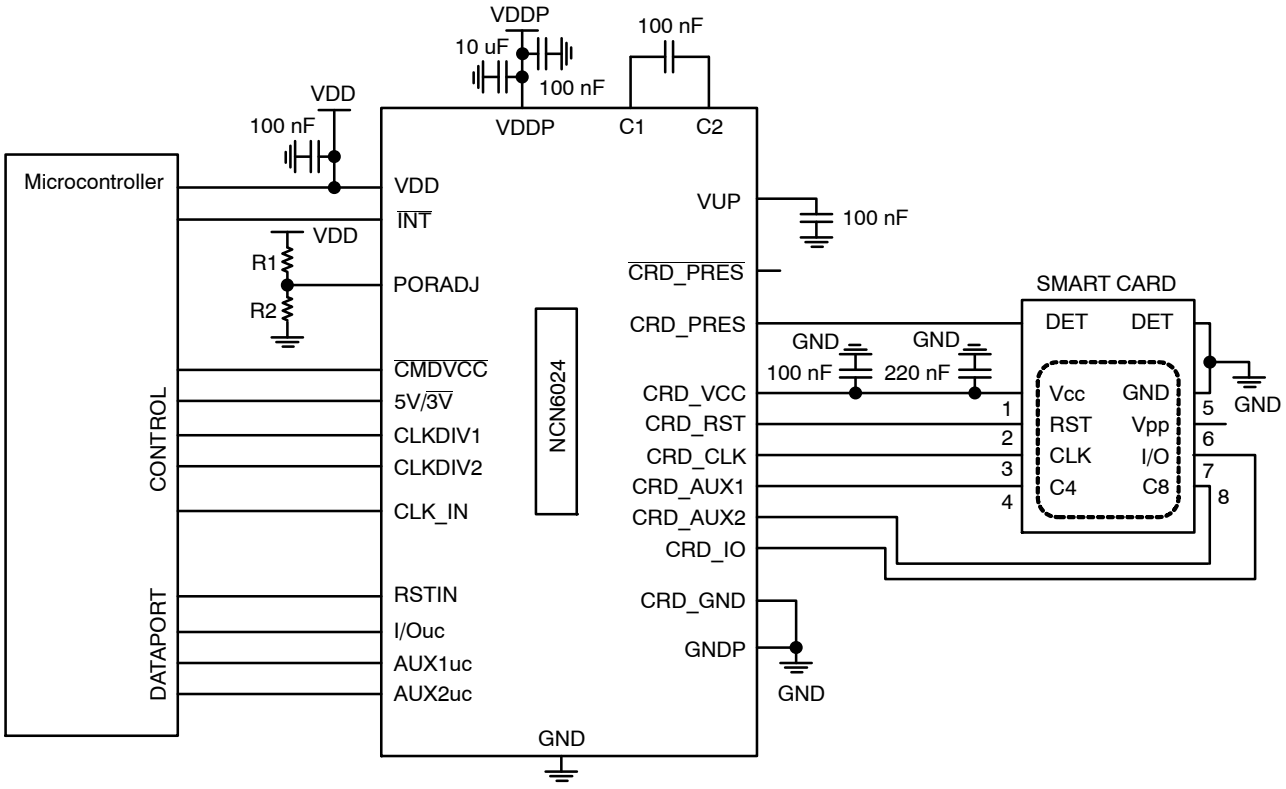


Figure 1. Typical Smart Card Interface Application

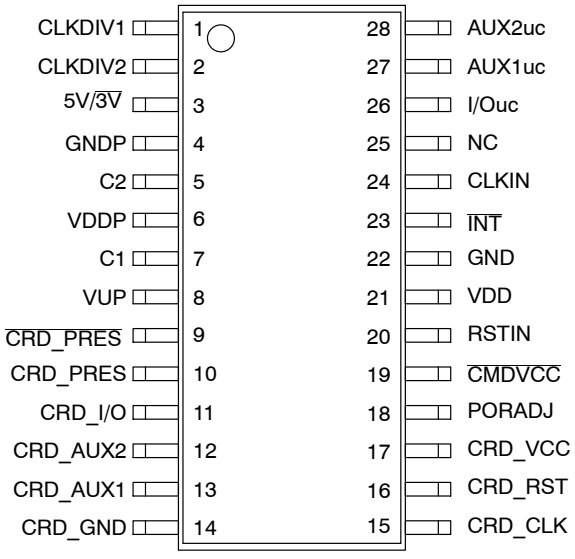


Figure 2. SOIC−28 and TSS0P−28 Pinout (Top View)

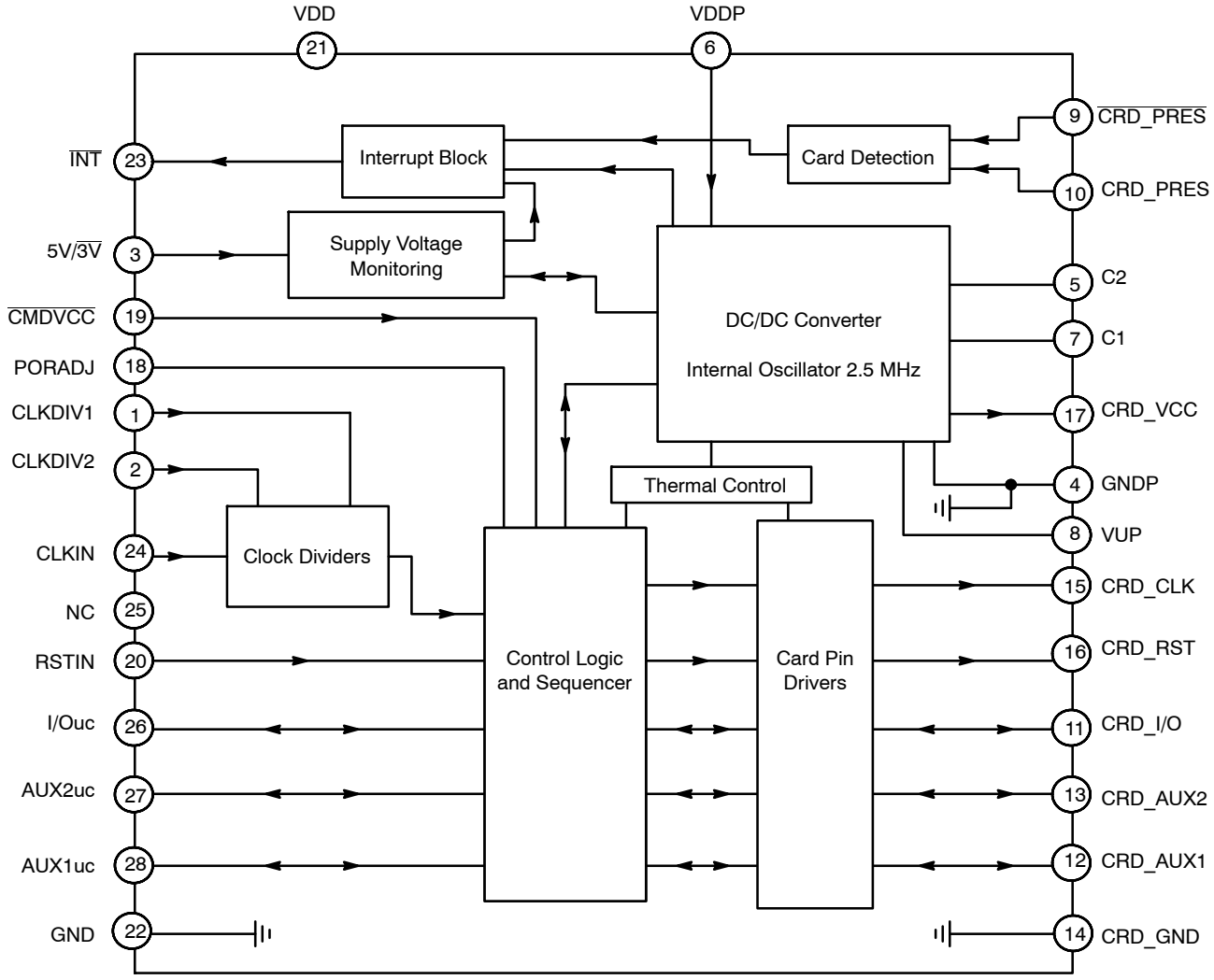


Figure 3. NCN6024 Block Diagram

PIN FUNCTION AND DESCRIPTION

Pin #	Name	Type	Description
1	CLKDIV1	Input	This pin coupled with CLKDIV2 is used to program the clock frequency division ratio (Table 1).
2	CLKDIV2	Input	This pin coupled with CLKDIV1 is used to program the clock frequency division ratio (Table 1).
3	5V/$\overline{3V}$	Input	Allows selecting card V_{CC} power supply voltage. CRD_VCC = 5 V when 5V/$\overline{3V}$ = HIGH or 3 V when 5V/$\overline{3V}$ = LOW
4	GNDP	GND	DC/DC Converter Power Supply Ground
5	C2	Power	DC/DC Converter Capacitor pin number 2 − A 100 nF capacitor is connected between this pin and pin C1. The capacitor has to feature an ESR lower than 100 mΩ
6	VDDP	Power	DC/DC Converter Power Supply Voltage
7	C1	Power	DC/DC Converter Capacitor pin number 1 − A 100 nF capacitor is connected between this pin and pin C2. The capacitor has to feature an ESR lower than 100 mΩ
8	VUP	Power	Charge−pump output tank capacitor − a very low ESR 100 nF capacitor (ESR< 100 mΩ) is connected between this pin and GNDP
9	$\overline{CRD_PRES}$	Input	Card presence pin active (card present) when $\overline{CRD_PRES}$ = Low. A built−in debounce timer of about 8 ms is activated when a card is inserted.
10	CRD_PRES	Input	Card presence pin active (card present) when CRD_PRES = High. A built−in debounce timer of about 8 ms is activated when a card is inserted.

PIN FUNCTION AND DESCRIPTION

Pin #	Name	Type	Description
11	CRD_I/O	Input/ Output	This pin handles the connection to the serial I/O (C7) of the card connector. A bi−directional level translator adapts the serial I/O signal between the card and the micro controller. A 13 kΩ (typical) pullup resistor to CRD_VCC provides a High impedance state for the smart card I/O link.
12	CRD_AUX2	Input/ Output	This pin handles the connection to the chip card's serial auxiliary AUX2 I/O pin (C8). A bi−directional level translator adapts the serial I/O signal between the card and the micro controller. A 13 kΩ (typical) pullup resistor to CRD_VCC provides a High impedance state for the smart card C8 pin.
13	CRD_AUX1	Input/ Output	This pin handles the connection to the chip card's serial auxiliary AUX1 I/O pin (C4). A bi−directional level translator adapts the serial I/O signal between the card and the micro controller. An 13 kΩ (typical) pullup resistor to CRD_VCC provides a High impedance state for the smart card C4 pin.
14	CRD_GND	GND	Card Ground
15	CRD_CLK	Output	This pin is connected to the CLOCK card connector's pin (Chip card's pin C3). The Clock signal comes from the CLKIN input through clock dividers and level shifter.
16	CRD_RST	Output	This pin is connected to the chip card's RESET pin (C2) through the card connector. A level translator adapts the external Reset (RSTIN) signal to the smart card.
17	CRD_VCC	Power	This pin is connected to the smart card power supply pin. An internal DC/DC converter is programmable using the pin 5V/$\overline{3V}$ to supply either 5 V or 3 V output voltage. An external distributed ceramic capacitor ranging from 320 nF to 500 nF recommended must be connected across CRD_VCC and CRD_GND. This set of capacitor (if distributed) must be low ESR (< 100 mΩ).
18	PORADJ	Input	Power−on reset threshold adjustment input pin for changing the reset threshold due to an external resistor power divider. Needs to be connected to ground when unused.
19	$\overline{\text{CMDVCC}}$	Input	Command VCC pin. Activation sequence Enable/Disable pin (active Low). The activation sequence is enabled by toggling $\overline{\text{CMDVCC}}$ High to Low and when a card is present.
20	RSTIN	Input	This Reset input connected to the host and referred to V_{DD} (microcontroller side), is connected to the smart card Reset pin through the internal level shifter which translates the level according to the CRD_VCC programmed value.
21	VDD	Power	This pin is connected to the system controller power supply. It configures the level shifter input stage to accept the signals coming from the controller. A 0.1 μF capacitor shall be used to bypass the power supply voltage. When V_{DD} is below 2.35 V typical the card pins are disabled.
22	GND	GND	Ground
23	$\overline{\text{INT}}$	Output	The interrupt request is activated LOW on this pin. This is enabled when a card is present and the card presence is detected by CRD_PRES or $\overline{\text{CRD_PRES}}$ pins. Similarly an interrupt is generated when CRD_VCC is overloaded. 20 kΩ typical integrated pullup resistor to V_{DD}.
24	CLKIN	Input	Clock Input for External Clock
25	NC		Unconnected
26	I/Ouc	Input/ Output	This pin is connected to an external micro−controller. A bi−directional level translator adapts the serial I/O signal between the smart card and the external controller. A built−in constant 13 kΩ (typical) resistor provides a high impedance state.
27	AUX1uc	Input/ Output	This pin is connected to an external micro−controller. A bi−directional level translator adapts the serial C4 signal between the smart card and the external controller. A built−in constant 13 kΩ (typical) resistor provides a high impedance state.
28	AUX2uc	Input/ Output	This pin is connected to an external micro−controller. A bi−directional level translator adapts the serial C8 signal between the smart card and the external controller. A built−in constant 13 kΩ (typical) resistor provides a high impedance state.

ATTRIBUTES

Characteristics	Values
ESD protection Human Body Model (HBM) (Note 1) Card Pins (Card Interface Pins 9 – 17) All Other Pins Machine Model (MM) Card Pins (Card Interface Pins 9 – 17) All Other Pins	 8 kV 2 kV 400 V 150 V
Moisture sensitivity (Note 2) SOIC−28 and TSSOP−28	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch−up Test	

1. Human Body Model (HBM), R = 1500 Ω, C = 100 pF.
2. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 3)

Rating	Symbol	Value	Unit
DC/DC Converter Power Supply Voltage	V_{DDP}	$-0.3 \le VDDP \le 5.5$	V
Power Supply from Microcontroller Side	V_{DD}	$-0.3 \le VDD \le 5.5$	V
External Card Power Supply	CRD_VCC	$-0.3 \le CRD_VCC \le 5.5$	V
Charge Pump Output	V_{UP}	$-0.3 \le V_{UP} \le 5.5$	
Digital Input Pins	V_{in}	$-0.3 \le V_{in} \le V_{DD}$	V
Digital Output Pins (I/Ouc, AUX1uc, AUX2uc, $\overline{INT}$)	V_{out}	$-0.3 \le V_{out} \le V_{DD}$	V
Smart Card Output Pins	V_{out}	$-0.3 \le V_{out} \le CRD_V_{CC}$	V
Thermal Resistance Junction−to−Air SOIC−28 TSSOP−28	$R_{\theta JA}$	75 76	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+125	°C
Storage Temperature Range	T_{stg}	−65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C

POWER SUPPLY SECTION (V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25°C; F_{CLKIN} = 10 MHz)

Pin	Symbol	Rating	Min	Typ	Max	Unit
6	V_{DDP}	DC/DC Converter Power Supply, CRD_VCC = 3V and 5V, $\|I_{CC}\| \leq$ 65 mA $\|I_{CC}\| \leq$ 15 mA (Note 4)	 4.5 3.0	 5.0	 5.5 5.5	V
6	I_{DDP}	Inactive Mode	–	–	0.3	mA
6	I_{DDP}	DC Operating Supply Current, F_{CLKIN} = 10 MHz, $Cout_{CRD_CLK}$ = 33 pF, $\|I_{CRD_VCC}\|$ = 0	–	–	5.0	mA
6	I_{DDP}	DC Operating Supply Current, CRD_V_{CC} = 5 V, I_{CRD_VCC} = 65 mA CRD_V_{CC} = 3 V, I_{CRD_VCC} = 65 mA	–	–	 200 200	mA
21	V_{DD}	Operating Voltage	2.7	–	5.5	V
21	I_{VDD}	Inactive Mode 0 Standby Current	–	–	0.6	mA
21	I_{VDD}	Operating Current – F_{CLK_IN} = 10 MHz, $Cout_{CRD_CLK}$ = 33 pF, $\|I_{CRD_VCC}\|$ = 0	–	–	1	mA
21	$UVLOV_{DD}$	Undervoltage Lockout (UVLO), No External Resistor at Pin PORADJ (Connected to GND), Falling V_{DD} Level	2.25	2.35	2.45	V
21	UVLOHys	UVLO Hysteresis, No External Resistor at Pin PORADJ (Connected to GND)	50	100	150	mV
PORADJ PIN						
18	V_{PORth+}	External Rising Threshold Voltage on V_{DD} for Power On Reset – Pin PORADJ	1.18	1.25	1.32	V
18	V_{PORth-}	External Falling Threshold voltage on V_{DD} for Power On Reset – Pin PORADJ	1.11	1.18	1.24	V
18	V_{PORHys}	Hysteresis on V_{PORth} (pin PORADJ)	40	75	110	mV
18	t_{POR}	Width of Power−On Reset Pulse (Note 5) No External Resistor on PORADJ External Resistor on PORADJ	 4 4	 8 8	 12 12	ms
18	I_{IL}	Low Level Input Leakage Current, V_{IL}<0.5 V (Pulldown Current Source)		5		μA
DC/DC CONVERTER						
	F_{CLK}	DC/DC Converter Clock Frequency when Card Active (Note 5)	2.6	3.5	4.5	MHz
8	V_{UP}	Output Voltage on pin V_{UP} (average value) CRD_V_{CC} = 5V CRD_V_{CC} = 3V	 5.0 5.0	 5.23 5.23	 5.5 5.5	V
17	C_{CRD_VCC}	Output Capacitance on card power supply CRD_VCC (Notes 5, 6)		320	800	nF
17	CRD_V_{CC}	Output Card Supply Voltage @ 4.5 V< V_{DDP} < 5.5 V (including ripple) CRD_V_{CC} = 3.0 V @ $I_{load} \leq$ 65 mA CRD_V_{CC} = 5.0 V @ $I_{load} \leq$ 65 mA	 2.85 4.75	 3.00 5.00	 3.15 5.25	V
17	CRD_V_{CC}	Output Card Supply Voltage @ 4.5 V< V_{DDP} < 5.5 V with Current−Load Pulses of 40 nAs/t < 400 ns and $\|I_{CC}\|$ < 200 mA Peak Current (Including Ripple) CRD_V_{CC} = 3.0 V CRD_V_{CC} = 5.0 V	 2.70 4.60	 3.00 5.00	 3.30 5.30	 V V
17	I_{CRD_VCC}	Card Supply Current @ CRD_V_{CC} = 3.0 V @ CRD_V_{CC} = 5.0 V			 65 65	mA
17	$I_{CRD_VCC_SC}$	Short−Circuit Current – CRD_V_{CC} Shorted to Ground		110	150	mA
17	ΔV_{CRD_VCC}	Output Card Supply Voltage Ripple Peak−to−Peak (Note 5)			350	mV
17	CRD_V_{CCSR}	Slew Rate on CRD_V_{CC} Up or Down (Note 5)	0.05	0.10	0.22	V/μs

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Min start−up VDDP voltage = 3.3 V.
5. Guaranteed by design and characterization.
6. These values take into account the tolerance of the cms capacitor used. The allowed values are single 330 nF or distributed 100 nF + 220 nF or 100 nF + 330 nF or distributed capacitor combination not exceeding 800 nF (470 nF + 330 nF).

DIGITAL INPUT/OUTPUT SECTION CLKIN, RSTIN, I/Ouc, AUX1uc, AUX2uc, CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, 5V/$\overline{\text{3V}}$
(V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25°C; F_{CLKIN} = 10 MHz)

Pin	Symbol	Rating	Min	Typ	Max	Unit
24	F_{CLKIN}	Clock Frequency on Pin CLKIN (with Divider Ratio ≥ 2) (Note 5)	–	–	27	MHz
1, 2, 3, 19, 20, 24, 26, 27, 28	V_{IL}	Input Voltage Level Low: CLKIN, RSTIN, I/Ouc, AUX1uc, AUX2uc, CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, 5V/$\overline{\text{3V}}$	−0.3	–	0.3 x V_{DD}	V
1, 2, 3, 19, 20, 24, 26, 27, 28	V_{IH}	Input Voltage Level High: CLKIN, RSTIN, I/O, AUX1, AUX2, CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, 5V/$\overline{\text{3V}}$	0.7 x V_{DD}	–	V_{DD} + 0.3	V
1, 2, 3, 19, 20, 24	I_{IL}	CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, RSTIN, CLKIN, 5V/3V Low Level Input Leakage Current, V_{IL} = 0 V	–	–	1.0	μA
1, 2, 3, 19, 20, 24	I_{IH}	CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, RSTIN, CLKIN, 5V/3V Low Level Input Leakage Current, V_{IH} = V_{DD}	–	–	1.0	μA
26, 27, 28	I_{IL}	I/Ouc, AUX1uc, AUX2uc Low Level Input Leakage Current, V_{IL} = 0 V	–	–	600	μA
26, 27, 28	I_{IH}	I/Ouc, AUX1uc, AUX2uc High Level Input Leakage Current, V_{IH} = V_{DD}	–	–	10	μA
26, 27, 28	V_{OH}	I/Ouc, AUX1uc, AUX2uc data channels, @ Cs ≤ 30 pF High Level Output Voltage (CRD_I/O = CRD_AUX1 = CRD_AUX2 = CRD_V_{CC}) I_{OH} = −40 μA	0.75 x V_{DD}	–	V_{DD} + 0.1	V
	V_{OL}	Low Level Output Voltage (C_I/O= CRD_AUX1 = CRD_AUX2 = 0 V) I_{OL} = +1 mA	0	–	0.3	V
	$t_{Ri/Fi}$	Input Rising/Falling Times (Note 5)	–	–	1.2	μs
	$t_{Ro/Fo}$	Output Rising/Falling Times (Note 5)	–	–	0.1	μs
26, 27, 28	F_{bidi}	Maximum Frequency through Bidirectional I/O, AUX1 and AUX2 Channels (Note 5)	–	–	1	MHz
26, 27, 28	R_{pu}	I/0uc, AUX1uc, AUX2uc Pullup Resistor	8.0	11	16	kΩ
23	V_{OH}	Output High Voltage $\overline{\text{INT}}$ @ I_{OH} = −15 μA (Source)	0.75 x V_{DD}	–	–	V
23	V_{OL}	Output Low Voltage $\overline{\text{INT}}$ @ I_{OL} = 2 mA (Sink)	0	–	0.30	V
23	R_{INT}	$\overline{\text{INT}}$ Pullup Resistor	14	20	26	kΩ

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SMART CARD INTERFACE SECTION, CRD_IO, CRD_AUX1, CRD_AUX2, CRD_CLK, CRD_RST, CRD_PRES, $\overline{\text{CRD_PRES}}$ (V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25°C; F_{CLKIN} = 10 MHz)

Pin	Symbol	Rating	Min	Typ	Max	Unit
16		CRD_RST @ CRD_V_{CC} = 3.0 V, 5.0 V				
	V_{OH}	Output RESET V_{OH} @ I_{rst} = −200 μA	0.9 x CRD_V_{CC}	–	CRD_V_{CC}	V
	V_{OL}	Output RESET V_{OL} @ I_{rst} = 200 μA	–	–	0.20	V
	V_{OH}	Output RESET V_{OH} @ I_{rst} = −20 mA	0	–	0.4	V
	V_{OL}	Output RESET V_{OL} @ I_{rst} = 20 mA	CRD_V_{CC} − 0.4	–	CRD_V_{CC}	V
	t_R	Output RESET Risetime @ C_{out} = 100 pF (Note 5)	–	–	100	ns
	t_F	Output RESET Falltime @C_{out} = 100 pF (Note 5)	–	–	100	ns
	t_d	RSTIN to CRD_RST Delay − Reset Enabled (Note 5)	–	–	2	μs
15		CRD_CLK @ CRD_V_{CC} = 3.0 V or 5.0 V				
	F_{CRDCLK}	Output Frequency (Note 5)	–	–	20	MHz
	V_{OH}	Output CRD_CLK V_{OH} @ I_{clk} = −200 μA	0.9 x CRD_V_{CC}	–	CRD_V_{CC}	V
	V_{OL}	Output CRD_CLK V_{OL} @ I_{clk} = 200 μA	0	–	+0.2	V
	V_{OH}	Output CRD_CLK V_{OH} @ I_{clk} = −70 mA	0	–	0.4	V
	V_{OL}	Output CRD_CLK V_{OL} @ I_{clk} = 70 mA	CRD_V_{CC} −0.4	–	CRD_V_{CC}	V
	F_{DC}	Output Duty Cycle (Note 5)	45	–	55	%
		Rise & Fall time (Note 5)				
	t_{rills}	Output CRD_CLK Risetime @ C_{out} = 30 pF	–	–	16	ns
	t_{ulsa}	Output CRD_CLK Falltime @ C_{out} = 30 pF	–	–	16	ns
	SR	Slew Rate @ Cout = 33 pF (Note 5)	0.2	–	–	V/ns
11, 12, 13		CRD_AUX1, CRD_AUX2, CRD_IO @ CRD_V_{CC} = 3.0 V, 5.0 V				
	V_{IH}	Input Voltage High Level	2.15	–	CRD_V_{CC}+0.3	V
	V_{IL}	Input Voltage Low Level	0.30	–	0.80	V
	I_{IL}	Low Level Input Current V_{IL} = 0 V	–	–	600	μA
	I_{IH}	High Level Input Current V_{IH} = CRD_V_{CC}	–	–	10	μA
	V_{OH}	Output V_{OH} @ I_{OH} = −40 μA	0.75 x CRD_V_{CC}	–	CRD_V_{CC}+0.1	V
	V_{OL}	Output V_{OL} @ I_{OL} = 1 mA, V_{IL} = 0 V	0	–	0.30	V
	$t_{Ri/Fi}$	Input Rising/Falling Times	–	–	1.2	μs
	$t_{Ro/Fo}$	Output Rising/Falling Times / C_{out} = 80 pF	–	–	0.1	μs
11, 12, 13	R_{PU}	CRD_AUX1, CRD_AUX2, CRD_IO Pullup Resistor	8.0	11	16	kΩ
	t_{IO}	Propagation delay IOuc −> CRD_IO and CRD_IO −> IOuc (Falling Edge) (Note 5)	–	–	200	ns
	tpu	Active pull−up pulse width buffers I/O, AUX1 & AUX2 (Note 5)	–	–	200	ns
9, 10		CRD_PRES, $\overline{\text{CRD_PRES}}$ Card Detection Digital Filter Delay: (Note 5)				μs
	T_{CRDIN}	Card Insertion	25	50	150	
	T_{CRDOFF}	Card Extraction	25	50	150	
9, 10		CRD_PRES, $\overline{\text{CRD_PRES}}$				V
	V_{IH}	Card Presence Voltage High Level	0.7 x V_{DD}		V_{DD} + 0.3	
	V_{IL}	Card Presence Voltage Low Level	−0.3		0.3 x V_{DD}	

SMART CARD INTERFACE SECTION, CRD_IO, CRD_AUX1, CRD_AUX2, CRD_CLK, CRD_RST, CRD_PRES, $\overline{\text{CRD_PRES}}$ (V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25°C; F_{CLKIN} = 10 MHz)

Pin	Symbol	Rating	Min	Typ	Max	Unit
9, 10	$\lvert I_{IH}\rvert$	CRD_PRES, $\overline{\text{CRD_PRES}}$ Low level input leakage current, $V_{IH} = V_{DD}$ CRD_PRES $\overline{\text{CRD_PRES}}$		 5	 10 1	μA
	$\lvert I_{IL}\rvert$	High level input leakage current, V_{IL} = 0 V CRD_PRES $\overline{\text{CRD_PRES}}$		 5	 1 10	
9, 10	$T_{debounce}$	Debounce Time CRD_PRES and $\overline{\text{CRD_PRES}}$ (Note 5)	5	8	11	ms
11, 12, 13, 16	I_{CRD_IO}	CRD_IO, CRD_AUX1, CRD_AUX2 Current Limitation	–	–	15	mA
15	I_{CRD_CLK}	CRD_CLK Current Limitation	–	–	70	mA
16	I_{CRD_RST}	CRD_RST Current Limitation	–	–	20	mA
	t_{act}	Activation Time (Note 5)	30	–	220	μs
	t_{deact}	Deactivation Time (Note 5)	30	–	100	μs
	Temp $_{SD}$	Shutdown Temperature	–	150	–	°C

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POWER SUPPLY

The NCN6024 smart card interface has two power supplies: VDD and VDDP.

VDD is usually common to the system controller and the interface. The applied VDD range can go from 2.7 V up to 5.5 V. If VDD goes below 2.35 V typical ($UVLO_{VDD}$) a power-down sequence is automatically performed. In that case the interrupt ($\overline{\text{INT}}$) pin is set Low.

A built−in charge−pump−based DC/DC converter followed by a Low Drop−Out (LDO) regulator is used to provide the 3 V or 5 V power supply voltage (CRD_VCC) to the card. VDDP is the converter's input voltage for which 2 voltage ranges can be considered: 3.0 V ≤ VDDP ≤ 5.5 V with ICC ≤ 15 mA and 4.5 V ≤ VDDP ≤ 5.5 V with ICC ≤ 65 mA. VUP is the charge−pump converter's output. It is connected to the LDO input. A reservoir capacitor of 100 nF is connected to VUP. CRD_VCC is the LDO output. Even if the converter can operate with a single output reservoir capacitor as low as 100 nF at CRD_VCC, it is recommended to use a capacitor of at least 320 nF in order to satisfy optimally the datasheet specifications (100 nF + 220 nF or 330 nF or 100 nF + 330 nF or 470 nF). To minimize dI/dt effects, the fly capacitor (100 nF) and the reservoir capacitors VUP and CRD_VCC have to be connected as close as possible to the corresponding device's pin and feature very low ESR values (lower than 50 mΩ). The fly capacitor is connected between C1 and C2. The decoupling capacitors on VDD and VDDP respectively 100 nF and 10 μF have also to be connected close to the respective IC pins.

The CRD_VCC pin can source up to 65 mA continuously over the VDDP range (5 V ± 10%), the absolute maximum current being internally limited below 150 mA (Typical at 110 mA). CRD_VCC can stay in the range 4.6 V – 5.30 V during current transient up to 200 mA (peak current) over less than 400 ns of current pulse duration such as the charge transient is lower than 40 nAs.

There's no specific sequence for applying VDD or VDDP. They can be applied to the interface in any sequence. After powering the device $\overline{\text{INT}}$ remains Low until a card is inserted.

SUPPLY VOLTAGE MONITORING

The supply voltage monitoring block includes the Power On Reset (POR) circuitry and the under voltage lockout (UVLO) detection (VDD voltage dropout detection). PORADJ pin allows the user, according to the considered application, to adjust the VDD UVLO threshold. If not used PORADJ pin is connected to Ground.

The input supply voltage is continuously monitored to prevent under voltage operation. At power up, the system initializes the internal logic during POR timing and no further signal can be provided or supported during this period. Such initialization takes place when the input voltage rises between 2 V to 2.6 V about typical.

The system is ready to operate when the input voltage has reached the minimum 2.7 V. Considering this, the NCN6024 will detect an Under-Voltage situation when the input supply voltage will drop below 2.35 V typical. When VDD goes down below the UVLO falling threshold a deactivation sequence is performed.

The device is inactive during power-on and power-off of the VDD supply (8 ms reset pulse).

PORADJ pin is used to modify the UVLO threshold according to the below relationship considering an external

resistor divider R1 / R2 (see block diagram Figure 1) and the PORADJ internal 5 μA pull−down current source Ipd :

$$UVLO = \frac{R1 + R2}{R2} V_{POR} + R1\ Ipd$$

If PORADJ is connected to Ground the VDD UVLO threshold (VDD falling) is typically 2.35 V. In some cases it can be interesting to adjust this threshold at a higher value and by the way increase the VDD supply dropout detection level which enables a deactivation sequence if the VDD voltage is too low.

For example, there're microcontrollers for which the minimum supply voltage insuring a correct operating is higher than 2.55 V, increasing $UVLO_{VDD}$ (VDD falling) is consequently necessary. Considering for instance a resistor bridge with R1 = 56 kΩ, R2 = 42 kΩ and V_{POR-} = 1.18 V typical the VDD dropout detection level can be increased up to:

$$UVLO = \frac{59k + 42k}{42k} V_{POR-} + 56k \times 5\ \mu A = 3.03\ V$$

The minimum dropout detection voltage should be higher than 2 V.

The maximum detection level may be up to VDD.

CLOCK DIVIDER:

The input clock can be divided by 1/1, 1/2, 1/4, or 1/8, depending upon the specific application, prior to be applied to the smart card driver. These division ratios are programmed using pins CLKDIV1 and CLKDIV2 (see Table 1). The input clock is provided externally to pin CLKIN.

Table 1. Clock Frequency Programming

CLKDIV1	CLKDIV2	F_{CRD_CLK}
0	0	CLKIN/8
0	1	CKLKIN / 4
1	0	CLKIN
1	1	CLKIN / 2

The clock input stage (CLKIN) can handle a 27 MHz maximum frequency signal (considering a division ratio ≥ 2). Of course, the ratio must be defined by the user to cope with Smart Card considered in a given application

In order to avoid any duty cycle out of the 45% / 55% range specification, the divider is synchronized by the last flip flop, thus yielding a constant 50% duty cycle, whatever be the divider ratio 1/2, 1/4 or 1/8. On the other hand, the output signal Duty Cycle cannot be guaranteed 50% if the division ratio is 1 and if the input Duty Cycle signal is not within the 46 − 56% range at the CLKIN input.

When the signal applied to CLKIN is coming from the external controller, the clock will be applied to the card under the control of the microcontroller or similar device after the activation sequence has been completed.

DATA I/O, AUX1 and AUX2 LEVEL SHIFTERS

The three bidirectional level shifters I/O, AUX1 and AUX2 adapt the voltage difference that might exist between the micro-controller and the smart card. These three channels are identical. The first side of the bidirectional level shifter dropping Low (falling edge) becomes the driver side until the level shifter enters again in the idle state pulling High CRD_IO and I/Ouc.

Passive 11 kΩ pull-up resistors have been internally integrated on each terminal of the bidirectional channel. In addition with these pull-up resistors, an active pull-up circuit provides a fast charge of the stray capacitance.

The current to and from the card I/O lines is limited internally to 15 mA and the maximum frequency on these lines is 1 MHz.

STANDBY MODE

After a Power-on reset, the circuit enters the standby mode. A minimum number of circuits are active while waiting for the microcontroller to start a session:

- All card contacts are inactive
- Pins I/Ouc, AUX1uc and AUX2uc are in the high-impedance state (11 kΩ pull−up resistor to VDD)
- Card pins are inactive and pulled Low
- Supply Voltage monitoring is active
- The internal DC/DC converter oscillator is running.

POWER-UP

In the standby mode the microcontroller can check the presence of a card using the signals $\overline{INT}$ and $\overline{CMDVCC}$ as shown in Table 2:

Table 2. Card Presence State

$\overline{INT}$	$\overline{CMDVCC}$	State
HIGH	HIGH	Card present
LOW	HIGH	Card not present

If a card is detected present ($\overline{CRD_PRES}$ or CRD_PRES active) the controller can start a card session by pulling $\overline{CMDVCC}$ Low. Card activation is run (t0, Figure 5). This Power−Up Sequence makes sure all the card related signals are LOW during the CRD_VCC positive going slope. These lines are validated when CRD_VCC is stable and above the minimum voltage specified. When the CRD_VCC voltage reaches the programmed value (3.0 V or 5.0 V), the circuit activates the card signals according to the following sequence:

- CRD_VCC is powered-up at its nominal value (t1)
- I/O, AUX1 and AUX2 lines are activated (t2)
- Then Clock channel is activated and the clock signal is applied to the card (t3)
- Finally the Reset level shifter is enabled (t4)

The clock can also be applied to the card using a RSTIN mode allowing controlling the clock starting by setting RSTIN Low (Figure 4). Before running the activation sequence, that is before setting Low $\overline{CMDVCC}$ RSTIN is set High. In these initial conditions CRD_CLK starts when RSTIN is pulled Low. This allows a precise count of clock pulses before toggling CRD_RST High for ATR (Answer To Reset) request.

The internal activation sequence activates the different channels according to a specific hardware built-it sequencing internally defined but at the end the actual activation sequencing is the responsibility of the application software and can be redefined by the micro-controller to comply with the different standards and the different ways the standards manage this activation (for example light differences exist between the EMV and the ISO7816 standards).

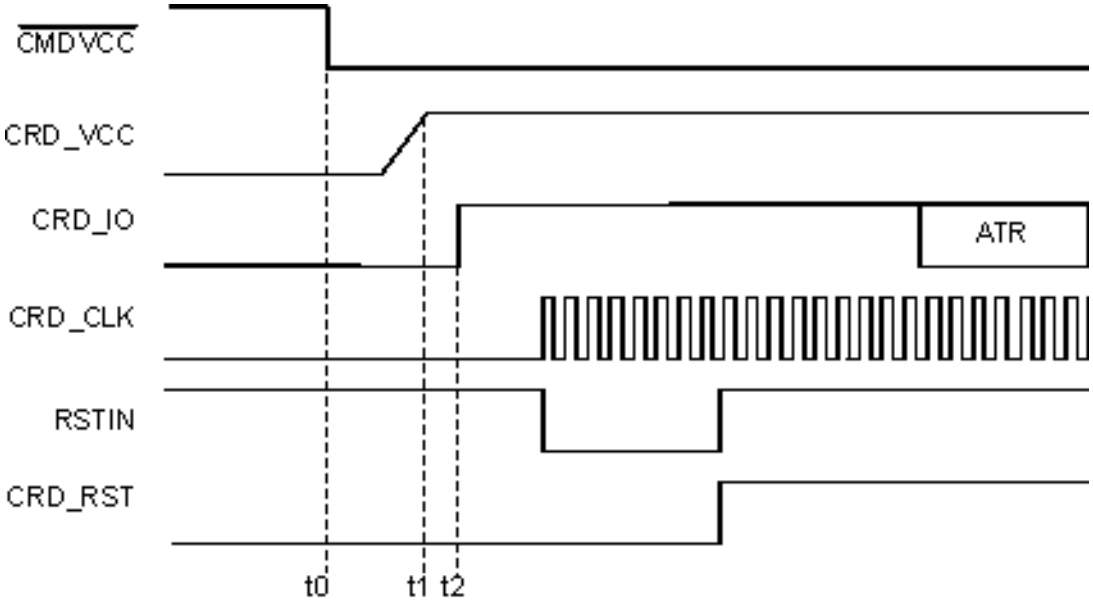


Figure 4. Activation Sequence − RSTIN mode (RSTIN Starting High)

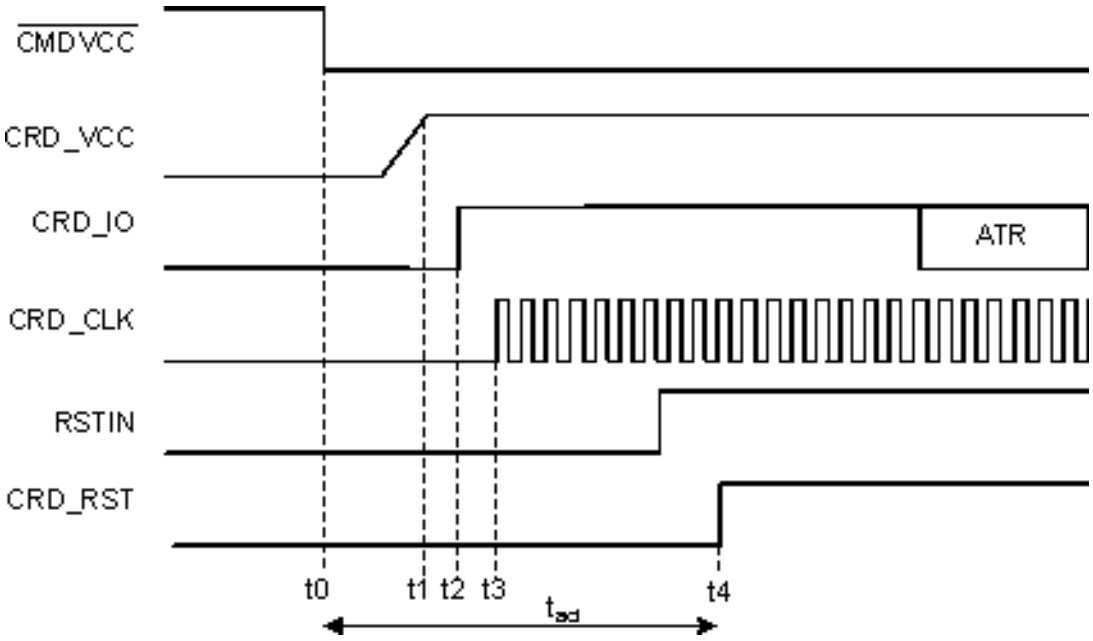


Figure 5. Activation Sequence − Normal Mode

POWER-DOWN

When the communication session is completed the NCN6024 runs a deactivation sequence by setting High $\overline{\text{CMDVCC}}$. The below power down sequence is executed:

- CRD_RST is forced to Low
- CRD_CLK is set Low 12 μs after CRD_RST.
- CRD_IO, CRD_AUX1 and CRD_AUX2 are pulled Low
- Finally CRD_VCC supply can be shut-off.

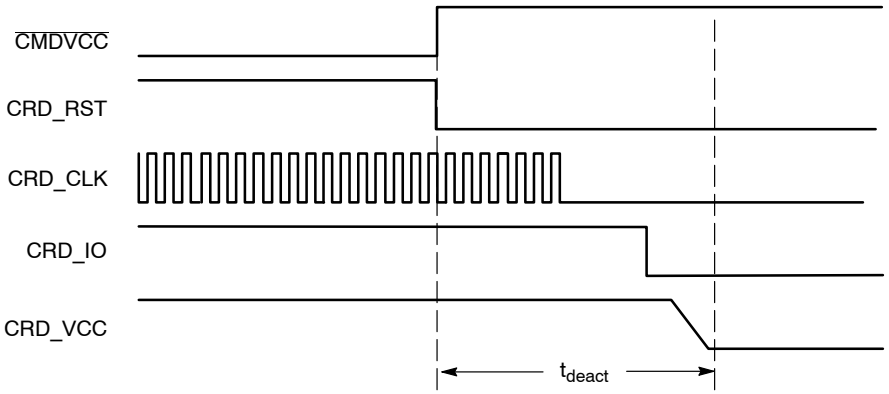


Figure 6. Deactivation Sequence

FAULT DETECTION

In order to protect both the interface and the external smart card, the NCN6024 provides security features to prevent failures or damages as depicted here after.

- Card extraction detection
- VDD under voltage detection
- Short-circuit or overload on CRD_VCC
- Card pin current limitation: in the case of a short circuit to ground. No feedback is provided to the external MPU.
- DC/DC operation: the internal circuit continuously senses the CRD_VCC voltage (in the case of either over or under voltage situation).
- DC/DC operation: under-voltage detection on VDDP or overload on VUP
- Overheating

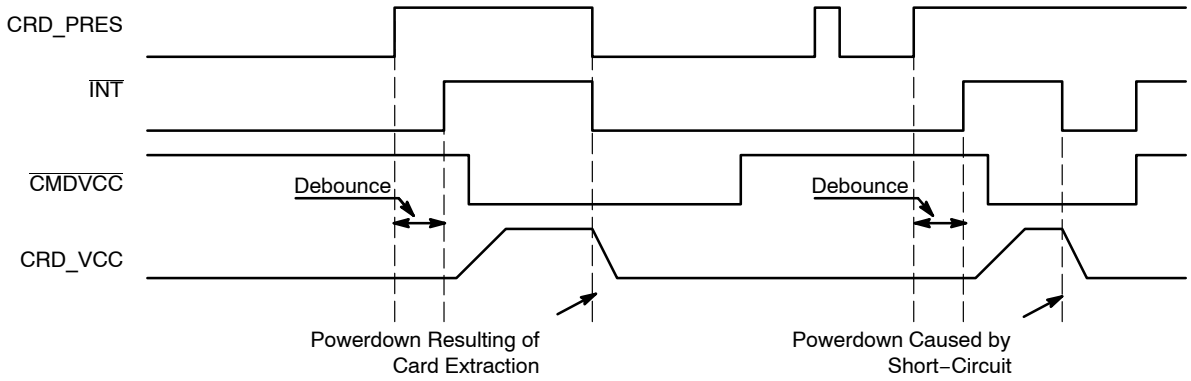


Figure 7. Fault Detection and Interrupt Management

Interrupt Pin Management:

A card session is opened by toggling $\overline{\text{CMDVCC}}$ High to Low.

Before a card session, $\overline{\text{CMDVCC}}$ is supposed to be in a High position. $\overline{\text{INT}}$ is Low if no card is present in the card connector (Normally open or normally closed type). $\overline{\text{INT}}$ is High if a card is present. If a card is inserted ($\overline{\text{INT}}$ = High) and if VDD drops below the UVLO threshold then $\overline{\text{INT}}$ pin drops Low immediately. It turns back High when VDD increases again over the UVLO limit (including hysteresis), a card being still present.

During a card session, $\overline{\text{CMDVCC}}$ is Low and $\overline{\text{INT}}$ pin goes Low when a fault is detected. In that case a deactivation is immediately and automatically performed (see Figure 6). When the microcontroller resets $\overline{\text{CMDVCC}}$ to High it can sense the $\overline{\text{INT}}$ level again after having got completed the deactivation.

As illustrated by Figure 7 the device has a debounce timer of 8 ms typical duration. When a card is inserted, output $\overline{\text{INT}}$ goes High only at the end of the debounce time. When the card is removed a deactivation sequence is automatically and immediately performed and $\overline{\text{INT}}$ goes Low.

ESD PROTECTION

The NCN6024 includes devices to protect the pins against the ESD spikes voltages. To cope with the different ESD

voltages developed across these pins, the built in structures have been designed to handle either 2 kV, when related to the micro controller side, or 8 kV when connected with the external contacts (HBM model). Practically, the CRD_RST, CRD_CLK, CRD_IO, CRD_AUX1, CRD_AUX2, CRD_PRES and $\overline{\text{CRD_PRES}}$ pins can sustain 8 kV. The CRD_VCC pin has the same ESD protection and can source up to 65 mA continuously, the absolute maximum current being internally limited with a max at 150 mA. The CRD_VCC current limit depends on VDDP and CRD_VCC.

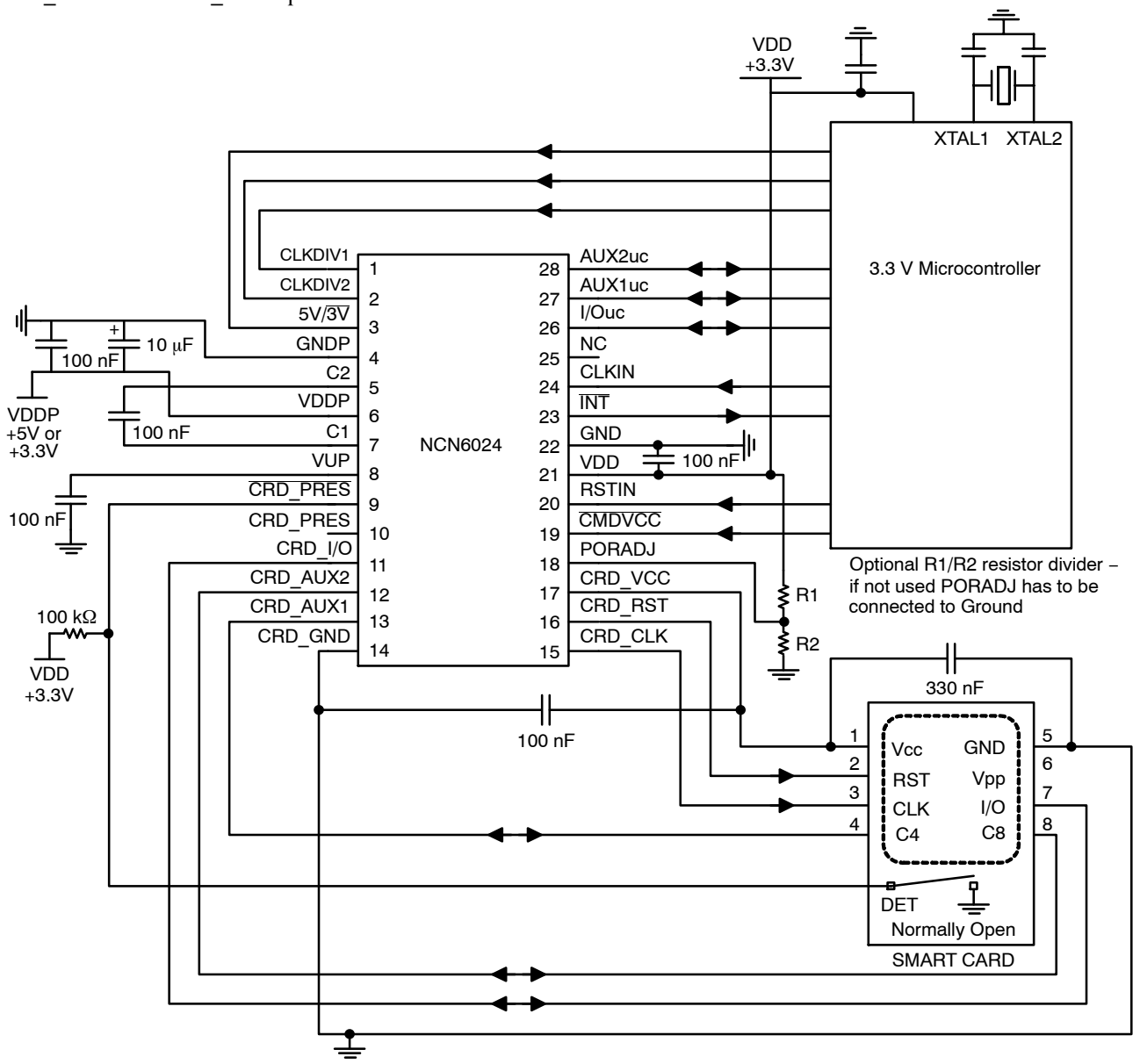


Figure 8. Application Schematic

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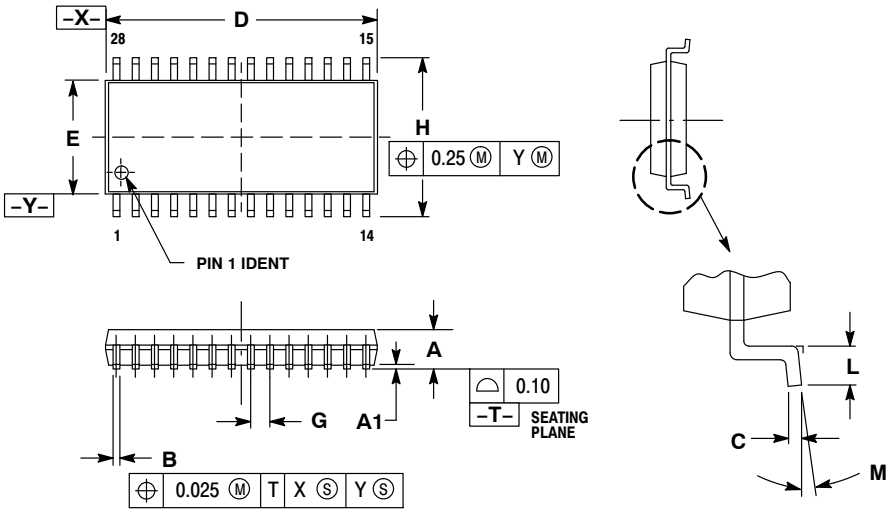
Device	Package	Shipping†
NCN6024DWR2G*	SOIC−28 (Pb−Free)	1000 / Tape & Reel
NCN6024DTBR2G	TSSOP−28 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*Consult Sales Office

PACKAGE DIMENSIONS

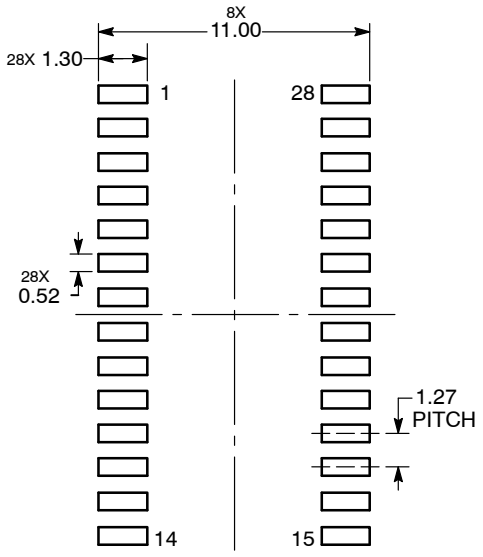
SOIC−28 WB
CASE 751F−05
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBER PR5OTRUSION SHALL NOT BE 0.13 TOTATL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
G	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
M	0 °	8 °

SOLDERING FOOTPRINT*

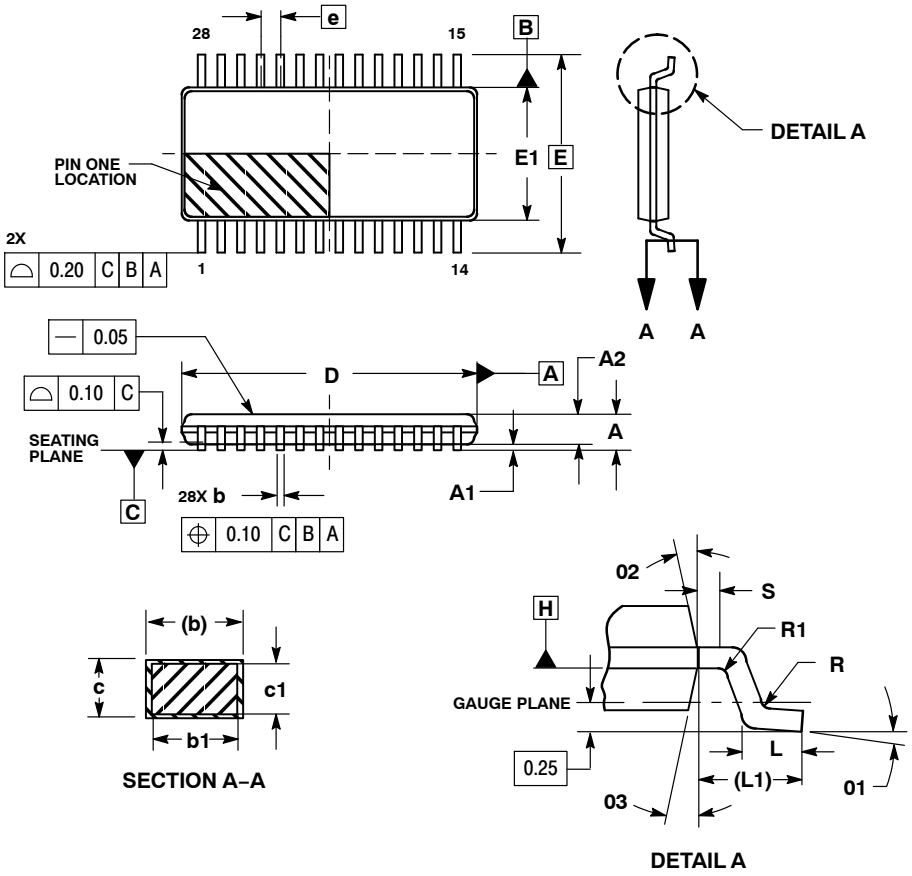


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

28 LEAD TSSOP
CASE 948AA−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	9.60	9.80
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.45	0.75
L1	1.00 REF	
R	0.09	−−−
R1	0.09	−−−
S	0.20	−−−
01	0 °	8 °
02	12 °REF	
03	12 °REF	

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