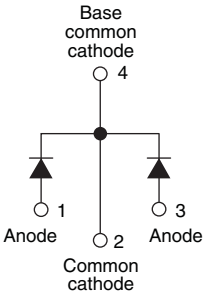
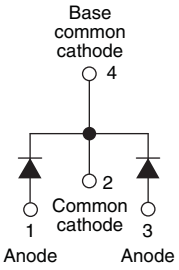
High Performance Schottky Generation 5.0, 2 x 3 A

I-PAK (TO-251AA)

D-PAK (TO-252AA)



VS-6CUT10-E



VS-6CWT10FN-E

FEATURES

- 175 °C high performance Schottky diode
- Very low forward voltage drop
- Extremely low reverse leakage
- Optimized V_F vs. I_R trade off for high efficiency
- Increased ruggedness for reverse avalanche capability
- RBSOA available
- Negligible switching losses
- Submicron trench technology
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT

APPLICATIONS

- Specific for PV cells bypass diode
- High efficiency SMPS
- High frequency switching
- Output rectification
- Reverse battery protection
- Freewheeling
- DC/DC systems
- Increased power density systems

PRODUCT SUMMARY	
Package	D-PAK (TO-252AA), I-PAK (TO-251AA)
$I_{F(AV)}$	2 x 3 A
V_R	100 V
V_F at I_F	0.63 V
I_{RM} max.	1 mA at 125 °C
T_J max.	175 °C
Diode variation	Common cathode
E_{AS}	12 mJ

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
V_{RRM}		100	V
V_F	3 A_{pk}, T_J = 125 °C (typical, per leg)	0.6	
T_J	Range	- 55 to 175	°C

VOLTAGE RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	VS-6CUT10-E VS-6CWT10FN-E	UNITS
Maximum DC reverse voltage	V_R	T_J = 25 °C	100	V

ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current	per leg	$I_{F(AV)}$	50 % duty cycle at T_C = 166 °C, rectangular waveform		3	A
	per device				6	
Maximum peak one cycle non-repetitive surge current per leg		I_{FSM}	5 µs sine or 3 µs rect. pulse	Following any rated load condition and with rated V_{RRM} applied	440	
			10 ms sine or 6 ms rect. pulse		70	
Non-repetitive avalanche energy per leg		E_{AS}	T_J = 25 °C, I_{AS} = 4 A, L = 1.5 mH		12	mJ
Repetitive avalanche current per leg		I_{AR}	Limited by frequency of operation and time pulse duration so that $T_J < T_J$ max. I_{AS} at T_J max. as a function of time pulse. See fig. 8		I_{AS} at T_J max.	A

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Forward voltage drop per leg	V_{FM} (1)	3 A	T_J = 25 °C	0.720	0.79	V
		6 A		0.825	0.91	
		3 A	T_J = 125 °C	0.60	0.63	
		6 A		0.69	0.74	
Reverse leakage current per leg	I_{RM} (1)	T_J = 25 °C	V_R = Rated V_R	0.3	30	µA
		T_J = 125 °C		0.3	1	mA
Junction capacitance per leg	C_T	V_R = 5 V_{DC} (test signal range 100 kHz to 1 MHz), 25 °C		114	-	pF
Series inductance per leg	L_S	Measured lead to lead 5 mm from package body		8.0	-	nH
Maximum voltage rate of change	dV/dt	Rated V_R		-	10 000	V/µs

Note

(1) Pulse width < 300 µs, duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	T_J, T_{Stg}		- 55 to 175	°C
Maximum thermal resistance, junction to case per leg	R_{thJC}	DC operation	4.7	°C/W
Maximum thermal resistance, junction to case per device			2.35	
Typical thermal resistance, case to heatsink	R_{thCS}		0.3	
Approximate weight			0.3	g
			0.01	oz.
Marking device		Case style I-PAK	6CUT10	
		Case style D-PAK	6CWT10FN	

For technical questions within your region, please contact one of the following:
DiodesAmericas@vishay.com, DiodesAsia@vishay.com, DiodesEurope@vishay.com

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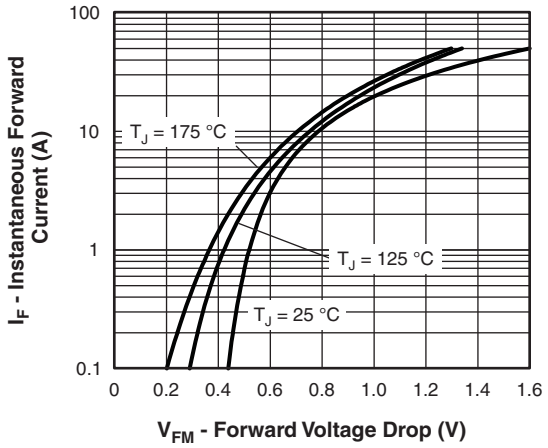

Fig. 1 - Maximum Forward Voltage Drop Characteristics

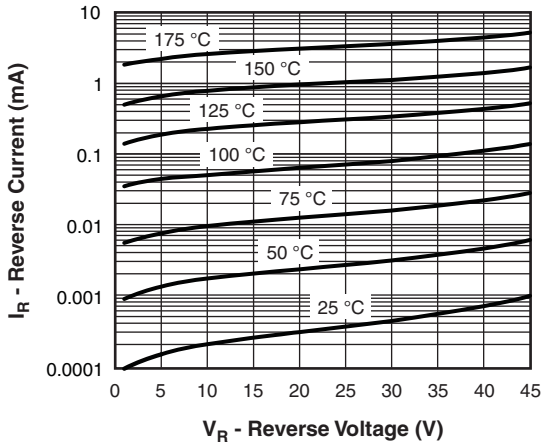

Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

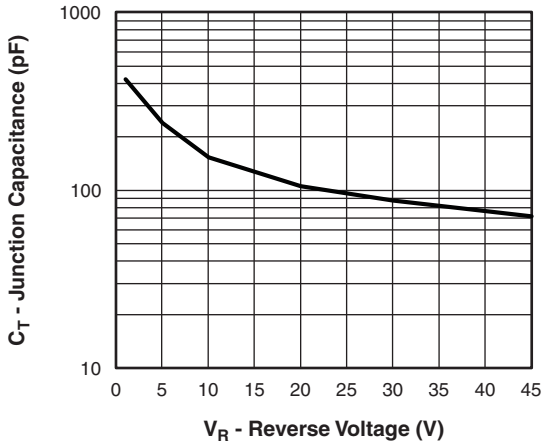

Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

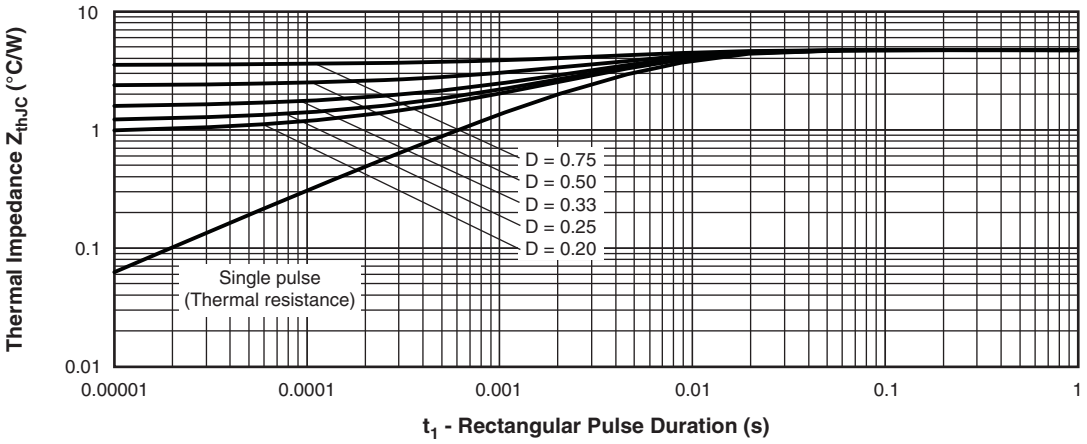

Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

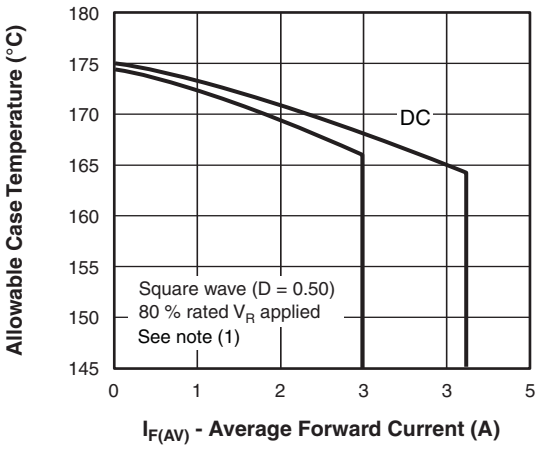

Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

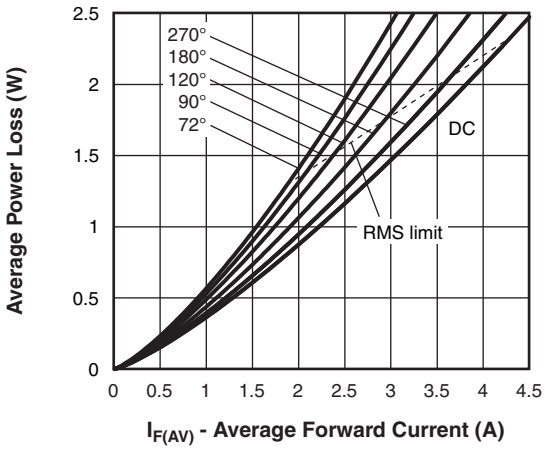

Fig. 6 - Forward Power Loss Characteristics

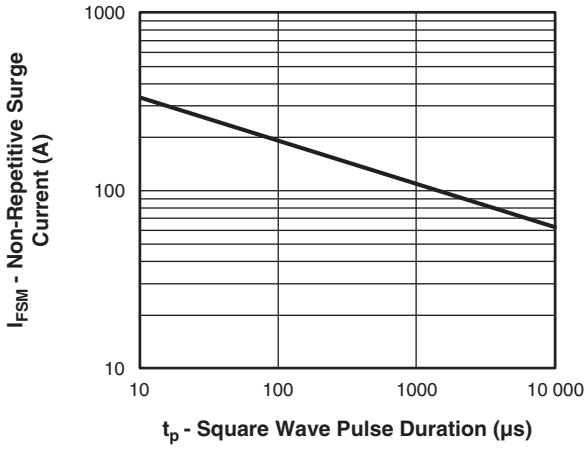

Fig. 7 - Maximum Non-Repetitive Surge Current

Note

(1) Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC}$;
Pd = Forward power loss = $I_{F(AV)} \times V_{FM}$ at ($I_{F(AV)}$/D) (see fig. 6);
Pd_{REV} = Inverse power loss = $V_{R1} \times I_R$ (1 - D); I_R at V_{R1} = 80 % rated V_R

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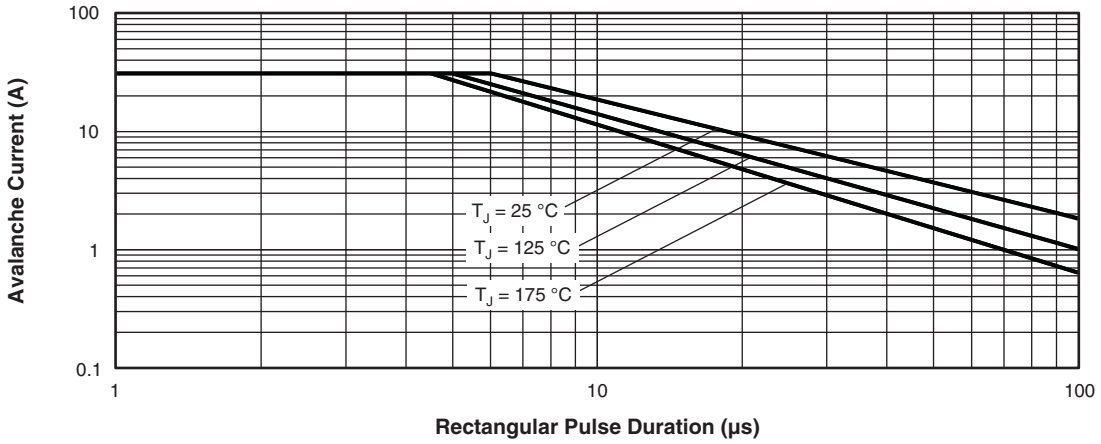


Fig. 8 - Reverse Bias Safe Operating Area (Avalanche Current vs. Rectangular Pulse Duration)

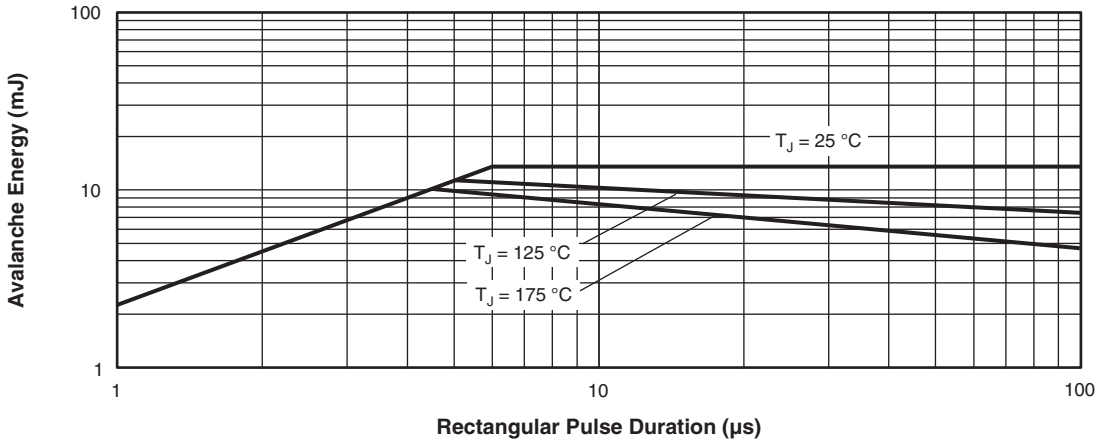
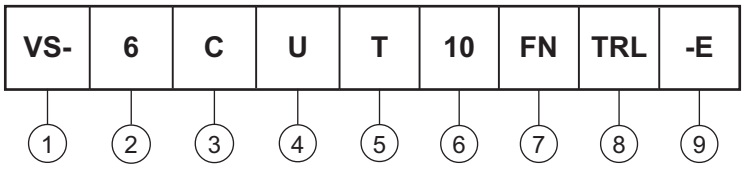


Fig. 9 - Reverse Bias Safe Operating Area (Avalanche Energy vs. Rectangular Pulse Duration)

ORDERING INFORMATION TABLE

Device code



1 - Vishay Semiconductors product

2 - Current rating (2 x 3 A)

3 - Circuit configuration:

C = Common cathode

4 - Package:

- U = I-PAK
- W = D-PAK

5 - T = Trench

6 - Voltage rating (10 = 100 V)

7 - TO-252AA (D-PAK)

8 - D-PAK, I-PAK:

None = Tube (75 pieces)

D-PAK only:

- TR = Tape and reel
- TRL = Tape and reel (left oriented)
- TRR = Tape and reel (right oriented)

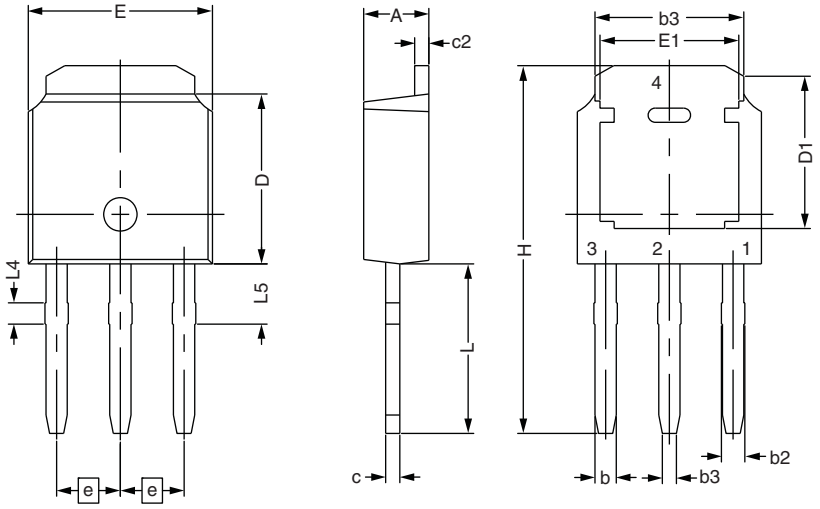
9 - Environmental digit:

-E = RoHS compliant and terminations lead (Pb)-free

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95024
Part marking information	www.vishay.com/doc?95097

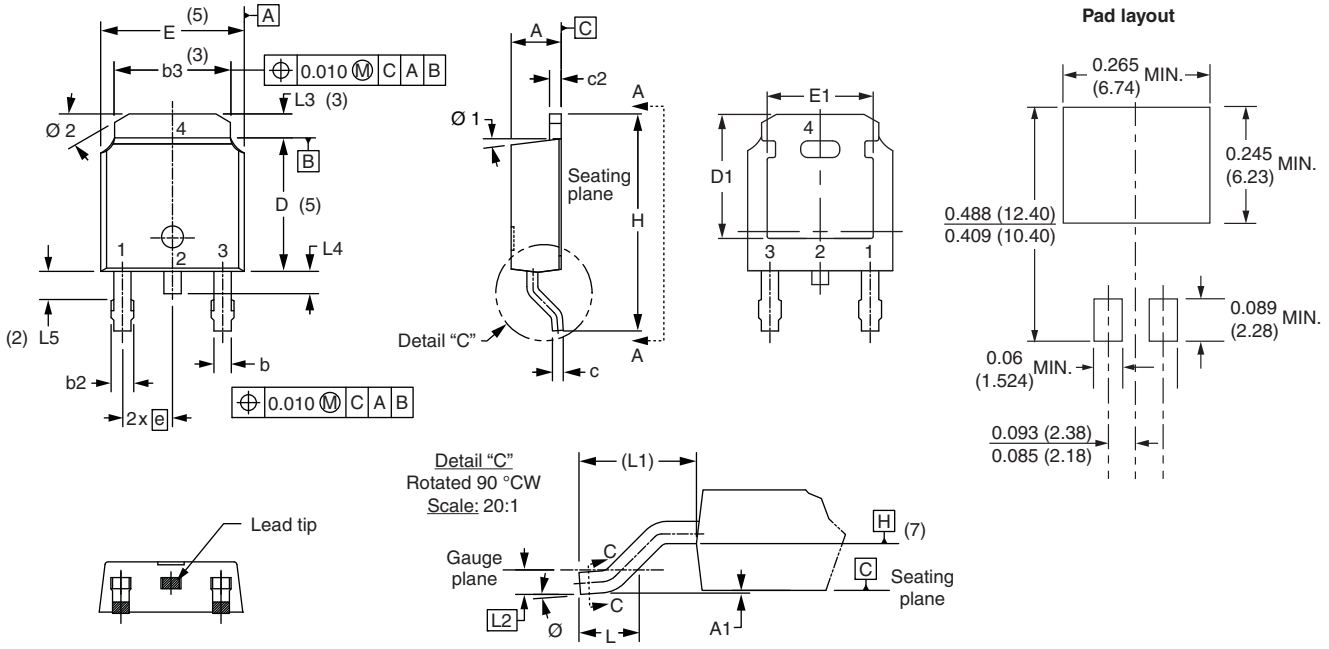
I-PAK - S, D-PAK

DIMENSIONS FOR I-PAK - S in millimeters



SYMBOL	DIMENSIONAL REQUIREMENTS		
	MIN.	NOM.	MAX.
E	6.40	6.60	6.70
L	3.98	4.13	4.28
L4	0.66	0.76	0.86
L5	1.96	2.16	2.36
D	6.00	6.10	6.20
H	11.05	11.25	11.45
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
b4	0.41	0.51	0.61
e	2.286 BSC		
A	2.20	2.30	2.38
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D1	5.30	-	-
E1	4.40	-	-

DIMENSIONS FOR D-PAK in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	0.094	
A1	-	0.13	-	0.005	
b	0.64	0.89	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	3
c	0.46	0.61	0.018	0.024	
c2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	5
D1	5.21	-	0.205	-	3
E	6.35	6.73	0.250	0.265	5
E1	4.32	-	0.170	-	3

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
e	2.29 BSC		0.090 BSC		
H	9.40	10.41	0.370	0.410	
L	1.40	1.78	0.055	0.070	
L1	2.74 BSC		0.108 REF.		
L2	0.51 BSC		0.020 BSC		
L3	0.89	1.27	0.035	0.050	3
L4	-	1.02	-	0.040	
L5	1.14	1.52	0.045	0.060	2
Ø	0°	10°	0°	10°	
Ø1	0°	15°	0°	15°	
Ø2	25°	35°	25°	35°	

Notes

(1) Dimensioning and tolerancing as per ASME Y14.5M-1994

(2) Lead dimension uncontrolled in L5

(3) Dimension D1, E1, L3 and b3 establish a minimum mounting surface for thermal pad

(4) Section C - C dimension apply to the flat section of the lead between 0.13 and 0.25 mm (0.005 and 0.10") from the lead tip

(5) Dimension D, and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body

(6) Dimension b1 and c1 applied to base metal only

(7) Datum A and B to be determined at datum plane H

(8) Outline conforms to JEDEC outline TO-252AA

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