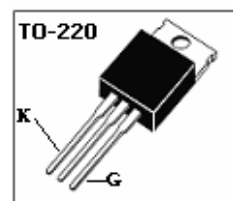
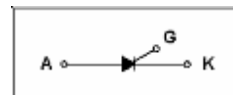




Silicon Controlled Rectifier

Features

- * Repetitive Peak Off-State Voltage : 600V
- * R.M.S On-State Current($I_{T(RMS)}$)=12A
- * Average On-State Current ($I_{T(AV)}$)=7.5A
- * Non-isolated Type



General Description

Passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

Absolute Maximum Ratings ($T_a=25^\circ\text{C}$ unless otherwise specified)

T_{stg}	—Storage Temperature	-40~150°C
T_j	—Operating Junction Temperature	125°C
V_{DRM}	—Repetitive Peak Off-State Voltage	600V
I_T (RMS)	—R.M.S On-State Current (all conduction angles)	12A
$I_{T(AV)}$	—Average On-State Current (Half Sine Wave : $T_C = 109^\circ\text{C}$)	7.5A
I_{TSM}	—Surge On-State Current (1/2 Cycle, 50Hz, Sine Wave, Non-repetitive)	100A
I^2t	—Circuit Fusing Considerations($t = 10\text{ms}$)	50A ² s
P_{GM}	—Forward Peak Gate Power Dissipation ($T_a=25^\circ\text{C}$)	5W
$P_{G(AV)}$	—Forward Average Gate Power Dissipation (over any 20 ms period)	0.5W
I_{FGM}	—Forward Peak Gate Current	2A
V_{RGM}	—Reverse Peak Gate Voltage	5V

**Electrical Characteristics** ($T_a=25^\circ\text{C}$ unless otherwise specified)

Symbol	Items	Min.	Typ.	Max.	Unit	Conditions
I_{DRM}	Repetitive Peak Off-State Current			20 500	μA	$V_{\text{AK}}=V_{\text{DRM}}$ $T_c=25^\circ\text{C}$ $T_c=125^\circ\text{C}$
V_{TM}	Peak On-State Voltage (1)			1.75	V	$I_{\text{TM}}=23\text{A}$, $t_p=380\mu\text{s}$
I_{GT}	Gate Trigger Current (2)			15	mA	$V_{\text{AK}}=12\text{V}(\text{DC})$, $R_L=10\text{ ohm}$
V_{GT}	Gate Trigger Voltage (2)			1.5	V	$V_{\text{AK}}=12\text{V}(\text{DC})$, $R_L=10\text{ ohm}$ $T_c=25^\circ\text{C}$
V_{GD}	Non-Trigger Gate Voltage	0.2			V	$V_{\text{AK}}=12\text{V}$, $R_L=100\text{ ohm}$ $T_c=125^\circ\text{C}$
I_{H}	Holding Current			20	mA	$I_{\text{T}}=100\text{mA}$, Gate open, $T_c=25^\circ\text{C}$
$R_{\text{th(j-c)}}$	Thermal Resistance			1.3	$^\circ\text{C}/\text{W}$	Junction to Case
$R_{\text{th(j-a)}}$	Thermal Resistance		60		$^\circ\text{C}/\text{W}$	Junction to Ambient
dv/dt	Critical Rate of Rise Off-state Voltage	50			$\text{V}/\mu\text{s}$	Linear slope up to $V_{\text{D}}=V_{\text{DRM}}67\%$ Gate open $T_j=125^\circ\text{C}$

- Forward current applied for 1 ms maximum duration, duty cycle $\leq 1\%$.
- R_{GK} current is not included in measurement

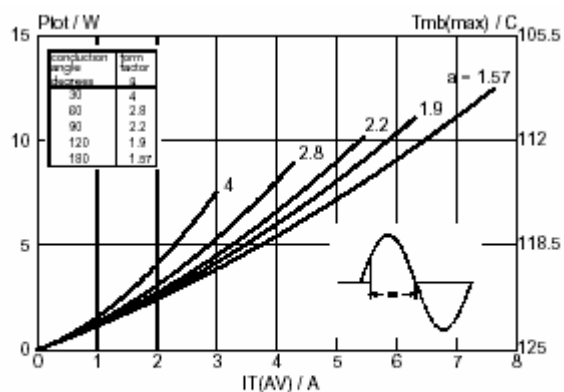
Performance Curves

Fig.1. Maximum on-state dissipation, P_{tot} versus average on-state current, $I_{\text{T(AV)}}$, where $a = \text{form factor} = I_{\text{T(RMS)}} / I_{\text{T(AV)}}$

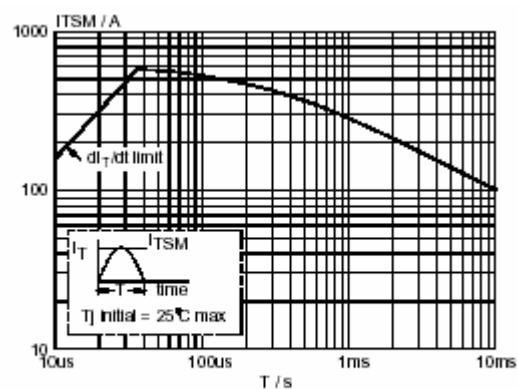


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM} versus pulse width t_p , for sinusoidal currents, $t_p \leq 10\text{ms}$.



Performance Curves

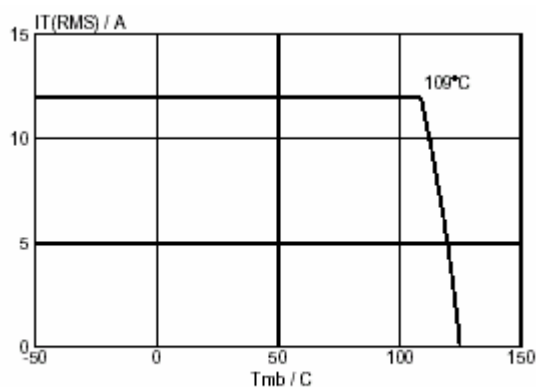


Fig.3. Maximum permissible rms current $I_{T(RMS)}$ versus mounting base temperature T_{mb} .

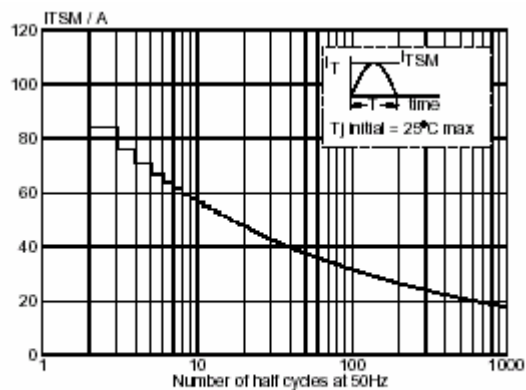


Fig.4. Maximum permissible non-repetitive peak on-state current I_{TSM} versus number of cycles, for sinusoidal currents, $f = 50 \text{ Hz}$.

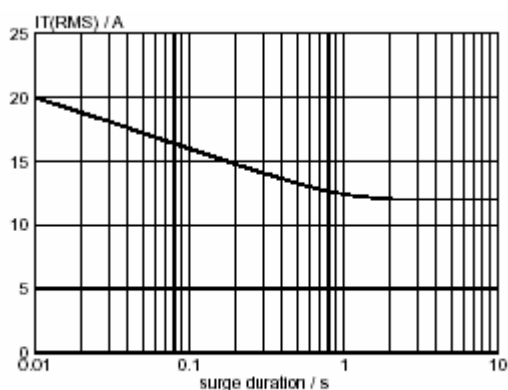


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$ versus surge duration, for sinusoidal currents, $f = 50 \text{ Hz}$; $T_{mb} \leq 109^\circ\text{C}$.

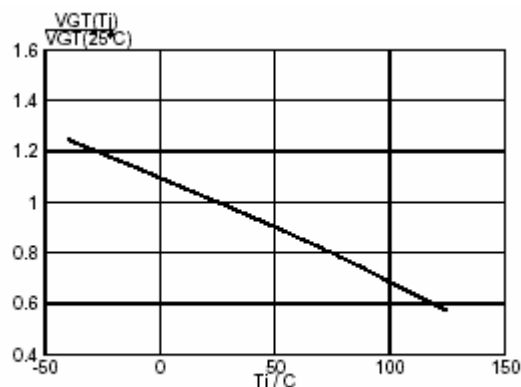


Fig.6. Normalised gate trigger voltage $V_{GT}(T_J) / V_{GT}(25^\circ\text{C})$, versus junction temperature T_J .

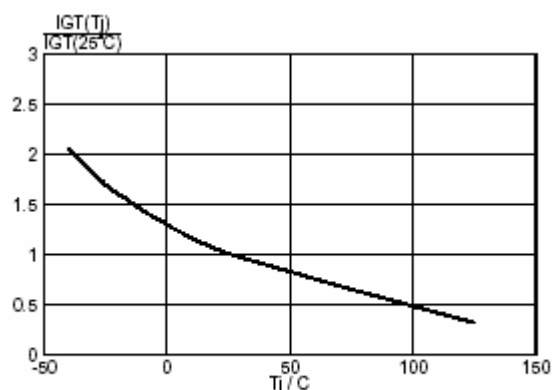


Fig.7. Normalised gate trigger current $I_{GT}(T_J) / I_{GT}(25^\circ\text{C})$, versus junction temperature T_J .

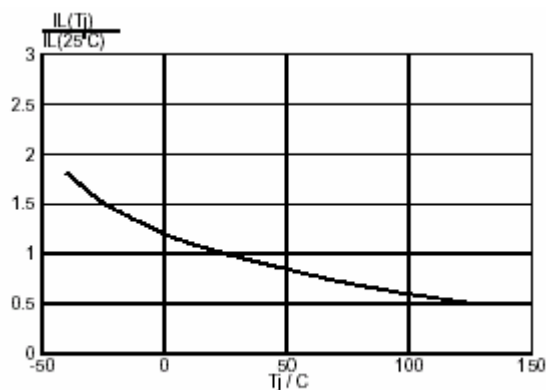


Fig.8. Normalised latching current $I_L(T_J) / I_L(25^\circ\text{C})$, versus junction temperature T_J .



Performance Curves

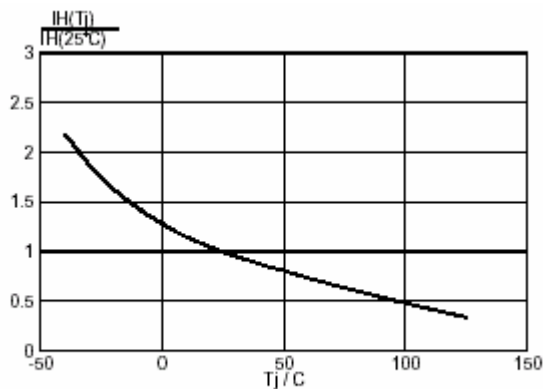


Fig. 9. Normalised holding current $I_H(T_j) / I_H(25^\circ\text{C})$, versus junction temperature T_j .

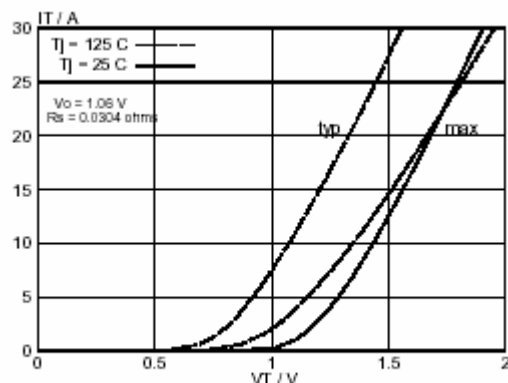


Fig. 10. Typical and maximum on-state characteristic.

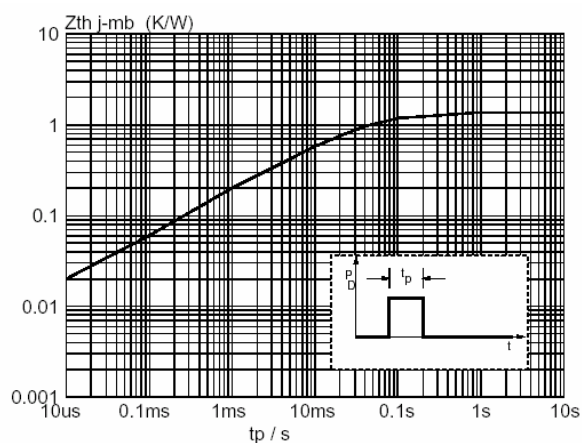


Fig. 11. Transient thermal impedance $Z_{th(j-mb)}$ versus pulse width t_p .

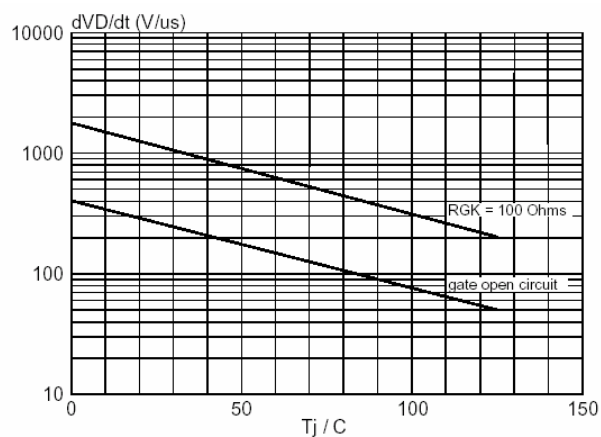


Fig. 12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j .