FAIRCHILD SEMICONDUCTOR®

October 2009

FAN9611 / FAN9612
Interleaved Dual BCM PFC Controllers

Features

- Sync-Lock™ Interleaving Technology for 180° Out-of-Phase Synchronization Under All Conditions
- Automatic Phase Disable at Light Load
- Dead-Phase Detect Protection
- 2.0A Sink, 1.0A Source, High-Current Gate Drivers
- High Power Factor, Low Total Harmonic Distortion
- Voltage-Mode Control with $(V_{IN})^2$ Feedforward
- Closed-Loop Soft-Start with User-Programmable Soft-Start Time for Reduced Overshoot
- Minimum Restart Frequency to Avoid Audible Noise
- Maximum Switching Frequency Clamp
- Brownout Protection with Soft Recovery
- Non-Latching OVP on FB Pin and Latching Second-Level Protection on OVP Pin
- Open-Feedback Protection
- Power-Limit and Current Protection for Each Phase
- Low Startup Current of 80µA Typical
- Works with DC and 50Hz to 400Hz AC Inputs

Applications

- 100-1000W AC-DC Power Supplies
- Large Screen LCD-TV, PDP-TV, RP-TV Power
- High-Efficiency Desktop and Server Power Supplies
- Networking and Telecom Power Supplies
- Solar Micro Inverters

Description

The FAN9611/12 family of interleaved dual Boundary-Conduction-Mode (BCM) Power-Factor-Correction (PFC) controllers operate two parallel-connected boost power trains 180° out of phase. Interleaving extends the maximum practical power level of the control technique from about 300W to greater than 800W. Unlike the continuous conduction mode (CCM) technique often used at higher power levels, BCM offers inherent zero-current switching of the boost diodes, which permits the use of less expensive diodes without sacrificing efficiency. Furthermore, the input and output filters can be smaller due to ripple current cancellation and effective doubling of the switching frequency.

The converters operate with variable frequency, which is a function of the load and the instantaneous input / output voltages. The switching frequency is limited between 18kHz and 600kHz. The Pulse Width Modulators (PWM) implement voltage-mode control with input voltage feedforward. When configured for PFC applications, the slow voltage regulation loop results in constant on-time operation within a line cycle. This PWM method, combined with the BCM operation of the boost converters, provides automatic power factor correction.

The controllers offers bias UVLO (10V / 7.5V for FAN9611 and 12.5V / 7.5V for FAN9612), input brownout, input over-voltage, over-current, open-feedback, output over-voltage, and redundant latching over-voltage protections. Furthermore, the converters' output power is limited independently of the input RMS voltage. Synchronization between the power stages is maintained under all operating conditions.

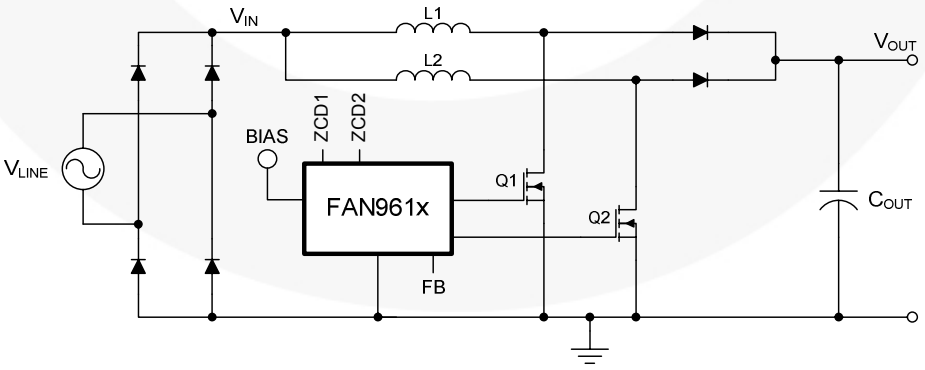


Figure 1. Simplified Application Diagram

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Ordering Information

Part Number	Eco Status	Package	Packing Method	Packing Quantity
FAN9611MX (Preliminary)	RoHS	16-Lead, Small Outline Integrated Circuit (SOIC)	Tape and Reel	2,500
FAN9612MX	RoHS	16-Lead, Small Outline Integrated Circuit (SOIC)	Tape and Reel	2,500

Notes:

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

This device passed wave soldering test by JESD22A-111.

Package Outlines

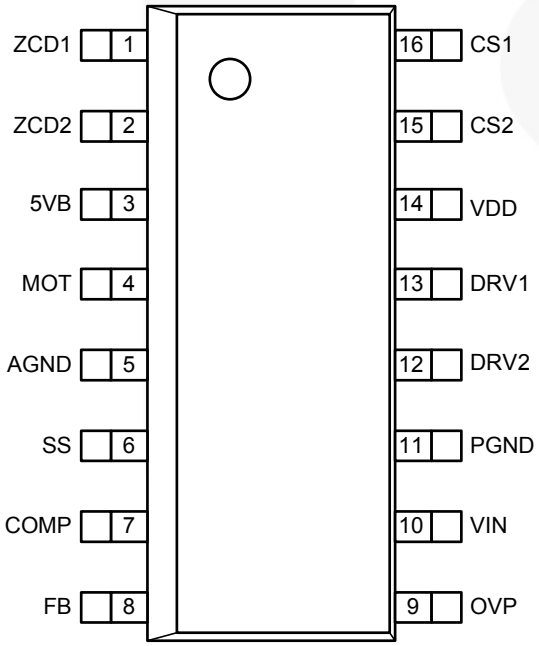


Figure 2. SOIC-16 (Top View)

Thermal Resistance Table

Package	Suffix	Thermal Resistance	
		Θ_{JL} (1)	Θ_{JA} (2)
16-Lead SOIC	M	35°C/W	50 – 120°C/W (3)

Notes:

1. Typical Θ_{JL} is specified from semiconductor junction to lead.
2. Typical Θ_{JA} is dependent on the PCB design and operating conditions, such as air flow. The range of values covers a variety of operating conditions utilizing natural convection with no heatsink on the package.
3. This typical range is an estimate; actual values depend on the application.

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Typical Application Diagram

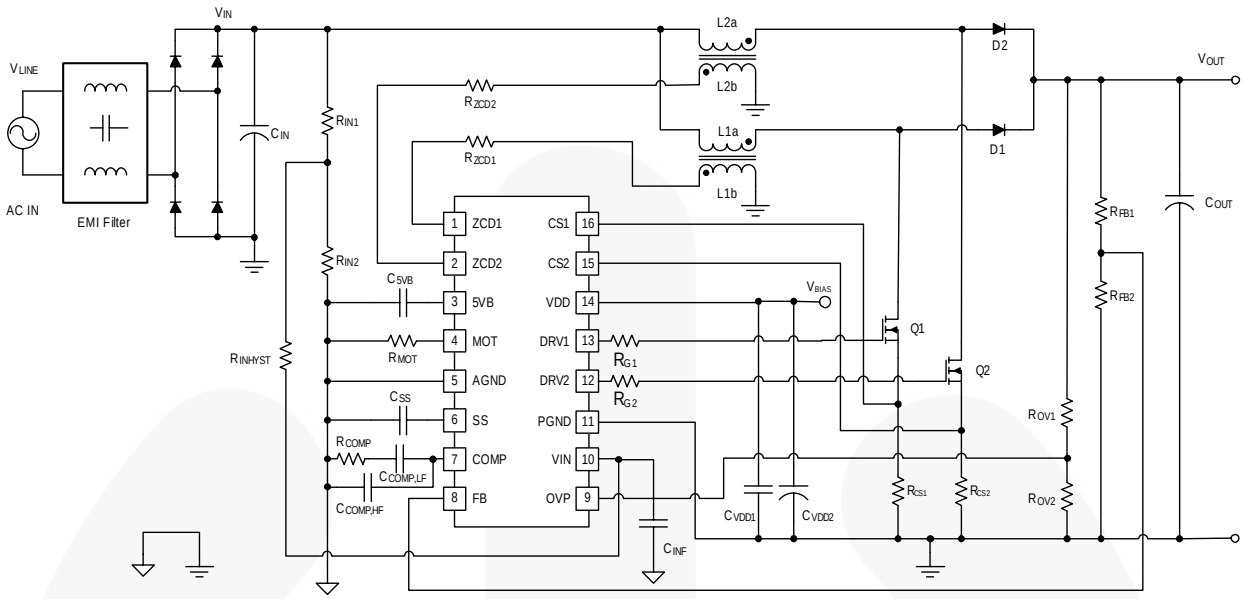


Figure 3. Typical Application Diagram

Block Diagram

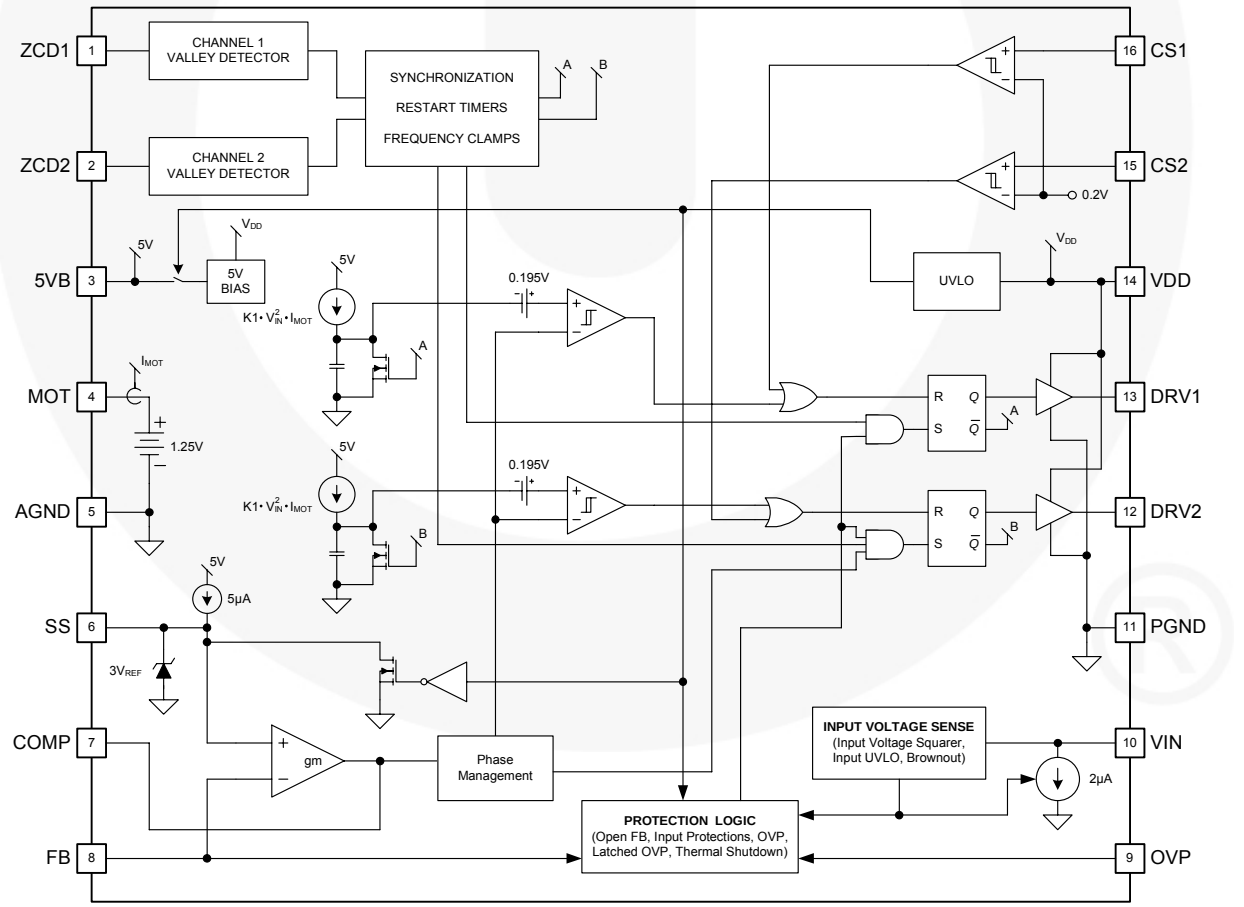


Figure 4. Block Diagram

Pin Configuration

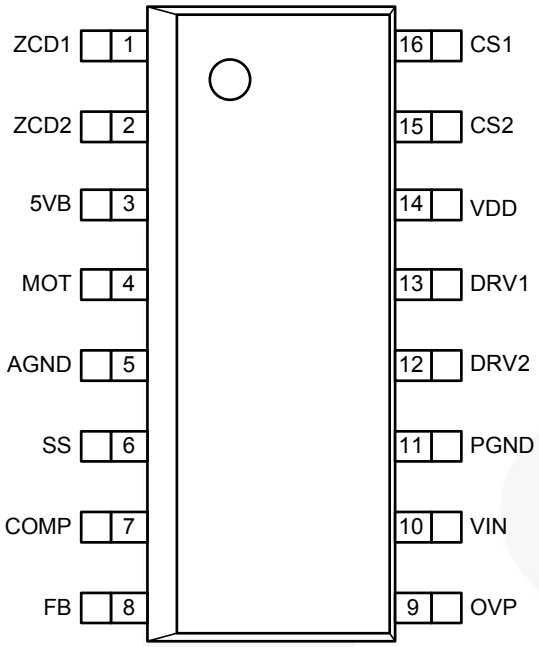


Figure 5. Pin Layout (Top-View)

Pin Definitions

Pin #	Name	Description
1	ZCD1	**Zero Current Detector for Phase 1** of the interleaved boost power stage.
2	ZCD2	**Zero Current Detector for Phase 2** of the interleaved boost power stage.
3	5VB	**5V Bias**. Bypass pin for the internal supply, which powers all control circuitry on the IC.
4	MOT	**Maximum On-Time** adjust for the individual power stages.
5	AGND	**Analog Ground**. Reference potential for all setup signals.
6	SS	**Soft-Start Capacitor**. Connected to the non-inverting input of the error amplifier.
7	COMP	**Compensation Network** connection to the output of the g_M error amplifier
8	FB	**Feedback pin** to sense the converter's output voltage; inverting input of the error amplifier.
9	OVP	**Output Voltage** monitor for the independent, second-level, latched OVP protection.
10	VIN	**Input Voltage** monitor for brownout protection and input voltage feedforward.
11	PGND	**Power Ground** connection.
12	DRV2	**Gate Drive Output for Phase 2** of the interleaved boost power stage.
13	DRV1	**Gate Drive Output for Phase 1** of the interleaved boost power stage.
14	VDD	**External Bias Supply** for the IC.
15	CS2	**Current Sense Input for Phase 2** of the interleaved boost power stage.
16	CS1	**Current Sense Input for Phase 1** of the interleaved boost power stage.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	Supply Voltage to AGND & PGND		-0.3	20.0	V
V_{BIAS}	5VB Voltage to AGND & PGND		-0.3	5.5	V
	Voltage On Input Pins to AGND (Except FB Pin)		-0.3	V_{BIAS} + 0.3	V
	Voltage On FB Pin (Current Limited)		-0.3	V_{DD} + 0.8	V
	Voltage On Output Pins to PGND (DRV1, DRV2)		-0.3	V_{DD} + 0.3	V
I_{OH}, I_{OL}	Gate Drive Peak Output Current (Transient)			2.5	A
	Gate Drive Output Current (DC)			0.05	A
T_L	Lead Soldering Temperature (10 Seconds)			+260	ºC
T_J	Junction Temperature		-40	+150	ºC
T_{STG}	Storage Temperature		-65	+150	ºC
ESD	Electrostatic Discharge Protection Level	Human Body Model, JEDEC JESD22-A114	2		kV
		Charged Device Model, JEDEC JESD22-C101	1		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage Range	9	12	18	V
V_{INS}	Signal Input Voltage	0		5	V
I_{SNK}	Output Current Sinking (DRV1, DRV2)	1.5	2.0		A
I_{SRC}	Output Current Sourcing (DRV1, DRV2)	0.8	1.0		A
$L_{MISMATCH}$	Boost Inductor Mismatch **Note:** While the recommended maximum inductor mismatch is ±10% for optimal current sharing and ripple-current cancellation, there is no absolute maximum limit. If the mismatch is greater than ±10%, current sharing is proportionately worse requiring over-design of the power supply. However, the accurate 180° out-of-phase synchronization is still maintained providing current cancellation although its effectiveness is reduced.		±5%	±10%	
T_A	Operating Ambient Temperature	-40		+125	ºC

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Electrical Characteristics

Unless otherwise noted, V_{DD} = 12V, T_J = -40°C to +125°C. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
$I_{STARTUP}$	Startup Supply Current	$V_{DD} = V_{ON} – 0.2V$		80	110	µA
I_{DD}	Operating Current	Output Not Switching		3.7	5.2	mA
I_{DD_DYM}	Dynamic Operating Current(4)	f_{SW} = 50kHz; C_{LOAD} = 2nF		4	6	mA
V_{ON}	UVLO Start Threshold, FAN9611	V_{DD} Increasing	9.5	10.0	10.5	V
	UVLO Start Threshold, FAN9612		12.0	12.5	13.0	V
V_{OFF}	UVLO Stop Threshold Voltage	V_{DD} Decreasing	7.0	7.5	8.0	V
V_{HYS}	UVLO Hysteresis, FAN9611	$V_{ON} – V_{OFF}$		2.5		V
	UVLO Hysteresis, FAN9612			5.0		V
Bias Regulator (C_{5VB} = 0.1µF)						
V_{5VB}	5VB Output Voltage	T_A = 25°C; I_{LOAD} = 1mA		5.0		V
		Total Variation Over Line, Load, and Temperature	4.8		5.2	
I_{OUT_MAX}	Maximum Output Current		5.0			mA
Error Amplifier						
V_{EA}	Voltage Reference	T_A = 25°C	2.95	3.00	3.05	V
		Total Variation Over Line, Load, and Temperature	2.91		3.075	
I_{BIAS}	Input Bias Current	V_{FB} = 1V to 3V; $\lvert V_{SS} – V_{FB}\rvert \le 0.1V$	–0.2		0.2	µA
I_{OUT_SRC}	Output Source Current	V_{SS} = 3V; V_{FB} = 2.9V	-13.7	-8	-4	µA
I_{OUT_SINK}	Output Sink Current	V_{SS} = 3V; V_{FB} = 3.1V	4	8	12	µA
V_{OH}	Output High Voltage		4.5	4.7	V5VB	V
V_{OL}	Output Low Voltage	I_{SINK} < 100µA	0.0	0.1	0.2	V
g_M	Transconductance		50	78	115	µmho
PWM						
$V_{RAMP,OFST}$	PWM Ramp Offset	T_A = 25°C	120	195	270	mV
$t_{ON,MIN}$	Minimum On-Time	$V_{FB} > V_{SS}$			0	µs
Maximum On-Time						
V_{MOT}	Maximum On-Time Voltage	R = 125kΩ	1.16	1.23	1.30	V
$t_{ON,MAX}$	Maximum On-Time	R = 125kΩ; V_{VIN} = 2.5V; V_{COMP} > 4.5V; T_A = 25°C	3.4	5.0	6.6	µs
Restart Timer (Each Channel)						
$f_{SW,MIN}$	Minimum Switching Frequency	$V_{FB} > V_{PWM_OFFSET}$	15.5	18.5	23.0	kHz
Frequency Clamp (Each Channel)						
$f_{SW,MAX}$	Maximum Switching Frequency		520	605	750	kHz

Continued on the following page…

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Electrical Characteristics (Continued)

Unless otherwise noted, V_{DD} = 12V, T_J = -40°C to +125°C. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Current Sense						
V_{CS}	CS Input Threshold Voltage Limit		0.19	0.21	0.23	V
I_{CS}	CS Input Current	V_{CSX} = 0V to 1V	–0.2		0.2	µA
t_{CS_DELAY}	CS to Output Delay	CS Stepped from 0V to 5V		85	100	ns
Zero Current Detection						
V_{ZCD_IN}	Input Voltage Threshold(4)		–0.1	0	0.1	V
V_{ZCD_H}	Input High Clamp Voltage	I_{ZCD} = 0.5mA	0.8	1.0	1.2	V
V_{ZCD_L}	Input Low Clamp Voltage	I_{ZCD} = –0.5mA	–0.7	–0.5	–0.3	V
I_{ZCD_SRC}	Source Current Capability(4)				1	mA
I_{ZCD_SNK}	Sink Current Capability(4)				10	mA
t_{ZCD_DLY}	Turn-On Delay(4)	ZCDx to OUTx		180		ns
Output						
I_{SINK}	OUTx Sink Current, Mid-Voltage(4)	V_{OUTx} = V_{DD}/2; C_{LOAD} = 0.1µF		2.0		A
I_{SOURCE}	OUTx Source Current, Mid-Voltage(4)	V_{OUTx} = V_{DD}/2; C_{LOAD} = 0.1µF		1.0		A
t_{RISE}	Rise Time	C_{LOAD} = 1nF, 10% to 90%		10	25	ns
t_{FALL}	Fall Time	C_{LOAD} = 1nF, 90% to 10%		5	20	ns
V_{O_UVLO}	Output Voltage During UVLO	V_{DD} = 5V; I_{OUT} = 100µA			1	V
I_{RVS}	Reverse Current Withstand(4)			500		mA
Soft-Start (C_{SS} = 0.1µF)						
I_{SS_MAX}	Maximum Soft-Start Current	V_{COMP} < 3.0V	–8	–5	–2	µA
I_{SS_MIN}	Minimum Soft-Start Current	V_{COMP} > 4.5V	–0.62	–0.20	–0.05	µA
Input Protection						
V_{IN_BO}	Input Brownout Threshold		0.76	0.95	1.10	V
V_{IN_OVP}	Input OVP Threshold		3.1	3.7	4.3	V
V_{IN_RATIO}	OVP Threshold / BO Threshold		3.6	4.0	4.3	
I_{VINSNK}	VIN Sink Current	V_{VIN} > 1.1V	–0.2		0.2	µA
		V_{VIN} < 0.8V	1.4	2	2.5	µA
Phase Management						
$V_{PH,DROP}$	Phase Dropping Threshold	V_{COMP} Decreasing, Transition from Dual to Single Phase	0.660	0.740	0.825	V
$V_{PH,ADD}$	Phase Adding Threshold	V_{COMP} Increasing, Transition from Single to Dual Phase	0.84	0.92	1.00	V
Over-Voltage Protection Using FB Pin – Cycle-by-Cycle (Input)						
V_{OVPNL}	Non-Latching OVP Threshold (+8% above $V_{OUT_NOMINAL}$)	T_A = 25°C DRV1=DRV2=0V	3.15	3.25	3.35	V
V_{OVPNL_HYS}	OVP Hysteresis	FB Decreasing		0.24		V
Over-Voltage Protection Using OVP Pin – Latching (Input)						
V_{OVPLCH}	Latching OVP Threshold (+15%)	DRV1=DRV2=0V	3.36	3.50	3.65	V

Note:

4. Not tested in production.

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Theory of Operation

1. Boundary Conduction Mode

The boost converter is the most popular topology for power factor correction in AC-to-DC power supplies. This popularity can be attributed to the continuous input current waveform provided by the boost inductor and to the fact that the boost converter's input voltage range includes 0V. These fundamental properties make close to unity power factor easier to achieve.

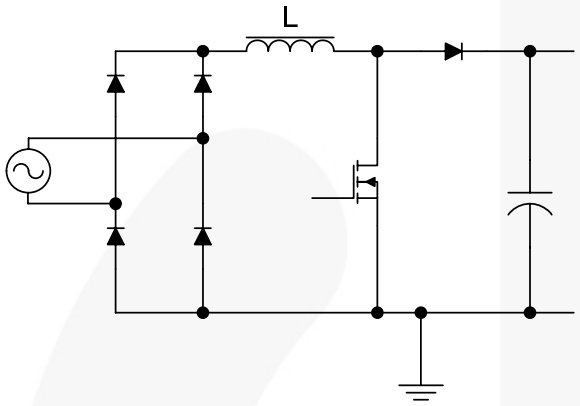


Figure 6. Basic PFC Boost Converter

The boost converter can operate in continuous conduction mode (CCM) or in boundary conduction mode (BCM). These two descriptive names refer to the current flowing in the energy storage inductor of the boost power stage.

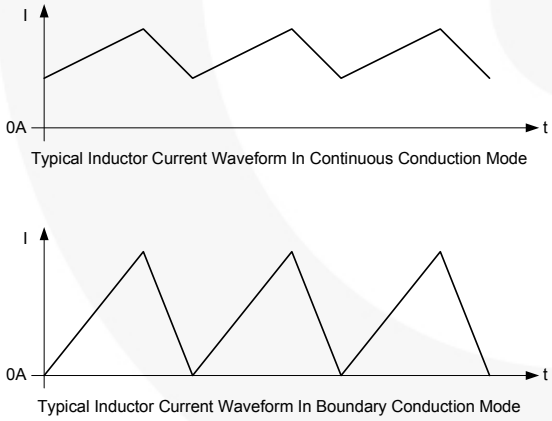


Figure 7. CCM vs. BCM Control

As the names indicate, the current in Continuous Conduction Mode (CCM) is continuous in the inductor; while in Boundary Conduction Mode (BCM), the new switching period is initiated when the inductor current returns to zero.

There are many fundamental differences in CCM and BCM operations and the respective designs of the boost converter.

The FAN9611/12 utilizes the boundary conduction mode control algorithm. The fundamental concept of this operating mode is that the inductor current starts from zero in each switching period, as shown in the lower waveform in Figure 7. When the power transistor of the boost converter is turned on for a fixed amount of time, the peak inductor current is proportional to the input voltage. Since the current waveform is triangular, the average value in each switching period is also proportional to the input voltage. In the case of a sinusoidal input voltage waveform, the input current of the converter follows the input voltage waveform with very high accuracy and draws a sinusoidal input current from the source. This behavior makes the boost converter in BCM operation an ideal candidate for power factor correction.

This mode of control of the boost converter results in a variable switching frequency. The frequency depends primarily on the selected output voltage, the instantaneous value of the input voltage, the boost inductor value, and the output power delivered to the load. The operating frequency changes as the input voltage follows the sinusoidal input voltage waveform. The lowest frequency operation corresponds to the peak of the sine waveform at the input of the boost converter. Even larger frequency variation can be observed as the output power of the converter changes, with maximum output power resulting in the lowest operating frequency. Theoretically, under zero-load condition, the operating frequency of the boost converter would approach infinity. In practice, there are natural limits to the highest switching frequency. One such limiting factor is the resonance between the boost inductor and the parasitic capacitances of the MOSFET, the diode, and the winding of the choke, in every switching cycle.

Another important characteristic of the BCM boost converter is the high ripple current of the boost inductor, which goes from zero to a controlled peak value in every switching period. Accordingly, the power switch is stressed with high peak current. In addition, the high ripple current must be filtered by an EMI filter to meet high-frequency noise regulations enforced for equipment connecting to the mains. The effects usually limit the practical output power level of the converter.

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2. Interleaving

The FAN9611/12 control IC is configured to control two boost converters connected in parallel, both operated in boundary conduction mode. In this arrangement, the input and output voltages of the two parallel converters are the same and each converter is designed to process approximately half the total output power.

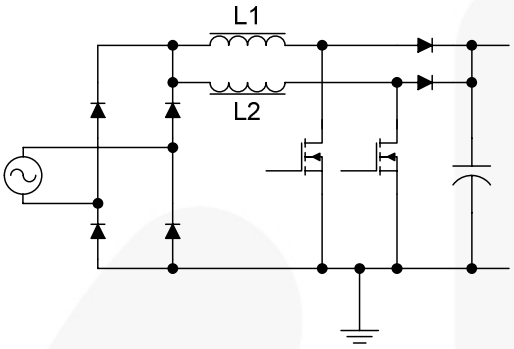


Figure 8. Interleaved PFC Boost Operation

Parallel power processing is penalized by the increased number of power components, but offers significant benefits to keep current and thermal stresses under control and to increase the power handling capability of the otherwise limited BCM PFC control solution. Furthermore, the switches of the two boost converters can be operated 180 degrees out of phase from each other. The control of parallel converters operating 180 degrees out of phase is called interleaving. Interleaving provides considerable ripple current reduction at the input and output terminals of the power supply, which favorably affects the input EMI filter requirements and reduces the high-frequency RMS current of the power supply output capacitor.

There is an obvious difficulty in interleaving two BCM boost converters. Since the converter's operating frequency is influenced by component tolerances in the power stage and in the controller, the two converters operate at different frequencies. Therefore special attention must be paid to ensure that the two converters are locked to 180-degree out-of-phase operation. Consequently, synchronization is a critical function of an interleaved boundary conduction mode PFC controller. It is implemented in the FAN9611/12 using proprietary and dedicated circuitry called Sync-Lock™ interleaving technology.

3. Voltage Regulation, Voltage Mode Control

The power supply's output voltage is regulated by a negative feedback loop and a pulse width modulator. The negative feedback is provided by an error amplifier that compares the feedback signal at the inverting input to a reference voltage connected to the non-inverting input of the amplifier. Similar to other PFC applications, the error amplifier is compensated with high DC gain for accurate voltage regulation, but very low bandwidth to suppress line frequency ripple present across the output capacitor of the converter. The line frequency ripple is the result of the constant output power of the converter and the fact that the input power is the product of a sinusoidal current and a sinusoidal voltage thus follows a sine square function. Eliminating the line frequency component from the feedback system is imperative to maintain low total harmonic distortion (THD) in the input current waveform.

The pulse width modulator implements voltage mode control. This control method compares an artificial ramp to the output of the error amplifier to determine the desired on-time of the converter's power transistor to achieve output voltage regulation.

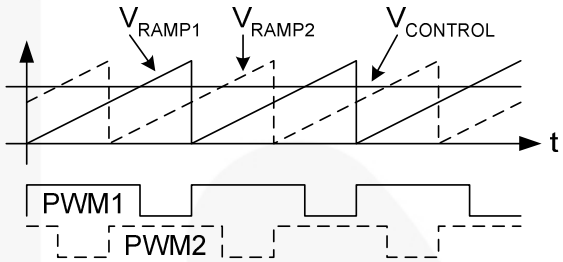


Figure 9. PWM Operation

In FAN9611/12, there are two PWM sections corresponding to the two parallel power stages. For proper interleaved operation, two independent 180-degree out-of-phase ramps are needed; which necessitates the two pulse width modulators. To ensure that the two converters process the same amount of power, the artificial ramps have the same slope and use the same control signal generated by the error amplifier.

4. Input-Voltage Feedforward

Basic voltage-mode control, as described in the previous section, provides satisfactory regulation performance in most cases. One important characteristic of the technique is that input voltage variation to the converter requires a corrective action from the error amplifier to maintain the output at the desired voltage. When the error amplifier has adequate bandwidth, as in most DC-DC applications, it is able to maintain regulation within a tolerable output voltage range during input voltage changes.

On the other hand, when voltage-mode control is used in power factor corrector applications; the error amplifier bandwidth, and its capability to quickly react to input voltage changes, is severely limited. In these cases, the input voltage variation can cause excessive overshoot or droop at the converter output as the input voltage goes up or down.

To overcome this shortcoming of the voltage-mode PWM circuit in PFC applications, input-voltage feedforward is often employed. It can be shown mathematically that a PWM ramp proportional to the square of the input voltage rejects the effect of input voltage variations on the output voltage and eliminates the need of any correction by the error amplifier.

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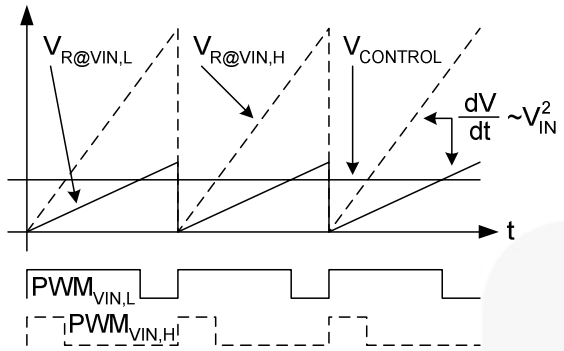


Figure 10. Input-Voltage Feedforward

When the PWM ramp is made proportional to the input voltage squared, the system offers other noteworthy benefits. The first is the input voltage-independent small signal gain of the closed loop power supply, which makes compensation of the voltage regulation loop much easier. The second side benefit is that the output of the error amplifier becomes directly proportional to the input power of the converter. This phenomenon is very significant and it is re-visited in Section 9 describing light-load operation.

5. Starting a PWM Cycle

The principle of boundary conduction mode calls for a pulse width modulator able to operate with variable frequency and initiate a switching period whenever the current in the boost inductor reaches zero. Therefore, BCM controllers cannot utilize a fixed frequency oscillator circuit to control the operating frequency. Instead, a zero current detector is used to sense the inductor current and turn on the power switch once the current in the boost inductor reaches zero. This process is facilitated by an auxiliary winding on the boost inductor. The voltage waveform of the auxiliary winding can be used for indirect detection of the zero inductor current condition of the boost inductor. Therefore it should be connected to the zero current detect input, as shown in Figure 11.

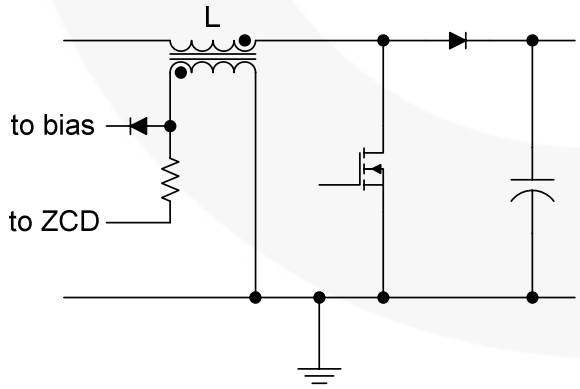


Figure 11. Simple Zero-Current Detection Method

The auxiliary winding can also be used to generate bias for the PFC controller when an independent bias power supply is not present in the system.

At startup condition and in the unlikely case of missing zero current detection, the lack of an oscillator would mean that the converter stops operating. To overcome these situations, a restart timer is employed to kick start the controller and provide the first turn-on command, as shown in Figure 12.

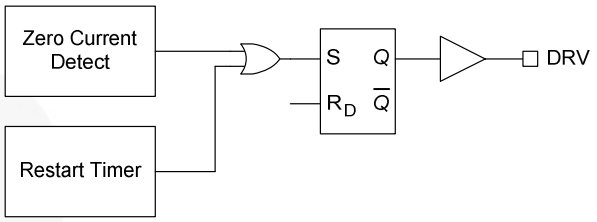


Figure 12. PWM Cycle Start

6. Terminating the Conduction Interval

Terminating the conduction period of the boost transistor in boundary conduction mode controllers is similar to any other pulse width modulator. During normal operation, the PWM comparator turns off the power transistor when the ramp waveform exceeds the control voltage provided by the error amplifier. In the FAN9611/12 and in similar voltage-mode PWMs, the ramp is a linearly rising waveform at one input of the comparator circuit.

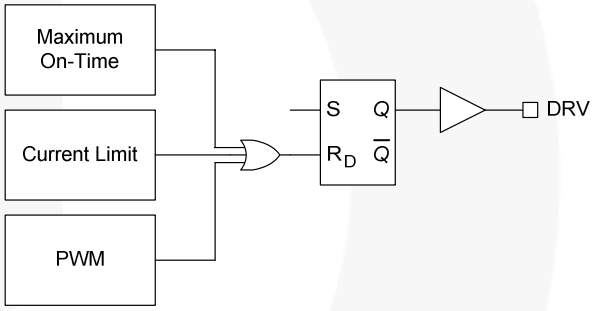


Figure 13. Conduction Interval Termination

In addition to the PWM comparator, the current limit circuit and a timer circuit limiting the maximum on-time of the boost transistor can also terminate the gate drive pulse of the controller. These functions provide protection for the power switch against excessive current stress.

7. Protecting the Power Components

In general, power converters are designed with adequate margin for reliable operation under all operating conditions. However, it might be difficult to predict dangerous conditions under transient or certain fault situations. Therefore, the FAN9611/12 contains dedicated protection circuits to monitor the individual peak currents in the boost inductors and in the power transistors. Furthermore, the boost output voltage is sensed by two independent mechanisms to provide over-voltage protection for the power transistors, rectifier diodes, and the output energy storage capacitor of the converter.

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8. Power Limit

The architecture and operating principle of FAN9611/12 also provides inherent input power limiting capability.

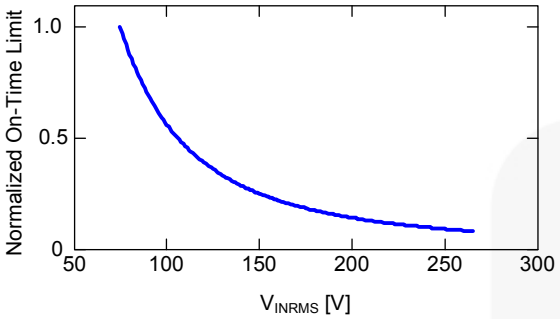


Figure 14. On-Time vs. V_{IN_RMS}

When the slope of the PWM ramp is made proportional to the square of the input RMS voltage, the maximum on-time of the boost power switch becomes inversely proportional to the square of $V_{IN,RMS}$, as represented in Figure 14. In boundary-conduction mode, the peak current of the boost transistor is proportional to its on time. Therefore, controlling the maximum pulse width of the gate drive signal according to the curve shown is an effective method to implement an input-voltage independent power limit for the boost PFC.

9. Light-Load Operation (Phase Management)

One of the parameters determining the operating frequency of a boundary conduction mode converter is the output power. As the load decreases, lower peak currents are commanded by the pulse width modulator to maintain the output voltage at the desired set point. Lower peak current means shorter on-time for the power transistor and shorter time interval to ramp the inductor current back to zero at any given input voltage. As a result, the operating frequency of the converter increases under light load condition.

As the operating frequency and corresponding switching losses increase, conduction losses diminish at the same time. Therefore, the power losses of the converter are dominated by switching losses at light load. This phenomenon is especially evident in a BCM converter.

To improve light-load efficiency, FAN9611/12 disables one of the two interleaved boost converters automatically when the output power falls below approximately 12% of the maximum power limit level. By managing the number of phases used at light load, the FAN9611/12 can maintain high efficiency for a wider load range of the power supply.

Normal interleaved operation of the two boost converters resumes automatically once the output power exceeds approximately 19% of the maximum power limit level of the converter.

By adjusting the maximum on-time (using R_{MOT}), the phase management thresholds can be adjusted upward, as described in the “Adjusting the Phase-Management Thresholds” section of Application Information in this datasheet.

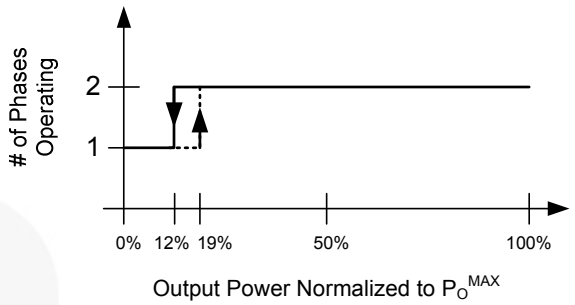


Figure 15. Automatic Phase-Control Operation

10. Brownout Protection with Soft Recovery

An additional protection function usually offered by PFC ICs is input brownout protection to prevent the converter from operating below a user-defined minimum input voltage level. For this function to work, the input voltage of the converter is monitored. When the voltage falls below the brownout protection threshold, the converter stops working. The output voltage of the boost converter falls until the load stops drawing current from the output capacitor or until the input voltage gets back to its nominal range and operation resumes.

As the output falls, the voltage at the feedback pin falls proportionally, according to the feedback divider ratio. To facilitate soft recovery after a brownout condition, the soft-start capacitor – which is also the reference voltage of the error amplifier – is pulled lower by the feedback network. This effectively pre-conditions the error amplifier to provide closed-loop, soft-start-like behavior during the converter’s recovery from a brownout situation. Once the input voltage goes above the brownout protection threshold, the converter resumes normal operation. The output voltage rises back to the nominal regulation level following the slowly rising voltage across the soft-start capacitor.

11. Soft Starting the Converter

During startup, the boost converter peak charges its output capacitor to the peak value of the input voltage waveform. The final voltage level, where the output is regulated during normal operation, is reached after the converter starts switching. There are two fundamentally different approaches used in PWM controllers to control the startup characteristics of a switched-mode power supply. Both methods use some kind of soft-start mechanism to reduce the potential overshoot of the converter’s output after the desired output voltage level is reached.

The first method is called open-loop soft-start and relies on gradually increasing the current or power limit of the converter during startup. In this case, the voltage error amplifier is typically saturated, commanding maximum current until the output voltage reaches its final value. At that time, the voltage between the error amplifier inputs changes polarity and the amplifier slowly comes out of saturation. While the error amplifier recovers and before it starts controlling the output voltage, the converter operates with full power. Thus, output voltage

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overshoot is unavoidable in converters utilizing the open-loop soft-start scheme.

This method is especially dangerous in power-factor-corrector applications because the error amplifier's bandwidth is typically limited to a very low crossover frequency. The slow response of the amplifier can cause considerable overshoot at the output.

FAN9611/12 employs closed-loop soft-start where the reference voltage of the error amplifier is slowly increased to its final value. When the current and power limits of the converter are properly taken into consideration, the output voltage of the converter follows the reference voltage. This ensures that the error amplifier stays in regulation during soft start and the output voltage overshoot can be eliminated.

Functional Description

1. Detecting Zero Inductor Current (ZCD1, ZCD2)

Each ZCD pin is internally clamped close to 0V (GND). Any capacitance on the pin is ineffective in providing any delay in ZCD triggering. The internal sense circuit is a true differentiator to catch the valley of the drain waveforms. The resistor between the auxiliary winding of the boost inductor and the ZCD pin is only used for current limiting. The maximum source current during zero current detection must be limited to 0.5mA. Source and sink capability of the pin is about 1mA, providing sufficient margin for the higher source current required during the on-time of the power MOSFETs.

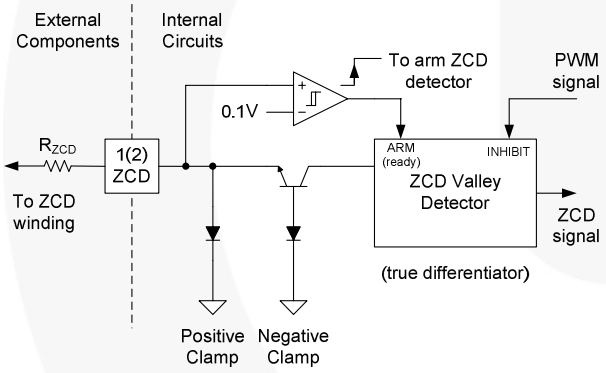


Figure 16. Zero-Current Detect Circuit

The R_{ZCD} resistor value can be approximated by:

$$R_{ZCD} = \frac{1}{0.5mA} \cdot \frac{V_O}{2} \cdot \frac{N_{AUX}}{N_{BOOST}} \quad (1)$$

2. 5V Bias Rail (5VB)

This is the bypass capacitor pin for the internal 5V bias rail powering the control circuitry. The recommended capacitor value is 220nF. At least a 100nF, good-quality, high-frequency, ceramic capacitor should be placed in close proximity to the pin.

The 5V rail is a switched rail. It is actively held LOW when the FAN9611/12 is in under-voltage lockout. Once the UVLO turn-on threshold is exceeded at the VDD pin, the 5V rail is turned on, providing a sharp edge that can be used as an indication that the chip is running. Potentially, this behavior can be utilized to control the inrush current limiting circuit.

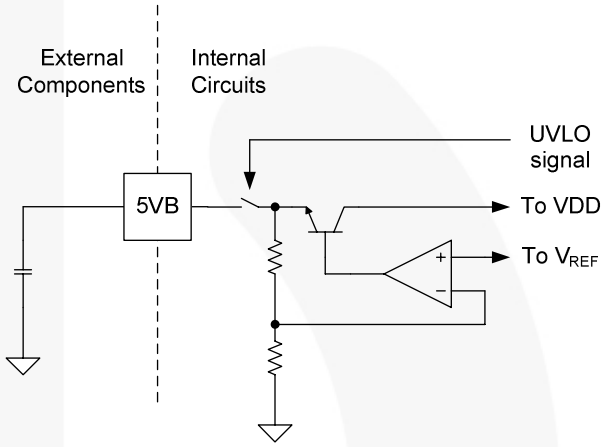


Figure 17. 5V Bias

3. Maximum On-Time Control (MOT)

Maximum on-time, MOT, (of the boost MOSFET) is set by a resistor to analog ground (AGND). The FAN9611/12 implements input-voltage feedforward. The maximum on-time is a function of the RMS input voltage. The voltage on the MOT pin is 1.25V during operation (constant DC voltage). The maximum on-time of the power MOSFETs can be approximated by:

$$t_{ON,MAX} = R_{MOT} \cdot 120 \cdot 10^{-12} \cdot \frac{2.4}{1.25} \cdot \frac{1}{V_{INSNS,PK}^2} \quad (2)$$

where $V_{INSNS,PK}$ is the peak of the AC input voltage as measured at the VIN pin (must be divided down, *see the VIN pin description*).

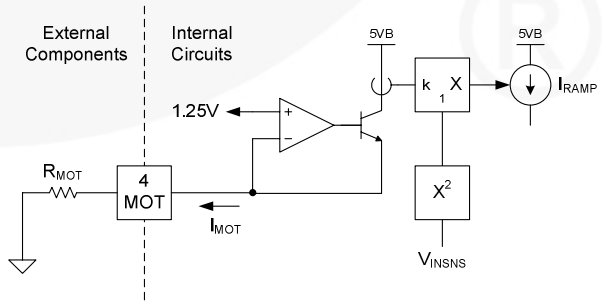


Figure 18. Maximum On-Time Control (MOT)

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4. Analog Ground (AGND) and Power Ground (PGND)

Analog ground connection (AGND) is the GND for all control logic biased from the 5V rail. Internally, the AGND and PGND pins are tied together by two anti-parallel diodes to limit ground bounce difference due to bond wire inductances during the switching actions of the high-current gate drive circuits. It is recommended to connect AGND and PGND pins together with a short, low-impedance trace on the PCB (right under the IC).

PGND is the reference potential (0V) for the high-current gate-drive circuit. Two bypass capacitors should be connected between the VDD pin and the PGND pin. One is the V_{DD} energy storage capacitor, which provides bias power during startup until the bootstrap power supply comes up. The other capacitor shall be a good-quality ceramic bypass capacitor, as close as possible to PGND and VDD pins to filter the high peak currents of the gate driver circuits. The value of the ceramic bypass capacitor is a strong function of the gate charge requirement of the power MOSFETs and its recommended value is between 1μF and 4.7μF to ensure proper operation.

5. Soft-Start (SS)

Soft-start is programmed with a capacitor between the SS pin and AGND. This is the non-inverting input of the transconductance (g_M) error amplifier.

At startup, the soft-start capacitor is quickly pre-charged to a voltage approximately 0.2V below the voltage on the feedback pin (FB) to minimize startup delay. Then a 5μA current source takes over and charges the soft-start capacitor slowly, ramping up the voltage reference of the error amplifier. By ramping up the reference slowly, the voltage regulation loop can stay closed, actively controlling the output voltage during startup. While the SS capacitor is charging, the output of the error amplifier is monitored. In case the error voltage (COMP) ever exceeds 3.5V, indicating that the voltage loop is close to saturation, the 5μA soft-start current is reduced. Therefore, the soft start is automatically extended to reduce the current needed to charge the output capacitor, reducing the output power during startup. This mechanism is integrated to prevent the voltage loop from saturation. The charge current of the soft-start capacitor can be reduced from the initial 5μA to as low as 0.5μA minimum.

In addition to modulating the soft-start current into the SS capacitor, the SS pin is clamped approximately 0.2V above the FB pin. This is useful in preventing the SS capacitor from running away from the FB pin and defeating the closed-loop soft-start. During the zero crossing of the input source waveform, the input power is almost zero and the output voltage can not be raised. Therefore the FB voltage stays flat or even decays while the SS voltage keeps rising. This is a problem if closed-loop soft-start should be maintained. By clamping the SS voltage to the FB pin, this problem can be mitigated.

Furthermore, during brownout condition, the output voltage of the converter might fall, which is reflected at the FB pin. When FB voltage goes 0.2V below the voltage on the SS pin, it starts discharging the soft-start capacitor. The soft-start capacitor remains 0.2V above the FB voltage. When the brownout condition is over, the converter returns to normal operation gracefully, following the slow ramp up of the soft-start capacitor at the non-inverting input of the error amplifier.

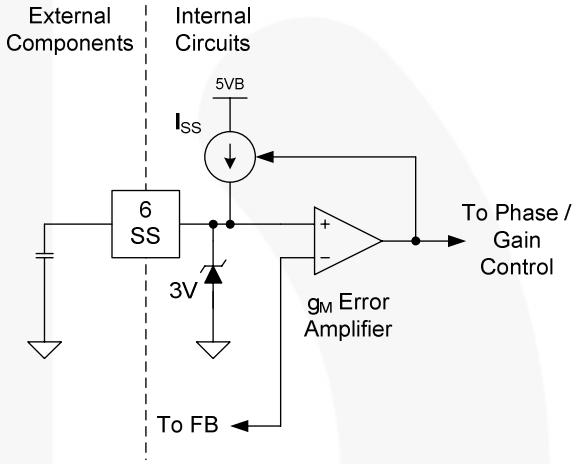


Figure 19. Soft-Start Programming

6. Error Amplifier Compensation (COMP)

COMP pin is the output of the error amplifier. The voltage loop is compensated by a combination of R_S and C_S to AGND at this pin. The control range of the error amplifier is between 0.175V and 4.3V. When the COMP voltage is below about 0.175V, the PWM circuit skips pulses. Above 4.3V, the maximum on-time limit terminates the conduction of the boost switches.

Due to the input-voltage feedforward, the output of the error amplifier is proportional to the input power of the converter, independent of the input voltage. In addition, also due to the input-voltage feedforward, the maximum power capability of the converter and the loop gain is independent of the input voltage. The controller's phase-management circuit monitors the error amplifier output and switches to single-phase operation when the COMP voltage falls below ~0.7V and returns to two-phase operation when the error voltage exceeds 0.96V. These thresholds correspond to about 12.2% and 18.5% of the maximum power capability of the design.

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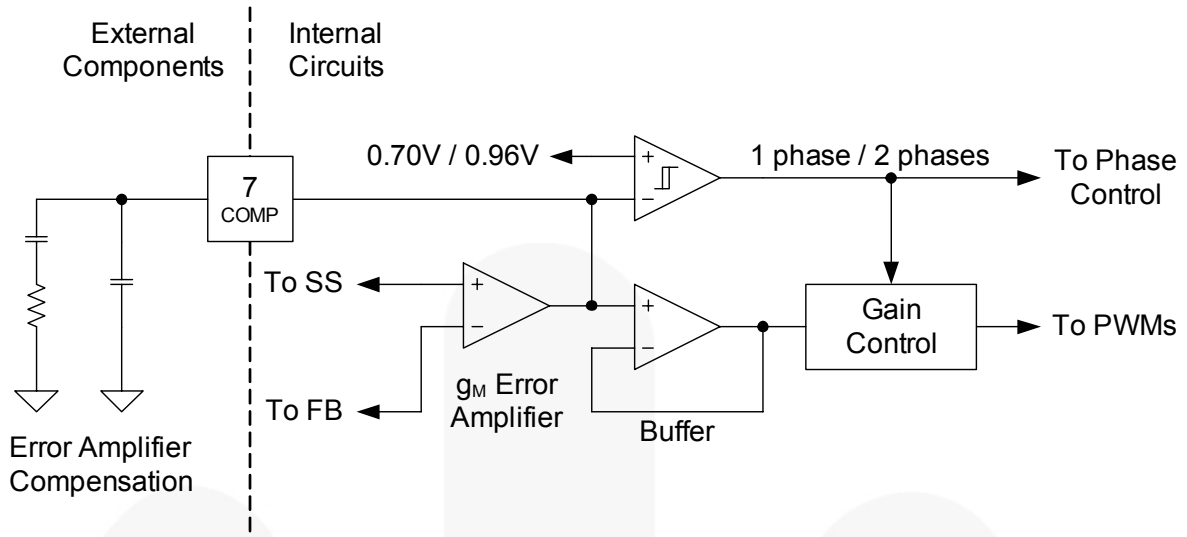


Figure 20. Error Amplifier Compensation Circuitry

7. Output Voltage Feedback (FB)

The feedback pin receives the divided-down output voltage of the converter. In regulation, the FB pin should be 3V, which is the reference used at the non-inverting input of the error amplifier. Due to the g_M type error amplifier, the FB pin is always proportional to the output voltage and can be used for over-voltage protection as well. A non-latching over-voltage detection circuit monitors the FB pin and prevents the boost MOSFETs from turning on when the FB voltage exceeds 3.25V. Operation resumes automatically when the FB voltage returns to its nominal 3V level.

The open feedback detection circuit is also connected to the FB pin. Since the output of the boost converter is charged to the peak of the input AC voltage when power is applied to the power supply, the detection circuit monitors the presence of this voltage. If the FB pin is below 0.5V, which would indicate a missing feedback divider (or wrong value causing dangerously-high regulation voltage), the FAN9611/12 does not send out gate drive signals to the boost transistors.

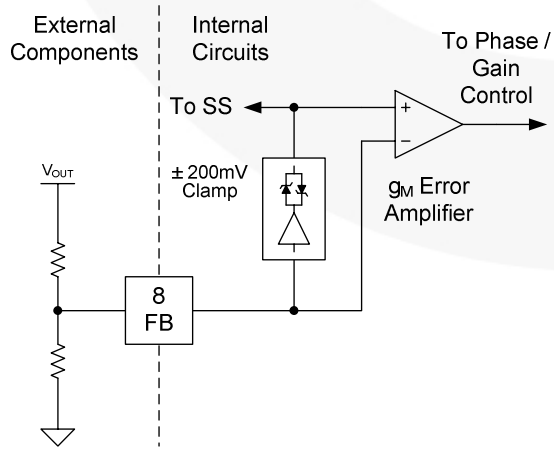


Figure 21. Output-Voltage Feedback Circuit

8. Secondary Output Voltage Sense (OVP)

A second-level latching over-voltage protection can be implemented using the OVP pin of the controller. The threshold of this circuit is set to 3.5V. There are two ways to program the secondary OVP.

Option 1, as shown in Figure 22, is to connect the OVP pin to the FB pin. In addition to the standard non-latching OVP (set at ~8%), this configuration provides a second OVP protection (set at ~15%), which is latched.

In the case where redundant over-voltage protection is preferred (also called double-OVP protection), a second separate divider from the output voltage can be used, as shown by Option 2 in Figure 22. In this case, the latching OVP protection level can be independently established below or above the non-latching OVP threshold, which is based on the feedback voltage (at the FB pin).

If latching OVP protection is not desired at all, the OVP pin should be grounded (Option 3).

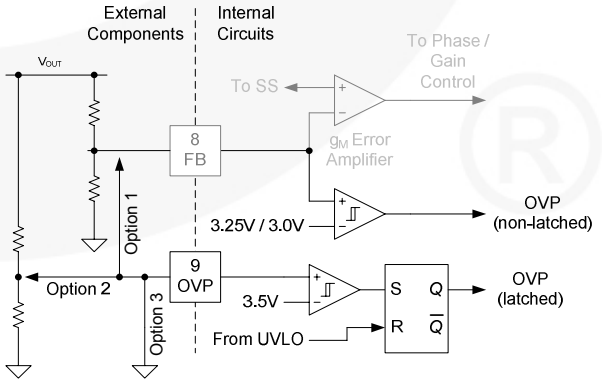


Figure 22. Secondary Over-Voltage Protection Circuit

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9. Input Voltage Sensing (V_{IN})

The input AC voltage is sensed at the VIN pin. The input voltage is used in three functions: input under-voltage lockout (brownout protection), input over-voltage protection, and input voltage feedforward in the PWM control circuit. All the functions require the RMS value of the input voltage waveform. Since the RMS value of the AC input voltage is directly proportional to its peak, it is sufficient to find the peak instead of the more complicated and slower method of integrating the input voltage over a half line cycle. The internal circuit of the VIN pin works with peak detection of the input AC waveforms. One of the important benefits of this approach is that the peak indicates the correct RMS value even at no load when the HF filter capacitor at the input side of the boost converter is not discharged around the zero crossing of the line waveform. Another notable benefit is that during line transients, when the peak exceeds the previously measured value, the input-voltage feedforward circuit can react immediately, without waiting for a valid integral value at the end of the half line period. Furthermore, lack of zero crossing detection could fool the integrator while the peak detector works properly during light-load operation.

The valid range for the peak of the AC input is between approximately 0.925V and 3.7V. This range is optimized for universal input voltage range of operation. If the peak of the sense voltage remains below the 0.925V threshold, input under-voltage or brownout condition is declared and the FAN9611/12 stops operating. Similarly, when the V_{IN} voltage exceeds 3.7V, the FAN9611/12 stops switching due to input over voltage. The input voltage is measured by a tracking analog-to-digital converter, which keeps the highest value (peak voltage) of the input voltage waveform. Once a measurement is taken, the converter tracks the input for at least 12ms before a new value is taken. This delay ensures at least one new peak value is captured before the new value is used.

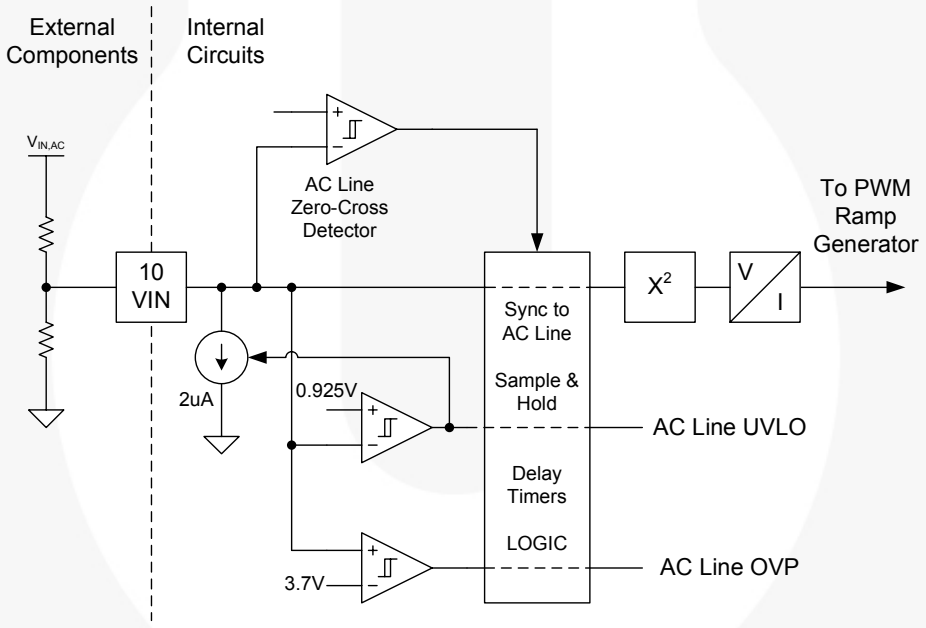


Figure 23. Input Voltage Sensing Circuit

The measured peak value is then used in the following half-line cycle while a new measurement is executed to be used in the next half line cycle. This operation is synchronized to the zero crossing of the line waveform. Since the input voltage measurement is held steady during the line half periods, this technique does not feed any AC ripple into the control loop. If line zero crossing detection is missing, the FAN9611/12 measures the input voltage in every 32ms; it can operate from a DC input as well. The following figures provide detail about the input voltage sensing method of the controller.

As can be seen from the waveforms, input voltage feedforward is instantaneous when the line voltage increases and has a half line cycle delay when the input voltage decreases. Any increase in input voltage would cause output over voltage due to the slow nature of the voltage regulation loop. This is successfully mitigated by the immediate action of the input-voltage feedforward circuit.

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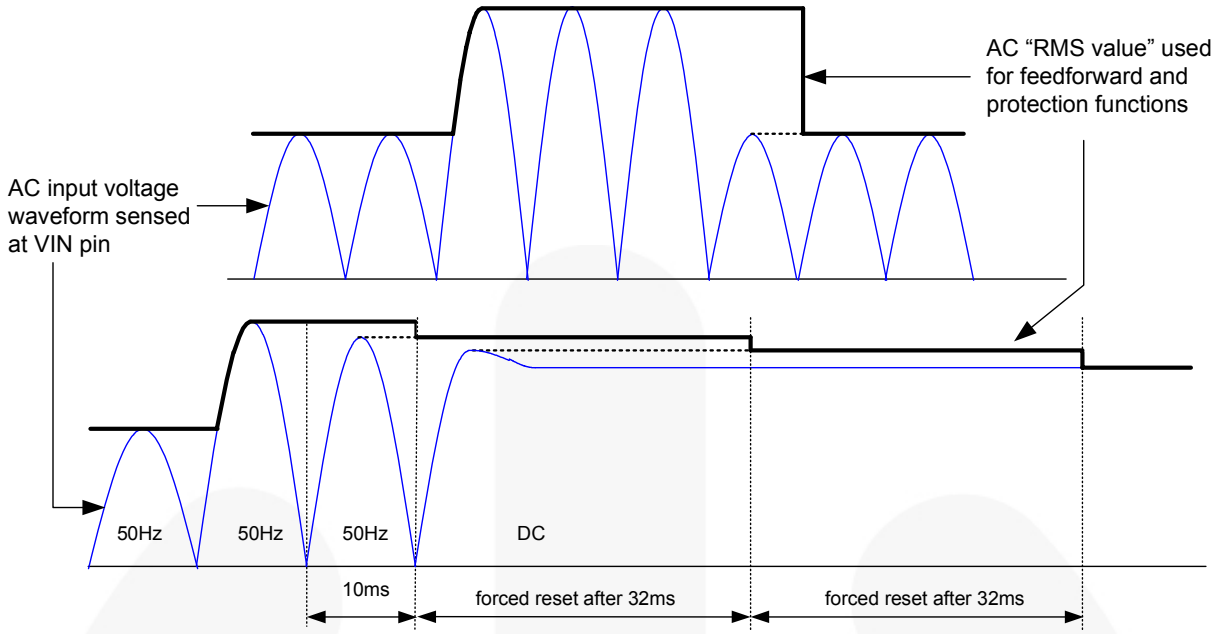


Figure 24. Input Voltage Sensing Waveforms

10. Gate Drive Outputs (DRV1; DRV2)

High-current driver outputs DRV1 and DRV2 have the capability to sink a minimum of 2A and source 1A. Due to the low impedance of these drivers, the 1A source current must be actively limited by an external gate resistor. The minimum external gate resistance is:

$$R_{GATE} = \frac{V_{DD}}{1A} \quad (3)$$

To take advantage of the higher sink current capability of the drivers, the gate resistor can be bypassed by a small diode to facilitate faster turn-off of the power MOSFETs. Traditional fast turn-off circuit using a PNP transistor instead of a simple bypass diode can be considered as well.

It is also imperative that the inductance of the gate drive loop is minimized to avoid excessive ringing. If optimum layout is not possible or the controller is placed on a daughter card, it is recommended to use an external driver circuit located near the gate and source terminals of the boost MOSFET transistors. Small gate charge power MOSFETs can be driven by a single 1A gate driver, such as the FAN3111C; while higher gate charge devices might require higher gate drive current capable devices, such as the single-2A FAN3100C or the dual-2A FAN3227C family of drivers.

11. MillerDrive™ Gate Drive Technology

FAN9611/12 output stage incorporates the MillerDrive™ architecture shown in Figure 25. It is a combination of bipolar and MOS devices which are capable of providing large currents over a wide range of supply voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between 1/3 to 2/3 V_{DD} and the MOS devices pull the output to the high or low rail.

The purpose of the MillerDrive™ architecture is to speed switching by providing high current during the Miller plateau region when the gate-drain capacitance of the MOSFET is being charged or discharged as part of the turn-on / turn-off process.

The output pin slew rate is determined by V_{DD} voltage and the load on the output. It is not user adjustable, but if a slower rise or fall time at the MOSFET gate is needed, a series resistor can be added.

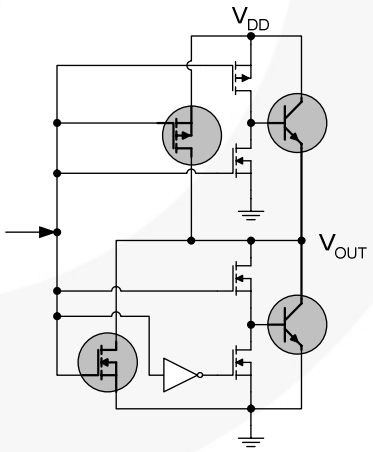


Figure 25. Current-Sense Protection Circuits

12. Bias Supply (V_{DD})

This is the main bias source for the FAN9611/12. The operating voltage range is between ~8V and 18V. The V_{DD} voltage is monitored by the under-voltage lockout (UVLO) circuit. At power-up, the V_{DD} voltage must exceed 12.5V (±1V) to enable operation. The FAN9611/12 stops operating when the V_{DD} voltage falls below 8V (±1V). *See PGND pin description for important bypass information.*

13. Current-Sense Protection (CS1, CS2)

The FAN9611/12 uses independent over-current protection for each of the power MOSFETs. The current-sense thresholds at the CS1 and CS2 pins are approximately 0.2V. The current measurements are strictly for protection purposes and are not part of the control algorithm. The pins can be directly connected to the non-grounded end of the current-sense resistors because the usual R-C filters of the leading-edge current spike are integrated in the IC.

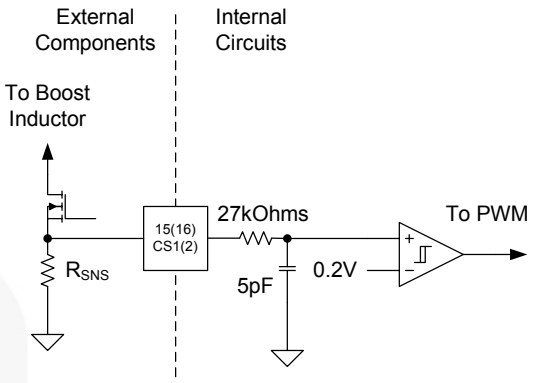


Figure 26. Current-Sense Protection Circuits

The time constant of the internal filter is approximately:

$$\tau = 27k\Omega \cdot 5pF = 130ns$$

or

$$\omega_P = \frac{1}{2 \cdot \pi \cdot 27k\Omega \cdot 5pF} = 1.2MHz \quad (4)$$

Application Information

1. Synchronization and Timing Functions

The FAN9611/12 employs a sophisticated synchronization sub-system. At the heart of the system is a dual-channel switching-frequency detector that measures the switching period of each channel in every switching cycle and locks their operating phase 180 degrees out of phase from each other. The slower operating frequency channel is dominant, but there is no master-slave arrangement. Moreover, as the frequency constantly changes due to the varying input voltage, either channel can be the slower dominant channel.

As opposed to the most common technique, where the phase relationship between the channels is provided by changing the on-time of one of the MOSFETs, the FAN9611/12 controls the phase relationship by inserting a turn-on delay before the next switching period starts for the faster running phase. As shown in the literature[1], the on-time modulation technique is not stable under all operating conditions, while the off-time modulation (or delaying the turn-on) is unconditionally stable under all operating conditions.

a. Restart Timer and Dead-Phase Detect Protection

The restart timer is an integral part of the Sync-Lock™ synchronizing circuit. It ensures exact 180-degree out-of-phase operation in restart timer operation. This is an important safety feature. In the case of a non-operating phase due to no ZCD detection, missing gate drive connection (for example no gate resistor), one of the power components failing in an open circuit, or similar errors, the other phase is locked into restart timer operation, preventing it from trying to deliver full power to the load. This is called the dead-phase detect protection.

The restart timer is set to approximately 18kHz, just above the audible frequency range, to avoid any acoustic noise generation.

b. Frequency Clamp

Just as the restart timer, the frequency clamp is integrated into the synchronization and ensures exact 180-degree out-of-phase operation when the operating frequency is limited. This might occur at very light-load operation or near the zero crossing region of the line voltage waveform. Limiting the switching frequency at light load can improve efficiency, but has a negative effect on power factor since the converter also enters true DCM operation. The frequency clamp is set to approximately 600kHz.

2. Adjusting the Output Voltage with Load

In some applications, the output voltage of the PFC boost converter is decreased at low power levels to boost the light load efficiency of the power supply.

Implementing this function with a circuit external to the FAN9611/12 is straightforward because the error amplifier reference (the positive input) is available on the soft-start (SS) pin, as shown in Figure 27. In the FAN9611/12 architecture, the power of the converter is proportional to the voltage on the COMP pin, minus a small offset. The voltage on the COMP pin is monitored to determine the operating power of the supply. Therefore the voltage on the SS pin can be adjusted lower to achieve the desired lower output voltage.

Several possible implementations to adjust the output voltage of the boost stage at light load are described in the application note AN-8021. It includes the universal output voltage adjust implementation which is modulated by input voltage to avoid the boost converter becoming a peak rectifier at high line and light load.

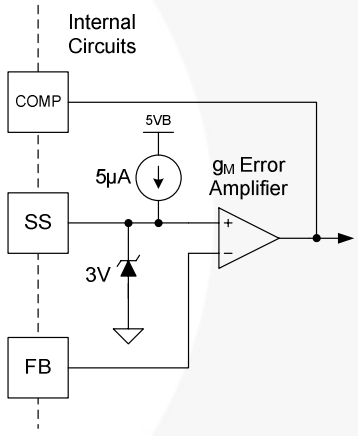


Figure 27. FAN9611/12 Error Amplifier Configuration

3. Adjusting the Output Voltage with Input Voltage

In some applications, the output voltage of the PFC boost converter is adjusted based on the input voltage only. This boost follower implementations increases the efficiency of the downstream DC-DC converter and therefore of the overall power supply.

Implementations for both the two-level boost and the linear boost follower (or tracking boost) are described in application note AN-8021.

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4. Adjusting the Phase-Management Thresholds

In any power converter, the switching losses become dominant at light load. For an interleaved converter where there are two or more phases, light-load efficiency can be improved by shutting down one of the phases at light load (also known as phase-shedding or phase-dropping operating).

The initial phase-management thresholds are fixed at approximately 12% and 19% of the maximum load power level. This means when the output power reaches 12%, the FAN9611/12 automatically goes from a two-phase to a single-phase operation (phase shed or phase drop). When the output power comes back up to 19%, the FAN9611/12 automatically goes from the single-phase to the two-phase operation (phase-add).

The default thresholds can be adjusted upward based on the application requirement; for example, to meet the Energy STAR 5.0 or the Climate Savers Computing efficiency requirements at 20% of the load. The phase drop threshold can be adjusted upward (for example to 25%) by adjusting the maximum on time.

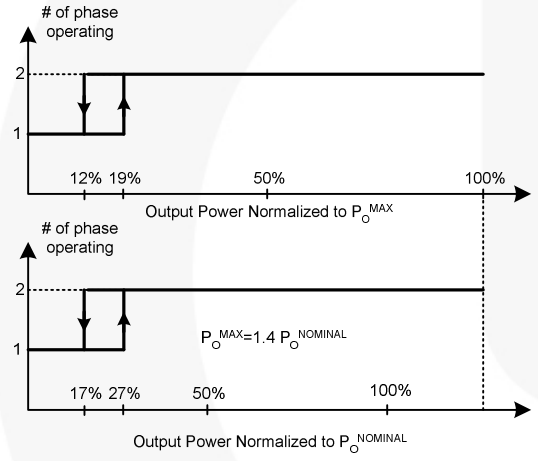


Figure 28. Adjusting Phase Management Thresholds

Since the phase management threshold is fixed at 12% and 19% of the maximum power limit level, the actual power management threshold as a percentage of nominal output power can be adjusted by the ratio between nominal power and maximum power limit level as shown in Figure 28. The second plot shows an example where the maximum power limit level is 1.4 times of nominal output power. By adjusting the maximum on-time (using R_{MOT}), the phase management thresholds can be adjusted upward.

Phase management is implemented such that the output of the error amplifier (V_{COMP}) does not have to change when the system toggles between single-phase and two-phase operations, as shown in Figure 29. The output of the error amplifier is proportional to the output power of the converter independently, whether one or both phases are operating in the power supply. Furthermore, because the maximum on-time limit is applied independently to each pulse-width modulator, the power handling capability of the converter with only one phase running is approximately half of the total output power that can be delivered when both phases are utilized.

Additional details on adjusting phase management are provided in the application note AN-6086.

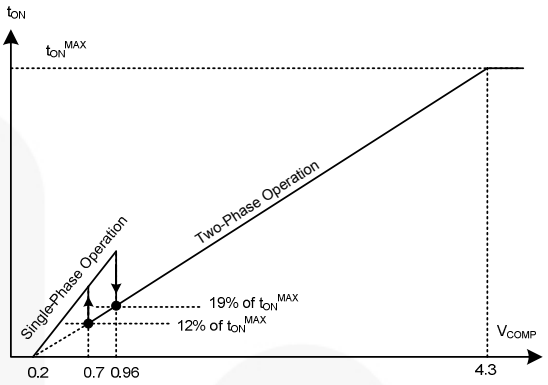


Figure 29. V_{COMP} vs. t_{ON}^{MAX}

5. Disabling the FAN9611/12

There are four ways to disable the FAN9611/12. It is important to understand how the part reacts for the various shutdown procedures.

a. Pull the SS Pin to GND. This method uses the error amplifier to stop the operation of the power supply. By pulling the SS pin to GND, the error amplifier's non-inverting input is pulled to GND. The amplifier senses that the inverting input (FB pin) is higher than the reference voltage and tries to adjust its output (COMP pin) to make the FB pin equal to the reference at the SS pin. Due to the slow speed of the voltage loop in PFC applications, this might take several line cycles. Thus, it is important to consider that by pulling the SS pin to GND, the power supply is not shut down immediately. Recovery from a shut down follows normal soft-start procedure when the SS pin is released.

b. Pull the FB Pin to GND. By pulling the FB pin below the open feedback protection threshold of approximately 0.5V, the power supply can be shut down immediately. It is imperative that the FB is pulled below the threshold very quickly since the power supply keeps switching until this threshold is crossed. If the feedback is pulled LOW softly and does not cross the threshold, the power supply tries to deliver maximum power because the FB pin is forced below the reference voltage of the error amplifier on the SS pin. Eventually, as FB is pulled to GND, the SS capacitor is pulled LOW by the internal clamp between the FB and SS pins. The SS pin stays approximately 0.2V higher than the FB pin itself. Therefore, recovery from a shut down state follows normal soft-start procedure when the FB pin is released as the voltage across the SS capacitor starts ramping from a low value.

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c. Pulling the COMP Pin to GND. When the COMP pin is pulled below the PWM ramp offset, approximately 0.195V, the FAN9611/12 stops sending gate drive pulses to the power MOSFETs. This condition is similar to pulse skipping under no-load condition. If any load is still present at the output of the boost PFC stage, the output voltage decreases. Consequently, the FB pin decreases and the SS capacitor voltage is pulled LOW by the internal clamp between the FB and SS pins. At that point, the operation and eventual recovery to normal operation is similar to the mechanism described above. If the COMP pin is held LOW for long enough to pull the SS pin LOW, the recovery follows normal soft-start procedure when the COMP pin is released. If the SS capacitor is not pulled LOW as a result of a momentary pull-down of the COMP pin, the recovery is still soft due to the fact that a limited current source is charging the compensation capacitors at the output of the error amplifier. Nevertheless, in this case, output voltage overshoot can occur before the voltage loop enters closed-loop operation and resumes controlling the output voltage again.

d. Pull the VIN Pin to GND. Since the VIN sense circuit is configured to ride through a single line cycle dropout test without shutting down the power supply, this method results in a delayed shutdown of the converter. The FAN9611/12 stops operation approximately 20ms to 32ms after the VIN pin is pulled LOW. The delay depends on the phase of the line cycle at which the pull-down occurs. This method triggers the input brownout protection (input under-voltage lockout), which gradually discharges the compensation capacitor. As the output voltage decreases, the FB pin falls, pulling LOW the SS capacitor voltage. Similarly to the shutdown, once the VIN pin is released, operation resumes after several milliseconds of delay needed to determine that the input voltage is above the turn-on threshold. At least one line cycle peak must be detected above the turn-on threshold before operation can resume at the following line voltage zero-crossing. The converter starts following normal soft-start procedure.

6. Layout and Connection Guidelines

For high-power applications, two or more PCB layers are recommended to effectively use the ground pattern to minimize the switching noise interference.

The FAN9611/12 incorporates fast-reacting input circuits, short propagation delays, and strong output stages capable of delivering current peaks over 1.5A to facilitate fast voltage transition times. Many high-speed power circuits can be susceptible to noise injected from their own output or external sources, possibly causing output re-triggering. These effects can be especially obvious if the circuit is tested in breadboard or non-optimal circuit layouts with long input or output leads. The following guidelines are recommended for all layout designs, but especially strongly for the single-layer PCB designs. *(For example of a 1-layer PCB design, see the Application Note AN-6086.)*

General

- Keep high-current output and power ground paths separate from analog input signals and signal ground paths.
- For best results, make connections to all pins as short and direct as possible.

Power Ground and Analog Ground

- Power ground (PGND) and analog ground (AGND) should meet at one point only.
- All the control components should be connected to AGND without sharing the trace with PGND.
- The return path for the gate drive current and V_{DD} capacitor should be connected to the PGND pin.
- Minimize the ground loops between the driver outputs (DRV1, DRV2), MOSFETs, and PGND.
- Adding the by-pass capacitor for noise on the VDD pin is recommended. It should be connected as close to the pin as possible.

Gate Drive

- The gate drive pattern should be wide enough to handle 1A peak current.
- Keep the controller as close to the MOSFETs as possible. This minimizes the length and the loop area (series inductance) of the high-current gate drive traces. The gate drive pattern should be as short as possible to minimize interference.

Current Sensing

- Current sensing should be as short as possible.
- To minimize switching noise, current sensing should not make a loop.

Input Voltage Sensing (V_{IN})

- Since the impedance of voltage divider is large and FAN9611/12 detects the peak of the line voltage, the VIN pin can be sensitive to the switching noise. The trace connected to this pin should not cross traces with high di/dt to minimize the interference.
- The noise bypass capacitor for V_{IN} should be connected as close to the pin as possible.

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Quick Setup Guide

The FAN9611/12 can be configured following the next steps outlined in this section. This Quick Setup Guide refers to the schematic diagram and component references of Figure 31. It uses the equations derived and explained in Application Note AN-6086.

In preparation to calculate the setup component values, the power supply specification must be known. Furthermore, a few power stage components must be pre-calculated before the controller design begins as their values determine the component selections.

Description	Name	Value
From Power Supply Specification:		
Minimum AC RMS Input (Turn-On)	$V_{LINE.ON}$	
Minimum AC RMS Input (Turn-Off) [1]	$V_{LINE.OFF}$	
Maximum AC RMS Input (OVP) [1]	$V_{LINE.MAX}$	
Minimum Line Frequency	$f_{LINE,MIN}$	
Nominal DC Output	V_{OUT}	
Output Voltage Ripple ($2 \cdot f_{LINE}$)	$V_{OUT,RIPPLE}$	
Latching Output OVP	$V_{OUT,LATCH}$	
Nominal Output Power (to Load)	P_{OUT}	
Desired Hold-Up Time	t_{HOLD}	
Minimum DC Output (End of t_{HOLD})	$V_{OUT,MIN}$	
Minimum Switching Frequency	$f_{SW,MIN}$	
Maximum DC Bias (for FAN9611/12)	V_{DDMAX}	
Pre-Calculated Power Stage Parameters:		
Estimated Conversion Efficiency	η	0.95
Maximum Output Power per Channel	$P_{MAX,CH}$	
Output Capacitance	C_{OUT}	
Boost Inductance per Channel	L	
Maximum On-Time per Channel	$t_{ON,MAX}$	
Turns Ratio (N_{BOOST} / N_{AUX})	N	10
Other Variables Used During the Calculations:		
Peak Inductor Current	$I_{L,PK}$	
Maximum DC Output Current (to Load)	$I_{O,MAX}$	
Calculated Component Values:		
Zero Current Detect Resistor	R_{ZCD1}, R_{ZCD2}	
Bypass Capacitor for 5V Bias	C_{5VB}	0.15µ
Maximum On-Time Set	R_{MOT}	
Soft-Start Capacitor	C_{SS}	
Compensation Capacitor	$C_{COMP,LF}$	
Compensation Resistor	R_{COMP}	
Compensation Capacitor	$C_{COMP,HF}$	
Feedback Divider	R_{FB1}	
Feedback Divider	R_{FB2}	
Over Voltage Sense Divider	R_{OV1}	
Over Voltage Sense Divider	R_{OV2}	
Input Voltage Sense Divider	R_{IN1}	
Input Voltage Sense Divider	R_{IN2}	
Brownout Hysteresis Set	R_{INHYST}	
Gate Drive Resistor	R_{G1}, R_{G2}	
Gate Drive Speed-Up Diode	D_{G1}, D_{G2}	
Bypass Capacitor for VDD_HF	C_{VDD1}	2.2µ
Startup Energy Storage for V_{DD}	C_{VDD2}	47µ
Current Sense Resistor	R_{CS1}, R_{CS2}	

Step 1: Input Voltage Range

FAN9611/12 utilizes a single pin (VIN) for input voltage sensing. The valid voltage range of the VIN pin is from 0.925V to 3.7V. A VIN pin voltage below 0.925V activates the line under-voltage lockout, while anything above 3.7V halts the operation due to input over-voltage protection. Thus, the ratio of $V_{LINE.MAX}$ and $V_{LINE.OFF}$ is always 4. Consequently, only one of those two parameters can be freely chosen by the designer. The turn-on voltage ($V_{LINE.ON}$) can be set independently of the other two thresholds, as demonstrated in Figure 30.

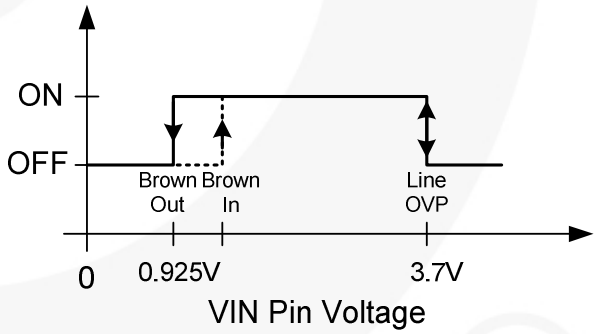


Figure 30. Simplified Turn-on and Turn-off Thresholds at the VIN Pin

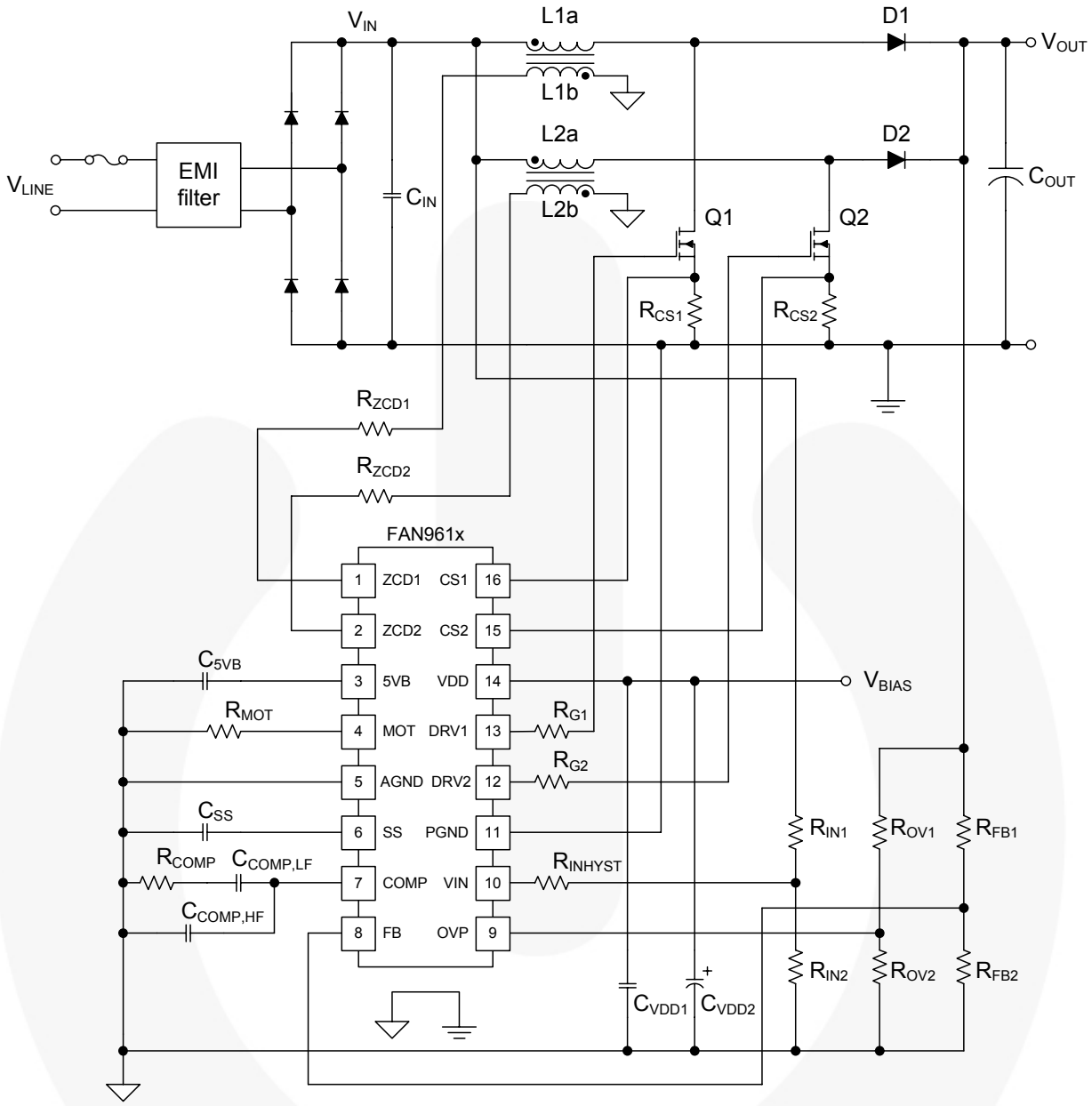


Figure 31. Interleaved BCM PFC Schematic Using FAN9611/12

Step 2: Estimated Conversion Efficiency

Use the estimated full-load power conversion efficiency. Typical value for an interleaved BCP PFC converter is in the 0.92 to 0.98 range. The efficiency is in the lower half of the range for low-power applications. Using state-of-the-art semiconductors, good quality ferrite inductors and selecting lower limit for minimum switching frequency positively impacts the efficiency of the system. In general, the value of 0.95 can be used unless a more accurate power budget is available.

Step 3: Maximum Output Power per Channel

$$P_{MAX,CH} = 1.2 \cdot \frac{P_{OUT}}{2} \quad (5)$$

A margin of 20% has been added to the nominal output power to cover reference inaccuracy, internal component tolerances, inductance mismatch, and current-sense resistor variation to the per-channel power rating.

Step 4: Output Capacitance

$$C_{OUT(RIPPLE)} = \frac{P_{OUT}}{4 \cdot f_{LINE,MIN} \cdot V_{OUT} \cdot V_{OUT,RIPPLE}} \quad (6)$$

$$C_{OUT(HOLD)} = \frac{2 \cdot P_{OUT} \cdot t_{HOLD}}{\left(V_{OUT} - \frac{V_{OUT,RIPPLE}}{2}\right)^2 - V_{OUT,MIN}^2} \quad (7)$$

The output capacitance must be calculated by two different methods. The first equation determines the capacitor value based on the allowable ripple voltage at the minimum line frequency. It is important to remember that the scaled version of this ripple is present at the FB pin. The feedback voltage is continuously monitored by the non-latching over voltage protection circuit. Its threshold is about 8% higher the nominal output voltage. To avoid triggering the OVP protection during normal operation, $V_{OUT,RIPPLE}$ should be limited to less 12% of the nominal output voltage, V_{OUT}.

The second expression yields the minimum output capacitance based on the required hold-up time based on the power supply specification. Ultimately, the larger of the two values satisfies both design requirements and has to be selected for C_{OUT}.

Step 5: Boost Inductance per Channel

$$L_{LINE,OFF} = \frac{\eta \cdot V_{LINE,OFF}^2 \cdot \left(V_{OUT} - \sqrt{2} \cdot V_{LINE,OFF}\right)}{2 \cdot f_{SW,MIN} \cdot V_{OUT} \cdot P_{MAX,CH}} \quad (8)$$

$$L_{LINE,MAX} = \frac{\eta \cdot V_{LINE,MAX}^2 \cdot \left(V_{OUT} - \sqrt{2} \cdot V_{LINE,MAX}\right)}{2 \cdot f_{SW,MIN} \cdot V_{OUT} \cdot P_{MAX,CH}} \quad (9)$$

The minimum switching frequency can occur either at the lowest or at the highest input line voltage. Accordingly, two boost inductor values are calculated and the lower of the two inductances must be selected. This L value keeps the minimum operating frequency above $f_{SW,MIN}$ under all operating conditions.

Step 6: Maximum On-Time per Channel

$$t_{ON,MAX} = \frac{2 \cdot L \cdot P_{MAX,CH}}{\eta \cdot V_{LINE,OFF}^2} \quad (10)$$

Step 7: Peak Inductor Current per Channel

$$I_{L,PK} = \frac{\sqrt{2} \cdot V_{LINE,OFF}}{L} \cdot t_{ON,MAX} \quad (11)$$

Step 8: Maximum DC Output Current

$$I_{OUT,MAX} = \frac{2 \cdot P_{MAX,CH}}{V_{OUT}} \quad (12)$$

Step 9: Zero Current Detect Resistors

$$R_{ZCD1} = R_{ZCD2} = \frac{0.5 \cdot V_{OUT}}{N \cdot 0.5mA} \quad (13)$$

where $0.5 \cdot V_{OUT}$ is the maximum amplitude of the resonant waveform across the boost inductor during zero current detection; N is the turns ratio of the boost inductor and the auxiliary winding utilized for the zero current detection; and 0.5mA is the maximum current of the ZCD pin during the zero current detection period.

Step 10: Maximum On-Time Setting Resistor

$$R_{MOT} = 4340 \cdot 10^6 \cdot t_{ON,MAX} \quad (14)$$

where R_{MOT} should be between 40kΩ and 130kΩ.

Step 11: Output Voltage Setting Resistors (Feedback)

$$R_{FB2} = \frac{3V \cdot V_{OUT}}{P_{FB}} = \frac{3V}{I_{FB}} \quad (15)$$

where 3V is the reference voltage of the error amplifier at its non-inverting input and P_{FB} or I_{FB} are selected by the designer. If the power loss associated to the feedback divider is critical to meet stand-by power consumption regulations, it might be beneficial to start the calculation by choosing P_{FB}. Otherwise, the current of feedback divider, I_{FB} should be set to approximately 0.4mA at the desired output voltage set point. This value ensures that parasitic circuit board and pin capacitances do not introduce unwanted filtering effect in the feedback path.

If the feedback divider is used to provide startup power for the FAN9611/12 *(see AN-6086 for implementation details)*, the following equation is used to calculate R_{FB2}:

$$R_{FB2} = \frac{3V \cdot \left[\sqrt{2} \cdot V_{LINE,ON} - (12.5V + 3 \cdot 0.7V)\right]}{0.12mA \cdot V_{OUT}} \quad (16)$$

where 3V is the reference voltage of the error amplifier at its non-inverting input; 12.5V is the controller's UVLO turn-on threshold; 0.12mA is the worst-case startup current required to start operation; and 3·0.7V accounts for the forward voltage drop of three diodes in series of the startup current. Once the value of R_{FB2} is determined, R_{FB1} is given by the following formula:

$$R_{FB1} = \left(\frac{V_{OUT}}{3V} - 1\right) \cdot R_{FB2} \quad (17)$$

R_{FB1} can be implemented as a series combination of two or three resistors; depending on safety regulations, maximum voltage, and or power rating of the selected resistor type.

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Step 12: Soft-Start Capacitor

$$C_{SS} = \frac{5\mu A \cdot C_{OUT} \cdot (R_{FB1} + R_{FB2})}{0.3 \cdot I_{OUT,MAX} \cdot R_{FB2}} \quad (18)$$

where 5μA is the charge current of the soft-start capacitor and $0.3 \cdot I_{OUT,MAX}$ is the maximum output current charging the output capacitor of the converter during the soft-start process. It is imperative to limit the charge current of the output capacitor to be able to maintain closed-loop soft-start of the converter. The 0.3 factor used in the C_{SS} equation can prevent output over voltage at the end of the soft-start period and provides sufficient margin to supply current to the load while the output capacitor is charging.

Step 13: Compensation Components

$$C_{COMP,LF} = \frac{g_M \cdot I_{OUT,MAX}}{4.1V \cdot C_{OUT} \cdot (2 \cdot \pi \cdot f_0)^2} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \quad (19)$$

where 4.1V is the control range of the error amplifier and f_0 is the desired voltage loop crossover frequency. It is important to consider that the lowest output ripple frequency limits the voltage loop crossover frequency. In PFC applications, that frequency is two times the AC line frequency. Therefore, the voltage loop bandwidth (f_0), is typically in the 5Hz to 15Hz range.

To guarantee closed-loop soft-start operation under all conditions, it is recommended that:

$$C_{COMP,HF} < 4 \cdot C_{SS} \quad (20)$$

This relationship is determined by the ratio between the maximum output current of the g_M error amplifier to the maximum charge current of the soft-start capacitor. Observing this correlation between the two capacitor values ensures that the compensation capacitor voltage can be adjusted faster than any voltage change taking place across the soft-start capacitor. Therefore, during startup the voltage regulation loop's response to the increasing soft-start voltage is not limited by the finite current capability of the error amplifier.

$$R_{COMP} = \frac{1}{2 \cdot \pi \cdot f_0 \cdot C_{COMP,LF}} \quad (21)$$

$$C_{COMP,HF} = \frac{1}{2 \cdot \pi \cdot f_{HFP} \cdot R_{COMP}} \quad (22)$$

where f_{HFP} is the frequency of a pole implemented in the error amplifier compensation network against high-frequency noise in the feedback loop. The pole should be placed at least a decade higher than f_0 to ensure that it does not interfere with the phase margin of the voltage regulation loop at its crossover frequency. It should also be sufficiently lower then the switching frequency of the converter so noise can be effectively attenuated. The recommended f_{HFP} frequency is around 120Hz in PFC applications.

Step 14: Over-Voltage Protection Setting (OVP)

$$R_{OV2} = \frac{3.5V \cdot V_{OUT,LATCH}}{P_{OVP}} \quad (23)$$

where 3.5V is the threshold voltage of the OVP comparator and P_{OVP} is the total dissipation of the resistive divider network. Typical P_{OVP} power loss is in the 50mW to 100mW range.

$$R_{OV1} = \left(\frac{V_{OUT,LATCH}}{3.5V} - 1 \right) \cdot R_{OV2} \quad (24)$$

R_{OV1} can be implemented as a series combination of two or three resistors; depending on safety regulations, maximum voltage, and or power rating of the selected resistor type.

Step 15: Input Line Voltage Sense Resistors

$$R_{IN2} = \frac{3.7V \cdot V_{LINE,MAX}}{\sqrt{2} \cdot P_{INSNS}} \quad (25)$$

where 3.7V is the threshold voltage of the line OVP comparator and P_{INSNS} is the total dissipation of the resistive divider network. Typical P_{INSNS} power loss is in the 50mW to 100mW range.

$$R_{IN1} = \left(\frac{\sqrt{2} \cdot V_{LINE,MAX}}{3.7V} - 1 \right) \cdot R_{IN2} \quad (26)$$

R_{IN1} can be implemented as a series combination of two or three resistors; depending on safety regulations, maximum voltage, and or power rating of the selected resistor type.

$$R_{INHYST} = \frac{\left(\frac{\sqrt{2} \cdot V_{LINE,ON} \cdot R_{IN2}}{R_{IN1} + R_{IN2}} - 0.925V \right)}{2\mu A} \quad (27)$$

where 0.925V is the threshold voltage of the line under-voltage lockout comparator and 2μA is the sink current provided at the VIN pin during line under-voltage (brownout) condition. The sink current, together with the terminating impedance of the VIN pin determines the hysteresis between the turn-on and turn-off thresholds.

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Step 16: Gate Resistors

It is recommended to place a low-value resistor between the gate drive outputs, the DRV1 and DRV2 pins and their corresponding power devices. The gate drive resistors have a beneficial effect to limit the current drawn from the V_{DD} bypass capacitor during the turn-on of the power MOSFETs and to attenuate any potential oscillation in the gate drive circuits.

$$R_{G1} = R_{G2} = \frac{VDD_{MAX}}{1.0\,A} \tag{28}$$

where 1.0A is the recommended peak value of the gate drive current.

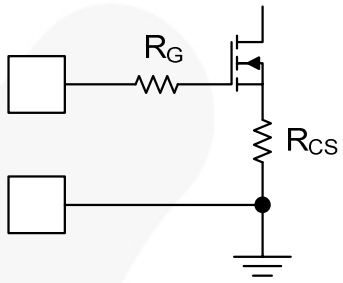


Figure 32. Recommended Gate Drive Schematic

Step 17: Current-Sense Resistors

$$R_{CS1} = R_{CS2} = \frac{0.18V}{I_{L,PK}} \tag{29}$$

where 0.18V is the worst-case threshold of the current limit comparator. The size and type of current sense resistors depends on their power dissipation and manufacturing considerations.

$$P_{RCS1} = 1.5 \cdot I_{L,PK}^2 \cdot R_{CS1} \cdot \left(\frac{1}{6} - \frac{4 \cdot \sqrt{2} \cdot V_{LINE,OFF}}{9 \cdot \pi \cdot V_{OUT}} \right) \tag{30}$$

where the 1.5 factor is used for the worst-case effect of the current limit threshold variation. When the current-sense resistor is determined, the minimum current-sense threshold must be used to avoid activating over current protection too early as the power supply approaches full-load condition. The worst-case power dissipation of the current sense resistor happens when the current sense threshold is at its maximum value defined in the datasheet. The ratio between the minimum and maximum thresholds squared (since the square of the current determines power dissipation) yields exactly the 1.5 factor used in the calculation.

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Typical Performance Characteristics — Supply

Typical characteristics are provided at T_A = 25°C and V_{DD} = 12V unless otherwise noted.

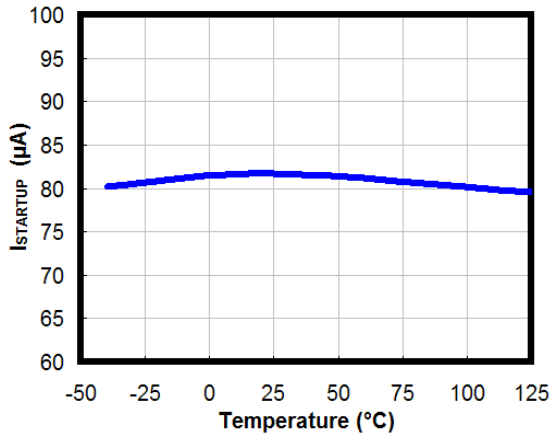


Figure 33. $I_{STARTUP}$ vs. Temperature

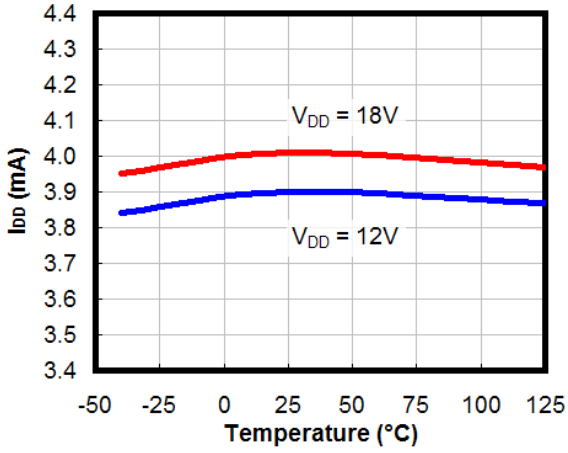


Figure 34. Operating Current vs. Temperature

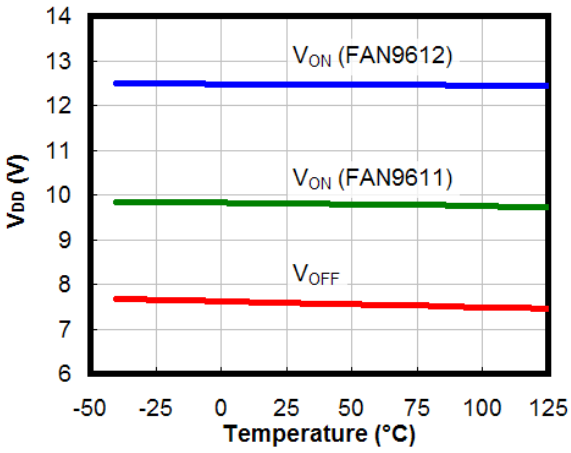


Figure 35. UVLO Thresholds vs. Temperature

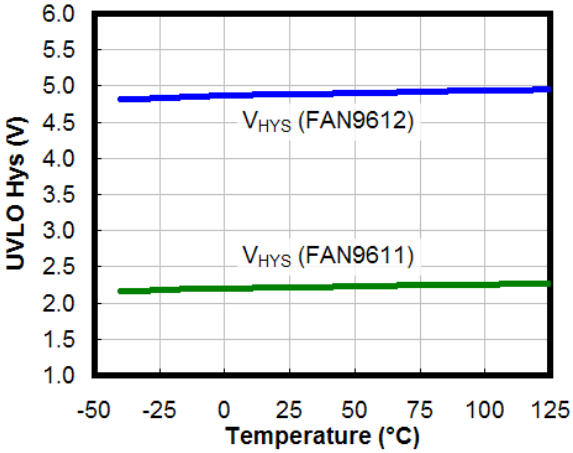


Figure 36. UVLO Hysteresis vs. Temperature

Typical Performance Characteristics — Control

Typical characteristics are provided at T_A = 25°C and V_{DD} = 12V unless otherwise noted.

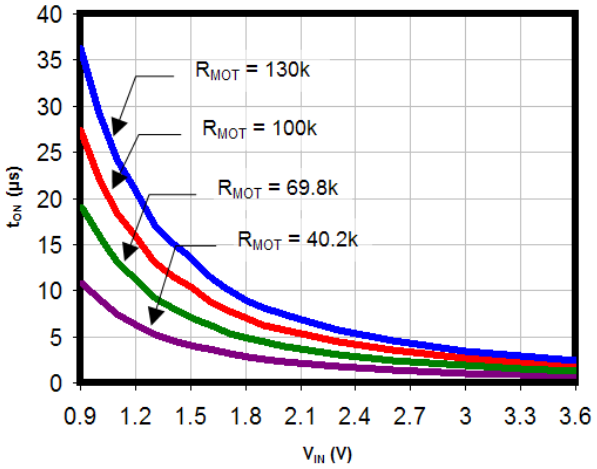


Figure 37. Transfer Function (Maximum On Time vs. V_{IN})

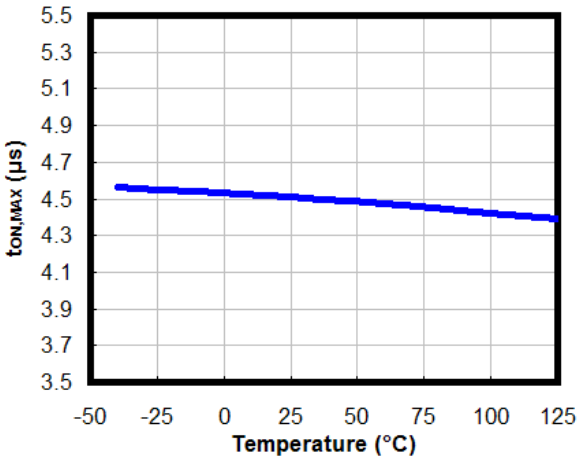


Figure 38. Maximum On Time vs. Temperature

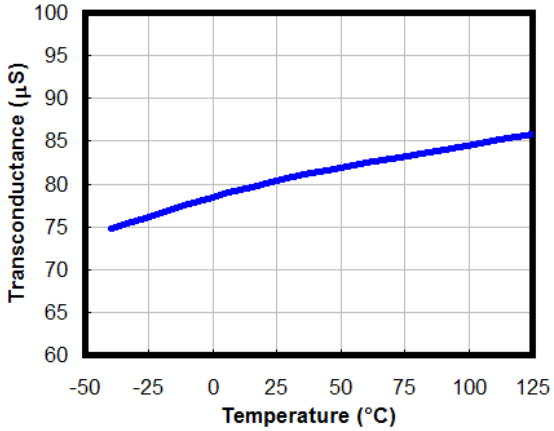


Figure 39. EA Transconductance (g_M) vs. Temperature

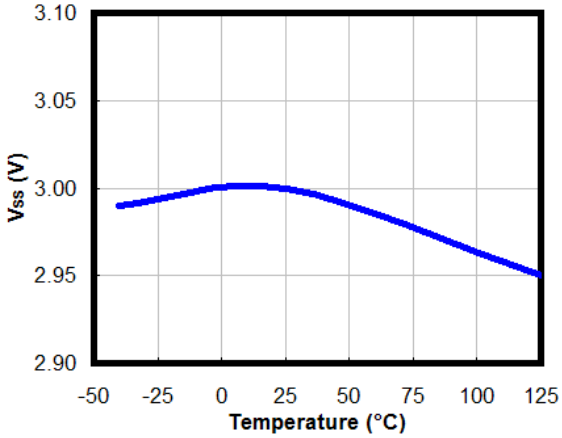


Figure 40. EA Reference vs. Temperature

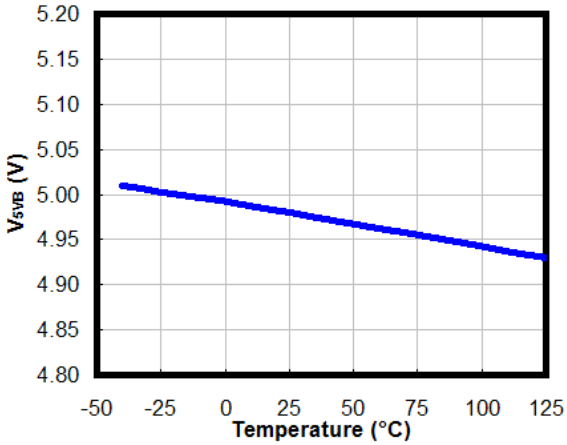


Figure 41. 5V Reference vs. Temperature

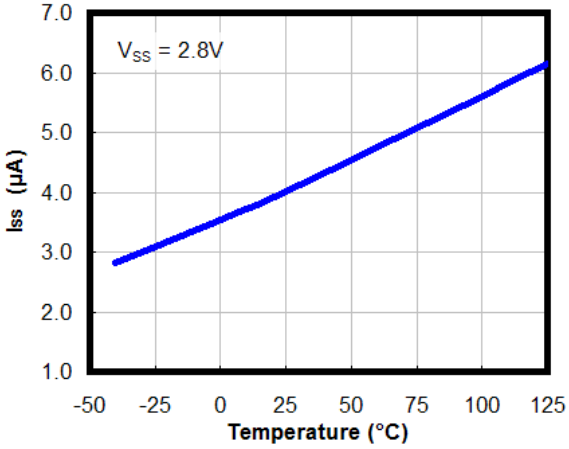


Figure 42. Soft-Start Current vs. Temperature

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Typical Performance Characteristics — Control

Typical characteristics are provided at T_A = 25°C and V_{DD} = 12V unless otherwise noted.

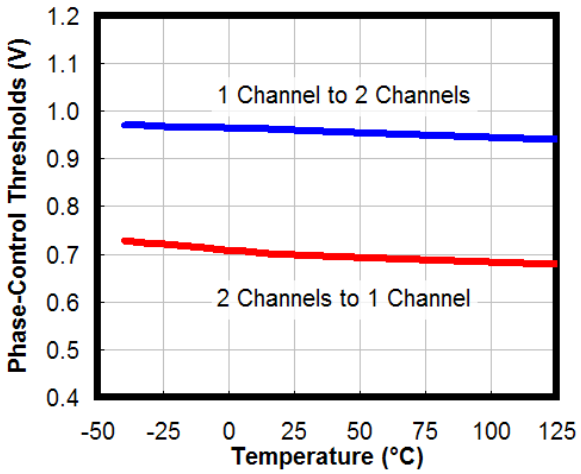


Figure 43. Phase-Control Thresholds vs. Temperature

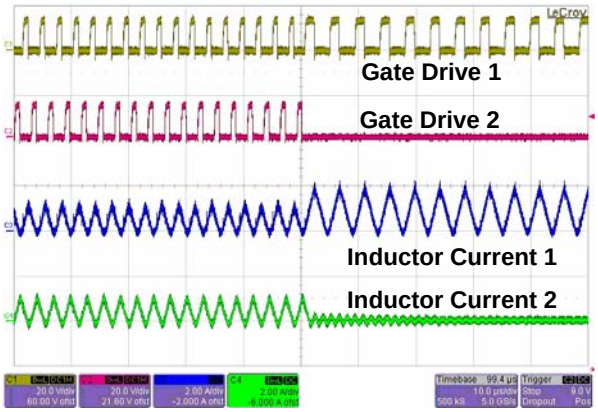


Figure 44. Phase-Dropping Operation

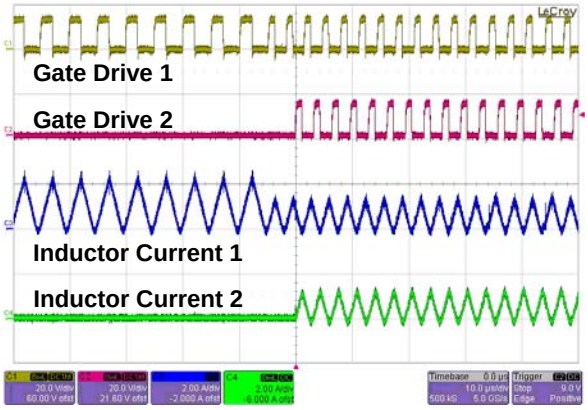


Figure 45. Phase-Adding Operation

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Typical Performance Characteristics — Protection

Typical characteristics are provided at T_A = 25°C and V_{DD} = 12V unless otherwise noted.

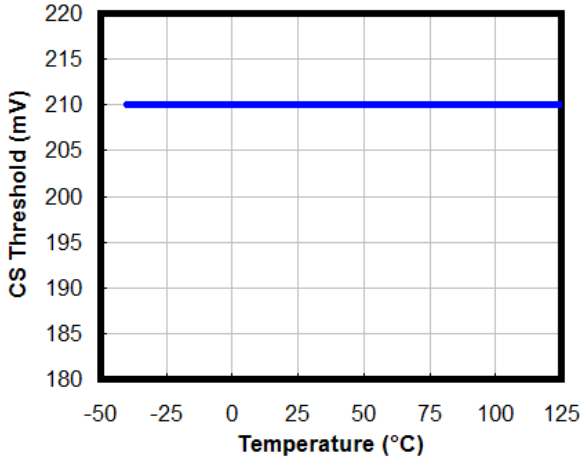


Figure 46. CS Threshold vs. Temperature

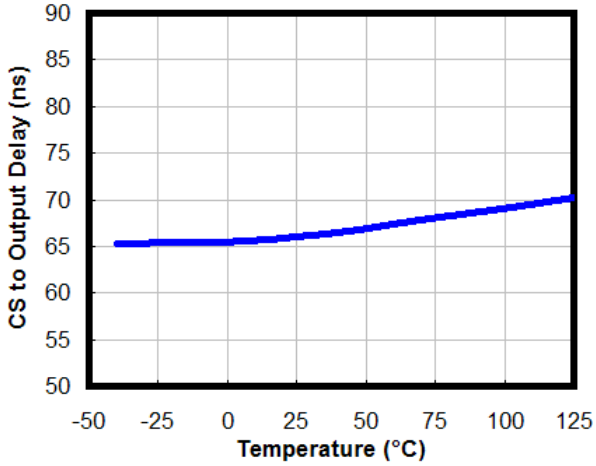


Figure 47. CS to OUT Delay vs. Temperature

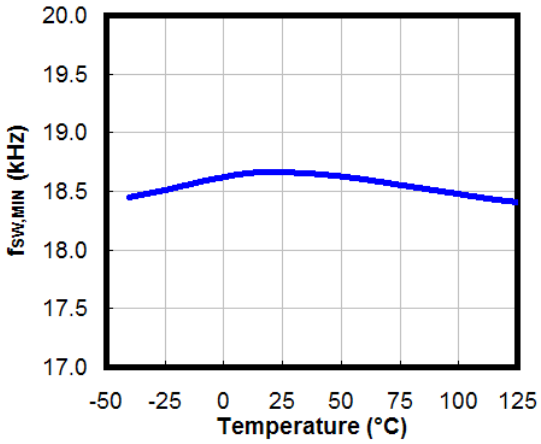


Figure 48. Restart Timer Frequency vs. Temperature

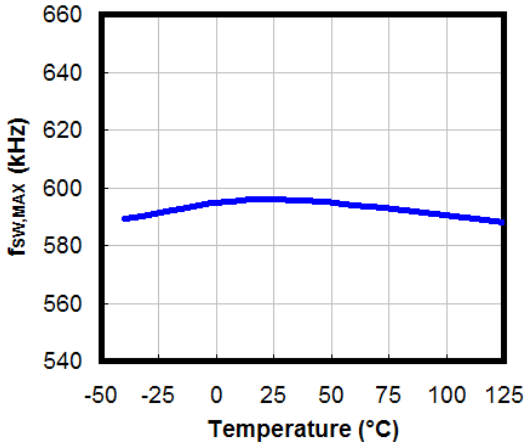


Figure 49. Maximum Frequency Clamp vs. Temperature

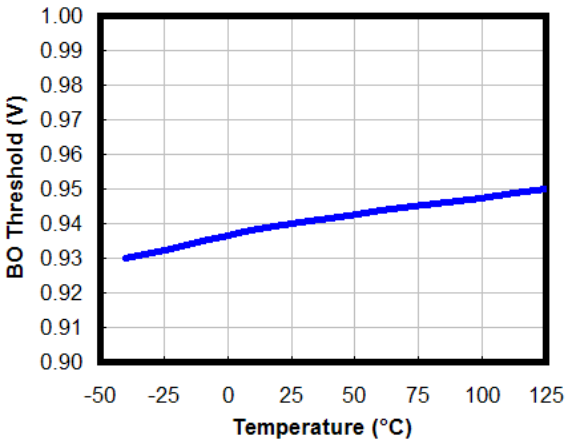


Figure 50. Brownout Threshold vs. Temperature

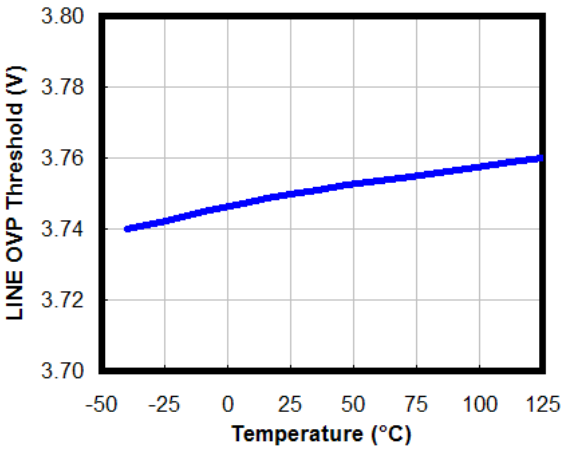


Figure 51. Line OVP vs. Temperature

Typical Performance Characteristics — Protection

Typical characteristics are provided at T_A = 25°C and V_{DD} = 12V unless otherwise noted.

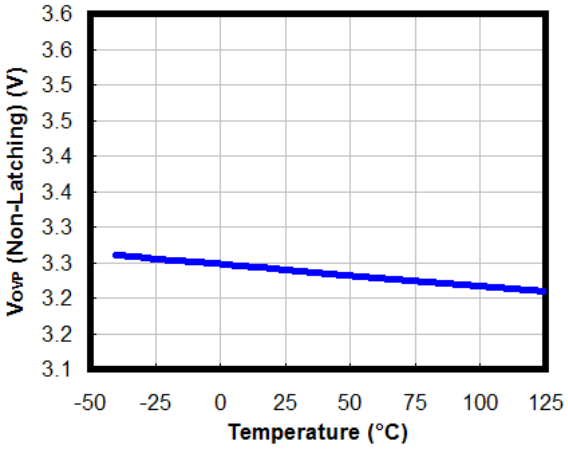


Figure 52. Non-Latching OVP vs. Temperature

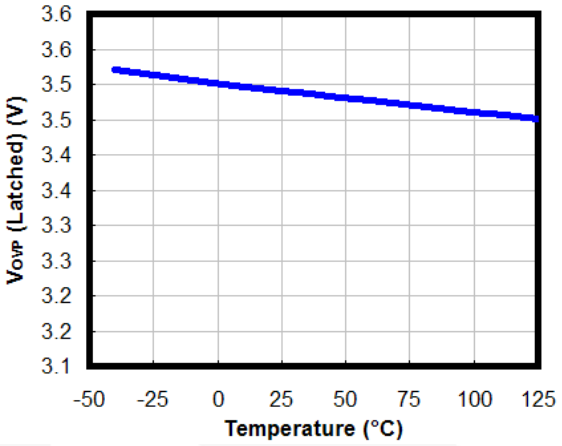


Figure 53. Latching OVP vs. Temperature

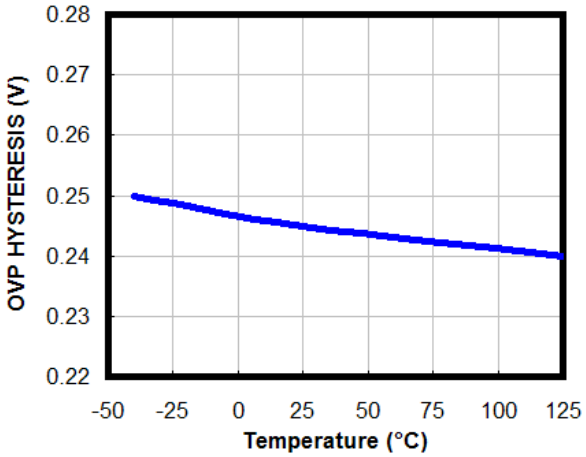


Figure 54. OVP Hysteresis vs. Temperature

Typical Performance Characteristics — Operation

Typical characteristics are provided at T_A = 25°C and V_{DD} = 12V unless otherwise noted.

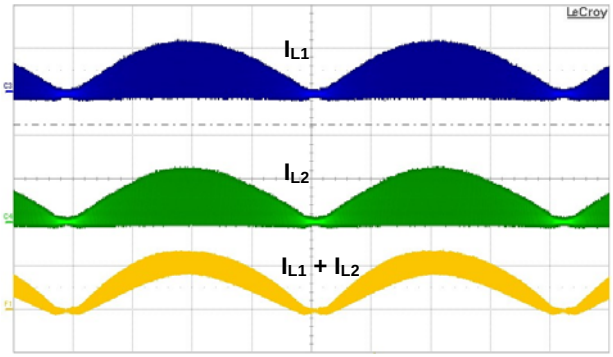


Figure 55. Ripple-Current Cancellation (110V_{AC})

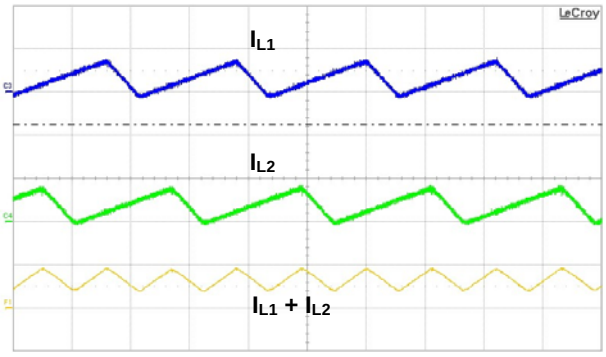


Figure 56. Ripple-Current Cancellation (110V_{AC})

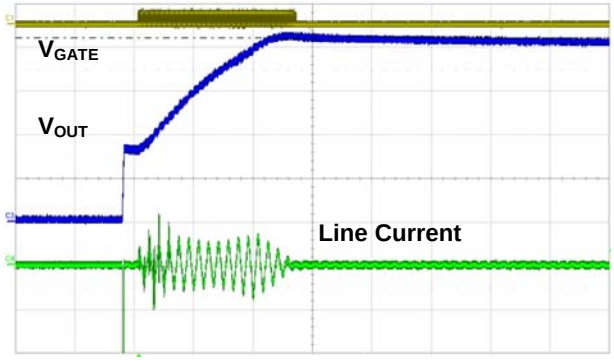


Figure 57. No-Load Startup at 115V_{AC}

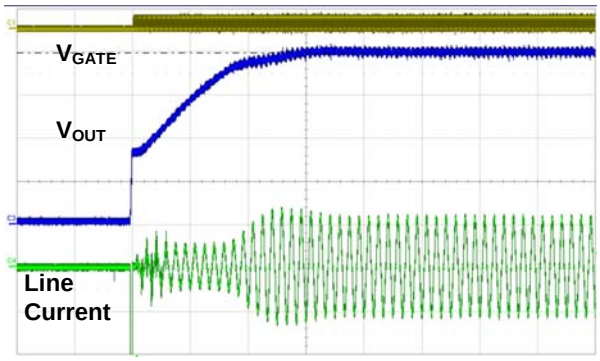


Figure 58. Full-Load Startup at 115V_{AC}

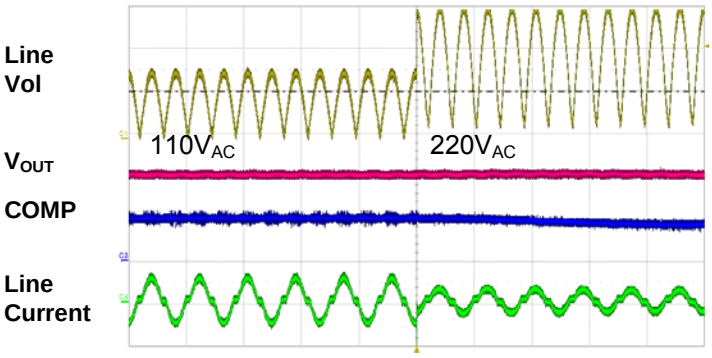


Figure 59. Input Voltage Feedforward

Note:

5. *For full performance operational characteristics at both low line (110V_{AC}) and high line (220V_{AC}), as well as at no-load and full-load, refer to FEB279 Evaluation Board User Guide: 400W Evaluation Board using FAN9612.*

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Evaluation Board

FEB279: 400W Evaluation Board Using FAN9611/12

FEB279 is an evaluation board for an interleaved dual boundary-conduction-mode PFC converter rated at 400W (400V/1A) power. With phase management, the efficiency is maintained above 96% even down at 10% of the rated output power. The efficiencies for full-load condition exceed 96% as shown below.

Figure 60 and Figure 61 show the phase management with the default minimum threshold values of the IC. They can be adjusted upwards to achieve a different efficiency profile (Figure 62 and Figure 63) where phase management thresholds are adjusted to 30% / 44% of the full load. *For the full specification, design schematic, bill of materials and test results, see the FEB279 — FAN9612 Evaluation Board User Guide.*

Input Voltage	Rated Output Power	Output Voltage (Rated Current)
V_{IN} Nominal: 85V~264V_{AC} V_{DD} Supply: 13V~18V_{DC}	400W	400V (1A)

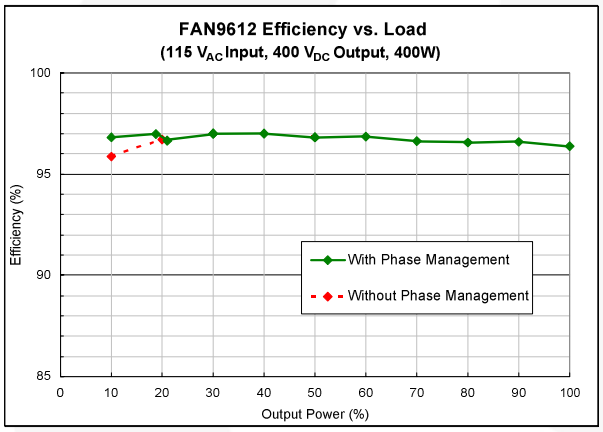


Figure 60. Measured Efficiency at 115V_{AC} (Default Thresholds)

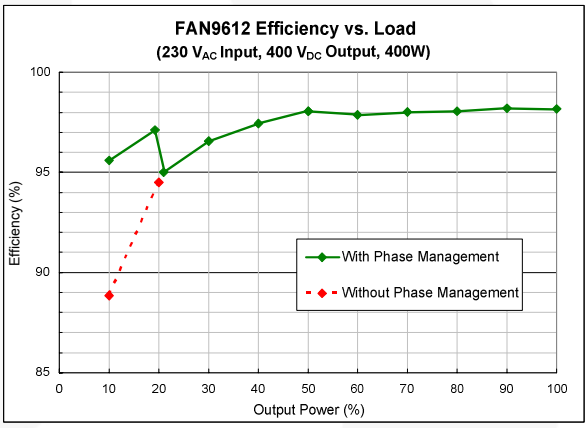


Figure 61. Measured Efficiency at 230V_{AC} (Default Thresholds)

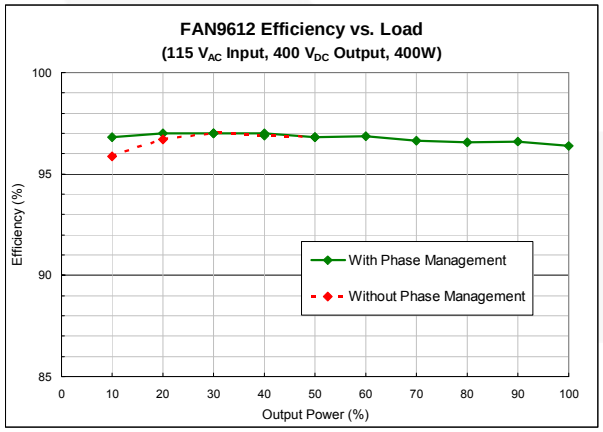


Figure 62. Measured Efficiency at 115V_{AC} (Adjusted Thresholds)

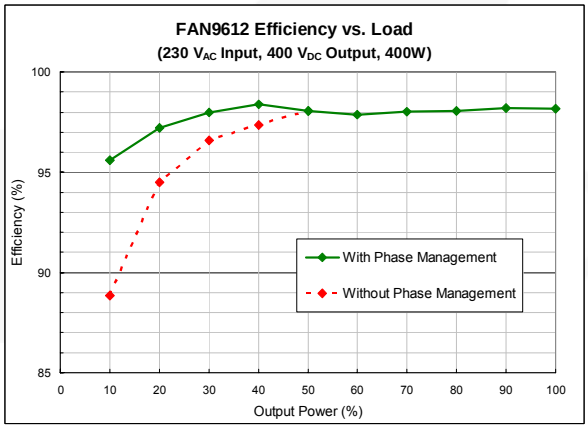


Figure 63. Measured Efficiency at 230V_{AC} (Adjusted Thresholds)

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Table 1. Related Products

Part Number	Description	PFC Control	Number of Pins	Comments
FAN7527B	Boundary Mode PFC Control IC	Single BCM (CRM)	8	Industry Standard Pin-Out
FAN7528	Dual Output Critical Conduction Mode PFC Controller	Single BCM (CRM)	8	Low THD for Boost-Follower Implementation
FAN7529	Critical Conduction Mode PFC Controller	Single BCM (CRM)	8	Low THD
FAN7530	Critical Conduction Mode PFC Controller	Single BCM (CRM)	8	Low THD, Alternate Pin-out of FAN7529 (Pins 2 and 3 Reversed)
FAN6961	Green Mode PFC	Single BCM (CRM)	8	Industry Standard Pin-out with Green Mode Functions
FAN9611	**Interleaved Dual BCM PFC Controller**	**Dual BCM (CRM)**	**16**	**Dual BCM (CRM), 180° Out-of-Phase, 10.0V UVLO**
FAN9612	**Interleaved Dual BCM PFC Controller**	**Dual BCM (CRM)**	**16**	**Dual BCM (CRM), 180° Out-of-Phase, 12.5V UVLO**

Related Resources

- *AN-6086: Design Consideration for Interleaved Boundary Conduction Mode (BCM) PFC Using FAN9612*
- *AN-8018: Fairchild Evaluation Board User Guide FEB279: 400W Evaluation Board using FAN9612*
- *AN-8021: Building Variable Output Voltage Boost PFC Converters Using FAN9612*

References

1. *L. Huber, B. Irving, C. Adragna and M. Jovanovich, "Implementation of Open-Loop Control for Interleaved DCM/BCM Boundary Boost PFC Converters", Proceedings of APEC '08, pp. 1010-1016.*
2. *C. Bridge and L. Balogh, "Understanding Interleaved Boundary Conduction Mode PFC Converters", Fairchild Power Seminars, 2008-2009.*

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Physical Dimensions

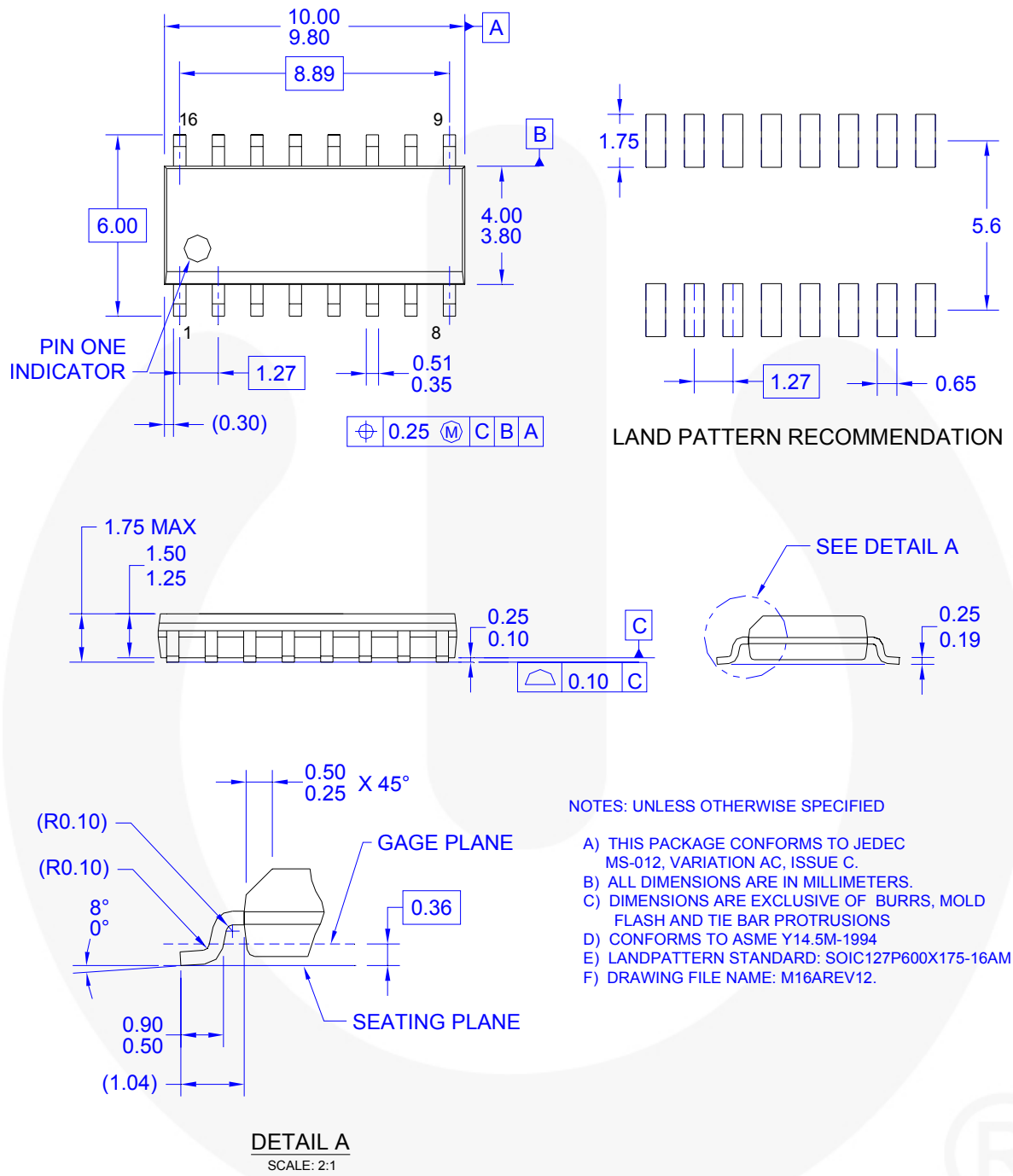


Figure 64. 16-Lead SOIC Package

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I43

Table 2. Revision History

Revision	Date	Description
1.0.0	July 2009	Initial Release of FAN9612
1.0.1	Aug 2009	Preliminary release of FAN9611 product added to the FAN9612 Released datasheet.

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