April 25, 2012

DS90C187

Low Power 1.8V Dual Pixel FPD-Link (LVDS) Serializer

General Description

The DS90C187 is a Low Power Serializer for portable battery powered application that reduces the size of the RGB interface between the host GPU and the Display.

The DS90C187 Serializer is designed to support dual pixel data transmission between Host and Flat Panel Display up to QXGA 2048x1536@60Hz resolutions. The transmitter converts up to 48 bits (Dual Pixel 24 bit color) of 1.8V LVCMOS data into two channels of 4 data + clock (4D+C) reduced width interface LVDS compatible data streams.

DS90C187 supports 3 modes of operation. In single pixel mode in/out mode, the device can drive up to SXGA+ 1400x1050@60Hz. In this mode, the device converts one bank of 24 bit RGB data to one channel of 4D+C LVDS data stream. In single pixel in / dual pixel out mode, the device can drive up to WUXGA+ 1920x1440@60Hz. In this configuration, the device provides single-to-dual pixel conversion and converts one bank of 24 bit RGB data into two channels of 4D +C LVDS streams at half the pixel clock rate. In dual pixel in / dual pixel out mode, the device can drive up to QXGA 2048x1536@60Hz or up to QSXGA 2560x2048@30Hz. In this mode, the device converts 2 channels of 24 bit RGB data into 2 channels of 4D+C LVDS streams. For all the modes, the device supports 18bpp and 24bpp color.

The DS90C187 is offered in a small 92 pin dual row QFN package and features single 1.8V supply for minimal power dissipation.

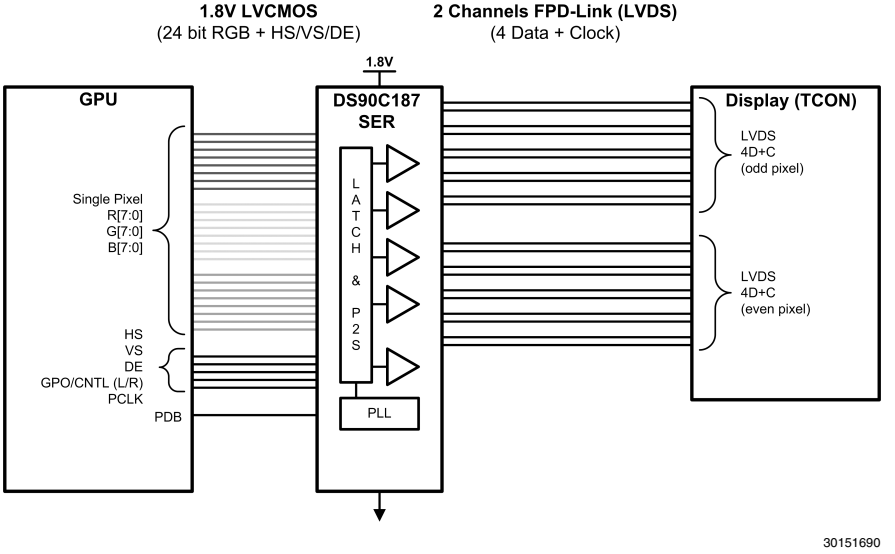
Features

- 100 mW typical power consumption at 185 MHz (SIDO mode)
- Drives QXGA/WQXGA class displays
- Three operating modes:
  - Single Pixel In / Single Pixel Out (SISO), 105 MHz max
  - Single Pixel In / Dual Pixel Out (SIDO), 185 MHz
  - Dual Pixel In / Dual Pixel Out (DIDO), 105 MHz
- Supports 24 bit RGB, 48 bit RGB
- Optional low power mode supports 18 bit RGB, 36 bit RGB
- Supports 3D+C, 4D+C, 6D+C, 6D+2C, 8D+C, and 8D+2C LVDS configurations
- Compatible with FPD-Link, and FlatLink Deserializers
- 1.8V VDDIO & Core Supply
- Interfaces directly with 1.8V LVCMOS
- Less than 1mW power consumption in Sleep Mode
- Spread Spectrum Clock Compatible
- Small 7mm x 7mm x 0.9 mm 92–pin dual row QFN package

Applications

- Media Tablet Devices
- eBook / Notebooks / Laptops
- Portable Display Monitors

Typical Application Diagram

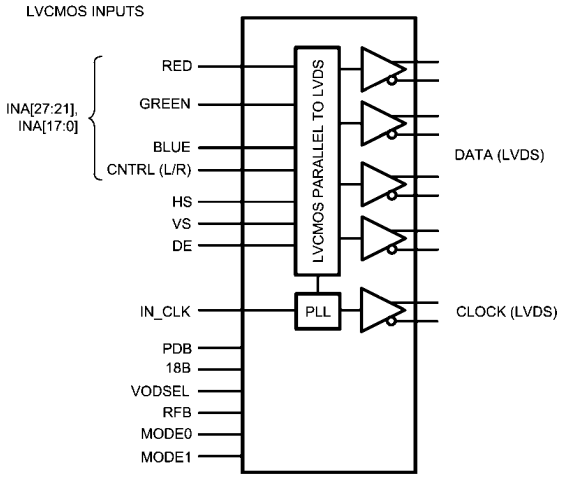


Single Pixel In Dual Pixel Out (SIDO) Mode

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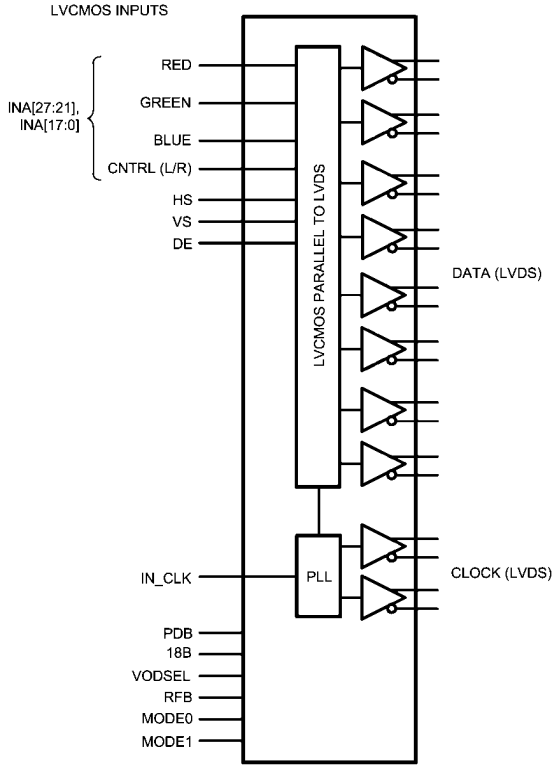
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Functional Block Diagrams



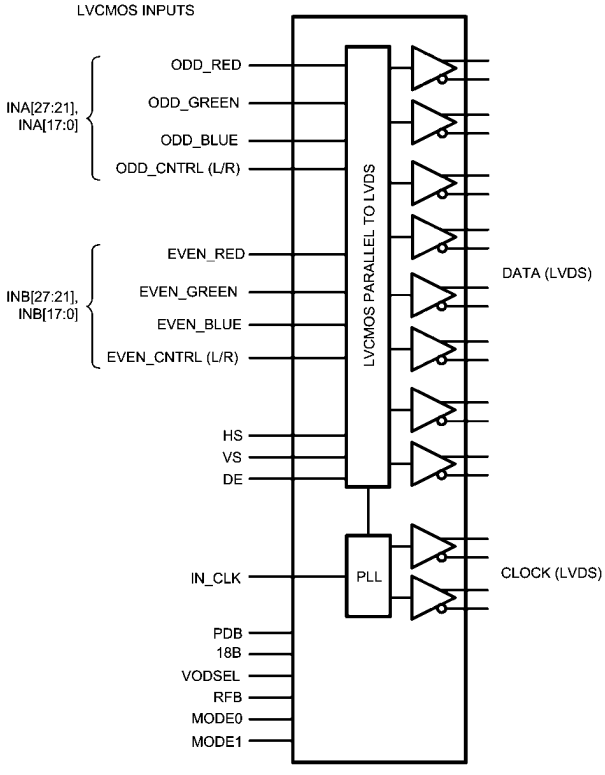
DS90C187 – SERIALIZER
Single Pixel In / Single Pixel Out
(SISO)

30151694



DS90C187 – SERIALIZER
Single Pixel In / Dual Pixel Out (SIDO)

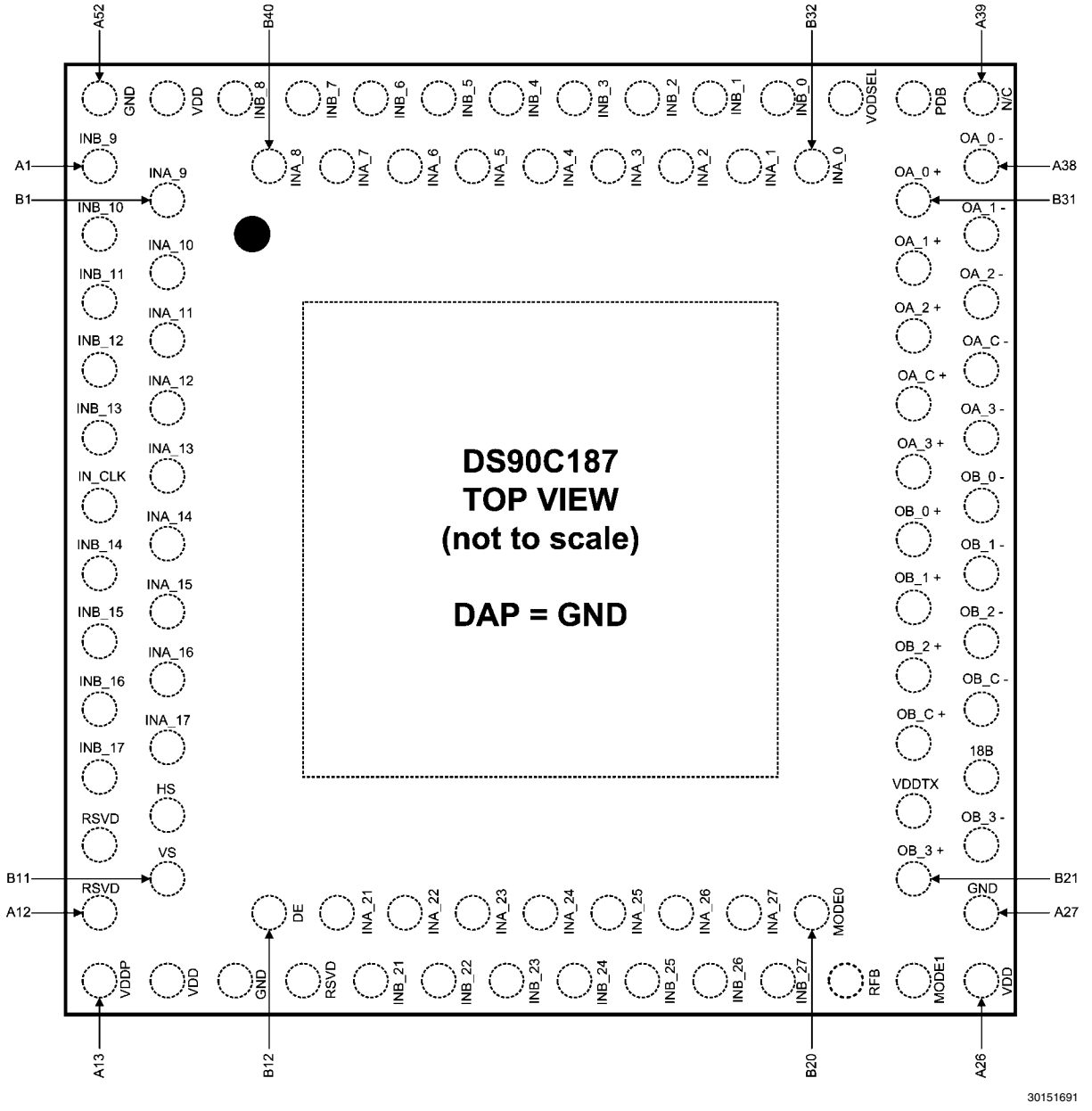
30151695



DS90C187 – SERIALIZER
Dual Pixel In / Dual Pixel Out (SIDO)

30151696

Connection Diagram



Ordering Information

Order Number	Package Description	Package ID	Supplied As
DS90C187LFE/NOPB	92–pin dual row QFN, 7.0 X 7.0 X 0.9 mm, 0.5 mm pitch	LFA92A	250 units on Tape and Reel
DS90C187LF/NOPB	92–pin dual row QFN, 7.0 X 7.0 X 0.9 mm, 0.5 mm pitch	LFA92A	1000 units on Tape and Reel
DS90C187LFX/NOPB	92–pin dual row QFN, 7.0 X 7.0 X 0.9 mm, 0.5 mm pitch	LFA92A	2500 units on Tape and Reel

DS90C187 Pin Descriptions — Serializer

Pin Name	I/O	No.	Description
1.8V LVCMOS VIDEO INPUTS			
INA_[27:21], INA_[17:9], INA_[8:0]	I	B19–B13, B9–B1, B40–B32	Channel A Data Inputs Typically consists of 8 Red, 8 Green, 8 Blue and a general purpose or L/R control bit. Includes pull down.
INB_[27:21], INB_[17:14], INB_[13:9], INB_[8:0]	I	A23–A17, A10–A7, A5–A1, A50–A42	Channel B Data Inputs Typically consists of 8 Red, 8 Green, 8 Blue and a general purpose or L/R control bit. Includes pull down.
HS (INA_18), VS (INA_19), DE (INA_20)	I	B10, B11, B12	Video Control Signal Inputs – HS = Horizontal Sync, VS = Vertical SYNC, and DE = Data Enable
IN_CLK	I	A6	Pixel Input Clock Includes pull down.
1.8V LVCMOS CONTROL INPUTS			
MODE0, MODE1	I	B20, A25	Mode Control Inputs (MODE1, MODE0) 00 = Single In / Single Out 01 = Single In / Dual Out 10 = Dual In / Dual Out 11 = **Reserved** Includes pull down.
RFB	I	A24	Rising / Falling Clock Edge Select Input – 0 = Falling Edge, 1 = Rising Edge Includes pull down.
PDB	I	A40	Power Down (Sleep) Control Input – 0 = Sleep (Power Down mode), 1 = device active (enabled) Includes pull down.
18B	I	A29	18 bit / 24 bit Control Input – 0 = 24 bit mode, 1 = 18 bit mode Includes pull down.
VODSEL	I	A41	VOD Level Select Input – 0 = Low swing, 1 = Normal swing Includes pull down.
N/C	I	A39	**no connect pin — leave open**
RSVD	I	A11, A12, A16	**Reserved – Tie to Ground.**
LVDS OUTPUTS			
OA_C+, OA_C-	O	B28, A35	Channel A LVDS Output Clock — Expects 100 Ω DC load.
OA_[3:0]+, OA_[3:0]-	O	B27, B29–B31 A34, A36–A38	Channel A LVDS Output Data — Expects 100 Ω DC load.
OB_C+, OB_C-	O	B23, A30	Channel B LVDS Output Clock — Expects 100 Ω DC load.
OB_[3:0]+, OB_[3:0]-	O	B21, B24–B26, A28, A31–A33	Channel B LVDS Output Data — Expects 100 Ω DC load.
POWER and GROUND			
V_{DDTX}	P	B22	Power supply for LVDS Drivers, 1.8V.
V_{DD}	P	A14, A26, A51	Power supply pin for core, 1.8V.
V_{DDP}	P	A13	Power supply pin for PLL, 1.8V.
GND	G	A15, A27, A52	Ground pins.
DAP	G	DAP	**Connect DAP to Ground plane.**

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +2.5V
LVCMOS Input Voltage	−0.3V to VDD + 0.3V
LVDS Driver Output Voltage	−0.3V to +3.6V
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Package Derating: θ_{JA}	35.1°C/W above +22°C

ESD Ratings:

HBM	> ±8 kV
CDM	> ±1.25 kV
MM	>±250 V

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage	1.71	1.80	1.89	V
Operating Free Air Temperature ($T_{A)}$)	−10	+25	+70	°C
Differential Load Impedance	80	100	120	Ω
Supply Noise Voltage			<90	mV_{p-p}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			$0.65V_{DD}$		V_{DD}	V
V_{IL}	Low Level Input Voltage			GND		$0.35V_{DD}$	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DD} = 1.71 V to 1.89 V		− 10	±1	+10	µA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω *Figure 3*	VODSEL = V_{IH}	160 (320)	300 (600)	450 (900)	mV (mV_{P-P})
			VODSEL = V_{IL}	110 (220)	180 (360)	300 (600)	mV (mV_{P-P})
ΔV_{OD}	Change in V_{OD} between Complimentary Output States					50	mV
V_{OS}	Offset Voltage			0.8	0.9	1.0	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States					50	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = GND, VODSEL = V_{DD}		−45	−35	−25	mA
SUPPLY CURRENT							
IDDT1	Serializer Worst Case Supply Current (includes load current)	Checkerboard pattern, R_L = 100 Ω, 18B = V_{IL}, VODSEL = V_{IH}, V_{DD} = 1.89 V, *Figure 1*	f = 105 MHz, MODE[1:0] = 00 (SISO)		60	85	mA
IDDT2			f = 185 MHz, MODE[1:0] = 01 (SIDO)		95	140	mA
IDDT3			f = 105 MHz, MODE[1:0] = 10 (DIDO)		100	150	mA

Symbol	Parameter	Conditions		Min	Typ	Max	Units
IDDTP	Serializer Supply Current PRBS-7	MODE[1:0] = 01 (SIDO) f = 150 MHz, R_L = 100 Ω, PRBS-7 Pattern *Figure 12*	18B = V_{IL}, VODSEL = V_{IL}, VDD = 1.8		55		mA
			18B = V_{IL}, VODSEL = V_{IH}, VDD = 1.8		75		mA
			18B = V_{IH}, VODSEL = V_{IL}, VDD = 1.8		49		mA
			18B = V_{IH}, VODSEL = V_{IH}, VDD = 1.8		65		mA
IDDTG	Serializer Supply Current 16 Grayscale	MODE[1:0] = 01 (SIDO) f = 150 MHz, R_L = 100 Ω, 16 Grayscale Pattern	18B = V_{IL}, VODSEL = V_{IL}, VDD = 1.8		53		mA
			18B = V_{IL}, VODSEL = V_{IH}, VDD = 1.8		71		mA
			18B = V_{IH}, VODSEL = V_{IL}, VDD = 1.8		48		mA
			18B = V_{IH}, VODSEL = V_{IH}, VDD = 1.8		63		mA
IDDZ	Power Down Supply Current	PDB = GND			18	200	µA

Recommended Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
TCIT	IN_CLK Transition Time *Figure 5*	MODE[1:0] = 00 or 10	1.0	T	4.0	ns
		MODE[1:0] = 01	1.0		2.0	ns
TCIP	IN_CLK Period *Figure 6*	MODE[1:0] = 00 or 10	9.53	T	40	ns
		MODE[1:0] = 01	5.40	T	20	ns
TCIH	IN_CLK High Time	*Figure 6*	0.35T	0.5T	0.65T	ns
TCIL	IN_CLK Low Time		0.35T	0.5T	0.65T	ns
TXIT	INA_x & INB_x Transition Time	*Figure 5*	1.5		0.3T	ns

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
TSTC	INn_x Setup to IN_CLK	*Figure 6*	0			ns
THTC	INn_x Hold from IN_CLK		2.5			ns
LLHT	LVDS Low-to-High Transition Time *Figure 4*(*Note 4*)			0.18	0.5	ns
LHLT	LVDS High-to-Low Transition Time (*Note 4*)			0.18	0.5	ns
TBIT	LVDS Output Bit Width	MODE[1:0] = 00, or 10		1/7 TCIP		ns
		MODE[1:0] = 01		2/7 TCIP		ns

Symbol	Parameter		Min	Typ	Max	Units
TPPOS0	Transmitter Output Pulse Positions Normalized for Bit 0	*Figure 9*		1		UI
TPPOS1	Transmitter Output Pulse Positions Normalized for Bit 1			2		UI
TPPOS2	Transmitter Output Pulse Positions Normalized for Bit 2			3		UI
TPPOS3	Transmitter Output Pulse Positions Normalized for Bit 3			4		UI
TPPOS4	Transmitter Output Pulse Positions Normalized for Bit 4			5		UI
TPPOS5	Transmitter Output Pulse Positions Normalized for Bit 5			6		UI
TPPOS6	Transmitter Output Pulse Positions Normalized for Bit 6			7		UI
ΔTPPOS	Variation in Transmitter Pulse Position (Bit 6 — Bit 0)			±0.06		UI
TCCS	LVDS Channel to Channel Skew			110		ps
TJCC	Jitter Cycle-to-Cycle	MODE0, MODE1 = 0, f = 105 MHz, (*Note 4*)		0.028	0.035	UI
TPLLS	Phase Lock Loop Set (Enable Time)	*Figure 7*			1	ms
TPDD	Powerdown Delay	*Figure 8* (*Note 5*)			100	ns
TSD	Latency Delay	MODE0 = 0, MODE1 = 1 or 0 *Figure 10* (*Note 4*)		2*TCIP + 10.54	2*TCIP + 13.96	ns
TLAT	Latency Delay for Single Pixel In / Dual Pixel Out Mode	MODE0 = 1, MODE1 = 0 *Figure 10* (*Note 4*)		9*TCIP + 4.19	9*TCIP + 6.36	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{DD}, V_{DDTX} and V_{DDP} = 1.8V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: Parameter is guaranteed by characterization and is not tested at final test.

Note 5: Parameter is guaranteed by design and is not tested at final test.

AC Timing Diagrams

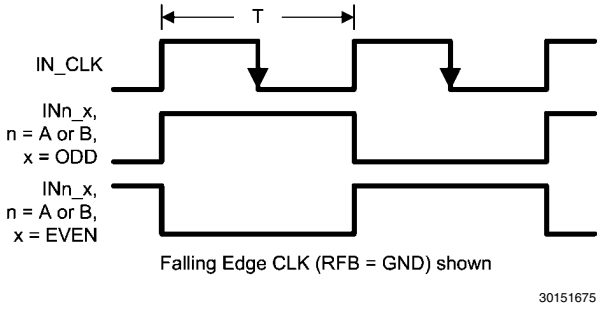


FIGURE 1. Checker Board Test Pattern (*Note 6*, *Note 8*)

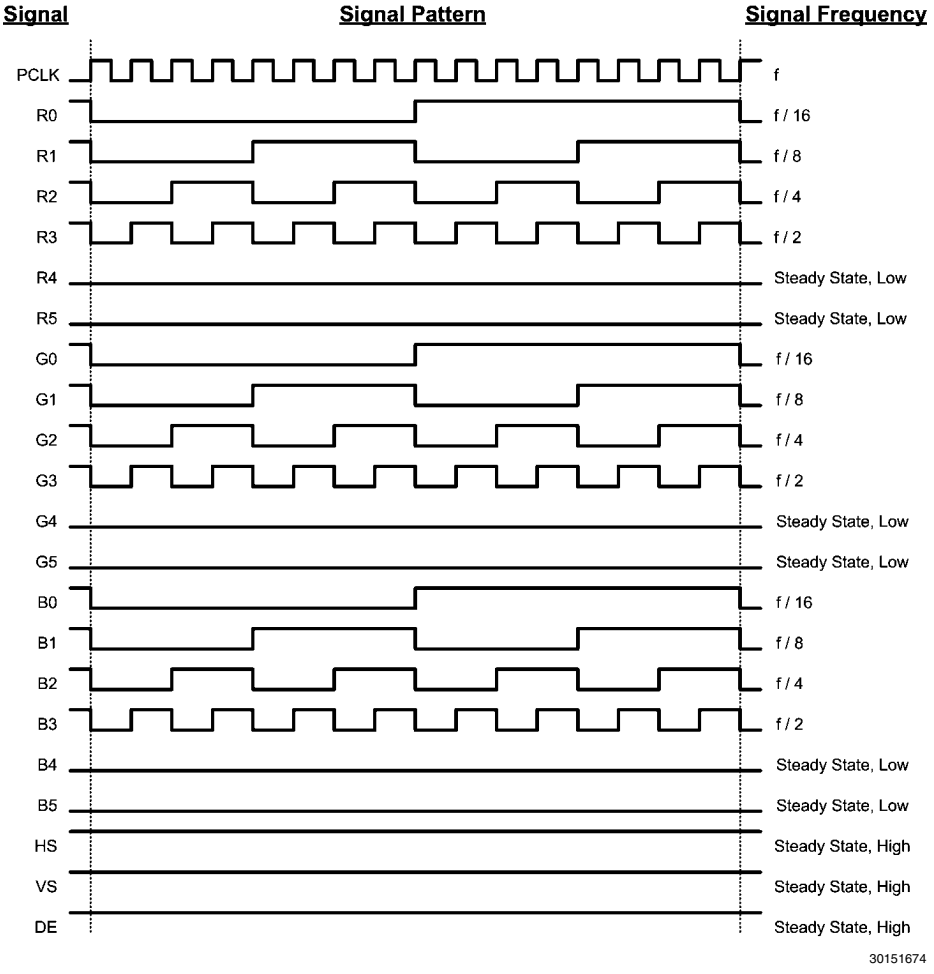


FIGURE 2. "16 Gray Scale" Test Pattern (Falling Edge Clock shown) (*Note 7*, *Note 8*)

Note 6: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVCMOS/ I/O.

Note 7: Recommended pin to signal mapping for 18 bits per pixel, customer may choose to define differently. The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 8: Figures 1, 2 show a falling edge data strobe (IN_CLK).

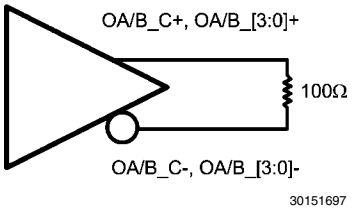


FIGURE 3. DS90C187 (Transmitter) LVDS Output Load

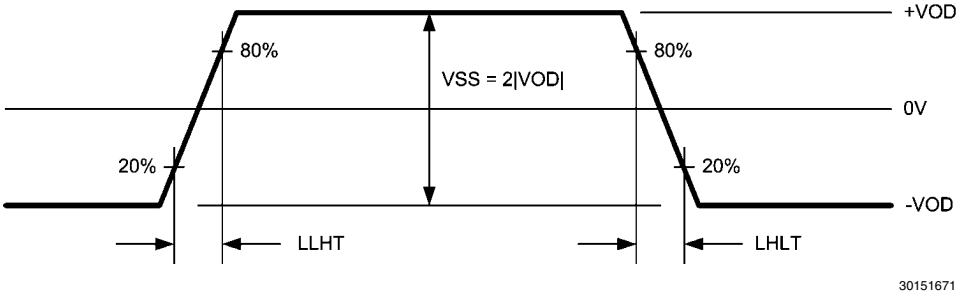


FIGURE 4. LVDS Output Transition Times

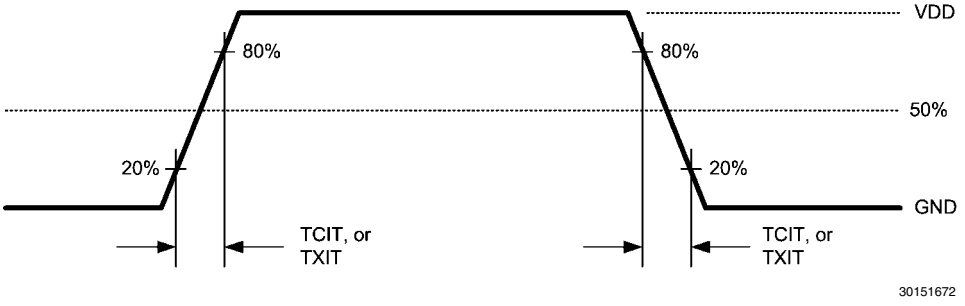


FIGURE 5. LVCMOS Input Transition Times

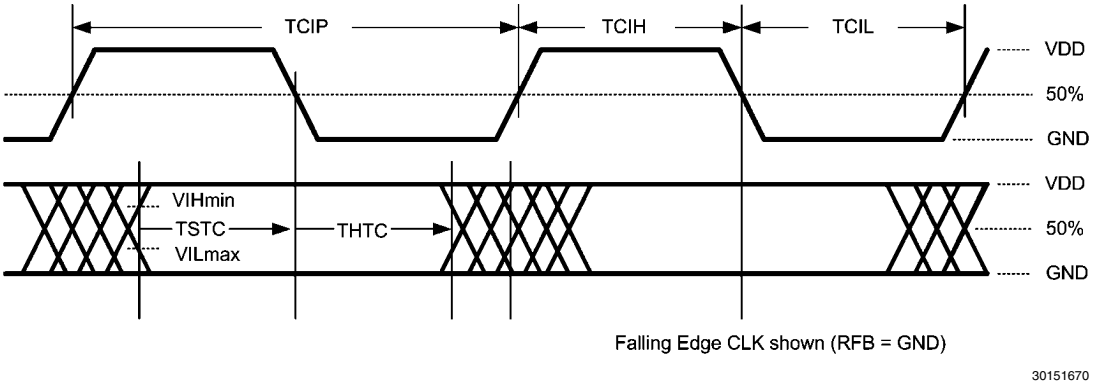


FIGURE 6. LVCMOS Input Setup/Hold and Clock High/Low Times (Falling Edge Strobe)

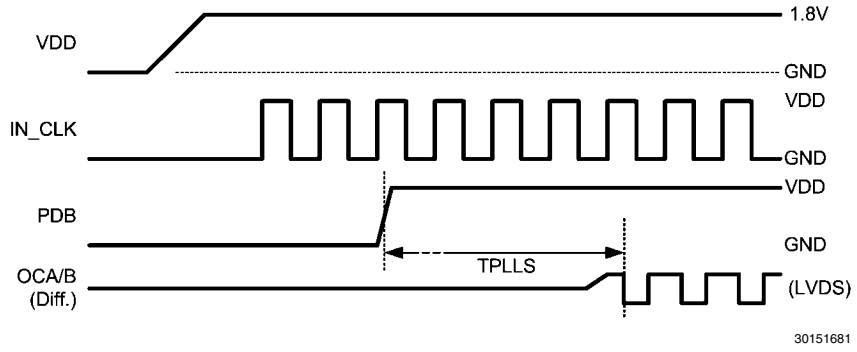


FIGURE 7. Start Up / Phase Lock Loop Set Time

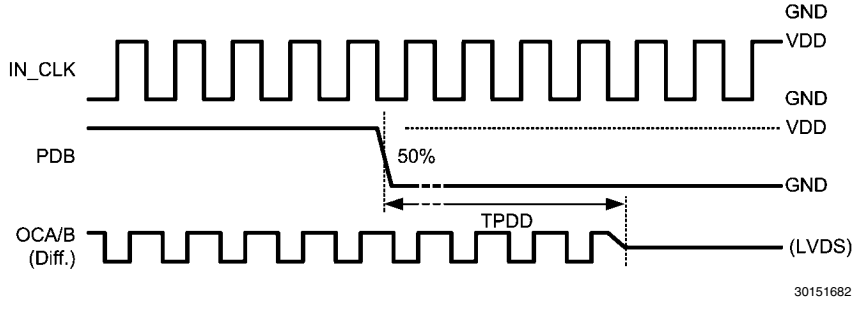


FIGURE 8. Sleep Mode / Power Down Delay

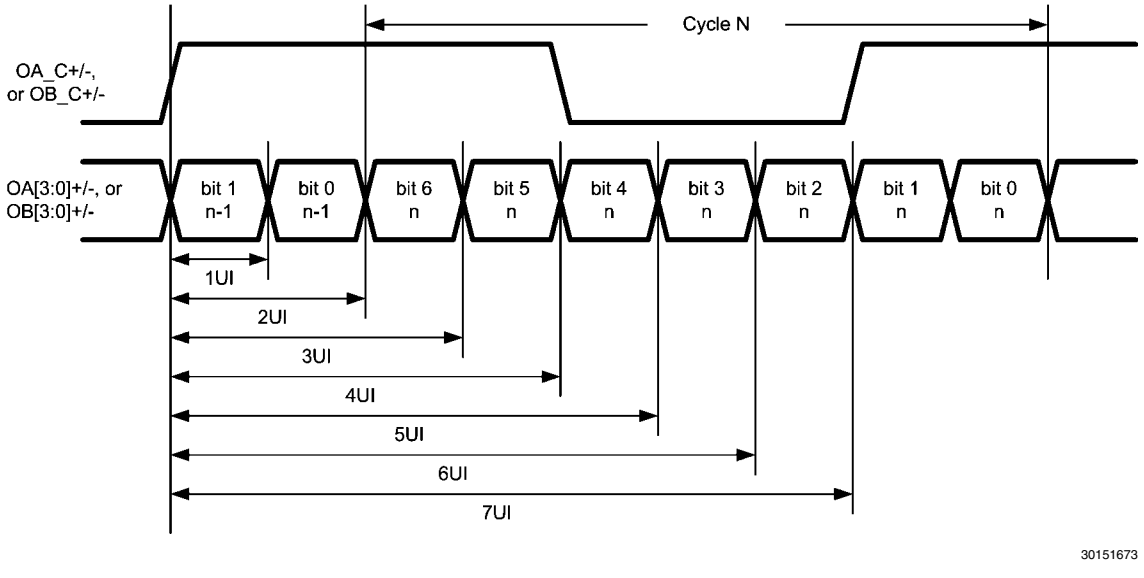


FIGURE 9. LVDS Serial Bit Positions

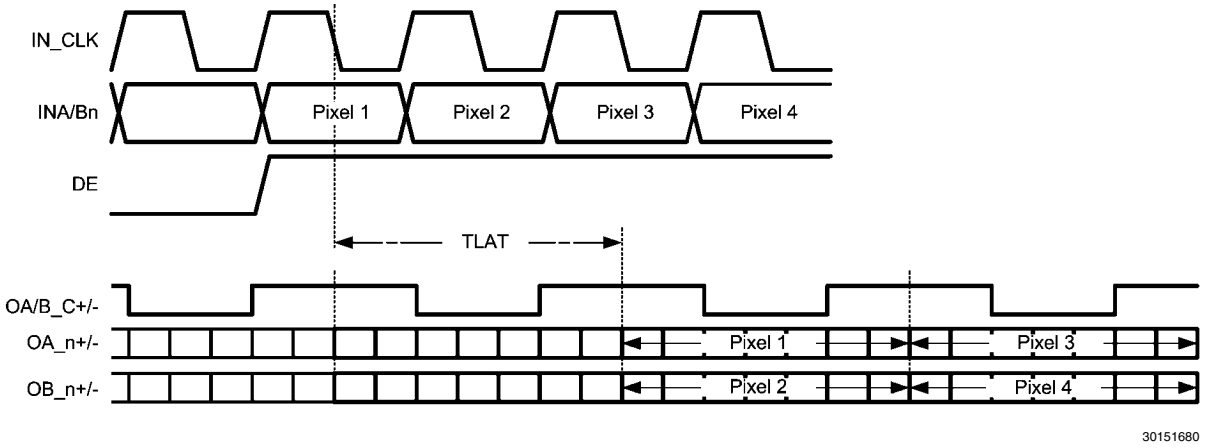


FIGURE 10. Single In Dual Out Mode Timing and Latency

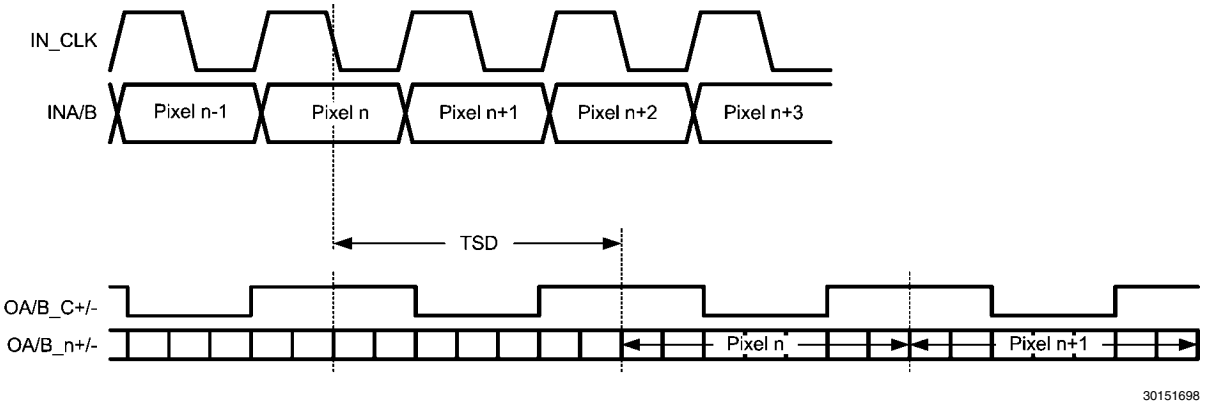


FIGURE 11. Single In Single Out / Dual In Dual Out Latency

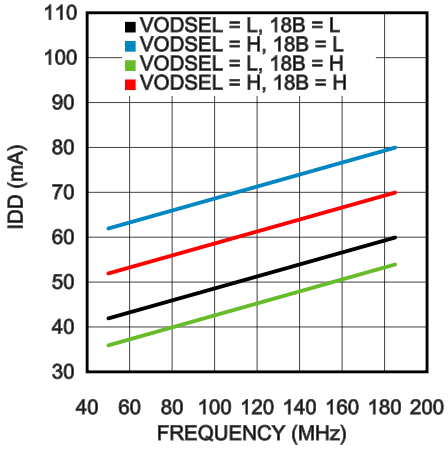


FIGURE 12. Typ Current Draw — Single In/Dual Out Mode — PRBS-7 Data Pattern

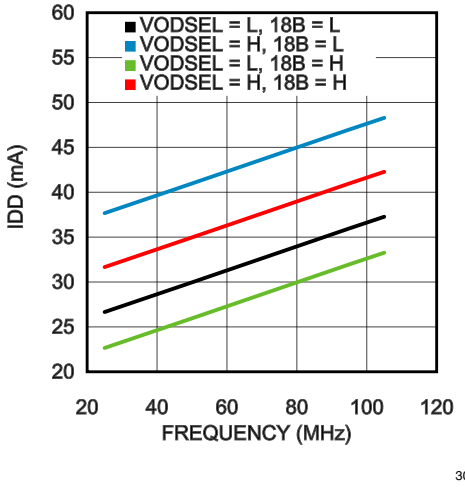


FIGURE 13. Typ Current Draw — Single In/Single Out Mode — PRBS-7 Data Pattern

LVDS Interface / TFT Color Data Recommended Mapping

Different color mapping options exist. Check with the color mapping of the Deserializer / TCON device that is used to ensure compatible mapping for the application. The DS90C187 supports three modes of operation for single and dual pixel applications supporting either 24bpp or 18bpp color depths.

In the Dual Pixel / 24bpp mode, eight LVDS data lines are provided along with two LVDS clock lines (8D+2C). The Deserializer may utilize one or two clock lines. The 53 bit interface typically assigns 24 bits to RGB for the odd pixel, 24 bits to RGB for the even pixel, 3 bits for the video control signals (HS, VS and DE), 1 bit for odd pixel and 1 bit for even pixel which can be ignored or used for general purpose data, control or L/R signaling.

A reduced width input interface is also supported with a Single-to-Dual Pixel conversion where the data is presented at double rate (same clock edge, 2X speed, see *Figure 10*) and the DE transition is used is flag the first pixel. Also note in both 8D+2C configurations, the three video control signals are sent over **both** the A and B outputs. The DES / TCON may recover one set, or both depending upon its implementation. The Dual Pixel / 24bpp 8D+2C LVDS Interface Mapping is shown in *Figure 14*.

A Dual Pixel / 18bpp mode is also supported. In this configuration OA3 and OB3 LVDS output channels are placed in TRI-STATE® to save power. Their respective inputs are ignored. (*Figure 15*)

In the Single Pixel / 24bpp mode, four LVDS data lines are provided along with a LVDS clock line (4D+C). The 28 bit interface typically assigns 24 bits to RGB color data, 3 bits to video control (HS, VS and DE) and one spare bit can be ignored, used for L/R signaling or function as a general purpose bit. The Single Pixel / 24bpp 4D+C LVDS Interface Mapping is shown in *Figure 16*.

A Single Pixel / 18bpp mode is also supported. In this configuration the OA3 LVDS output channel is placed in TRI-STATE® to save power. Its respective inputs are ignored. (*Figure 17*)

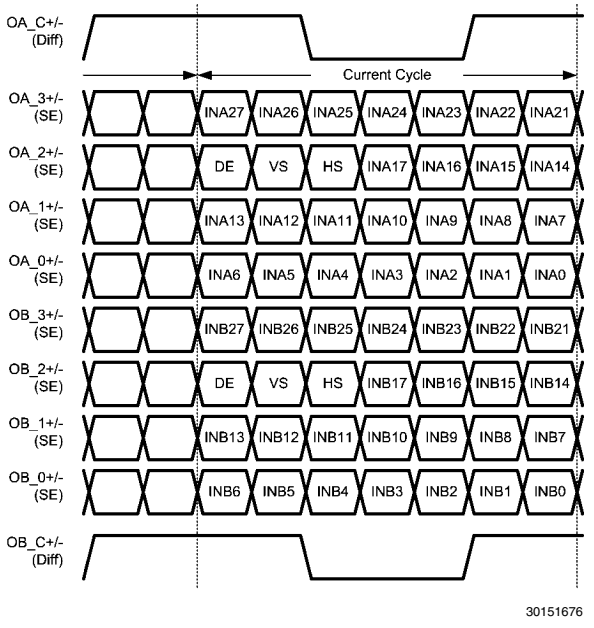


FIGURE 14. Dual Pixel / 24bpp LVDS Mapping

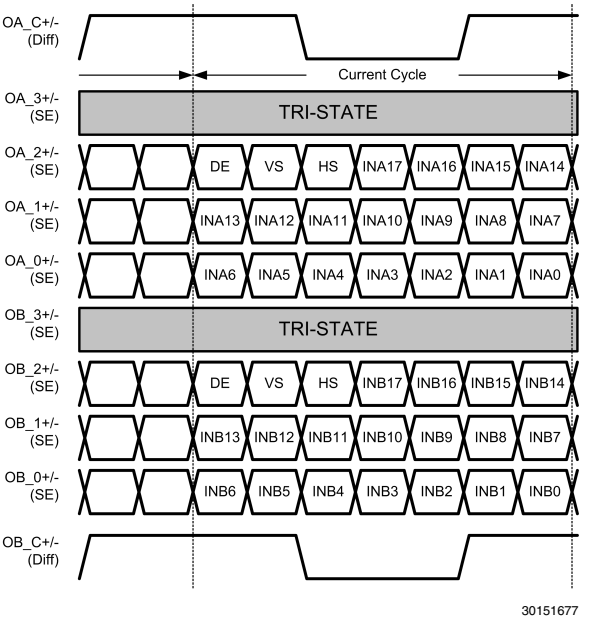


FIGURE 15. Dual Pixel / 18bpp LVDS Mapping

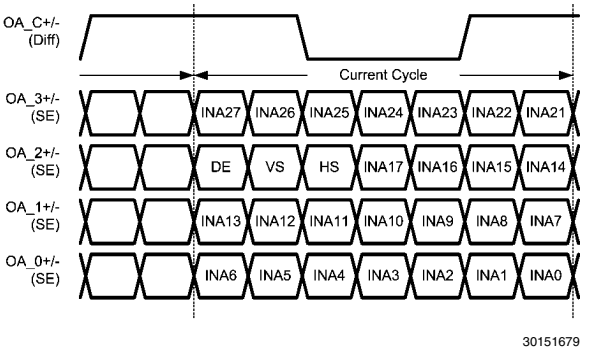


FIGURE 16. Single Pixel / 24bpp LVDS Mapping

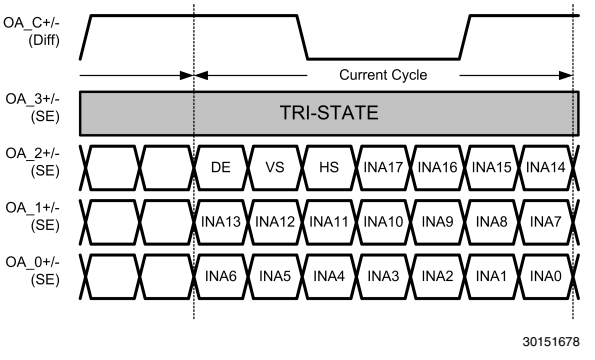


FIGURE 17. Single Pixel / 18bpp LVDS Mapping

COLOR MAPPING INFORMATION

A defacto color mapping is shown next. Different color mapping options exist. Check with the color mapping of the Deserializer / TCON device that is used to ensure compatible mapping for the application.

Single Pixel Input / 24bpp / MSB on CH3

DS90C187 Input	Color Mapping	Note
INA_22	R7	MSB
INA_21	R6	
INA_5	R5	
INA_4	R4	
INA_3	R3	
INA_2	R2	
INA_1	R1	
INA_0	R0	LSB
INA_24	G7	MSB
INA_23	G6	
INA_11	G5	
INA_10	G4	
INA_9	G3	
INA_8	G2	
INA_7	G1	
INA_6	G0	LSB
INA_26	B7	MSB
INA_25	B6	
INA_17	B5	
INA_16	B4	
INA_15	B3	
INA_14	B2	
INA_13	B1	
INA_12	B0	
DE	DE	Data Enable*
VS	VS	Vertical Sync
HS	HS	Horizontal Sync
INA_27	GP	General Purpose

Single Pixel Input / 24bpp / LSB on CH3

DS90C187 Input	Color Mapping	Note
INA_5	R7	MSB
INA_4	R6	
INA_3	R5	
INA_2	R4	
INA_1	R3	
INA_0	R2	
INA_22	R1	
INA_21	R0	LSB
INA_11	G7	MSB
INA_10	G6	
INA_9	G5	
INA_8	G4	
INA_7	G3	
INA_6	G2	
INA_24	G1	
INA_23	G0	LSB
INA_17	B7	MSB
INA_16	B6	
INA_15	B5	
INA_14	B4	
INA_13	B3	
INA_12	B2	
INA_26	B1	
INA_25	B0	
DE	DE	Data Enable*
VS	VS	Vertical Sync
HS	HS	Horizontal Sync
INA_27	GP	General Purpose

Single Pixel Input / 18bpp

DS90C187 Input	Color Mapping	Note
INA_5	R5	MSB
INA_4	R4	
INA_3	R3	
INA_2	R2	
INA_1	R1	
INA_0	R0	LSB
INA_11	G5	MSB
INA_10	G4	
INA_9	G3	
INA_8	G2	
INA_7	G1	
INA_6	G0	LSB
INA_17	B5	MSB
INA_16	B4	
INA_15	B3	
INA_14	B2	
INA_13	B1	
INA_12	B0	
DE	DE	Data Enable*
VS	VS	Vertical Sync
HS	HS	Horizontal Sync

Dual Pixel Input / 24bpp

DS90C187 Input	Color Mapping	Note
INA_22	O_R7	MSB
INA_21	O_R6	
INA_5	O_R5	
INA_4	O_R4	
INA_3	O_R3	
INA_2	O_R2	
INA_1	O_R1	
INA_0	O_R0	LSB
INA_24	O_G7	MSB
INA_23	O_G6	
INA_11	O_G5	
INA_10	O_G4	
INA_9	O_G3	
INA_8	O_G2	
INA_7	O_G1	
INA_6	O_G0	LSB
INA_26	O_B7	MSB
INA_25	O_B6	
INA_17	O_B5	
INA_16	O_B4	
INA_15	O_B3	
INA_14	O_B2	
INA_13	O_B1	
INA_12	O_B0	
INB_22	E_R7	
INB_21	E_R6	
INB_5	E_R5	
INB_4	E_R4	
INB_3	E_R3	
INB_2	E_R2	
INB_1	E_R1	
INB_0	E_R0	
INB_24	E_G7	
INB_23	E_G6	
INB_11	E_G5	
INB_10	E_G4	
INB_9	E_G3	
INB_8	E_G2	
INB_7	E_G1	
INB_6	E_G0	
INB_26	E_B7	
INB_25	E_B6	
INB_17	E_B5	
INB_16	E_B4	
INB_15	E_B3	
INB_14	E_B2	
INB_13	E_B1	
INB_12	E_B0	
DE	DE	Data Enable*
VS	VS	Vertical Sync
HS	HS	Horizontal Sync
INA_27	GP	General Purpose
INB_27	GP	General Purpose

Functional Description

DS90C187 converts a wide parallel LVCMOS input bus into banks of FPD-Link LVDS data. The device can be configured to support RGB-888 (24 bit color) or RGB-666 (18 bit color) in three main configurations: single pixel in / single pixel out; single pixel in / dual pixel out; dual pixel in / dual pixel out. The DS90C187 has several power saving features including: selectable VOD, 18 bit / 24 bit mode select, and a power down pin control.

Device Configuration

The MODE0 and MODE1 pins are used to configure the DS90C187 into the three main operation modes as shown in the table below.

TABLE 1. Mode Configurations

MODE1	MODE0	CONFIGURATION
0	0	Single Pixel Input / Single Pixel Output (SISO)
0	1	Single Pixel Input / Dual Pixel Output (SIDO)
1	0	Dual Pixel Input / Dual Pixel Output (DIDO)
1	1	**RESERVED**

Single Pixel Input / Single Pixel Output

When MODE0 and MODE1 are both set to low, data from INA_[27:0], HS, VS and DE is serialized and driven out on OA_[3:0]+/- with OA_C+/-. If 18B_MODE is LOW, then OA_3+/- is powered down and the corresponding LVCMOS input signals are ignored.

In this configuration IN_CLK can range from 25 MHz to 105 MHz, resulting in a total maximum payload of 700 Mbps (28 bits * 25MHz) to 2.94 Gbps (28 bits * 105 MHz). Each LVDS driver will operate at a speed of 7 bits per input clock cycle, resulting in a serial line rate of 175 Mbps to 735 Mbps. OA_C+/- will operate at the same rate as IN_CLK with a duty cycle ratio of 57:43.

Single Pixel Input / Dual Pixel Output

When MODE0 is HIGH and MODE1 is LOW, data from INA_[27:0], HS, VS and DE is serialized and driven out on OA_[3:0]+/- and OB_[3:0]+/- with OA_C+/- and OB_C+/-. If 18B_MODE is LOW, then OA_3+/- and OB_3+/- are powered down and the corresponding LVCMOS input signals are ignored. The input LVCMOS data is split into odd and even pixels starting with the odd (first) pixel outputs OA_[3:0]+/- and then the even (second) pixel outputs OB_[3:0]+/-. The splitting of the data signals starts with DE (data enable) transitioning from logic LOW to HIGH indicating active data (see *Figure 10*). **The number of clock cycles during blanking must be an EVEN number.** This configuration will allow the user to interface with two FPD-Link receivers or other dual pixel inputs.

In this configuration IN_CLK can range from 50 MHz to 185 MHz, resulting in a total maximum payload of 1.4 Gbps (28 bits * 50 MHz) to 5.18 Gbps (28 bits * 185 MHz). Each LVDS driver will operate at a speed of 7 bits per 2 input clock cycles, resulting in a serial line rate of 175 Mbps to 647.5 Mbps. OA_C+/- and OA_B+/- will operate at ½ the rate as IN_CLK with a duty cycle ratio of 57:43.

Dual Pixel Input / Dual Pixel Output

When MODE0 is LOW and MODE1 is set to HIGH, data from INA_[27:0], HS, VS and DE is serialized and driven out on OA_[3:0]+/- with OA_C+/-, while data from INB_[27:0], HS, VS and DE is serializer and driven out on OB_[3:0]+/- with OB_C+/-. If 18B_MODE is LOW, then OA_3+/- and OB_3+/- is powered down and the corresponding LVCMOS input signals are ignored.

In this configuration IN_CLK can range from 25 MHz to 105 MHz, resulting in a total maximum payload of 1.325 Gbps (53 bits * 25 MHz) to 5.565 Gbps (53 bits * 105 MHz). Each LVDS driver will operate at a speed of 7 bits per input clock cycle, resulting in a serial line rate of 175 Mbps to 735 Mbps. OA_C+/- and OB_C+/- will operate at the same rate as IN_CLK with a duty cycle ratio of 57:43.

Pixel Clock Edge Select (RFB)

The RFB pin determines the edge that the input LVCMOS data is latched on. If RFB is HIGH, input data is latched on the RISING EDGE of the pixel clock (IN_CLK). If RFB is LOW, the input data is latched on the FALLING EDGE of the pixel clock. Note: This can be set independently of receiver's output clock strobe.

TABLE 2. Pixel Clock Edge

RFB	Result
0	FALLING edge
1	RISING edge

Power Management

The DS90C187 has several features to assist with managing power consumption. The device can be configured through the MODE0 and MODE1 control pins to enable only the required number of LVDS drivers for each application. The 18B_MODE pin allows the DS90C187 to power down the unused LVDS driver(s) for RGB-666 (18 bit color) applications for an additional level of power management. If no clock is applied to the IN_CLK pin, the DS90C187 will enter a low power state. To place the DS90C187 in its lowest power state, the device can be powered down by driving the PDB pin to LOW.

Sleep Mode (PDB)

The DS90C187 provides a power down feature. When the device has been powered down, current draw through the supply pins is minimized and the PLL is shut down. The LVDS drivers are also powered down with their outputs pulled to GND through 100Ω resistors (not TRI-STATE®).

TABLE 3. Power Down Select

PDB	Result
0	SLEEP Mode (default)
1	ACTIVE (enabled)

LVDS Outputs

The DS90C187's LVDS drivers are compatible with ANSI/TIA/EIA-644–A LVDS receivers. The LVDS drivers can output a power saving low V_{OD}, or a high V_{OD} to enable longer trace and cable lengths by configuring the VODSEL pin.

TABLE 4. VOD Select

VODSEL	Result
0	±180 mV (360 mVpp)
1	±300 mV (600 mVpp)

Any unused LVDS outputs that are not powered down or put into TRI-STATE® due to the MODE0, MODE1, or 18B pins should be externally terminated differentially with a 100 ohm resistor. For example, when driving a timing controller (TCON) that only requires an 8D + C LVDS interface, rather than 8D + 2C, the unused clock line should be terminated near the package of the DS90C187. For more information regarding the output state of unused LVDS drivers, refer to the next section, 18 bit / 24 bit Color Mode (18B). For more information regarding the electrical characteristics of the LVDS outputs, refer to the LVDS DC Characteristics and LVDS Switching Specifications.

18 bit / 24 bit Color Mode (18B)

The 18B pin can be used to further save power by powering down the 4th LVDS driver in each used bank when the application requires only 18 bit color or 3D+C LVDS. Set the 18B pin to logic HIGH to TRI-STATE® OA_3+/- and OB_3+/- (if the device is configured for dual pixel output). For 24 bit color applications this pin should be set to logic LOW. Note that the power down function takes priority over the TRI-STATE® function. So if the device is configured for 18 bit color Single Pixel In/Single Pixel Out, LVDS channel OB_3+/- will be powered down and not TRI-STATE®. If an LVDS driver is powered down, each output terminal is pulled low by a 100 ohm resistor to ground.

TABLE 5. Color DepthConfigurations

18B	Result
0	24bpp, LVDS 4D+C or 8D+2C
1	18bpp, LVDS 3D+C or 6D+2C

LVCMOS Inputs

The DS90C187 has two banks of 24 data inputs, one set of video control signal (HS, VS and DE) inputs and several device configuration LVCMOS pins. All LVCMOS input pins are designed for 1.8V LVCMOS logic. All LVCMOS inputs, including clock, data and configuration pins, have an internal pull down resistor to set a default state. If any inputs are unused, they can be left as no connect (NC) or connected to ground.

Applications Information

Power Up Sequence

The V_{DD} power supply pins do not require a specific power on sequence and can be powered on in any order. However, the PDB pin should only be set to logic HIGH once the power sent to all supply pins is stable. Active clock and data inputs should not be applied to the DS90C187 until all of the input power pins have been powered on, settled to the recommended operating voltage and the PDB pin has be set to logic HIGH..

The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

Power up sequence (DS90C187 PDB input initially LOW):

1. Ramp up LCD power (maybe 0.5ms to 10ms) but keep backlight turned off.
2. Wait for additional 0-200ms to ensure display noise won't occur.
3. Toggle DS90C187 power down pin to PDB = V_{IH}.
4. Enable video source output; start sending black video data.
5. Send >1ms of black video data; this allows the DS90C187 to be phase locked, and the display to show black data first.
6. Start sending true image data.
7. Enable backlight.

Power Down sequence (DS90C187 PDB input initially HIGH):

1. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low.
2. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for >2 frame times.
3. Set DS90C187 power down pin to PDB = GND.
4. Disable the video output of the video source.
5. Remove power from the LCD panel for lowest system power.

Power Supply Filtering

The DS90C187 has several power supply pins at 1.8V. It is important that these pins all be connected and properly bypassed. Bypassing should consist of at least one 0.1µF capacitor placed on each pin, with an additional 4.7µF – 22µF capacitor placed on the PLL supply pin (VDDPLL). 0.01µF capacitors are typically recommended for each pin. Additional filtering including ferrite beads may be necessary for noisy systems. It is recommended to place a 0 ohm resistor at the bypass capacitors that connect to each power pin to allow for additional filtering if needed. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50µF — 100µF range.

Layout Guidelines

Circuit board layout and stack-up for the LVDS serializer devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. This practice is easier to implement in dense pcbs with many layers and may not be practical in simpler boards. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with vias on both ends of the capacitor.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency. Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the QFN (LLP) style package is provided in Application Note: AN-1187.

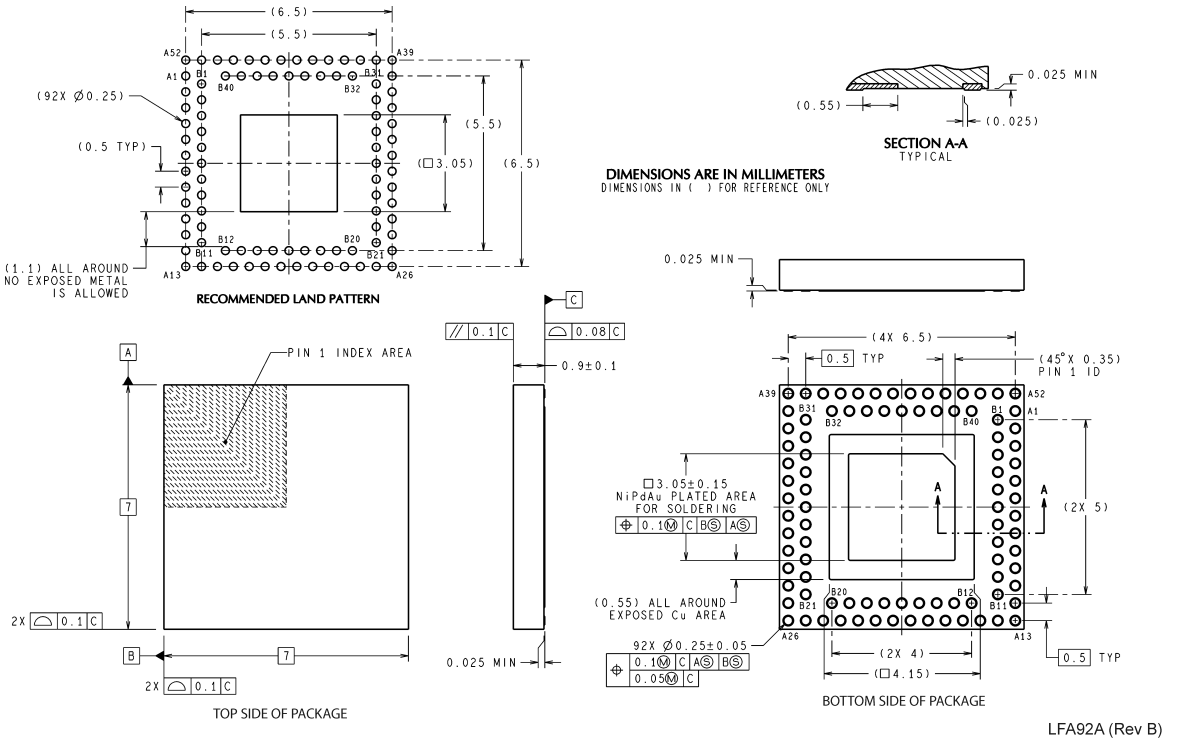
LVDS Interconnect Guidelines

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use differential connectors when above 500Mbps
- Minimize skew within the pair
- Use the S/2S/3S rule in spacings
  - — S = space between the pairs
  - — 2S = space between pairs
  - — 3S = space to LVCMOS signals
- Place ground vias next to signal vias when changing between layers
- When a signal changes reference planes, place a bypass cap and vias between the new and old reference plane

For more tips and detailed suggestions regarding high speed board layout principles, please consult the LVDS Owner's Manual at: http://www.ti.com/lvds

Physical Dimensions inches (millimeters) unless otherwise noted



Dimensions show in millimeters
TI Package Number LFA92A

Notes

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