VIA Labs, Inc.

Data Sheet

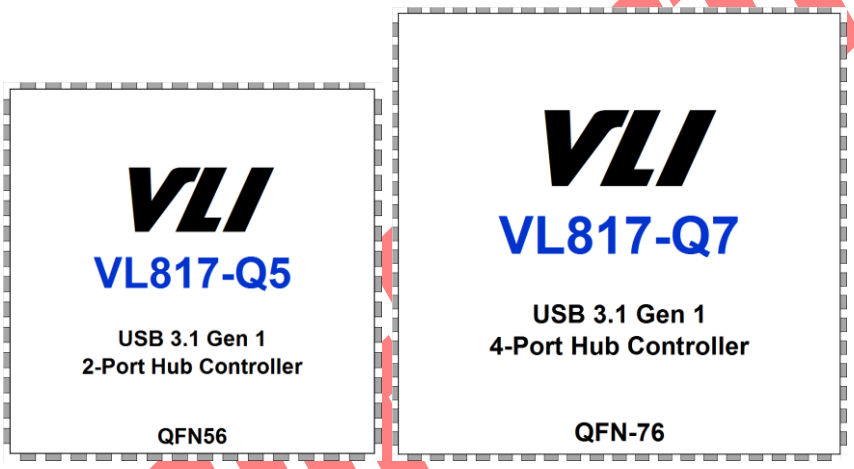
VL817 (B0)

USB 3.1 Gen 1 Hub Controller

January 18th , 2017

Revision 0.70

Preliminary



Revision History

Rev	Date	Note	Initial
0.70	01/18/2017	Preliminary Release.	EC

Contents

List of Figures

Product Features

VL817

USB 3.1 Gen 1 4/2-Port Hub Controller

- **USB 3.1 Compliant**
  - Compliant to Universal Serial Bus 3.1 Specification
    - Meets all USB 3.1 ECN through Jan 2017
  - Compliant to Universal Serial Bus 2.0 Specification
    USB 2.0 Hub Supports MTT
  - Supports Simultaneous Operation of Any Combination of SuperSpeed, High-Speed, Full-Speed, and Low-Speed Devices
  - Supports USB Power Saving Features such as Link Power Management, Ux States, Selective Suspend, and Function Suspend
  - In-house USB PHY employs advanced CMOS process for low power consumption

- **Integrated USB Devices**
  - USB HID Class Device (Optional)
    Implemented as a USB 2.0 Virtual Device, Facilitates FW Update or Media Control Buttons
    Configurable Behavior – Always Present / Disabled
  - USB Billboard Class 1.1 Device (Optional)
    Implemented as a USB 2.0 Virtual Device
    Configurable Behavior – Expose When Necessary / Always Present / Disabled

- **Full Sideband Signal Support**
  - Supports both Individual and Ganged Mode Operation for All Ports
  - Supports PWM LED Status Lights
  - SPI Interface for Firmware. Firmware Upgradable over USB.
  - Management Interface for Specialized Applications

- **Comprehensive USB Battery Charging Support**
  - Supports USB Battery Charging Specification v1.2 (SDP, CDP, DCP)
  - Support for Vendor Specific Charging Modes eg. Apple 2.4A, Samsung, etc.
  - Supports YD/T 1591-2009
  - Supports Stand-Alone Charging when System is Suspend, Shut Down, or Disconnected
  - Any Combination of DFPs can be Configured to Support USB Battery Charging

- **Power and Package**
  - Requires 3.3V and 1.1V Inputs
  - 25MHz Xtal
  - Integrated Voltage Regulators Generate All Required Voltages from 5V Input
    5V to 1.1V Switching DC-DC Regulator
    5V to 3.3V LDO Regulator
  - QFN 76L green package (9x9x0.85 mm)
  - QFN 56L green package (7x7x0.85 mm)

VL817 System Overview

VIA Lab's VL817 is a modern USB 3.1 Gen 1 Hub Controller, featuring an optimized cost-structure and full compliance with USB 3.1 Gen 1 specification including ECNs and Compliance Testing Updates through Jan 2017. VL817 is offered in both 2-port and 4-port configurations, and features integrated voltage regulators, new lower-power design, and comprehensive USB Charging support. VL817 supports any combination of SuperSpeed (5Gbps), High Speed (480Mbps), Full Speed (12Mbps), and Low Speed (1.5Mbps) devices, and the integrated USB 2.0 hub's Multiple Transaction Translators feature provides increased performance when multiple Full Speed devices are simultaneously used. The integrated 5V DC-DC switching regulator enables VL817 to be powered directly from 5V USB VBus, reducing BOM cost while offering high power efficiency.

VL817 features a flexible firmware architecture, providing a framework for custom functions in addition to in-field updates. Various parameters including Tx equalization setting and GPIO behavior are changeable via firmware, including the optionally configurable USB Charging Controller for charging various devices such as smartphones and tablets.

VL817-based hub devices work under Windows, Mac OS X, and various Linux kernels without additional drivers. VL817-based hub devices are also compatible with non-x86 devices and platforms that support USB hub functions such as smart phones, tablets, and set-top boxes. It is well suited for all USB hub applications such as standalone USB hubs, Notebook/Ultrabook docking stations/port-replicators, desktop PC front panel, motherboard on-board hub, and USB hub compound devices. VL817 incorporates multiple optional USB 2.0 Virtual Devices including USB Billboard, and USB HID to support Media Control Buttons such as Play/Pause, Volume Up/Down, etc.

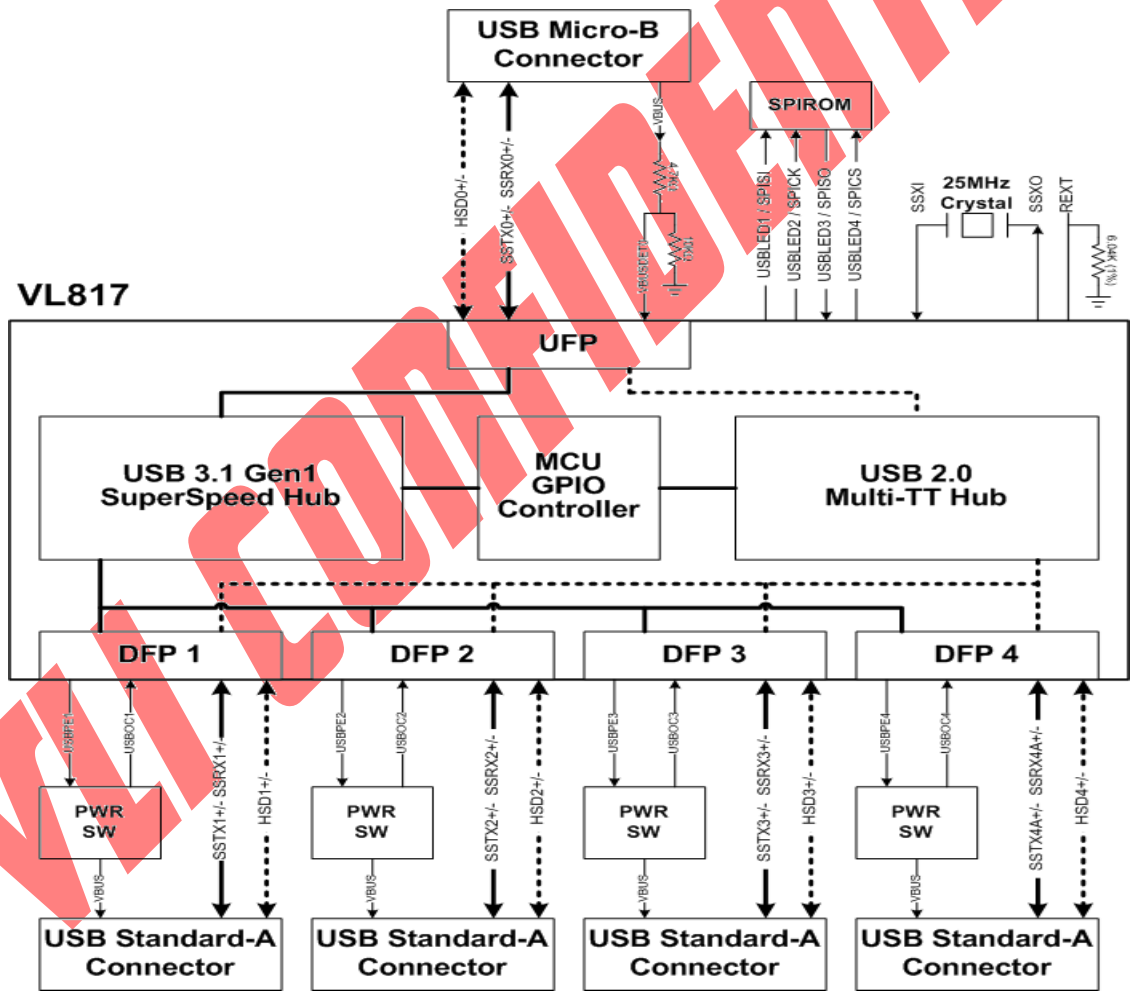


Figure 1 – VL817 Block Diagram

USB Battery Charging Behavior

3 Concepts of Rapid Charging over USB:

- **Rapid Charging over USB enables charging of devices at rates in excess of baseline USB standards.**

  The current limit of USB 2.0 is 500mA for configured devices, and the current limit of USB 3.0 is 900mA for configured devices. Depending on the device, Rapid Charging implementations typically feature current limits between 1000mA to 2400mA.

- **It is the Host/Hub's responsibility to advertise Rapid Charging capabilities, and it is the Device's responsibility to recognize and determine those capabilities.**

  Rapid Charging over USB enables charging at rates in excess of baseline USB specifications, so in order to prevent a situation where a device sinks more current than what a port is rated for, different manufacturers employ various charging schemes in an attempt to ensure safe and reliable operation with their respective device and charger. It goes without saying that Rapid Charging will only occur when both Host/Hub and Device supports it.

- **The rate at which a device charges is dependent upon the device.**

  This means that the device must determine the host/hub port's capabilities to determine which charging mode to use. Also, the rate at which a device charges can vary depending on the status of the device. For example, some devices only charge at their maximum rate when the battery is nearly depleted. When the battery is nearly full, they may switch to a trickle-charge mode. The Host/Hub rapid-charging port has no control over this behavior.

Supported USB Charging Modes

SDP – Standard Downstream Port
This is a typical USB 2.0 or USB 3.0 port and does not explicitly support Rapid USB Charging. SDP is constrained to the current limits as defined in the USB 2.0 or USB 3.0 spec which are 500mA and 900mA respectively. While the actual current limit is enforced by the polyfuse or power-switch providing current-limiting functionality for the downstream port, most USB devices will not draw more than 500mA or 900mA under USB 2.0 or USB 3.0 modes.

CDP – Charging Downstream Port
CDP is defined in the USB Battery Charging Specification 1.2 and enables devices that are able to correctly recognize CDP to simultaneously function as a USB device while drawing up to 1.5A for Rapid Charging when connected to the downstream port of a USB Host or Hub that advertises CDP capability.

DCP – Dedicated Charging Port
DCP is defined in the USB Battery Charging Specification 1.2 and has been in use on an unofficial basis prior to the official USB Battery Charging Specification. DCP is a dedicated charging mode, so when a device is charging under DCP, regular USB operations such as data transfer to the device are not supported.

Special Modes
Various vendors such as Apple, RIM, Motorola, etc. may employ different detection mechanisms compared to other USB devices and thus, may enter Rapid Charging under the previously mentioned charging modes. VL817 supports an auto detection mechanism that provides charging for the majority of devices.

Pinout (VL817-Q7)

Figure 2 – VL817-Q7 Pin Diagram

Pin List (VL817-Q7)

Table 1 – VL817-Q7 Pin List

Pin	Pin Name	Pin	Pin Name
1	SSTX1+	39	LX
2	SSTX1-	40	VCC11FB
3	VCC11_L1	41	USBOC3
4	SSRX1+	42	USBPE3
5	SSRX1-	43	VCC33D1
6	VCC33_L1	44	EXTPWRON
7	HSD1+	45	VBUSDET
8	HSD1-	46	VCCD4
9	VCCD2	47	SSTX0-
10	SSTX4+	48	SSTX0+
11	SSTX4-	49	VCC11_L0
12	VCC11_L4	50	SSRX0-
13	SSRX4+	51	SSRX0+
14	SSRX4-	52	VCC33_L0
15	VCC33_L4	53	HSD0+
16	HSD4+	54	HSD0-
17	HSD4-	55	SSXI
18	USBOC2	56	SSXO
19	USBPE2	57	SSREXT
20	VCCLDO5	58	VCC33M
21	VCC33O	59	SSTX3+
22	VCCD3	60	SSTX3-
23	TESTEN	61	VCC11_L3
24	RESET#	62	SSRX3+
25	USBOC1	63	SSRX3-
26	USBPE1	64	VCC33_L3
27	USBOC4	65	HSD3+
28	USBPE4	66	HSD3-
29	VCC33D2	67	VCCD1
30	GPIOB	68	SSTX2+
31	GPIOA	69	SSTX2-
32	USBLED4 / SPICS	70	VCC11_L2
33	USBLED3 / SPISO	71	SSRX2+
34	USBLED2 / SPICK	72	SSRX2-
35	USBLED1 / SPISI	73	VCC33_L2
36	GPIO2/SMCLK/USBHID	74	HSD2+
37	GPIO1/SMDAT/USBSUS	75	HSD2-
38	VCC5I	76	VCC11M

Pin Descriptions (VL817-Q7)

Signal Type Definition

Name	Type	Signal Description
Input	I	A Logic Input Only Signal
Output	O	A Logic Output Only Signal
Input/Output	I/O	A Logic Bi-Directional Signal
Power	PWR	A Power Pin
Ground	GND	A Ground Pin

USB 3.1 Interface

Pin Name	Pin #	I/O	Signal Description
SSTX0+	48	O	USB 3.1 UFP Differential TX+
SSTX0-	47	O	USB 3.1 UFP Differential TX–
SSRX0+	51	I	USB 3.1 UFP Differential RX+
SSRX0-	50	I	USB 3.1 UFP Differential RX–
SSTX1+	1	O	USB 3.1 DFP1 Differential TX+
SSTX1-	2	O	USB 3.1 DFP1 Differential TX–
SSRX1+	4	I	USB 3.1 DFP1 Differential RX+
SSRX1-	5	I	USB 3.1 DFP1 Differential RX–
SSTX2+	68	O	USB 3.1 DFP2 Differential TX+
SSTX2-	69	O	USB 3.1 DFP2 Differential TX–
SSRX2+	71	I	USB 3.1 DFP2 Differential RX+
SSRX2-	72	I	USB 3.1 DFP2 Differential RX–
SSTX3+	59	O	USB 3.1 DFP3 Differential TX+
SSTX3-	60	O	USB 3.1 DFP3 Differential TX–
SSRX3+	62	I	USB 3.1 DFP3 Differential RX+
SSRX3-	63	I	USB 3.1 DFP3 Differential RX–
SSTX4+	10	O	USB 3.1 DFP4 Differential TX+
SSTX4-	11	O	USB 3.1 DFP4 Differential TX–
SSRX4+	13	I	USB 3.1 DFP4 Differential RX+
SSRX4-	14	I	USB 3.1 DFP4 Differential RX–

USB 2.0 Interface

Pin Name	Pin #	I/O	Signal Description
HSD0+	53	I/O	USB 2.0 UFP Differential D+
HSD0–	54	I/O	USB 2.0 UFP Differential D–
HSD1+	7	I/O	USB 2.0 DFP1 Differential D+
HSD1–	8	I/O	USB 2.0 DFP1 Differential D–
HSD2+	74	I/O	USB 2.0 DFP2 Differential D+
HSD2–	75	I/O	USB 2.0 DFP2 Differential D–
HSD3+	65	I/O	USB 2.0 DFP3 Differential D+
HSD3–	66	I/O	USB 2.0 DFP3 Differential D–
HSD4+	16	I/O	USB 2.0 DFP4 Differential D+
HSD4–	17	I/O	USB 2.0 DFP4 Differential D–

Analog Command Block

Pin Name	Pin #	I/O	Signal Description
SSXI	55	O	25M Crystal Input
SSXO	56	I	25M Crystal Output
SSREXT	57	I	Connect to External Reference Resistor (6.04K+/- 1%)

Power and Ground

Pin Name	Pin #	I/O	Signal Description
GND	EPAD	GND	Ground
VCCD	9, 22, 46, 67	PWR	1.1V Core Power
VCC11	3, 12, 49, 61, 70	PWR	1.1V Analog Power
VCC11M	76	PWR	1.1V Analog Power
VCC33D	29, 43	PWR	3.3V Digital Power
VCC33	6, 15, 49, 64, 73	PWR	3.3V Analog Power
VCC33M	58	PWR	3.3V Analog Power
VCC5I	38	PWR	5-1.1V DC-DC Switching Regulator Input
LX	39	O	5-1.1V DC-DC Switching Regulator Output, Connect to Output Inductor (4.7uH) with Output Cap (10uF)
VCC11FB	40	I	5-1.1V DC-DC Switching Regulator Feedback
VCC5LDO	20	PWR	5-3.3V LDO Regulator Input
VCC33O	21	PWR	5-3.3V LDO Regulator Output Output Cap (4.7uF)

Test Pin

Pin Name	Pin #	I/O	Signal Description
TESTEN	23	I	Test Mode Enable Low: Normal mode. High: Test mode.
GPIO1/SMDAT/USBSUS	37	I/O	SMBus data with Proprietary Data Format. Open Drain. Available for GPIO Use via Firmware Setting.
GPIO2/SMCLK/USBHID	36	I/O	SMBus clock with Proprietary Data Format. Open Drain. Available for GPIO Use via Firmware Setting.

Side Band Signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
USBOC1	25	I	DFP1 USB OC USB Over Current Detection High: Normal Low: Port Over Current Event
USBPE1	26	O	DFP1 USB PE USB Power Enable Mode High: Enable Low: Off
USBOC2	18	I	DFP2 USB OC USB Over Current Detection High: Normal Low: Port Over Current Event
USBPE2	19	O	DFP2 USB PE USB Power Enable Mode High: Enable Low: Off
USBOC3	41	I	DFP3 USB OC USB Over Current Detection High: Normal Low: Port Over Current Event
USBPE3	42	O	DFP3 USB PE USB Power Enable Mode High: Enable Low: Off
USBOC4	27	I	DFP4 USB OC USB Over Current Detection High: Normal Low: Port Over Current Event
USBPE4	28	O	DFP4 USB PE USB Power Enable Mode High: Enable Low: Off
GPIOA	31	I/O	GPIO (FW Config)
GPIOB	30	I/O	GPIO (FW Config)
EXTPWRON	44	I	External Power Status (3.3V Max) High: External power attached Low: External power no detect
RESET#	24	I	System Reset Low: Reset High: Normal Operation
USBLED1/SPISI	35	I/O	DFP1 LED Indicator / SPISI shared pin. Active High Output for LED Use.
USBLED2/SPICLK	34	I/O	DFP2 LED Indicator / SPISCLK shared pin. Active High Output for LED Use.
USBLED3/SPISO	33	I/O	DFP3 LED Indicator / SPISO shared pin. Active High Output for LED Use.
USBLED4/SPICS	32	I/O	DFP4 LED Indicator / SPICS shared pin. Active High Output for LED Use
VBUSDET	45	I	UFP Vbus Detection (3.3V Max)

Pinout (VL817-Q5)

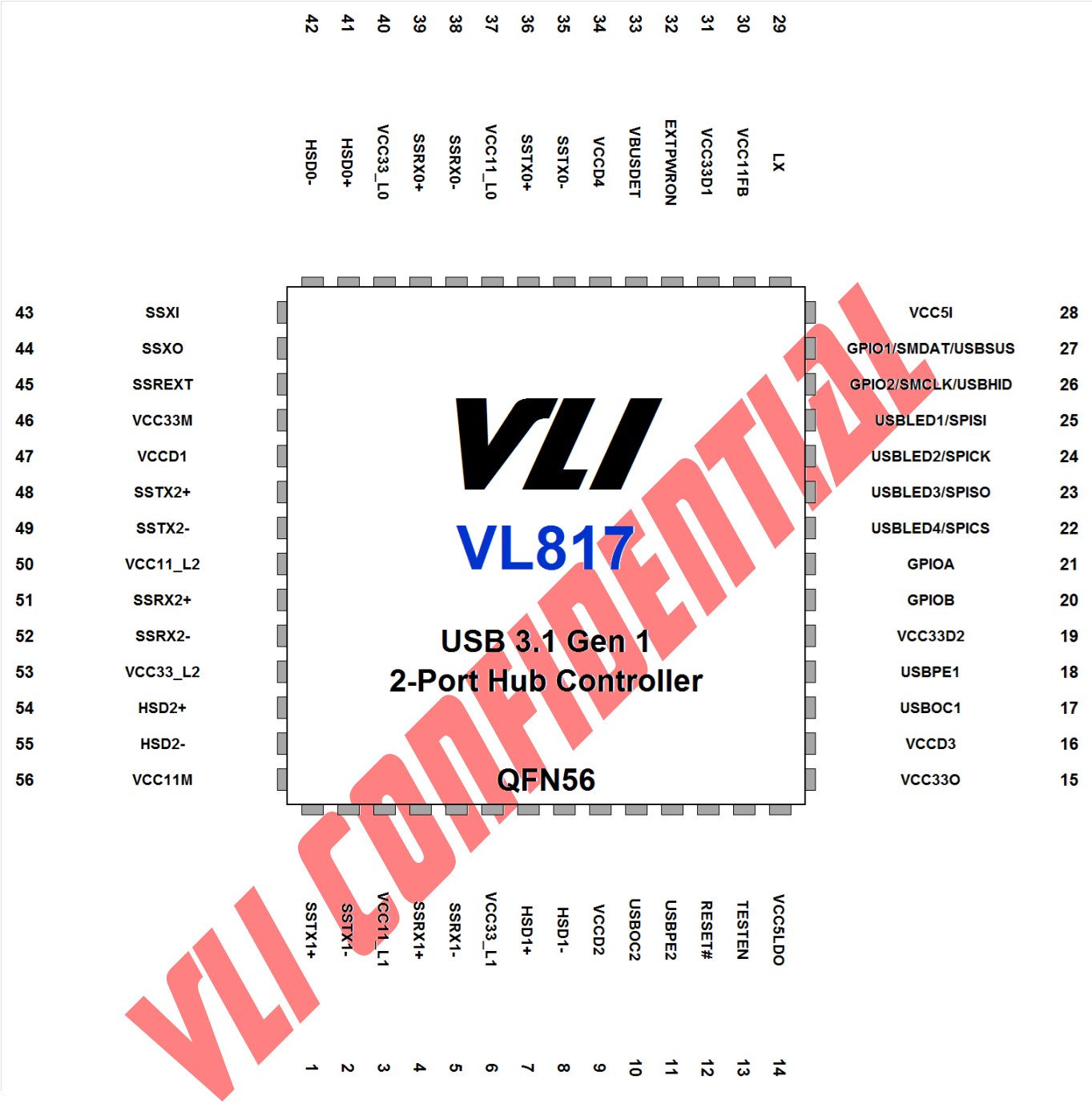


Figure 3 – VL817-Q5 Pin Diagram

Pin List (VL817-Q5)

Table 2 – VL817-Q5 Pin List

Pin	Pin Name	Pin	Pin Name
1	SSTX1+	29	LX
2	SSTX1-	30	VCC11FB
3	VCC11_L1	31	VCC33D1
4	SSRX1+	32	EXTPWRON
5	SSRX1-	33	VBUSDET
6	VCC33_L1	34	VCCD4
7	HSD1+	35	SSTX0-
8	HSD1-	36	SSTX0+
9	VCCD2	37	VCC11_L0
10	USBOC2	38	SSRX0-
11	USBPE2	39	SSRX0+
12	RESET#	40	VCC33_L0
13	TESTEN	41	HSD0+
14	VCCLDO5	42	HSD0-
15	VCC33O	43	SSXI
16	VCCD3	44	SSXO
17	USBOC1	45	SSREXT
18	USBPE1	46	VCC33M
19	VCC33D2	47	VCCD1
20	GPIOB	48	SSTX2+
21	GPIOA	49	SSTX2-
22	USBLED4 / SPICS	50	VCC11_L2
23	USBLED3 / SPISO	51	SSRX2+
24	USBLED2 / SPICK	52	SSRX2-
25	USBLED1 / SPISI	53	VCC33_L2
26	GPIO2/SMCLK/USBHID	54	HSD2+
27	GPIO1/SMDAT/USBSUS	55	HSD2-
28	VCC5I	56	VCC11M

Pin Descriptions (VL817-Q5)

Signal Type Definition

Name	Type	Signal Description
Input	I	A Logic Input Only Signal
Output	O	A Logic Output Only Signal
Input/Output	I/O	A Logic Bi-Directional Signal
Power	PWR	A Power Pin
Ground	GND	A Ground Pin

USB 3.1 Interface

Pin Name	Pin #	I/O	Signal Description
SSTX0+	36	O	USB 3.1 UFP Differential TX+
SSTX0-	35	O	USB 3.1 UFP Differential TX–
SSRX0+	39	I	USB 3.1 UFP Differential RX+
SSRX0-	38	I	USB 3.1 UFP Differential RX–
SSTX1+	1	O	USB 3.1 DFP1 Differential TX+
SSTX1-	2	O	USB 3.1 DFP1 Differential TX–
SSRX1+	4	I	USB 3.1 DFP1 Differential RX+
SSRX1-	5	I	USB 3.1 DFP1 Differential RX–
SSTX2+	48	O	USB 3.1 DFP2 Differential TX+
SSTX2-	49	O	USB 3.1 DFP2 Differential TX–
SSRX2+	51	I	USB 3.1 DFP2 Differential RX+
SSRX2-	52	I	USB 3.1 DFP2 Differential RX–

USB 2.0 Interface

Pin Name	Pin #	I/O	Signal Description
HSD0+	41	I/O	USB 2.0 UFP Differential D+
HSD0–	42	I/O	USB 2.0 UFP Differential D–
HSD1+	7	I/O	USB 2.0 DFP1 Differential D+
HSD1–	8	I/O	USB 2.0 DFP1 Differential D–
HSD2+	54	I/O	USB 2.0 DFP2 Differential D+
HSD2–	55	I/O	USB 2.0 DFP2 Differential D–

Analog Command Block

Pin Name	Pin #	I/O	Signal Description
SSXI	43	I	25M Crystal Input
SSXO	44	O	25M Crystal Output
SSREXT	45	I	Connect to External Reference Resistor (6.04K+/- 1%)

Power and Ground

Pin Name	Pin #	I/O	Signal Description
GND	EPAD	GND	Ground
VCCD	9, 16, 34, 47	PWR	1.1V Core Power
VCC11	3, 37, 50	PWR	1.1V Analog Power
VCC11M	56	PWR	1.1V Analog Power
VCC33D	19, 31	PWR	3.3V Digital Power
VCC33	6, 40, 53	PWR	3.3V Analog Power
VCC33M	46	PWR	3.3V Analog Power
VCC5I	28	PWR	5-1.1V DC-DC Switching Regulator Input
LX	29	O	5-1.1V DC-DC Switching Regulator Output, Connect to Output Inductor (4.7uH) with Output Cap (10uF)
VCC11FB	30	I	5-1.1V DC-DC Switching Regulator Feedback
VCC5LDO	14	PWR	5-3.3V LDO Regulator Input
VCC33O	15	PWR	5-3.3V LDO Regulator Output Output Cap (4.7uF)

Test Pin

Pin Name	Pin #	I/O	Signal Description
TESTEN	13	I	Test Mode Enable Low: Normal mode. High: Test mode.
GPIO1/SMDAT/USBSUS	27	I/O	SMBus data with Proprietary Data Format. Open Drain. Available for GPIO Use via Firmware Setting.
GPIO2/SMCLK/USBHID	26	I/O	SMBus clock with Proprietary Data Format. Open Drain. Available for GPIO Use via Firmware Setting.

Side Band Signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
USBOC1	17	I	DFP1 USB OC USB Over Current Detection High: Normal Low: Port Over Current Event
USBPE1	18	O	DFP1 USB PE USB Power Enable Mode High: Enable Low: Off
USBOC2	10	I	DFP2 USB OC USB Over Current Detection High: Normal Low: Port Over Current Event
USBPE2	11	O	DFP2 USB PE USB Power Enable Mode High: Enable Low: Off
GPIOA	21	I/O	GPIO (FW Config)
GPIOB	20	I/O	GPIO (FW Config)
EXTPWRON	32	I	External Power Status (3.3V Max) High: External power attached Low: External power no detect
RESET#	12	I	System Reset Low: Reset High: Normal Operation
USBLED1/SPISI	25	I/O	DFP1 LED Indicator / SPISI shared pin. Active High Output for LED Use.
USBLED2/SPICLK	24	I/O	DFP2 LED Indicator / SPISCLK shared pin. Active High Output for LED Use.
USBLED3/SPISO	23	I/O	DFP3 LED Indicator / SPISO shared pin. Active High Output for LED Use.
USBLED4/SPICS	22	I/O	DFP4 LED Indicator / SPICS shared pin. Active High Output for LED Use
VBUSDET	33	I	UFP Vbus Detection (3.3V Max)

Electrical Specification

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-40	125	°C	—
V_{33}	3.3V Power Supply Voltage	-0.5	3.63	V	—
V_{11}	1.1V Input Voltage	-0.5	1.26	V	—
V_{IN}	Input voltage at I/O pins	-0.5	(≦ 3.63) and (≦ V_{33}+0.3)	V	—
V_{ESD}	Electrostatic Discharge	-2000	2000	V	Human Body Model
θ_{jc}	Thermal resistance between junction and case	TBD		°C/W	2L & 4L PCB definitions follow JESD51-7
θ_{ja}	Thermal resistance between junction and ambient	TBD		°C/W	
P_D	Power dissipation	—	TBD	W	

Note: Stress above conditions may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described.

Note: About thermal factors, T_a is the concerned ambient temperature, and
$\theta_{ca} = \theta_{ja} - \theta_{jc}$
$T_J = \theta_{ja} * P_D + T_a$
$T_c = \theta_{ca} * P_D + T_a$

Operating Conditions

Symbol	Parameter	Min	Max	Unit	Note
T_A	Ambient Temperature	0	70	°C	—
T_j	Junction Temperature	0	125	°C	—
V_{33}	3.3V Power Supply Voltage	3.0	3.6	V	—
V_{11}	1.1V Input Voltage	1	1.2	V	—
V_{IL}	Input Low Voltage	—	0.8	V	—
V_{IH}	Input High Voltage	2.3	—	V	—
V_{OL}	Output Low Voltage	—	0.4	V	I_{OL}=4mA
V_{OH}	Output High Voltage	2.4	—	V	I_{OH}=4mA
I_{IL}	Input Leakage Current	—	+/-10	μA	$0<V_i<V_{33}$
I_{OZ}	Tristate Leakage Current	—	+/-20	μA	$0<V_o<V_{33}$

Timing Requirements for SPI Flash

SPI flash ROM is used to store the FW data for VL817 Timing guidelines are provided to assist in selection of appropriate and compatible SPI flash. To ensure SPI flash suitability, not only should the timing requirements conform to the provided guidelines, but actual testing with VL817 should also be done.

Symbol	Parameters	Condition	Value	Unit
f_{CT}	Clock Frequency for fast read mode(*)	Max value must larger than	15	MHz
f_{C}	Clock Frequency for read mode	Max value must larger than	15	MHz
t_{RI}	Input Rise time	Max value must larger than	5	ns
t_{FI}	Input Fall time	Max value must larger than	5	ns
t_{CKH}	SCK High Time	Min value must smaller than	20	ns
t_{CKL}	SCK Low Time	Min value must smaller than	20	ns
t_{CEH}	CE# High Time	Min value must smaller than	100	ns
t_{CS}	CE# Setup Time	Min value must smaller than	20	ns
t_{CH}	CE# Holde Time	Min value must smaller than	100	ns
t_{DS}	Data In Setup Time	Min value must smaller than	20	ns
t_{DH}	Data In Hold Time	Min value must smaller than	20	ns
t_{HS}	Hold Setup Time	Not Utilized		
t_{HD}	Hold Time	Not Utilized		
t_{V}	Output Valid	Max value must smaller than	20	ns
t_{OH}	Output Hold Time Normal Mode	Not Utilized		
t_{LZ}	Hold to Output Low Z	Not Utilized		
t_{HZ}	Hold to Output High Z	Not Utilized		
t_{DIS}	Output Disable Time	Not Utilized		
t_{EC}	Erase Time	Max value must smaller than	100	ms
t_{PP}	Page Program Time	Max value must smaller than	100	ms
t_{VCS}	Vcc Setup Time	Min value must smaller than	1	ms
t_{w}	Write Status Register Time (Flash bit)	Max value must smaller than	100	ms

*Fast read mode must be supported.

SERIAL INPUT/OUTPUT TIMING (1)

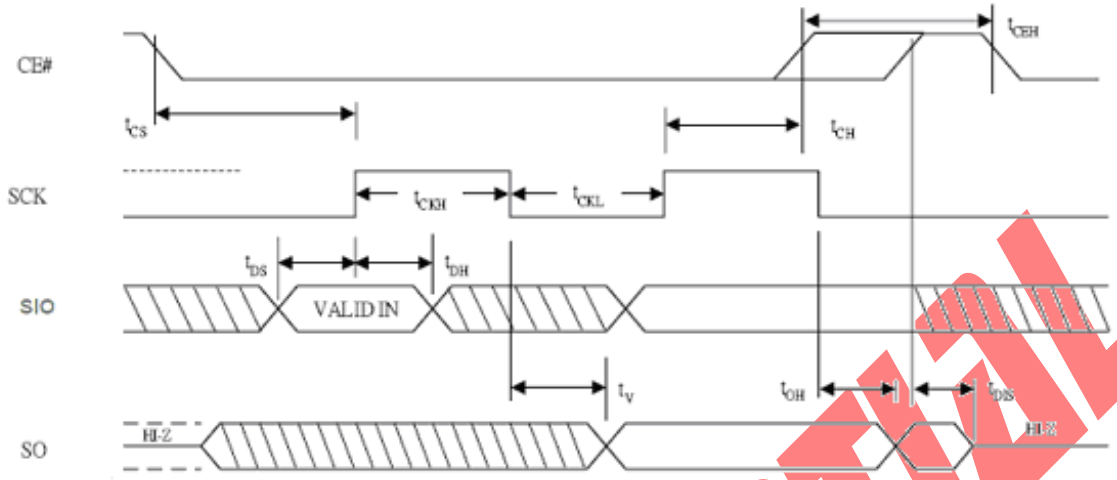


Figure 4 – Illustration of SPI Flash Interface Timing – (1)

HOLD TIMING

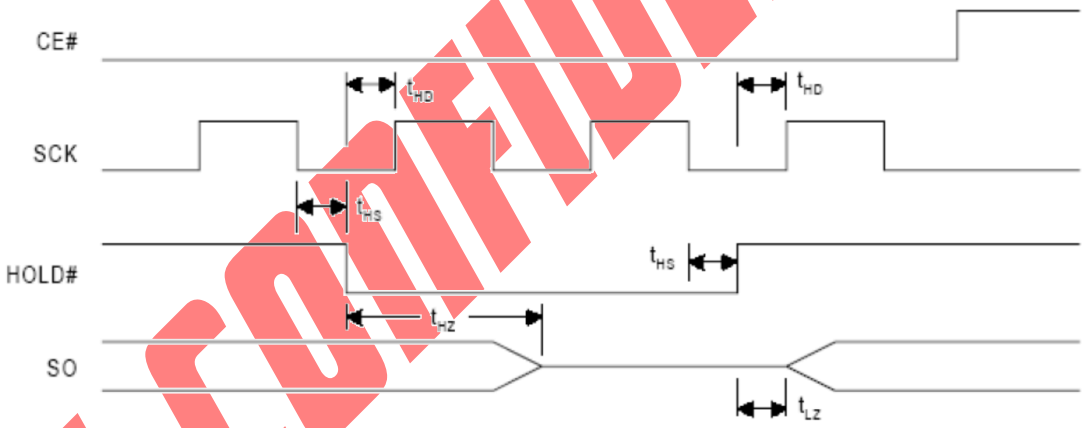


Figure 5 – Illustration of SPI Flash Interface Timing – (2)

General Reflow Profile Guidelines

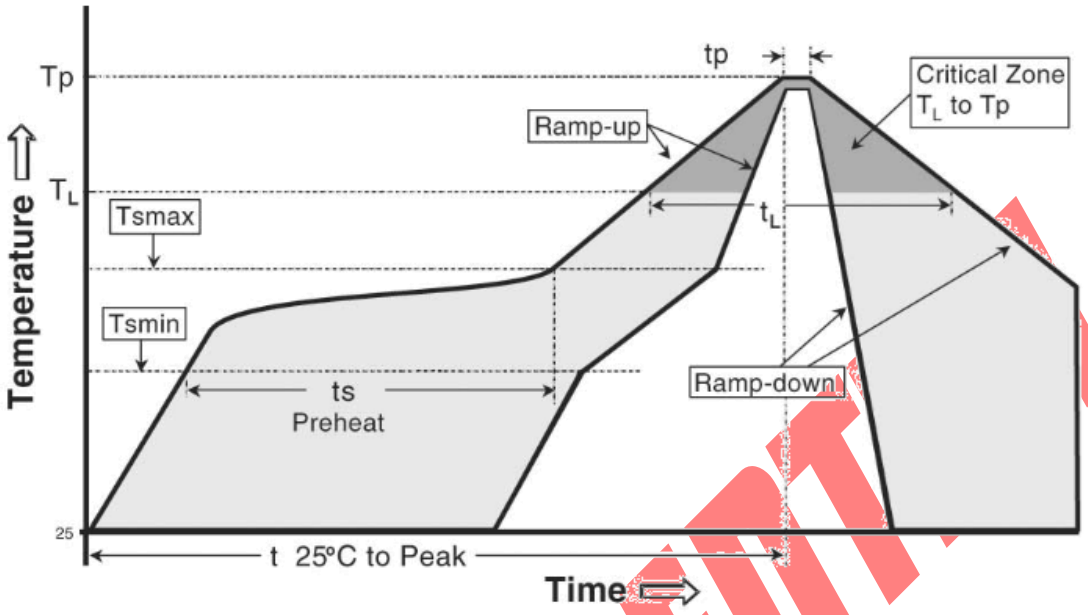


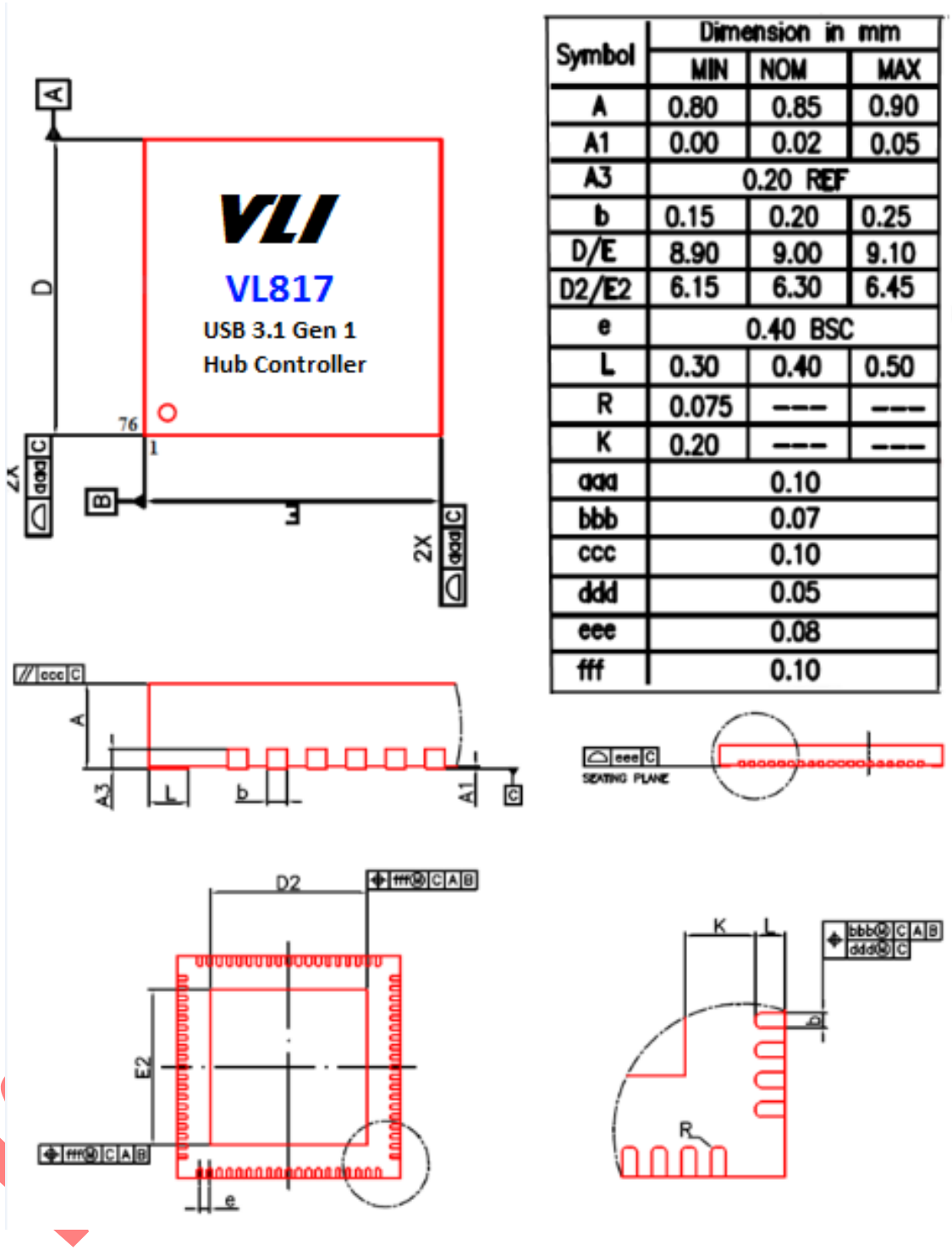
Figure 6 –Reflow

Profile Feature:	**Sn-Pb Eutectic**	**Pb-Free solder**
Average ramp-up rate (Liquidus Temperature (T_L) to Peak)	3°C/second max.	3°C/second max.
Preheat/Soak Temperature Min. (T_{smin}) Temperature Max. (T_{smax}) Time (min to max) (t_s)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-120 seconds
Ts(max) to Tl -Ramp-up Rate		3°C/second max.
Time maintained above: Temperature (T_L) Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak package body temperature(Tp) Time within 5°C of actual peak temperature(Tp)	225+5/-0°C 20 seconds	255 +5/0°C 30 seconds
Ramp-down rate (T_p to T_L)	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

***Note 1:** All temperatures refer to the center of package, measured on package body surface

***Note 2:** The reflow condition may vary with PCB design, pitch, size, reflow condition and solder suppliers, please contact your solder and reflow vendors.

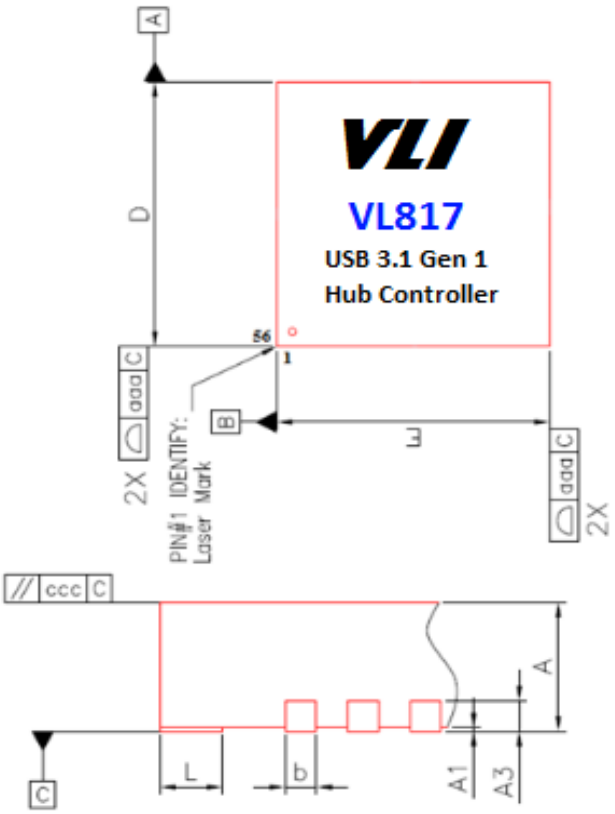
Package Mechanical Specifications (VL817-Q7)



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D/E	8.90	9.00	9.10
D2/E2	6.15	6.30	6.45
e		0.40 BSC	
L	0.30	0.40	0.50
R	0.075	---	---
K	0.20	---	---
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 7 – Mechanical Specification – QFN 76L 9x9x0.85 mm Package

Package Mechanical Specifications (VL817-Q5)



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	4.50	4.60	4.70
E2	4.50	4.60	4.70
e		0.40 BSC	
L	0.30	0.40	0.50
K	0.20	---	---
R	0.075	---	0.125
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 8 – Mechanical Specification – QFN 56L 7x7x0.85 mm Package

Package Top Side Marking & Ordering Information

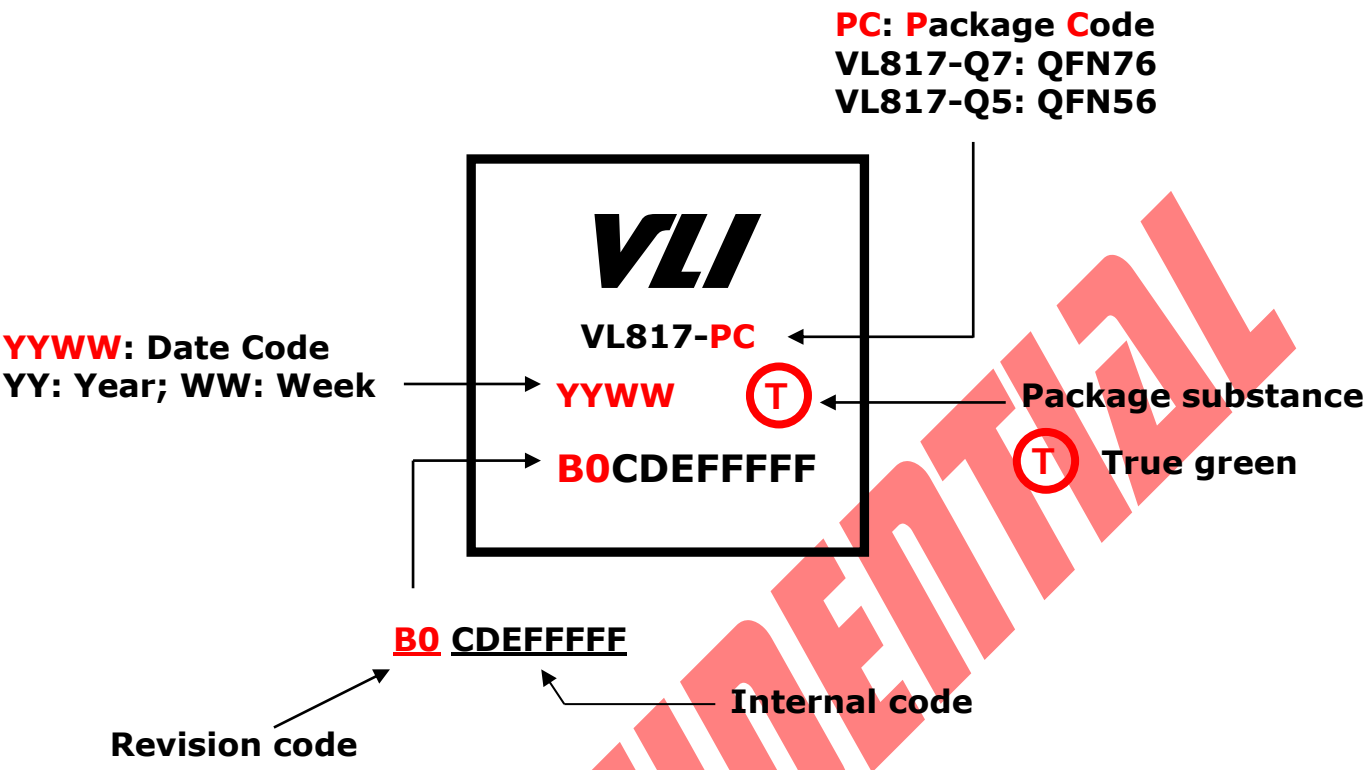


Figure 9 –Package Top Side Marking

Ordering Information

Part Number	Description	Package
VL817-Q7 (B0)	4-Port USB3.1 Gen1 Hub	QFN76 9x9 mm
VL817-Q5 (B0)	2-Port USB3.1 Gen1 Hub	QFN56 7x7 mm

VIA Labs, Inc.
www.via-labs.com
7F, 529-1, Zhongzheng Rd.,
Xindian District, New Taipei City 23148 Taiwan
Tel: (886-2) 2218-1838
Fax: (886-2) 2218-2553
Email: sales@via-labs.com.tw