NEC

MOS INTEGRATED CIRCUIT
μPD16704

240-OUTPUT TFT-LCD GATE DRIVER

DESCRIPTION

The μPD16704 is a TFT-LCD gate driver equipped with 240-output lines. It can output a high-gate scanning voltage in response to CMOS level input because it is provided with a level-shift circuit inside the IC circuit.

FEATURES

- CMOS level input (3.0 to 3.6 V)
- 240 outputs
- High-output voltage (V_{DD2} to V_{EE2}: 40 V MAX.)
- Double scan inversion function
- COG inversion

ORDERING INFORMATION

Part Number	Package
μPD16704P	Chip

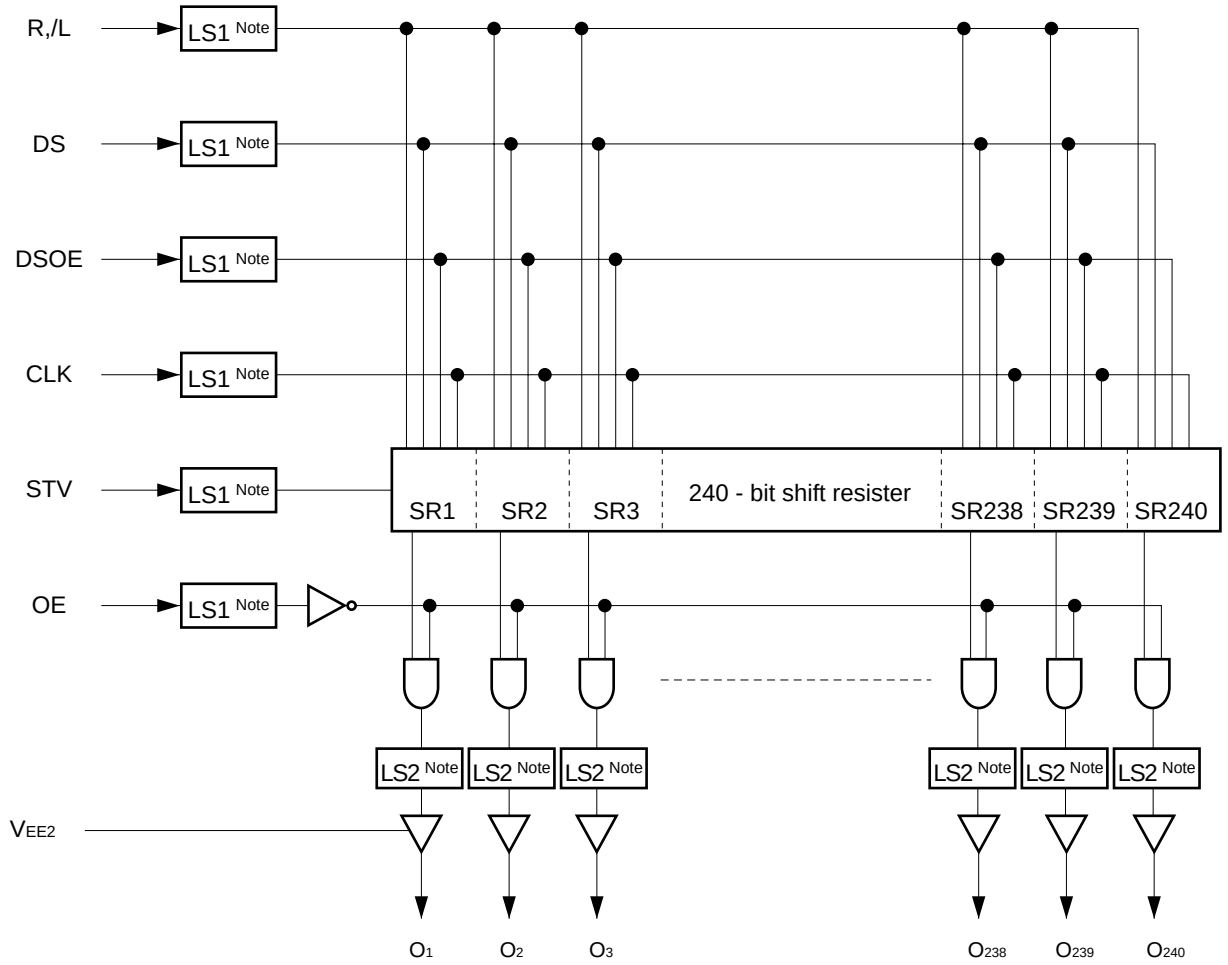
Remark Purchasing the above chip entail the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representavies.

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1. BLOCK DIAGRAM

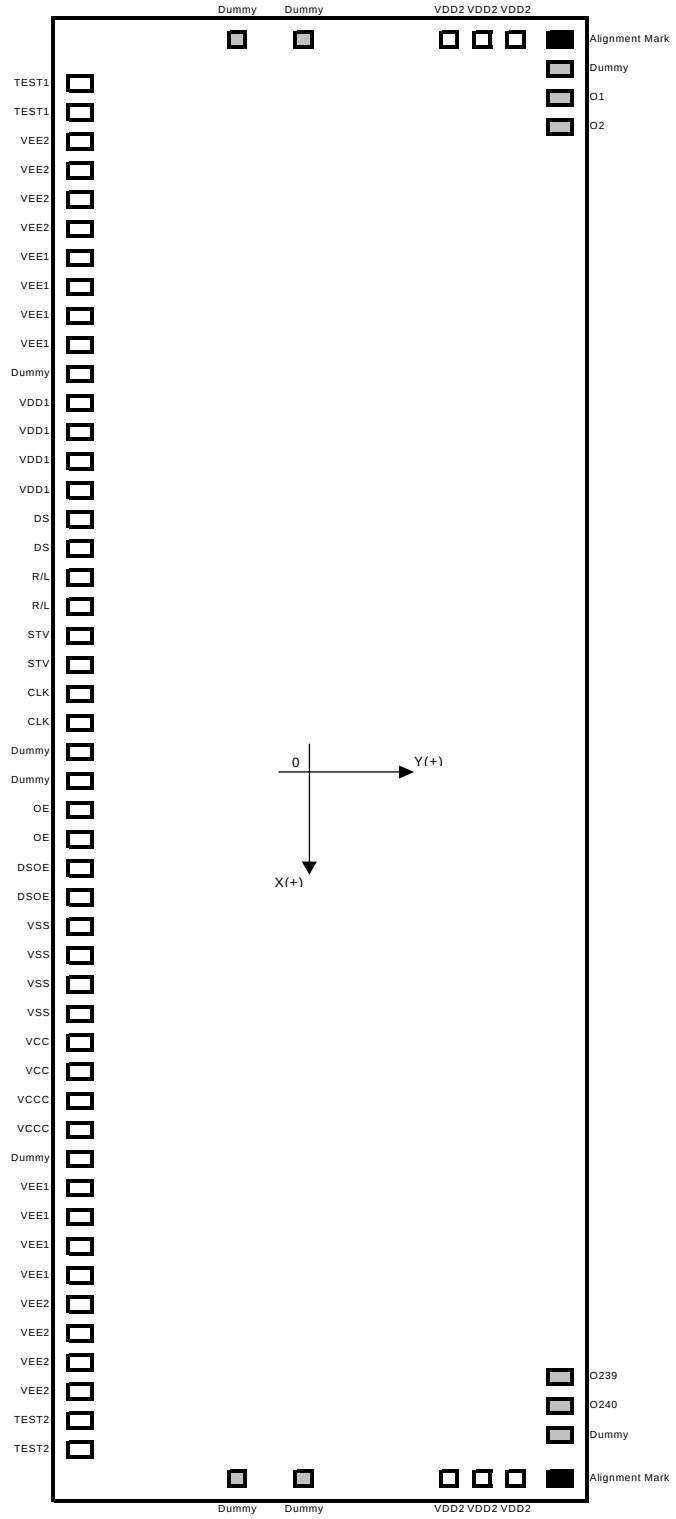


Note LS1: shifts CMOS level and internal level, LS2: shifts interval level and output level (V_{DD2} to V_{EE2}).

Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (IC Pad Surface)

Chip Size: 1.06 x 15.39 mm^2



- Bump size

  : 40 x 80 μm^2

  : 110 x 60 μm^2

- Alignment

  : 50 x 50 μm^2

Alignment Mark Coordinate (Unit: mm):
(7570, 405) , (–7570, 405)

Remark This figure does not specify the TCP package.

Figure 2–1. Pad Coordinate (1/3)

No	PAD Name	X[μm]	Y[μm]	Bump size (X:Y)[μm]
1	TEST1	-7061.8	-375.0	110:60
2	TEST1	-6931.8	-375.0	110:60
3	V_{EE2}	-6801.8	-375.0	110:60
4	V_{EE2}	-6671.8	-375.0	110:60
5	V_{EE2}	-6541.8	-375.0	110:60
6	V_{EE2}	-6411.8	-375.0	110:60
7	V_{EE1}	-6193.8	-375.0	110:60
8	V_{EE1}	-6063.8	-375.0	110:60
9	V_{EE1}	-5933.8	-375.0	110:60
10	V_{EE1}	-5803.8	-375.0	110:60
11	DUMMY	-5673.8	-375.0	110:60
12	V_{DD1}	-5490.8	-375.0	110:60
13	V_{DD1}	-5360.8	-375.0	110:60
14	V_{DD1}	-4999.0	-375.0	110:60
15	V_{DD1}	-4450.2	-375.0	110:60
16	DS	-4120.4	-375.0	110:60
17	DS	-3809.4	-375.0	110:60
18	RL	-3362.4	-375.0	110:60
19	RL	-2924.2	-375.0	110:60
20	STV	-2280.2	-375.0	110:60
21	STV	-1969.2	-375.0	110:60
22	CLK	-1522.2	-375.0	110:60
23	CLK	-1084.0	-375.0	110:60
24	DUMMY	-440.0	-375.0	110:60
25	DUMMY	182.2	-375.0	110:60
26	OE	826.2	-375.0	110:60
27	OE	1264.4	-375.0	110:60
28	DSOE	1711.4	-375.0	110:60
29	DSOE	2022.4	-375.0	110:60
30	V_{SS}	2194.2	-375.0	110:60
31	V_{SS}	2564.8	-375.0	110:60
32	V_{SS}	2926.6	-375.0	110:60
33	V_{SS}	3056.6	-375.0	110:60
34	VCC	3433.4	-375.0	110:60
35	VCC	4073.4	-375.0	110:60
36	VCCC	4450.2	-375.0	110:60
37	VCCC	5090.2	-375.0	110:60
38	DUMMY	5691.8	-375.0	110:60
39	V_{EE1}	5821.8	-375.0	110:60
40	V_{EE1}	5951.8	-375.0	110:60
41	V_{EE1}	6081.8	-375.0	110:60
42	V_{EE1}	6211.8	-375.0	110:60
43	V_{EE2}	6429.8	-375.0	110:60
44	V_{EE2}	6559.8	-375.0	110:60
45	V_{EE2}	6689.8	-375.0	110:60
46	V_{EE2}	6819.8	-375.0	110:60
47	TEST2	6949.8	-375.0	110:60
48	TEST2	7079.8	-375.0	110:60
49	DUMMY	7556.0	-220.0	80:40
50	DUMMY	7556.0	-80.0	80:40

No	PAD Name	X[μm]	Y[μm]	Bump size (X:Y)[μm]
51	V_{DD2}	7556.0	136.0	110:60
52	V_{DD2}	7556.0	216.0	110:60
53	V_{DD2}	7556.0	296.0	110:60
54	DUMMY	7200.0	310.5	40:80
55	O_{240}	7140.0	310.5	40:80
56	O_{239}	7080.0	310.5	40:80
57	O_{238}	7020.0	310.5	40:80
58	O_{237}	6960.0	310.5	40:80
59	O_{236}	6900.0	310.5	40:80
60	O_{235}	6840.0	310.5	40:80
61	O_{234}	6780.0	310.5	40:80
62	O_{233}	6720.0	310.5	40:80
63	O_{232}	6660.0	310.5	40:80
64	O_{231}	6600.0	310.5	40:80
65	O_{230}	6540.0	310.5	40:80
66	O_{229}	6480.0	310.5	40:80
67	O_{228}	6420.0	310.5	40:80
68	O_{227}	6360.0	310.5	40:80
69	O_{226}	6300.0	310.5	40:80
70	O_{225}	6240.0	310.5	40:80
71	O_{224}	6180.0	310.5	40:80
72	O_{223}	6120.0	310.5	40:80
73	O_{222}	6060.0	310.5	40:80
74	O_{221}	6000.0	310.5	40:80
75	O_{220}	5940.0	310.5	40:80
76	O_{219}	5880.0	310.5	40:80
77	O_{218}	5820.0	310.5	40:80
78	O_{217}	5760.0	310.5	40:80
79	O_{216}	5700.0	310.5	40:80
80	O_{215}	5640.0	310.5	40:80
81	O_{214}	5580.0	310.5	40:80
82	O_{213}	5520.0	310.5	40:80
83	O_{212}	5460.0	310.5	40:80
84	O_{211}	5400.0	310.5	40:80
85	O_{210}	5340.0	310.5	40:80
86	O_{209}	5280.0	310.5	40:80
87	O_{208}	5220.0	310.5	40:80
88	O_{207}	5160.0	310.5	40:80
89	O_{206}	5100.0	310.5	40:80
90	O_{205}	5040.0	310.5	40:80
91	O_{204}	4980.0	310.5	40:80
92	O_{203}	4920.0	310.5	40:80
93	O_{202}	4860.0	310.5	40:80
94	O_{201}	4800.0	310.5	40:80
95	O_{200}	4740.0	310.5	40:80
96	O_{199}	4680.0	310.5	40:80
97	O_{198}	4620.0	310.5	40:80
98	O_{197}	4560.0	310.5	40:80
99	O_{196}	4500.0	310.5	40:80
100	O_{195}	4440.0	310.5	40:80

Figure 2–1. Pad Coordinate (2/3)

No	PAD Name	X[um]	Y[um]	Bump size (X:Y)[um]
101	O_{194}	4380.0	310.5	40:80
102	O_{193}	4320.0	310.5	40:80
103	O_{192}	4260.0	310.5	40:80
104	O_{191}	4200.0	310.5	40:80
105	O_{190}	4140.0	310.5	40:80
106	O_{189}	4080.0	310.5	40:80
107	O_{188}	4020.0	310.5	40:80
108	O_{187}	3960.0	310.5	40:80
109	O_{186}	3900.0	310.5	40:80
110	O_{185}	3840.0	310.5	40:80
111	O_{184}	3780.0	310.5	40:80
112	O_{183}	3720.0	310.5	40:80
113	O_{182}	3660.0	310.5	40:80
114	O_{181}	3600.0	310.5	40:80
115	O_{180}	3540.0	310.5	40:80
116	O_{179}	3480.0	310.5	40:80
117	O_{178}	3420.0	310.5	40:80
118	O_{177}	3360.0	310.5	40:80
119	O_{176}	3300.0	310.5	40:80
120	O_{175}	3240.0	310.5	40:80
121	O_{174}	3180.0	310.5	40:80
122	O_{173}	3120.0	310.5	40:80
123	O_{172}	3060.0	310.5	40:80
124	O_{171}	3000.0	310.5	40:80
125	O_{170}	2940.0	310.5	40:80
126	O_{169}	2880.0	310.5	40:80
127	O_{168}	2820.0	310.5	40:80
128	O_{167}	2760.0	310.5	40:80
129	O_{166}	2700.0	310.5	40:80
130	O_{165}	2640.0	310.5	40:80
131	O_{164}	2580.0	310.5	40:80
132	O_{163}	2520.0	310.5	40:80
133	O_{162}	2460.0	310.5	40:80
134	O_{161}	2400.0	310.5	40:80
135	O_{160}	2340.0	310.5	40:80
136	O_{159}	2280.0	310.5	40:80
137	O_{158}	2220.0	310.5	40:80
138	O_{157}	2160.0	310.5	40:80
139	O_{156}	2100.0	310.5	40:80
140	O_{155}	2040.0	310.5	40:80
141	O_{154}	1980.0	310.5	40:80
142	O_{153}	1920.0	310.5	40:80
143	O_{152}	1860.0	310.5	40:80
144	O_{151}	1800.0	310.5	40:80
145	O_{150}	1740.0	310.5	40:80
146	O_{149}	1680.0	310.5	40:80
147	O_{148}	1620.0	310.5	40:80
148	O_{147}	1560.0	310.5	40:80
149	O_{146}	1500.0	310.5	40:80
150	O_{145}	1440.0	310.5	40:80

No	PAD Name	X[μm]	Y[μm]	Bump size (X:Y)[μm]
151	O_{144}	1380.0	310.5	40:80
152	O_{143}	1320.0	310.5	40:80
153	O_{142}	1260.0	310.5	40:80
154	O_{141}	1200.0	310.5	40:80
155	O_{140}	1140.0	310.5	40:80
156	O_{139}	1080.0	310.5	40:80
157	O_{138}	1020.0	310.5	40:80
158	O_{137}	960.0	310.5	40:80
159	O_{136}	900.0	310.5	40:80
160	O_{135}	840.0	310.5	40:80
161	O_{134}	780.0	310.5	40:80
162	O_{133}	720.0	310.5	40:80
163	O_{132}	660.0	310.5	40:80
164	O_{131}	600.0	310.5	40:80
165	O_{130}	540.0	310.5	40:80
166	O_{129}	480.0	310.5	40:80
167	O_{128}	420.0	310.5	40:80
168	O_{127}	360.0	310.5	40:80
169	O_{126}	300.0	310.5	40:80
170	O_{125}	240.0	310.5	40:80
171	O_{124}	180.0	310.5	40:80
172	O_{123}	120.0	310.5	40:80
173	O_{122}	60.0	310.5	40:80
174	O_{121}	0.0	310.5	40:80
175	O_{120}	-60.0	310.5	40:80
176	O_{119}	-120.0	310.5	40:80
177	O_{118}	-180.0	310.5	40:80
178	O_{117}	-240.0	310.5	40:80
179	O_{116}	-300.0	310.5	40:80
180	O_{115}	-360.0	310.5	40:80
181	O_{114}	-420.0	310.5	40:80
182	O_{113}	-480.0	310.5	40:80
183	O_{112}	-540.0	310.5	40:80
184	O_{111}	-600.0	310.5	40:80
185	O_{110}	-660.0	310.5	40:80
186	O_{109}	-720.0	310.5	40:80
187	O_{108}	-780.0	310.5	40:80
188	O_{107}	-840.0	310.5	40:80
189	O_{106}	-900.0	310.5	40:80
190	O_{105}	-960.0	310.5	40:80
191	O_{104}	-1020.0	310.5	40:80
192	O_{103}	-1080.0	310.5	40:80
193	O_{102}	-1140.0	310.5	40:80
194	O_{101}	-1200.0	310.5	40:80
195	O_{100}	-1260.0	310.5	40:80
196	O_{99}	-1320.0	310.5	40:80
197	O_{98}	-1380.0	310.5	40:80
198	O_{97}	-1440.0	310.5	40:80
199	O_{96}	-1500.0	310.5	40:80
200	O_{95}	-1560.0	310.5	40:80

Figure 2–1. Pad Coordinate (3/3)

No	PAD Name	X[μm]	Y[μm]	Bump size (X:Y)[μm]
201	O_{94}	-1620.0	310.5	40:80
202	O_{93}	-1680.0	310.5	40:80
203	O_{92}	-1740.0	310.5	40:80
204	O_{91}	-1800.0	310.5	40:80
205	O_{90}	-1860.0	310.5	40:80
206	O_{89}	-1920.0	310.5	40:80
207	O_{88}	-1980.0	310.5	40:80
208	O_{87}	-2040.0	310.5	40:80
209	O_{86}	-2100.0	310.5	40:80
210	O_{85}	-2160.0	310.5	40:80
211	O_{84}	-2220.0	310.5	40:80
212	O_{83}	-2280.0	310.5	40:80
213	O_{82}	-2340.0	310.5	40:80
214	O_{81}	-2400.0	310.5	40:80
215	O_{80}	-2460.0	310.5	40:80
216	O_{79}	-2520.0	310.5	40:80
217	O_{78}	-2580.0	310.5	40:80
218	O_{77}	-2640.0	310.5	40:80
219	O_{76}	-2700.0	310.5	40:80
220	O_{75}	-2760.0	310.5	40:80
221	O_{74}	-2820.0	310.5	40:80
222	O_{73}	-2880.0	310.5	40:80
223	O_{72}	-2940.0	310.5	40:80
224	O_{71}	-3000.0	310.5	40:80
225	O_{70}	-3060.0	310.5	40:80
226	O_{69}	-3120.0	310.5	40:80
227	O_{68}	-3180.0	310.5	40:80
228	O_{67}	-3240.0	310.5	40:80
229	O_{66}	-3300.0	310.5	40:80
230	O_{65}	-3360.0	310.5	40:80
231	O_{64}	-3420.0	310.5	40:80
232	O_{63}	-3480.0	310.5	40:80
233	O_{62}	-3540.0	310.5	40:80
234	O_{61}	-3600.0	310.5	40:80
235	O_{60}	-3660.0	310.5	40:80
236	O_{59}	-3720.0	310.5	40:80
237	O_{58}	-3780.0	310.5	40:80
238	O_{57}	-3840.0	310.5	40:80
239	O_{56}	-3900.0	310.5	40:80
240	O_{55}	-3960.0	310.5	40:80
241	O_{54}	-4020.0	310.5	40:80
242	O_{53}	-4080.0	310.5	40:80
243	O_{52}	-4140.0	310.5	40:80
244	O_{51}	-4200.0	310.5	40:80
245	O_{50}	-4260.0	310.5	40:80
246	O_{49}	-4320.0	310.5	40:80
247	O_{48}	-4380.0	310.5	40:80
248	O_{47}	-4440.0	310.5	40:80
249	O_{46}	-4500.0	310.5	40:80
250	O_{45}	-4560.0	310.5	40:80

No	PAD Name	X[μm]	Y[μm]	Bump size (X:Y)[μm]
251	O_{44}	-4620.0	310.5	40:80
252	O_{43}	-4680.0	310.5	40:80
253	O_{42}	-4740.0	310.5	40:80
254	O_{41}	-4800.0	310.5	40:80
255	O_{40}	-4860.0	310.5	40:80
256	O_{39}	-4920.0	310.5	40:80
257	O_{38}	-4980.0	310.5	40:80
258	O_{37}	-5040.0	310.5	40:80
259	O_{36}	-5100.0	310.5	40:80
260	O_{35}	-5160.0	310.5	40:80
261	O_{34}	-5220.0	310.5	40:80
262	O_{33}	-5280.0	310.5	40:80
263	O_{32}	-5340.0	310.5	40:80
264	O_{31}	-5400.0	310.5	40:80
265	O_{30}	-5460.0	310.5	40:80
266	O_{29}	-5520.0	310.5	40:80
267	O_{28}	-5580.0	310.5	40:80
268	O_{27}	-5640.0	310.5	40:80
269	O_{26}	-5700.0	310.5	40:80
270	O_{25}	-5760.0	310.5	40:80
271	O_{24}	-5820.0	310.5	40:80
272	O_{23}	-5880.0	310.5	40:80
273	O_{22}	-5940.0	310.5	40:80
274	O_{21}	-6000.0	310.5	40:80
275	O_{20}	-6060.0	310.5	40:80
276	O_{19}	-6120.0	310.5	40:80
277	O_{18}	-6180.0	310.5	40:80
278	O_{17}	-6240.0	310.5	40:80
279	O_{16}	-6300.0	310.5	40:80
280	O_{15}	-6360.0	310.5	40:80
281	O_{14}	-6420.0	310.5	40:80
282	O_{13}	-6480.0	310.5	40:80
283	O_{12}	-6540.0	310.5	40:80
284	O_{11}	-6600.0	310.5	40:80
285	O_{10}	-6660.0	310.5	40:80
286	O_9	-6720.0	310.5	40:80
287	O_8	-6780.0	310.5	40:80
288	O_7	-6840.0	310.5	40:80
289	O_6	-6900.0	310.5	40:80
290	O_5	-6960.0	310.5	40:80
291	O_4	-7020.0	310.5	40:80
292	O_3	-7080.0	310.5	40:80
293	O_2	-7140.0	310.5	40:80
294	O_1	-7200.0	310.5	40:80
295	DUMMY	-7260.0	310.5	40:80
296	V_{DD2}	-7556.0	296.0	110:60
297	V_{DD2}	-7556.0	216.0	110:60
298	V_{DD2}	-7556.0	136.0	110:60
299	DUMMY	-7556.0	-80.0	80:40
300	DUMMY	-7556.0	-220.0	80:40

3. PIN FUNCTIONS

(1/2)

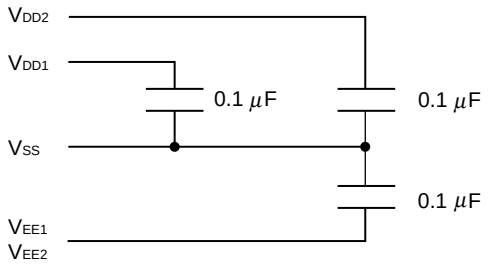
Pin Symbol	Pin Name	Pad No	I/O	Description
O_1 to O_{240}	Driver output	294 - 55	Output	These pins output scan signals that drive the vertical direction (gate lines) of a TFT-LCD. The output signals change in synchronization with the rising edge of shift clock CLK. The driver output amplitude is V_{DD2} to V_{EE2}.
R,/L	Shift direction select input	18, 19	Input	R,/L = H (right shift) : STV → O_1 → O_{240} R,/L = L (left shift) : STV → O_{240} → O_1
STV	Start pulse input/output	20, 21	I/O	This is the input of the internal shift register. The start pulse is written at the rising edge of shift clock CLK. The pulse range is less than one cycle of CLK. The input level is a V_{DD1} to V_{SS} (logic level).
CLK	Shift clock input	22, 23	Input	This pin inputs a shift clock to the internal shift register. The shift operation is performed in synchronization with the rising edge of this input.
OE	Output enable input	26, 27	Input	When this pin goes low level, the driver output is fixed to V_{EE2} level. The shift register is not cleared. Refer to **4. TIMING CHART** for details.
DS	Double scan control input	16, 17	Input	This pin outputs scan signals simultaneously from two outputs in synchronization with the rise of CLK when DS = H is written. Refer to **4. TIMING CHART** for details.
DSOE	Double scan pulse width control input	28, 29	Input	This pin controls the fall timing of one of the scan signals (the output side in normal scan mode) when the DS signal is used to output scan signals simultaneously from two outputs. This signal is input asynchronously to the clock. Refer to **4. TIMING CHART** for details.
VCC, VCCC	IC internal reference voltage	34, 35, 36, 37	–	Short the VCC pin to the VCCC pin so that these pins are in a floating state.
TEST1, TEST2	TEST pins	1, 2, 47, 48	–	Short TEST1 and TEST2 separately inside the IC. These pins are not connected to any other pins inside the IC.
Dummy	Dummy pin	11, 24, 25, 38, 49, 50, 54, 295, 299, 300	–	No dummy pins are connected to any other pins inside the IC.
V_{DD1}	Logic power supply	12 - 15	–	3.3 ± 0.3 V
V_{DD2}	Driver positive power supply	51 - 53, 296 - 298	–	15 to 25 V The driver output: high level

(2/2)

Pin Symbol	Pin Name	Pad No	I/O	Description
V_{SS}	Logic ground	30 - 33	–	Connect this pin to the ground of the system.
V_{EE1}	Negative power supply for internal operation	7 - 10, 39 - 42	–	–15 to –5 V
V_{EE2}	Driver negative power supply	3 - 6, 43 - 46	–	The driver output: low level (V_{EE2} to V_{EE1} < 6.0 V)

Cautions 1. To prevent latch-up, turn on power to V_{DD1}, V_{EE1}, V_{EE2}, V_{DD2}, and logic input in this order. Turn off power in the reverse order. These power up/down sequence must be observed also during transition period.

2. Insert a capacitor of about 0.1 μF between each power line, as shown below, to secure noise margin such as V_{IH} and V_{IL}.

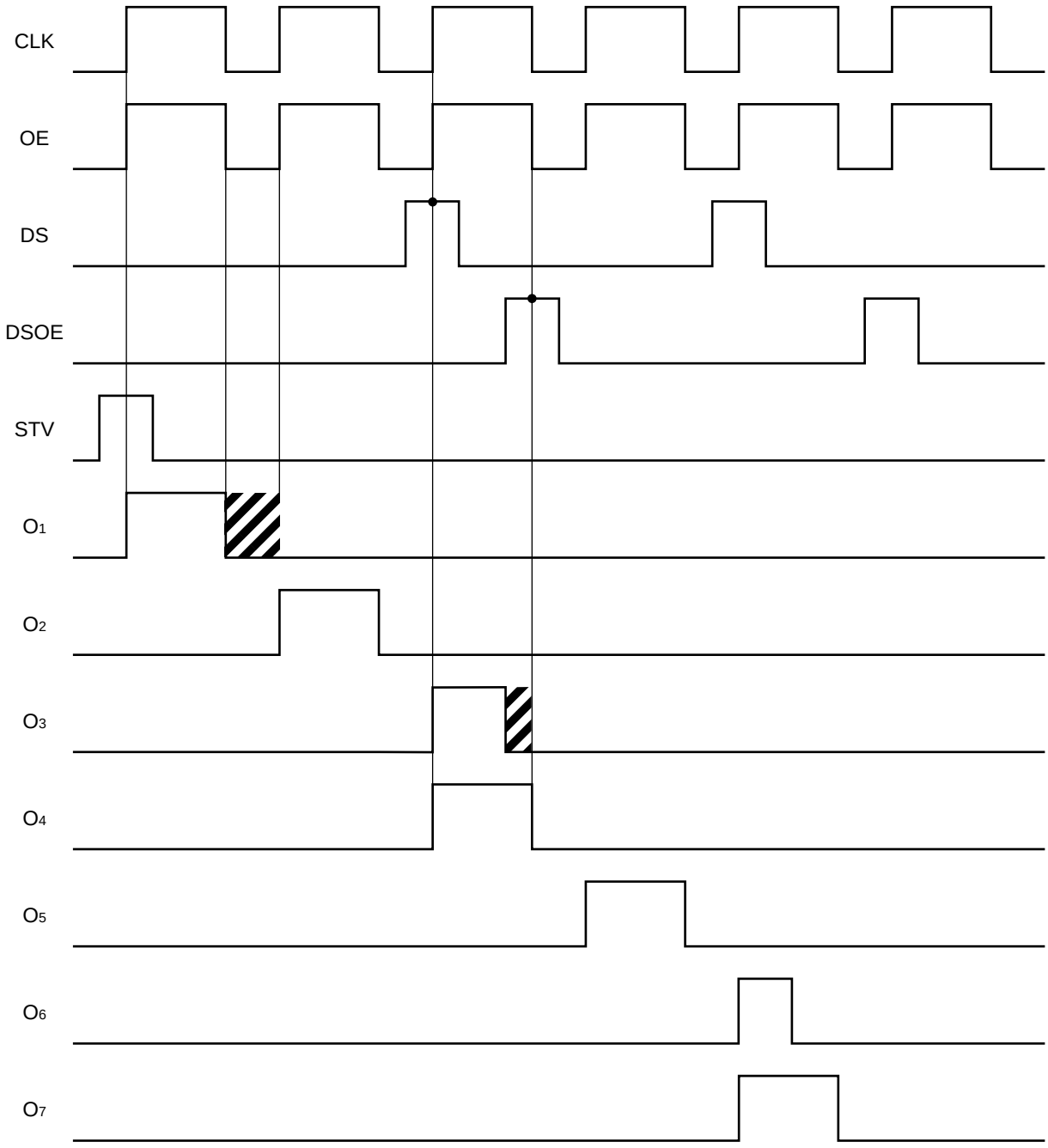


4. TIMING CHART (R,/L = H)

As shown in the figure below, when DS = H, scan signals are output successively from two outputs in synchronization with the rise of CLK (double scan operation).

It is also possible to accelerate the fall timing of one of the scan signals (the output side in normal scan mode) in a double scan operation by using the DSOE signal. DSOE is input asynchronously to the clock, and the output is fixed to V_{EE2} in the period between the rise of DSOE and the rise of CLK.

The DSOE signal is only enabled during a double scan operation.



5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{DD1}	–0.5 to +7.0	V
Driver Positive Supply Voltage	V_{DD2}	–0.5 to +28	V
Power Supply Voltage	V_{DD2} to V_{EE1}, V_{EE2}	–0.5 to +42	V
Internal Operation Negative Supply Voltage	V_{EE1}	–16 to + 0.5	V
Driver Negative Supply Voltage	V_{EE2}	V_{EE1} – 0.3 to V_{EE1} + 7.0	V
Input Voltage	V_I	–0.5 to V_{DD1} + 0.5	V
Operating Ambient Temperature	T_A	–30 to +85	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Caution Product qualify may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –30 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V_{DD1}	3.0	3.3	3.6	V
Driver Positive Supply Voltage	V_{DD2}	15	23	25	V
Internal Operation Negative Supply Voltage	V_{EE1}	–15	–10	–5.0	V
Power Supply Voltage	V_{DD2} to V_{EE1}	20	33	40	V
	V_{EE2} to V_{EE1}	0		6.0	V
Clock Frequency	f_{CLK}			500	kHz

Electrical Characteristics (T_A = –30 to +85°C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 23 V, V_{EE1} = V_{EE2} = –10 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level Input Voltage	V_{IH}	CLK, STV, R,/L, OE	0.8 V_{DD1}		V_{DD1}	V
Low-level Input Voltage	V_{IL}		V_{SS}		0.2 V_{DD1}	V
LCD Driver Output ON Resistance	R_{ON}	V_{OUT} = V_{EE2} + 1.0 V, or V_{DD2} – 1.0 V			2.0	kΩ
Input Leak Current	I_{IL}	V_I = 0 V or 3.6 V,			±1.0	μA
Dynamic Current Dissipation	I_{DD1}	V_{DD1}, f_{CLK} = 50 kHz, f_{STV} = 60 Hz, No load			1000	μA
	I_{DD2}	V_{DD2}, f_{CLK} = 50 kHz, f_{STV} = 60 Hz, No load			100	μA
	I_{EE}	V_{EE1}, f_{CLK} = 50 kHz, f_{STV} = 60 Hz, No load	–1000			μA

Switching Characteristics (T_A = –30 to +85°C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 23 V, V_{EE1} = V_{EE2} = –10 V, V_{SS} = 0 V)

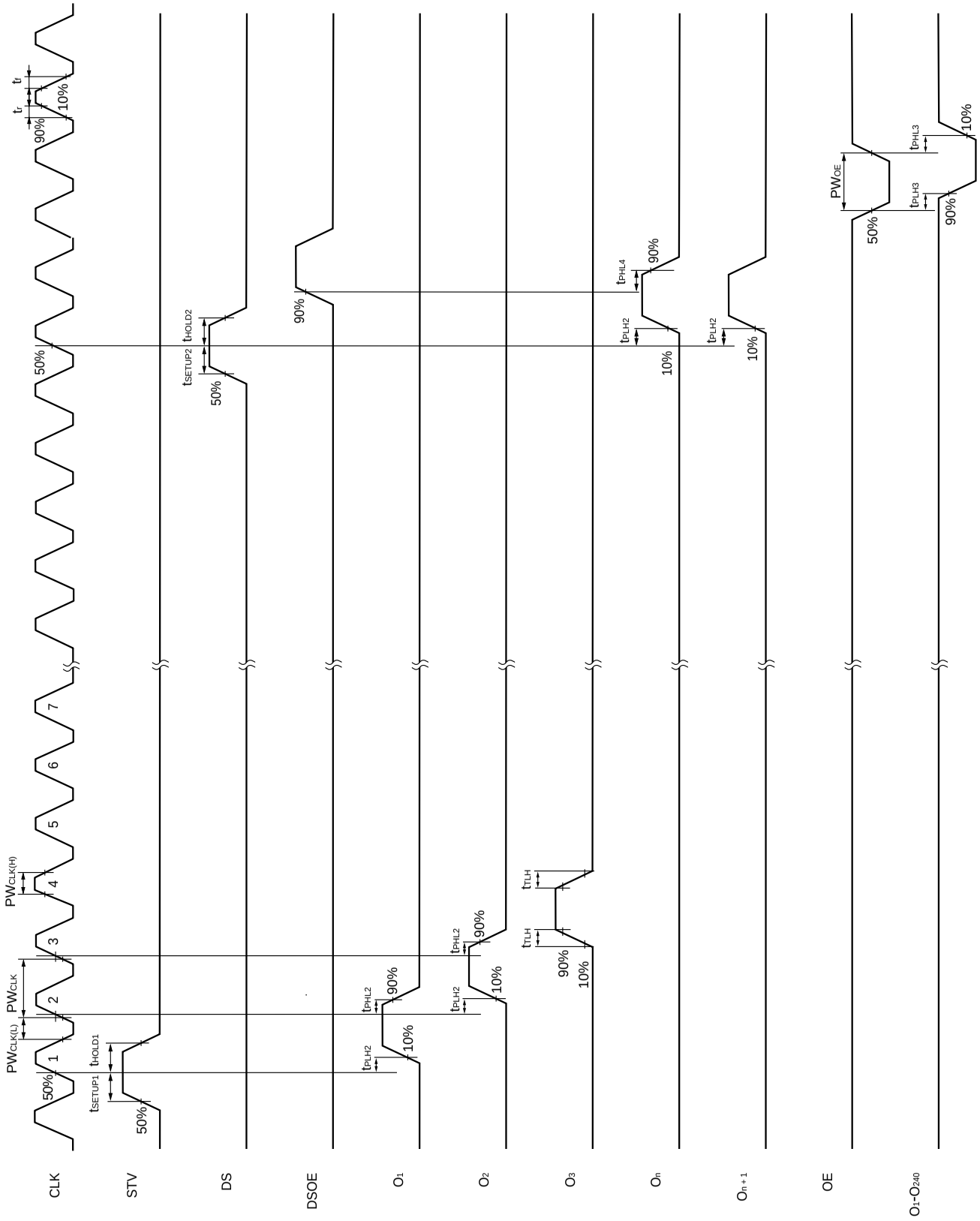
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Driver Output Delay Time	t_{PHL2}	C_L = 300 pF, CLK → O_n			800	ns
	t_{PLH2}				800	ns
	t_{PHL3}	C_L = 300 pF, OE → O_n			800	ns
	t_{PLH3}				800	ns
DSOE	t_{PHL4}				800	ns
Output Rise Time	t_{TLH}	C_L = 300 pF			1500	ns
Output Fall Time	t_{THL}				1500	ns
Input Capacitance	C_I	T_A = 25°C			15	pF

Timing Requirements (T_A = –30 to +85°C, V_{DD1} = 3.3 V ±0.3 V, V_{DD2} = 23 V, V_{EE1} = V_{EE2} = –10 V, V_{SS} = 0 V, t_r = t_f =20 ns (10 to 90%))

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse High Width	$PW_{CLK(H)}$		500			ns
Clock Pulse Low Width	$PW_{CLK(L)}$		500			ns
Enable Pulse Width	PW_{OE}	OE	1000			ns
Start Pulse Setup Time	t_{SETUP1}	STV ↑ → CLK ↑	200			ns
Start Pulse Hold Time	t_{HOLD1}	CLK ↑ → STV ↓	200			ns
Double Scan Setup Time	t_{SETUP2}	DS ↑ → CLK ↑	200			ns
Double Scan Hold Time	t_{HOLD2}	CLK ↑ → DS ↓	200			ns

Remark Unless otherwise specified, the input level is defined to be V_{IH} = 0.8 V_{DD1}, V_{IL} = 0.2 V_{DD1}.

Switching Characteristics Waveform (R,/L= H)



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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