

BSW841



SPDT Switch

DC~4GHz Wide Band Single Pole Double Throw Switch

Device Features

- Typical Isolation = 43.0 dB @ 2GHz
- Typical Insertion Loss = 0.6 dB @ 1GHz
- MSL 1, MSOP 8, Lead-free / Green / RoHS compliant
- Commercial, Industrial, Military wireless system, RFID



Product Description

BeRex's SPDT(Wide Band Single Pole Double Throw) Switch BSW841 is designed for Cellular & GSM band with low Insertion Loss and Isolation. This chip is fully passivated for enhanced performance and reliability and packaged in RoHS-compliant with MSOP8 surface mount package.

It must be used with back side ground soldering.

Typical Performance

Parameter	Frequency	Min	Typical	Max	Unit	Remark
Insertion Loss	DC ~ 1 GHz		0.6		MHz	
	DC ~ 2 GHz		0.7			
	DC ~ 3 GHz		0.8			
	DC ~ 4 GHz		0.9			
Isolation	DC ~ 1 GHz		50.1/51.5		dB	RF1/RF2
	DC ~ 2 GHz		43.5/45.0			
	DC ~ 3 GHz		33.0/34.0			
	DC ~ 4 GHz		27.0/27.5			
Return Loss / On State	DC ~ 1 GHz		26.0		dB	
	DC ~ 2 GHz		21.0			
	DC ~ 3 GHz		23.5			
	DC ~ 4 GHz		16.0			
Return Loss / Off State	0.5 ~ 4 GHz		17.0		dB	
Input P1 dB	DC ~ 1 GHz		24.0		dBm	
	DC ~ 2 GHz		23.0			
	DC ~ 3 GHz		22.0			
	DC ~ 4 GHz		22.0			
Input IP3	DC ~ 1 GHz		47.0		dBm	Two-Tone Input Power_5dBm/tone
	DC ~ 2 GHz		48.0			
	DC ~ 3 GHz		47.0			
	DC ~ 4 GHz		46.0			
Switching Speed	DC ~ 4 GHz		40		ns	tRISE, tFALL (10/90%RF) tON, tOFF(50%CTL to 10/90%RF)
	DC ~ 4 GHz		60			

Device performance _ measured on BeRex E/B at 25°C, 50ohm system, Vctl=0/+5Vdc, DC Blocks _ required each port.

Absolute Maximum Ratings

Parameter	Rating
Input Power	1W CW dBm
Storage Temperature	-55 to +155°C
Operating Temperature	-40 to +85°C

Operation of this device above any of these parameters may result in permanent damage.

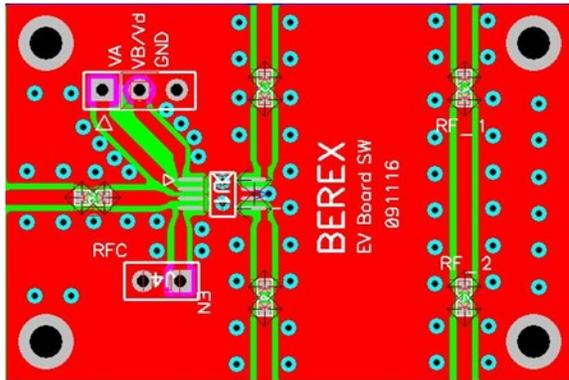
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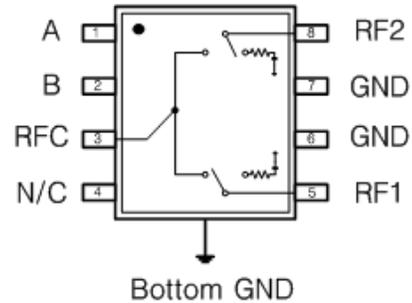
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Evaluation Board Drawing



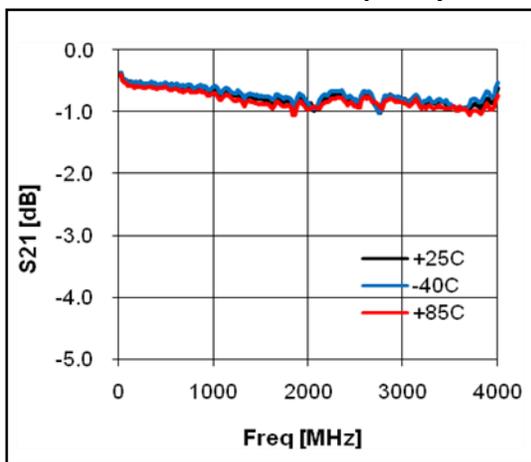
Function Block Diagram



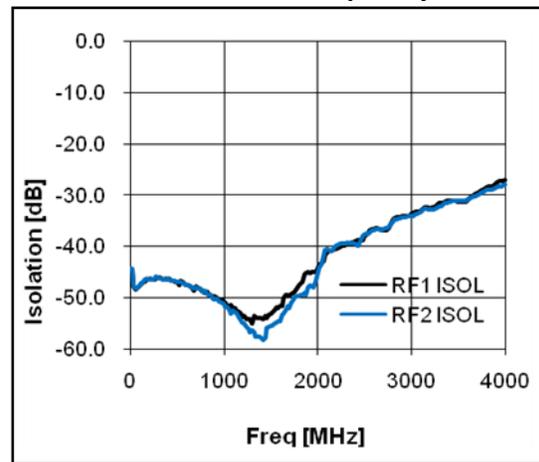
Pins 6, 7, Bottom Plate must be DC and RF grounded.

Typical Test Data

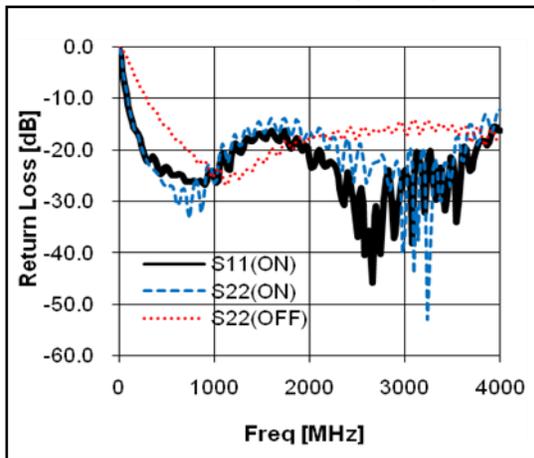
Insertion Loss vs. Frequency



Isolation vs. Frequency



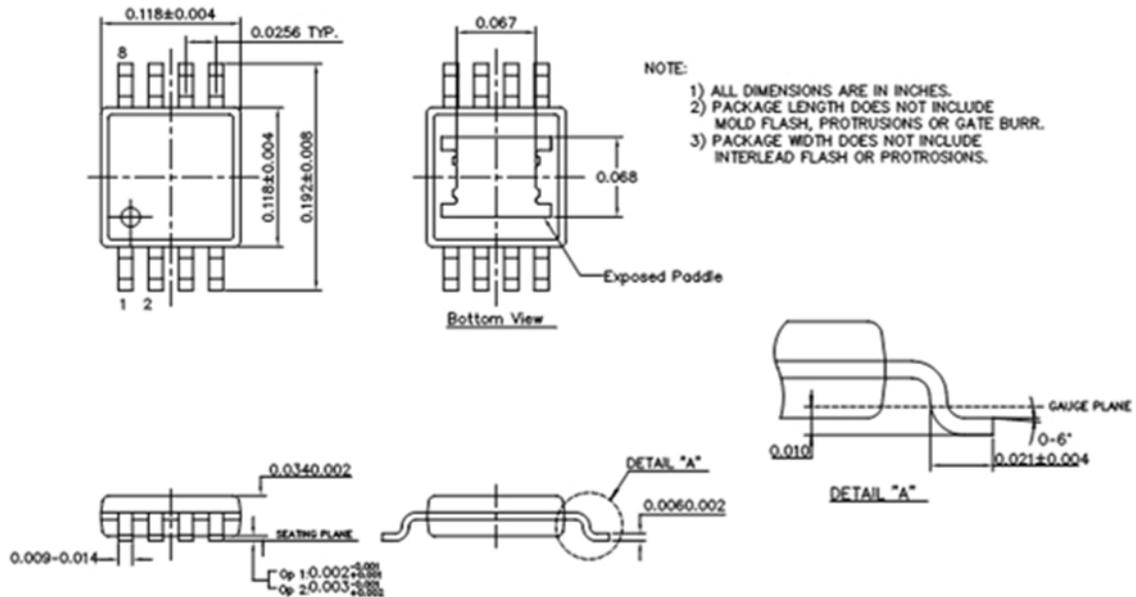
Return Loss vs. Frequency



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Package Outline Drawing

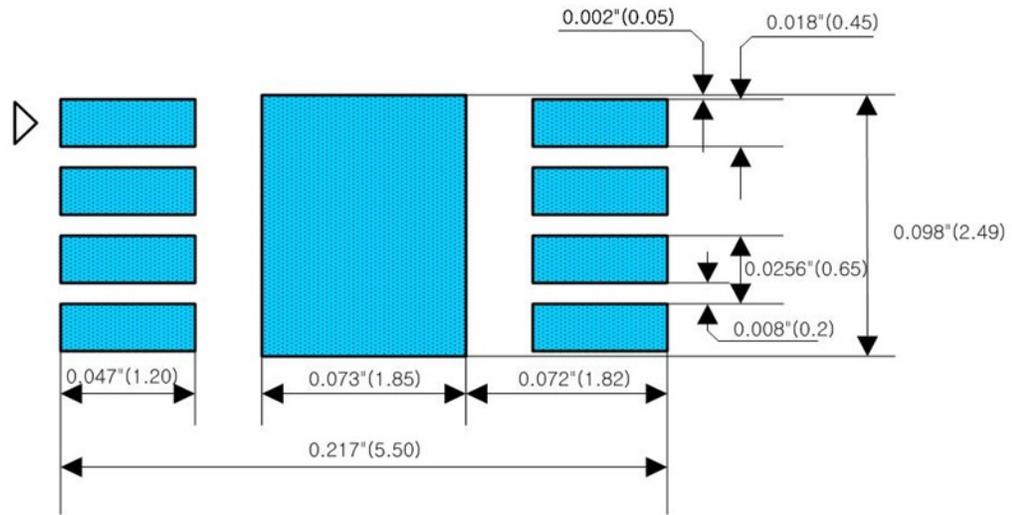


Truth Table

Control Voltage		Signal Path State	
A (Vdc)	B (Vdc)	RFC to RF1	RFC to RF2
0	+5	ON	OFF
+5	0	OFF	ON

Suggested PCB Land Pattern and PAD Layout

PCB Land Pattern



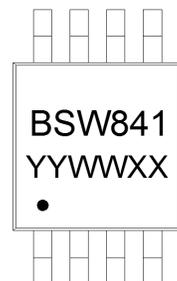
Note : 1. Connection to Bottom Ground with multiple via holes.

2. Via holes _ as many as possible.

3. All Dimensions _ millimeters.

4. PCB lay out _ on BeRex website.

Package Marking



Pin 1

YY = Year, WW = Working Week,
XX = Wafer No.

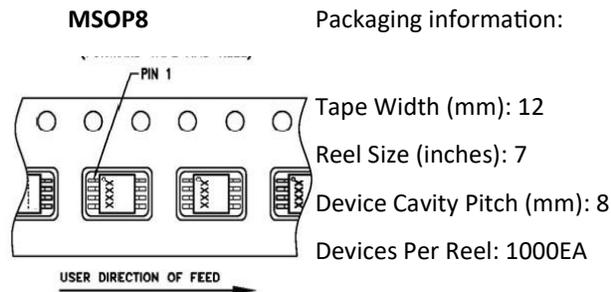
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Tape & Reel



Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating:	Class 1C
Value:	Passes <2000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114B
MSL Rating:	Level 1 at +265°C convection reflow
Standard:	JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling this device.

NATO CAGE code:

2	N	9	6	F
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