

Peak Reducing EMI Solution

Features

- Generates a 1x EMI optimized clock output.
- Input frequency: 6MHz - 10MHz
18MHz - 30MHz
- Output frequency: 6MHz - 10MHz
18MHz - 30MHz
- Two selectable down spread options.
- Selectable frequency range.
- Integrated loop filter components.
- Operates with a 3.3V supply.
- Low-power CMOS design.
- Commercial temperature range
- 8-pin SOIC and 8-pin TSSOP packages.

Product Description

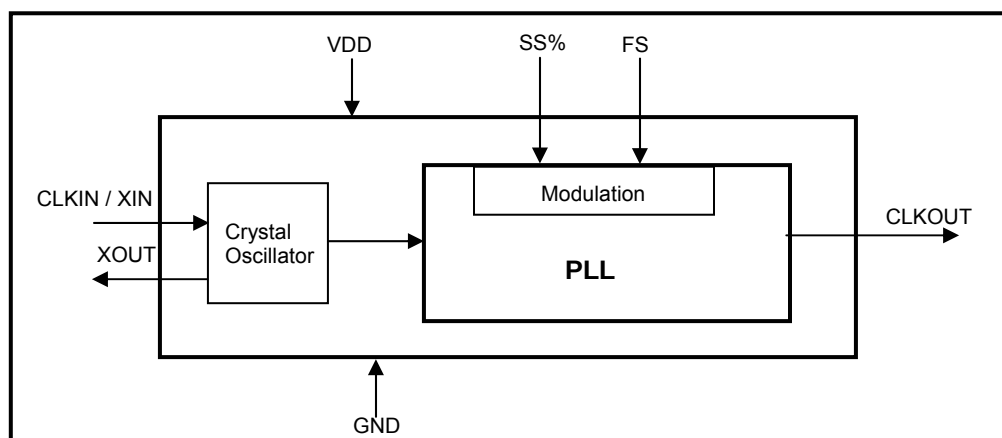
The ASM3P2180A is a versatile spread spectrum frequency modulator designed specifically for a wide range of clock frequencies. ASM3P2180A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream

clock and data dependent signals. ASM3P2180A allows significant system cost savings by reducing the number of circuit board layers, and shielding that are traditionally required to pass EMI regulations. ASM3P2180A modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, thereby decreasing the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal's bandwidth is called spread spectrum clock generation. ASM3P2180A uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all-digital method.

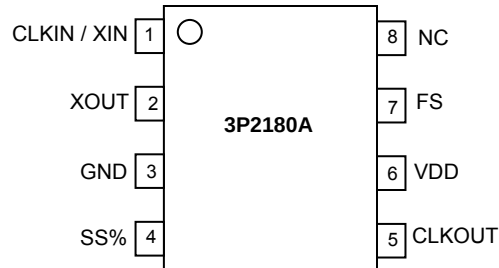
Applications

The ASM3P2180A is targeted towards notebook LCD displays, other displays using an LVDS interface, PC peripheral devices and embedded systems.

Block Diagram



Pin Diagram



Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN / XIN	I	Crystal connection or external reference clock input.
2	XOUT	O	Connection for an external crystal. If using an external reference, this pin must be left unconnected.
3	GND	P	Ground to entire chip.
4	SS%	I	Spread Selection Input. Has an internal pull-up resistor.
5	CLKOUT	O	Modulated Clock Output.
6	VDD	P	Power supply for the entire chip.
7	FS	I	Frequency selection bit. This pin selects the frequency range of operation. (Refer to the Frequency Range Selection Table). Has an internal pull-up resistor.
8	NC	-	No connect.

Frequency Range Selection

FS	Frequency Range (MHz)
0	6 -10
1	18-30

Spread Selection table

SS%	Frequency (MHz)		Deviation (%) (typ)
	FS=0	FS=1	
0	6	18	-2
	8	24	-1.5
	10	30	-1
1	6	18	-4
	8	24	-3
	10	30	-2

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD, VIN	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
TSTG	Storage temperature	-65 to +125	°C
Ts	Max. Soldering Temperature (10 sec)	260	°C
TJ	Junction Temperature	150	°C
TDV	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

DC Electrical Characteristics

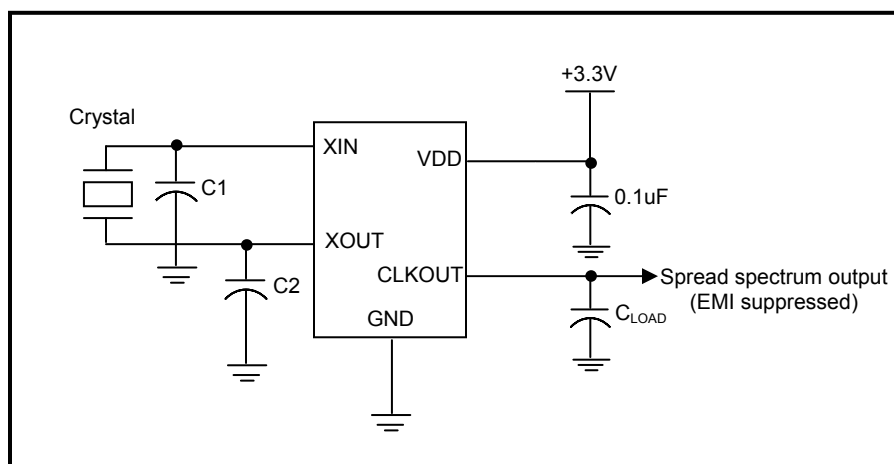
Symbol	Parameter	Min	Typ	Max	Unit
VIL	Input low voltage	GND – 0.3		0.8	V
VIH	Input high voltage	2.0		VDD + 0.3	V
IIL	Input low current (pull-up resistors on inputs SS%, FS)			-27	µA
IIH	Input high current			18	µA
IxOL	XOUT output low current (@ 0.4V, VDD = 3.3V)		3		mA
IxOH	XOUT output high current (@2.5V, VDD = 3.3V)		4		mA
VOL	Output low voltage (VDD = 3.3V, IOL = 4mA)			0.4	V
VOH	Output high voltage (VDD = 3.3V, IOH = 4mA)	2.5			V
ICC	Dynamic supply current normal mode (3.3V and 10pF loading)	10	15	25	mA
IDD *	Static supply current standby mode			7	mA
VDD	Operating voltage	2.8	3.3	3.7	V
tON	Power up time (first locked clock cycle after power up)		0.18		mS
ZOUT	Clock output impedance		50		Ω

*CLKIN pin pulled to GND

AC Electrical Characteristics

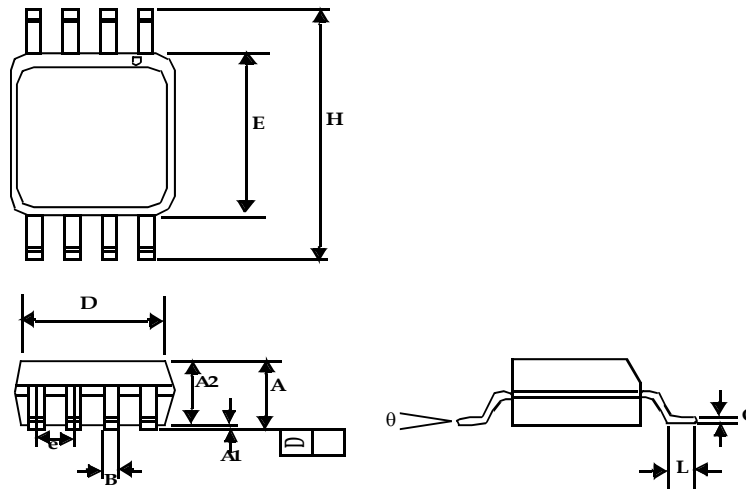
Symbol	Parameter		Min	Typ	Max	Unit
CLKIN	Input frequency	FS=0	6		10	MHz
		FS=1	18		30	
CLKOUT	Output frequency	FS=0	6		10	MHz
		FS=1	18		30	
t _{LH} *	Output rise time (measured at 0.8V to 2.0V)		1.2	1.3	1.4	nS
t _{HL} *	Output fall time (measured at 2.0V to 0.8V)		0.8	0.9	1.0	nS
t _{JC}	Jitter (cycle to cycle)			325		pS
t _D	Output duty cycle		45	50	55	%
*t _{LH} and t _{HL} are measured into a capacitive load of 15pF						

Typical Test Circuit



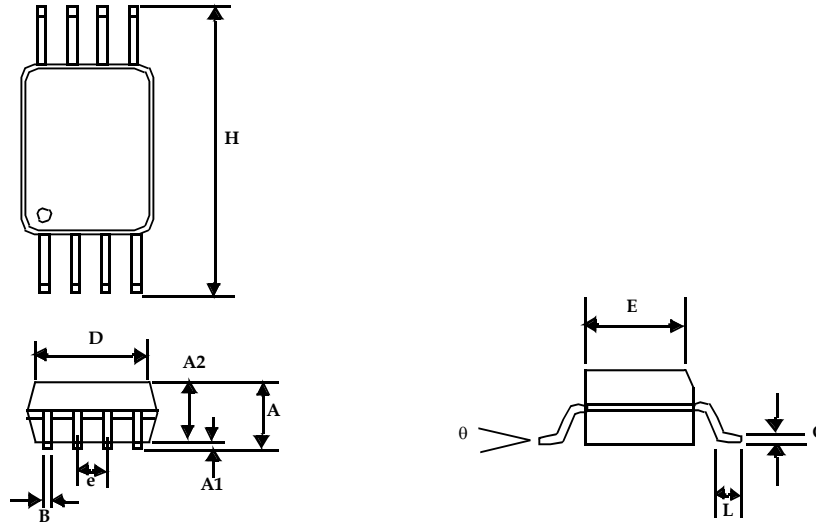
Package Information

8-Pin SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

8-Pin TSSOP Package

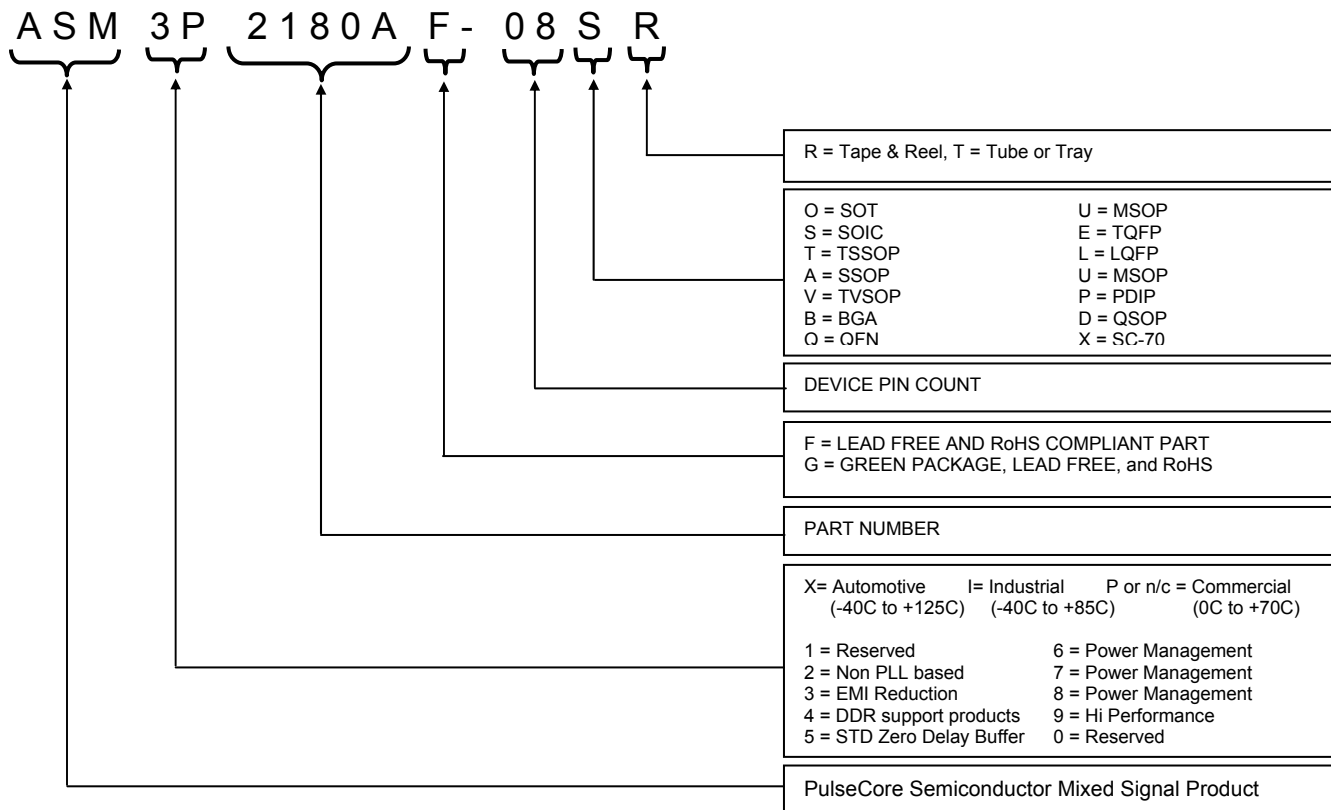


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

Ordering Codes

Part number	Marking	Package Type	Temperature
ASM3P2180AF-08ST	ASM3P2180AF	8-pin SOIC, tube, Pb Free	Commercial
ASM3P2180AF-08SR	ASM3P2180AF	8-pin SOIC, tape and reel, Pb Free	Commercial
ASM3P2180AF-08TT	ASM3P2180AF	8-pin TSSOP, tube, Pb Free	Commercial
ASM3P2180AF-08TR	ASM3P2180AF	8-pin TSSOP, tape and reel, Pb Free	Commercial
ASM3P2180AG-08ST	ASM3P2180AG	8-pin SOIC, tube, Green	Commercial
ASM3P2180AG-08SR	ASM3P2180AG	8-pin SOIC, tape and reel, Green	Commercial
ASM3P2180AG-08TT	ASM3P2180AG	8-pin TSSOP, tube, Green	Commercial
ASM3P2180AG-08TR	ASM3P2180AG	8-pin TSSOP, tape and reel, Green	Commercial

Device Ordering Information



Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.



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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003
Many PulseCore Semiconductor products are protected by issued patents or by applications for patent

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