LP87702-Q1 Dual Buck Converter and 5-V Boost With Diagnostic Functions

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
- Two High-Efficiency Step-Down DC-DC Regulators:
  - Maximum Output Current 3.5 A
  - Auto PWM/PFM and Forced-PWM Operations
  - Output Voltage = 0.7 V to 3.36 V
- 5-V Boost Regulator:
  - Maximum Output Current 600 mA
- 2-MHz, 3-MHz or 4-MHz Switching Frequency
- Two Inputs for External Voltage Monitoring
- Two Programmable Power-Good Signals
- Dedicated Reference Voltage for Diagnostics
- Window Watchdog With Reset Output
- External Clock Input to Synchronize Switching
- Spread-Spectrum Mode
- Programmable Start-up and Shutdown Delays and Sequencing With Enable Signal
- Configurable General Purpose Outputs (GPOs)
- I^2C-Compatible Interface Supporting Standard (100 kHz), Fast (400 kHz), Fast+ (1 MHz), and High-Speed (3.4 MHz) Modes
- Interrupt Function with Programmable Masking
- Output Short-Circuit and Overload Protection
- Overtemperature Warning and Protection
- Overvoltage Protection (OVP) and Undervoltage Lockout (UVLO)

2 Applications

Automotive Radar, Camera and Cluster Power Applications

3 Description

The LP87702-Q1 is designed to meet the power management requirements of the latest platform needs especially in automotive radar, camera and cluster applications. The device contains two step-down DC-DC converters, a 5-V boost converter, two voltage monitoring inputs for external power supplies, window watchdog and general purpose digital output signals. The device is controlled by an I^2C-compatible serial interface and by enable signals.

The automatic PWM/PFM (AUTO mode) operation gives high efficiency over a wide output current range for both boost and buck regulators. The LP87702-Q1 supports remote voltage sensing for buck regulators to compensate IR drop between the regulator output and the point-of-load thus improving the accuracy of the output voltage. In addition the switching clock can be forced to PWM mode and also synchronized to an external clock to minimize the disturbances.

The LP87702-Q1 device supports buck regulator load current measurement without the addition of external current sense resistors. In addition, the LP87702-Q1 device supports programmable start-up and shutdown delays and sequences including general purpose digital output signals synchronized to the enable signal. During start-up and voltage change, the device controls the output slew rate to minimize output voltage overshoot and the inrush current.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP87702-Q1	VQFN (32)	5.00 mm × 5.00 mm

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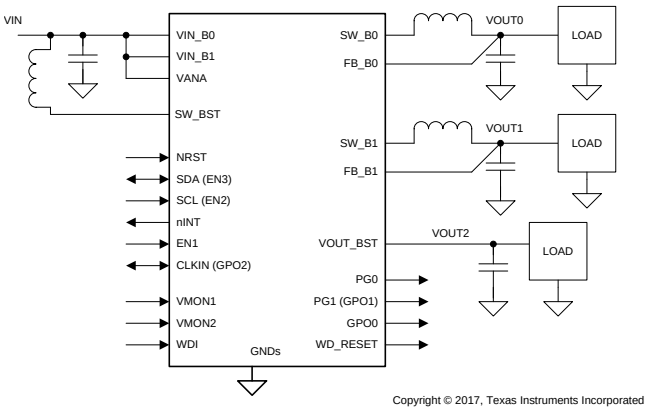
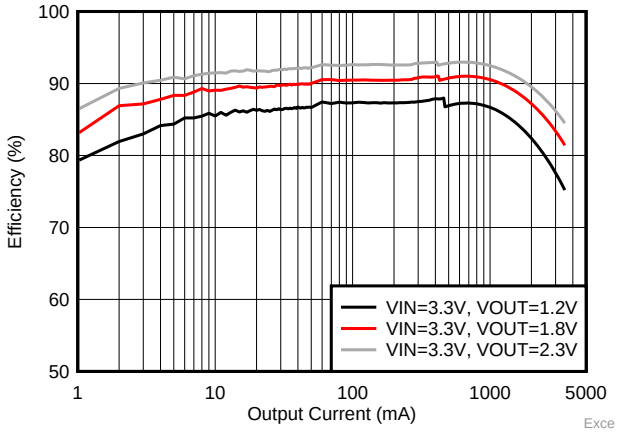
Simplified Schematic



Buck Efficiency vs Output Current



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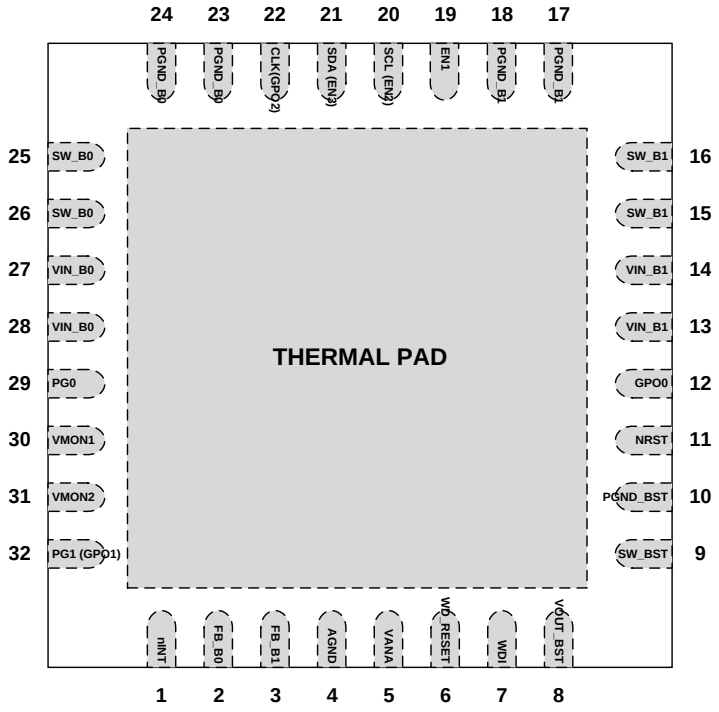
4 Revision History

DATE	REVISION	NOTES
December 2017	*	

5 Pin Configuration and Functions

RHB Package
32-Pin VQFN With Thermal Pad
Top View



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Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	nINT	D/O	Open-drain interrupt output. Active LOW.
2	FB_B0	A	Output voltage feedback for Buck0.
3	FB_B1	A	Output voltage feedback for Buck1.
4	AGND	G	Ground.
5	VANA	P	Supply voltage for analog and digital blocks. Must be connected to same node with VIN_Bx.
6	WD_RESET	D/O	Reset output from window watchdog
7	WDI	D/I	Digital input signal for window watchdog
8	VOUT_BST	P/O	Boost output.
9	SW_BST	P/I	Boost input.
10	PGND_BST	P/G	Power ground for boost.
11	NRST	D/I	Reset signal for the device.
12	GPO0	D/O	General purpose digital output 0.
13, 14	VIN_B1	P/I	Input for Buck1. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed.
15, 16	SW_B1	P/O	Buck1 switch node.
17, 18	PGND_B1	P/G	Power Ground for Buck1.
19	EN1	D/I	Programmable Enable 1 signal.
20	SCL	D/I	Serial interface clock input for I2C access. Connect a pullup resistor. Alternative function is programmable enable 2 signal.
21	SDA	D/I/O	Serial interface data input and output for I2C access. Connect a pullup resistor. Alternative function is programmable enable 3 signal.
22	CLKIN	D/I/O	External clock input. Alternative function is general purpose digital output 2 (GPO2). Second alternative function is watchdog disable (WD_DIS). Watchdog disable is not supported in P87702D.
23, 24	PGND_B0	P/G	Power ground for Buck0.
25, 26	SW_B0	P/O	Buck0 switch node.
27, 28	VIN_B0	P/I	Input for Buck0. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed.
29	PG0	D/O	Programmable power-good indication signal.
30	VMON1	A/I	Voltage monitoring input 1.
31	VMON2	A/I	Voltage monitoring input 2.
32	PG1	D/O	Programmable power-good indication signal. Alternative function is general purpose digital output 1 (GPO1).
Thermal pad	N/A	G	
A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin			

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
VIN_B0, VIN_B1, SW_BST, VANA	Voltage on input power connections	–0.3	6	V
SW_B0, SW_B1	Voltage on buck switch nodes	–0.3	(VIN_Bx + 0.3 V) with 6-V maximum	V
FB_B0, FB_B1	Voltage on buck voltage sense nodes	–0.3	(VANA + 0.3 V) with 6-V maximum	V
VOUT_BST	Voltage on boost output	–0.3	6	V
SCL (EN2), SDA (EN3), VMON1, VMON2	Voltage on voltage monitoring pins	–0.3	(VANA + 0.3 V) with 6-V maximum	V
NRST, EN1, nINT	Voltage on logic pins (input or output pins)	–0.3	6	V
PG0, PG1 (GPO1), GPO0, CLKIN (GPO2), WDI, WD_RESET	Voltage on logic pins (input or output pins)	–0.3	(VANA + 0.3 V) with 6-V maximum	V
VIN_B0, VIN_B1, SW_B0, SW_B1, PGND_B0, PGND_B1	Current on power pins (average current over 100 k hour lifetime, T_J = TBD°C)		TBD	A / pin
Junction temperature, T_{J-MAX}		−40	150	°C
Storage temperature, T_{stg}		–65	150	°C
Maximum lead temperature (soldering, 10 seconds)			260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 8, 9, 16, 17, 24, 25, 32)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
INPUT VOLTAGE				
VIN_B0, VIN_B1, SW_BST, VANA	Voltage on input power connections	2.8	5.5	V
VMON1, VMON2	Voltage on voltage monitoring pins	0	5.5	V
NRST, EN1, EN2, EN3, nINT	Voltage on logic pins (input or output pins)	0	5.5	
PG0, PG1 (GPO1), GPO0, CLKIN (GPO2), WDI, WD_RESET	Voltage on logic pins (input or output pins)	0	VANA	V
SCL, SDA	Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), Fast+ (1 MHz), and High-Speed (3.4 MHz) Modes	0	1.95	V
	Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), and Fast+ (1 MHz) Modes	0	VANA with 3.6-V maximum	V
TEMPERATURE				
Junction temperature, T_J		−40	140	°C
Ambient temperature, T_A		−40	125	°C

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6.4 Thermal Information

THERMAL METRIC(1)		RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.7	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	17.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.6	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Limits apply over the junction temperature range –40°C ≤ T_J ≤ +140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_J = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted(1) (2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL COMPONENTS						
C_{IN_BUCK}	Input filtering capacitance for buck regulators	Effective capacitance, connected from VIN_Bx to PGND_Bx	1.9	10		µF
C_{OUT_BUCK}	Output filtering capacitance for buck regulators	Effective total capacitance. Maximum includes POL capacitance.	15	22	100	µF
$C_{OUT\_BUCK\_POL}$	Point-of-load (POL) capacitance for buck regulators	Optional POL capacitance		22		µF
C_{OUT_BST}	Output filtering capacitance for boost regulator	Effective capacitance	10	22	40	µF
ESR_C	Input and output capacitor ESR	[1-10] MHz		2	10	mΩ
L_{BUCK}	Inductor for buck regulators	Inductance of the inductor		0.47		µH
			–30%		30%	
L_{BST}	Inductor for boost regulators	Inductance of the inductor, 2-MHz switching		1		µH
		Inductance of the inductor, 4-MHz switching		0.47		
		Inductance of the inductor	–30%		30%	
DCR_L	Inductor DCR			25		mΩ
BUCK REGULATORS						
$V_{(VIN\_Bx)}$, $V_{(VANA)}$	Input voltage range		2.8	3.7	5.5	V
V_{OUT_Bx}	Output voltage	Programmable voltage range	0.7	1	3.36	V
		Step size, 0.7 V ≤ V_{OUT} < 0.73 V		10		mV
		Step size, 0.73 V ≤ V_{OUT} < 1.4 V		5		
		Step size, 1.4 V ≤ V_{OUT} ≤ 3.36 V		20		
I_{OUT_Bx}	Output current	Output current			3.5(3)	A
	Minimum voltage difference between $V_{(VIN\_Bx)}$ and V_{OUT_Bx} for electrical characteristics	$V_{(VIN\_Bx)}$ – V_{OUT}, I_{OUT_Bx} ≤ 2 A	0.8			V
		$V_{(VIN\_Bx)}$ – V_{OUT}, I_{OUT_Bx} > 2 A	1			

(1) All voltage values are with respect to network ground.
(2) Minimum (MIN) and Maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers are not verified, but do represent the most likely norm.
(3) The maximum output current can be limited by the forward current limit $I_{LIM\ FWD}$. The maximum output current is also limited by the junction temperature and maximum average current over lifetime. The power dissipation inside the die increases the junction temperature and limits the maximum current depending of the length of the current pulse, efficiency, board and ambient temperature.

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Electrical Characteristics (continued)

Limits apply over the junction temperature range –40°C ≤ T_J ≤ +140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_J = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted(1) (2).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature	Force PWM mode, V_{OUT} < 1 V	–20		20	mV
		Force PWM mode, V_{OUT} ≥ 1 V	–2%		2%	
		PFM mode, V_{OUT} < 1 V, the average output voltage level is increased by maximum 20 mV	–20		40	mV
		PFM mode, V_{OUT} ≥ 1 V, the average output voltage level is increased by maximum 20 mV	–2%		2% + 20 mV	
	Ripple voltage	PWM mode, L = 0.47 µH		10		mV_{p-p}
		PFM mode, L = 0.47 µH		25		
DC_{LNR}	DC line regulation	I_{OUT} = $I_{OUT(max)}$		±0.05		%/V
DC_{LDR}	DC load regulation in PWM mode	V_{OUT_Bx} = 1 V, I_{OUT} from 0 to $I_{OUT(max)}$		0.3%		
T_{LDSR}	Transient load step response	I_{OUT} = 0 A to 3 A, T_R = T_F = 1 µs, PWM mode, V_{VIN_Bx} = 3.3V, V_{OUT_Bx} = 1 V, C_{OUT} = 22 + 22 µF, L = 0.47 µH, f_{SW} = 4 MHz		±60		mV
T_{LNSR}	Transient line response	$V_{(VIN\_Bx)}$ stepping 3 V ↔ 3.5 V, T_R = T_F = 10 µs, I_{OUT} = $I_{OUT(max)}$		±20		mV
$I_{LIM\ FWD}$	Forward current limit for both bucks (peak for every switching cycle)	Programmable range	1.5		4.5	A
		Step size		0.5		
		Accuracy, $V_{(VIN\_Bx)}$ ≥ 3 V, I_{LIM} = 4 A	–5%	7.5%	20%	
		Accuracy, 2.8 V ≤ $V_{(VIN\_Bx)}$ < 3 V, I_{LIM} = 4 A	–20%	7.5%	20%	
$I_{LIM\ NEG}$	Negative current limit		1.6	2	3	A
$R_{DS(ON)\ BUCK\ HS\ FET}$	On-resistance, high-side FET	Each phase, between VIN_Bx and SW_Bx pins (I = 1 A)		60	110	mΩ
$R_{DS(ON)\ BUCK\ LS\ FET}$	On-resistance, low-side FET	Each phase, between SW_Bx and PGND_Bx pins (I = 1 A)		55	80	mΩ
f_{SW}	Switching frequency, PWM mode OTP programmable	2-MHz setting or V_{OUT_Bx} < 0.8 V	1.8	2	2.2	MHz
		3-MHz setting and V_{OUT_Bx} ≥ 0.8 V	2.7	3	3.3	
		4-MHz setting and V_{OUT_Bx} ≥ 1.1 V	3.6	4	4.4	
	Start-up time (soft start)	From ENx to V_{OUT_Bx} = 0.35 V (slew-rate control begins)		120		µs
	Overshoot during start-up				50	mV
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 010, V_{VOUT_Bx} ≥ 0.7 V	–15%	10	15%	mV/µs
		SLEW_RATEx[2:0] = 011, V_{VOUT_Bx} ≥ 0.7 V	–15%	7.5	15%	
		SLEW_RATEx[2:0] = 100, V_{VOUT_Bx} ≥ 0.7 V	–15%	3.8	15%	
		SLEW_RATEx[2:0] = 101, V_{VOUT_Bx} ≥ 0.7 V	–15%	1.9	15%	
		SLEW_RATEx[2:0] = 110, V_{VOUT_Bx} ≥ 0.7 V	–15%	0.94	15%	
		SLEW_RATEx[2:0] = 111, V_{VOUT_Bx} ≥ 0.7 V	–15%	0.47	15%	
$I_{PFM-PWM}$	PFM-to-PWM switch - current threshold(5)			600		mA
$I_{PWM-PFM}$	PWM-to-PFM switch - current threshold(5)			240		mA
	Output pulldown resistance	Regulator disabled	80	115	150	Ω

(4) Applies when internal oscillator is used. The slew-rate can be limited by the current limit (forward or negative current limit), output capacitance and load current.
(5) The final PFM-to-PWM and PWM-to-PFM switchover current varies slightly and is dependant on the output voltage, input voltage and the inductor current level.

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Electrical Characteristics (continued)

Limits apply over the junction temperature range –40°C ≤ T_J ≤ +140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_J = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted[1] [2].

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST REGULATOR						
V_{IN_BST}	Input voltage range for boost power inputs		2.8[6]	3.3	4	V
V_{OUT_BST}	Output voltage	BOOST_VSET = 00		4.9		V
		BOOST_VSET = 01		5		
		BOOST_VSET = 10		5.1		
		BOOST_VSET = 11		5.2		
I_{OUT_BST}	Output current				0.6[7]	A
I_{LIM_BST}	Output current limit	BOOST_ILIM = 00, V_{IN_BST} < 3.6 V	0.8	1	1.2	A
		BOOST_ILIM = 01, V_{IN_BST} < 3.6 V	1.1	1.4	1.7	
		BOOST_ILIM = 10, V_{IN_BST} < 3.6 V	1.5	1.9	2.3	
		BOOST_ILIM = 11, V_{IN_BST} < 3.6 V	2.2	2.8	3.4	
$V_{OUT\_BST\_DC}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature	Default output voltage	–3%		3%	
	Ripple voltage, forced PWM mode	22 µF effective output capacitance		20		mV_{p-p}
	Ripple voltage, PFM mode	22 µF effective output capacitance		150		mV_{p-p}
DC_{LDR}	DC load regulation	I_{OUT} = 1 mA to $I_{OUT(max)}$		0.3%		
T_{LDSR}	Transient load step response	I_{OUT} = 1 mA to 250 mA, T_R = T_F = 1 µs, 22 µF effective output capacitance, V_{IN_BST} > 3 V	–220		220	mV
I_{SHORT}	Short-circuit current limitation	During start-up. Applies until V_{OUT_BST} = V_{IN_BST}		625		mA
$R_{DS(ON)\ BST\ HS\ FET}$	On-resistance, high-side FET	Pin-to-pin, between SW_BST and VOUT_BST pins (I = 250 mA)		145	220	mΩ
$R_{DS(ON)\ BST\ LS\ FET}$	On-resistance, low-side FET	Pin-to-pin, between SW_BST and PGND_BST pins (I = 250 mA)		90	175	mΩ
f_{SW}	Switching frequency	2-MHz setting	1.8	2	2.2	MHz
		4-MHz setting	3.6	4	4.4	MHz
	Start-up time	From enable to boost VOUT valid; C_{OUT_BST} = 22 µF		230		µs
	Output pulldown resistance	Regulator disabled		135		Ω

(6) Minimum boost-power input voltage is 3 V for P87702D.
(7) Maximum output current is 0.25 A for P87702D.

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Electrical Characteristics (continued)

Limits apply over the junction temperature range –40°C ≤ T_J ≤ +140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_J = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted[1] [2].

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL CLOCK AND PLL					
External input clock[8]	Nominal frequency	1		24	MHz
	Nominal frequency step size		1		
	Required accuracy from nominal frequency	–30%		10%	
External clock detection	Delay for missing clock detection			1.8	µs
	Delay and debounce for clock detection			20	
Clock change delay (internal to external)	Delay from valid clock detection to use of external clock		600		µs
PLL output clock jitter	Cycle to cycle		300		ps, p-p
MONITORING FUNCTIONS					
VANA voltage monitoring	Voltage threshold, VANA_THRESHOLD = 0		3.3		V
	Voltage threshold, VANA_THRESHOLD = 1		5.0		
	Voltage window, VANA_WINDOW = 0	±4%	±5%	±6%	
	Voltage window, VANA_WINDOW = 1	±9%	±10%	±11%	
VMON1 and VMON2 voltage monitoring thresholds	VMONx_THRESHOLD = 000		0.65		V
	VMONx_THRESHOLD = 001		0.8		
	VMONx_THRESHOLD = 010		1.0		
	VMONx_THRESHOLD = 011		1.1		
	VMONx_THRESHOLD = 100		1.2		
	VMONx_THRESHOLD = 101		1.3		
	VMONx_THRESHOLD = 110		1.8		
VMON1 and VMON2 voltage monitoring windows	VMONx_WINDOW = 00	±1%	±2%	±3%	
	VMONx_WINDOW = 01	±2%	±3%	±4%	
	VMONx_WINDOW = 10	±3%	±4%	±5%	
	VMONx_WINDOW = 11	±5%	±6%	±7%	
Buck0 and Buck1 voltage monitoring windows	BUCKx_WINDOW = 00	±20	±30	±40	mV
	BUCKx_WINDOW = 01	±37	±50	±63	
	BUCKx_WINDOW = 10	±57	±70	±83	
	BUCKx_WINDOW = 11	±77	±90	±103	
Boost voltage monitoring	BOOST_WINDOW = 00	±0.7%	±2%	±-3.3%	V
	BOOST_WINDOW = 01	±2.7%	±4%	±5.3%	
	BOOST_WINDOW = 10	±4.7%	±6%	±7.3%	
	BOOST_WINDOW = 11	±6.7%	±8%	±9.3%	
Deglitch time	VANA, VMONx and BOOST monitoring	12		17	µs
	BUCKx monitoring	6		9	

(8) The external clock frequency must be selected so that buck switching frequency is above 1.7 MHz.

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Electrical Characteristics (continued)

Limits apply over the junction temperature range –40°C ≤ T_J ≤ +140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_J = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted[1] [2].

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION FUNCTIONS						
	Thermal warning	Temperature rising, TDIE_WARN_LEVEL = 0	115	125	135	°C
		Temperature rising, TDIE_WARN_LEVEL = 1	130	140	150	
		Hysteresis		20		
	Thermal shutdown	Temperature rising	140	150	160	°C
		Hysteresis		20		
$VANA_{OVP}$	VANA overvoltage	Voltage rising	5.6	5.8	6.1	V
		Voltage falling	5.45	5.73	5.96	
		Hysteresis	40		200	mV
$VANA_{UVLO}$	VANA undervoltage lockout	Voltage rising	2.51	2.63	2.75	V
		Voltage falling	2.5	2.6	2.7	
	BUCKx short-circuit detection	Threshold		0.35		V
	BOOST short-circuit detection	Threshold		2.5		V
LOAD CURRENT MEASUREMENT FOR BUCK REGULATORS						
	Current measurement range	Maximum code			10.22	A
	Resolution	LSB		20		mA
	Measurement accuracy	I_{OUT} > 1 A		<10%		
	Measurement time	Auto mode (automatically changing to PWM mode for the measurement)		50		µs
		PWM mode		4		
CURRENT CONSUMPTION						
	Shutdown current consumption	NRST = 0		1		µA
	Standby current consumption, regulators disabled	NRST = 1		9		µA
	Active current consumption, one buck regulator enabled in auto mode, internal RC oscillator	I_{OUT_Bx} = 0 mA, not switching		60		µA
	Active current consumption, two buck regulators enabled in auto mode, internal RC oscillator	I_{OUT_Bx} = 0 mA, not switching		90		µA
	Active current consumption during PWM operation, one buck regulator enabled	I_{OUT_Bx} = 0 mA		15		mA
	Active current consumption during PWM operation, two buck regulators enabled	I_{OUT_Bx} = 0 mA		30		mA
	Active current consumption, boost regulator in PFM operation	I_{OUT_BST} = 0 mA		200		µA
	Active current consumption, boost regulator in PWM operation	I_{OUT_BST} = 0 mA, f_{SW} = 4 MHz		18		mA
	PLL and clock detector current consumption	Additional current consumption when enabled, 2-MHz external clock		2		mA

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Electrical Characteristics (continued)

Limits apply over the junction temperature range –40°C ≤ T_J ≤ +140°C, specified V_{VANA}, V_{VIN_Bx}, V_{VOUT_Bx}, V_{VOUT_BST}, and I_{OUT} range, unless otherwise noted. Typical values are at T_J = 25°C, V_{VANA} = V_{VIN_Bx} = 3.3 V, V_{OUT_BST} = 5 V and V_{OUT_Bx} = 1 V, unless otherwise noted[1] [2].

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT SIGNALS SCL, SDA, NRST, EN1, EN2, EN3, CLKIN, WDI						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.2			
V_{HYS}	Hysteresis of Schmitt Trigger inputs		10	80	200	mV
	ENx pulldown resistance	ENx_PD = 1		500		kΩ
	NRST pulldown resistance	Always enabled		500		kΩ
DIGITAL OUTPUT SIGNALS nINT, SDA						
V_{OL}	Output low level	SDA: I_{SOURCE} = 20 mA			0.4	V
		nINT: I_{SOURCE} = 2 mA			0.4	
R_P	External pullup resistor for nINT	to VIO supply		10		kΩ
DIGITAL OUTPUT SIGNALS PGOOD, PG1, GPO0, GPO1, GPO2, WD_RESET						
V_{OL}	Output low level	I_{SOURCE} = 2 mA			0.4	V
V_{OH}	Output high level, configured to push-pull	I_{SINK} = 2 mA	V_{VANA} – 0.4		V_{VANA}	
V_{PU}	Supply voltage for external pullup resistor, configured to open-drain				V_{VANA}	
R_{PU}	External pullup resistor, configured to open-drain			10		kΩ
ALL DIGITAL INPUTS						
I_{LEAK}	Input current	All logic inputs except NRST, over pin voltage range, when PD not enabled	−1		1	µA
		NRST, over pin voltage range. Other logic inputs when PD enabled	–1		20	µA

6.6 I²C Serial Bus Timing Parameters

See [1].			MIN	MAX	UNIT
f_{SCL}	Serial clock frequency	Standard mode		100	kHz
		Fast mode		400	
		Fast mode +		1	MHz
		High-speed mode, C_b = 100 pF		3.4	
		High-speed mode, C_b = 400 pF		1.7	
t_{LOW}	SCL low time	Standard mode	4.7		µs
		Fast mode	1.3		
		Fast mode +	0.5		
		High-speed mode, C_b = 100 pF	160		ns
		High-speed mode, C_b = 400 pF	320		
t_{HIGH}	SCL high time	Standard mode	4		µs
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode, C_b = 100 pF	60		ns
		High-speed mode, C_b = 400 pF	120		

(1) C_b refers to the capacitance of one bus line. C_b is expressed in pF units.

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I²C Serial Bus Timing Parameters (continued)

See (1).			MIN	MAX	UNIT
$t_{SU;DAT}$	Data setup time	Standard mode	250		ns
		Fast mode	100		
		Fast mode +	50		
		High-speed mode	10		
$t_{HD;DAT}$	Data hold time	Standard mode	0.01	3.45	µs
		Fast mode	0.01	0.9	
		Fast mode +	0.01		
		High-speed mode, C_b = 100 pF	10	70	ns
		High-speed mode, C_b = 400 pF	10	150	
$t_{SU;STA}$	Setup time for a start or a repeated start condition	Standard mode	4.7		µs
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160		ns
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard mode	4		µs
		Fast mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160		ns
t_{BUF}	Bus free time between a stop and start condition	Standard Mode	4.7		µs
		Fast Mode	1.3		
		Fast mode +	0.5		
$t_{SU;STO}$	Setup time for a stop condition	Standard Mode	4		µs
		Fast Mode	0.6		
		Fast mode +	0.26		
		High-speed mode	160		ns
t_{rDA}	Rise time of SDA signal	Standard mode		1000	ns
		Fast mode	20+0.1 C_b	300	
		Fast mode +		120	
		High-speed mode, C_b = 100 pF	10	80	
		High-speed mode, C_b = 400 pF	20	160	
t_{fDA}	Fall time of SDA signal	Standard mode		250	ns
		Fast mode	20+0.1 C_b	250	
		Fast mode +	20+0.1 C_b	120	
		High-speed mode, C_b = 100 pF	10	80	
		High-speed mode, C_b = 400 pF	20	160	
t_{rCL}	Rise time of SCL signal	Standard mode		1000	ns
		Fast mode	20+0.1 C_b	300	
		Fast mode +		120	
		High-speed mode, C_b = 100 pF	10	40	
		High-speed mode, C_b = 400 pF	20	80	
t_{rCL1}	Rise time of SCL signal after a repeated start condition and after an acknowledge bit	Standard mode		1000	ns
		Fast mode	20+0.1 C_b	300	
		Fast mode +		120	
		High-speed mode, C_b = 100 pF	10	80	
		High-speed mode, C_b = 400 pF	20	160	

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I²C Serial Bus Timing Parameters (continued)

See (1).			MIN	MAX	UNIT
t_{fCL}	Fall time of a SCL signal	Standard mode		300	ns
		Fast mode	20+0.1 C_b	300	
		Fast mode +	20+0.1 C_b	120	
		High-speed mode, C_b = 100 pF	10	40	
		High-speed mode, C_b = 400 pF	20	80	
C_b	Capacitive load for each bus line (SCL and SDA)			400	pF
t_{SP}	Pulse width of spike suppressed (Spikes shorter than indicated width are suppressed)	Fast mode, Fast mode +		50	ns
		High-speed mode		10	

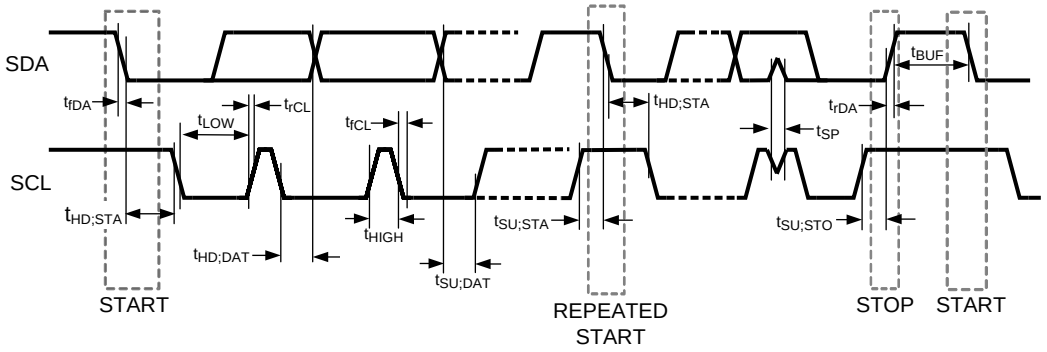

Figure 1. I²C Timing

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The LP87702-Q1 is a high-efficiency, high-performance power supply IC with two step-down DC-DC converter cores (Buck0 and Buck1) and Boost converter for automotive applications. Table 1 lists the output characteristics of the various regulators.

Table 1. Supply Specification

SUPPLY	OUTPUT		
	V_{OUT} RANGE (V)	RESOLUTION (mV)	I_{MAX} MAXIMUM OUTPUT CURRENT (mA)
Boost	4.9 to 5.2	100	600
Buck0	0.7 to 3.36	10 (0.7 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V)	3500
Buck1	0.7 to 3.36	10 (0.7 V to 0.73 V) 5 (0.73 V to 1.4 V) 20 (1.4 V to 3.36 V)	3500

The LP87702-Q1 regulators also support switching clock synchronization to an external clock. The nominal frequency of the external clock can be from 1 MHz to 24 MHz with 1-MHz steps. CLKIN is multiplexed with a general-purpose output (GPO2). Alternatively, optional spread spectrum mode can be enabled to reduce EMI.

LP87702-Q1 features include diagnostics, monitoring and protections for both device internal and system level operation :

- Soft start
- Input undervoltage lockout
- Programmable undervoltage or over- and undervoltage monitoring for the input (from VANA pin)
- Programmable undervoltage or over- and undervoltage monitoring for the buck and boost regulator outputs
- Two inputs (VMONx) with programmable undervoltage or over- and undervoltage thresholds, for monitoring external rails in the system
- One dedicated power-good output (PG0) to which selected monitoring signals can be combined
- Second programmable power-good output, multiplexed with general purpose output (GPO1)
- Power good flag with maskable interrupt
- Programmable window watchdog
- Buck and boost regulator overload detection
- Thermal warning with two selectable levels
- Thermal shutdown

LP87702-Q1 control interface :

- Dedicated EN1, EN2 and E3 inputs with programmable power-up/power-down sequence control
- Optional I2C (multiplexed with E2 and EN3 inputs)
- Interrupt signal (nINT) to host
- Reset input (NRST)
- One dedicated general purpose output (GPO0)

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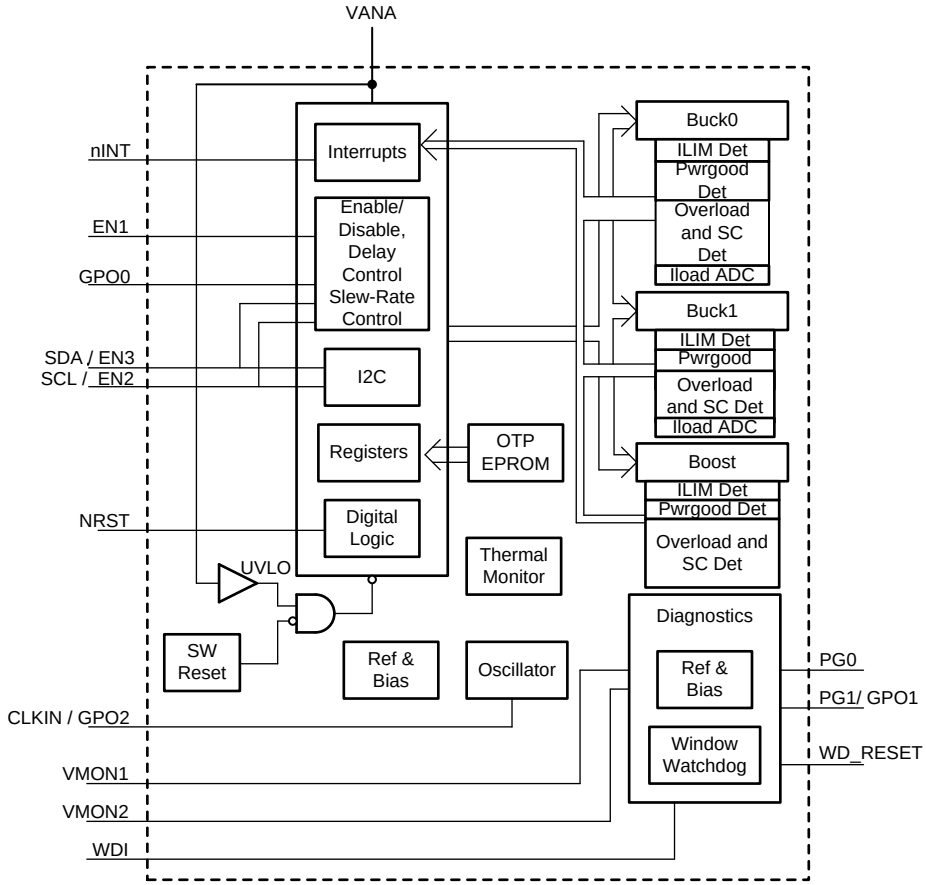
7.2 Functional Block Diagram



7.3 Feature Descriptions

7.3.1 Step-Down DC-DC Converters

7.3.1.1 Overview

The LP87702-Q1 includes two high-efficiency step-down DC-DC converter cores. The buck regulators deliver 0.7-V to 3.36-V regulated voltage rails from 2.8-V to 5.5-V input supply voltage. The cores are designed for flexibility; most of the functions are programmable, thus giving a possibility to optimize the regulator operation for each application :

- DVS support with programmable slew rate
- Automatic mode control based on the loading (PWM or PFM mode)
- Forced PWM mode option
- Optional external clock input to minimize crosstalk
- Optional spread spectrum technique to reduce EMI
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Programmable output voltage monitoring with maskable interrupt and selectable connection PG0 and/or PG1
- Average output current sensing (for PFM entry and load current measurement)

Some of the key parameters that can be programmed via registers (the default values are set by OTP bits):

- Output voltage

ADVANCE INFORMATION

Feature Descriptions (continued)

- Forced PWM operation
- Switch current limit
- Output voltage slew rate
- Enable and disable delays with ENx pin control

There are two modes of operation for the buck converter, depending on the output current required: pulse width modulation (PWM) and pulse-frequency modulation (PFM). The converter operates in PWM mode at high load currents of approximately 600 mA or higher. Lighter output current loads will cause the converter to automatically switch into PFM mode for reduced current consumption when forced PWM mode is disabled. The forced PWM mode can be selected to maintain fixed switching frequency at all load currents. When buck is disabled, buck output is isolated from the input voltage rail. Output has an optional pulldown resistor.

A block diagram of a single core is shown in Figure 2.

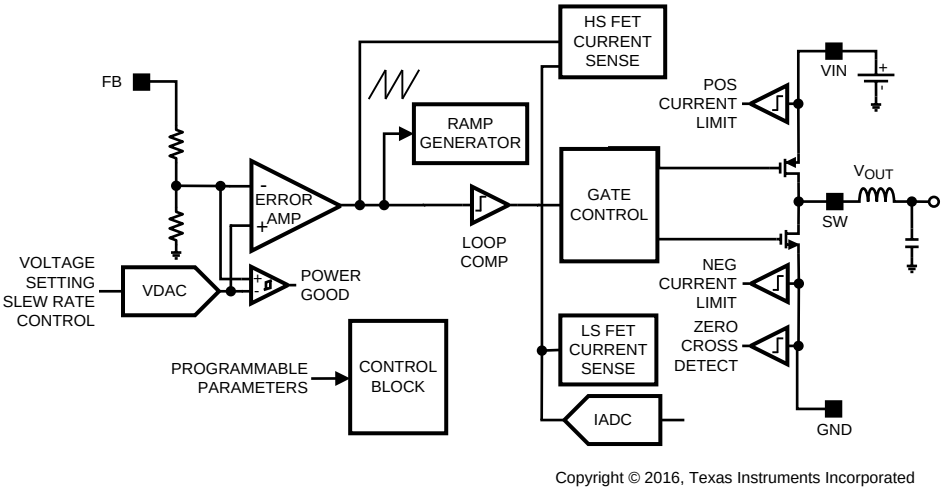


Figure 2. Detailed Block Diagram Showing One Core

7.3.1.2 Transition between PWM and PFM Modes

The LP87702-Q1 converter operates in PWM mode at load current of about 600 mA or higher. At lighter load current levels the device automatically switches into PFM mode for reduced current consumption when forced PWM mode is disabled (AUTO mode operation). By combining the PFM and the PWM modes a high efficiency is achieved over a wide output-load current range.

7.3.1.3 Buck Converter Load Current Measurement

Buck load current can be monitored via I^2C registers. The monitored buck converter is selected with the LOAD_CURRENT_BUCK_SELECT bit in SEL_I_LOAD register. A write to this selection register starts a current measurement sequence. The regulator is forced to PWM mode during the measurement. The measurement sequence is 50 µs long at maximum. LP87702-Q1 can be configured to give out an I_MEAS_INT interrupt in INT_TOP_1 register after the load current measurement sequence is finished. Load current measurement interrupt can be masked with I_MEAS_MASK bit in TOP_MASK_1 register. The measurement result can be read from registers I_LOAD_1 and I_LOAD_2. Register I_LOAD_1 bits give out the LSB bits and register I_LOAD_2 bit gives the MSB bit. The LSB bit corresponds to 20 mA in the measurement result, and maximum code corresponds to 10.22 A.

7.3.2 Boost Converter

The LP87702-Q1 device includes a boost regulator which delivers an output voltage programmable from 4.9 V to 5.2 V with 0.1-V step. Input voltage range is from 2.8 V to 4 V (3V to 4V in P87702D). The boost regulator has flexibility to support various application conditions:

- Automatic mode control based on the loading (PFM or PWM mode). PFM mode is not supported in P87702D
- Forced PWM option

ADVANCE INFORMATION

Feature Descriptions (continued)

- Optional external clock input to minimize crosstalk
- Optional spread spectrum technique to reduce EMI
- Synchronous rectification
- Current mode loop with PI compensator
- Soft start
- Programmable output voltage monitoring with maskable interrupt and selectable connection to PG0 and/or PG1

Following parameters can be programmed via registers, the default values are set by OTP bits unless otherwise noted:

- Output voltage (BOOST_VSET)
- Forced PWM operation (BOOST_FPWM)
- Switch current limit (BOOST_ILIM)
- Enable and disable delays with ENx pin control (BOOST_DELAY register)
- Output discharge resistor enable/disable when boost is disabled (BOOST_RDIS_EN bit, discharge is enabled by default)
- Output voltage monitoring enable/disable and monitoring window thresholds

There are two modes of operation for the boost converter, depending on the output current required: PWM and PFM. In AUTO mode the boost converter operates in PWM mode at high load currents. Lighter output current loads cause the converter to automatically switch into PFM mode for reduced current consumption when forced PWM mode is disabled. Exact threshold between PWM and PFM depends on conversion ratio. The forced PWM mode can be selected to maintain fixed switching frequency at all load currents. When boost is disabled, boost output is isolated from the input voltage rail. Output has an optional pulldown resistor.

Boost block has an alternate operating mode as a bypass/load switch. Input voltage range in this mode is from 4.5 V to 5.5 V. Operating mode is selected in OTP and is fixed, changing the mode on-the-fly is not supported. Bypass mode is not supported in P87702D.

7.3.3 Spread-Spectrum Mode

Systems with periodic switching signals may generate a large amount of switching noise in a set of narrowband frequencies (the switching frequency and its harmonics). The usual solution to reduce noise coupling is to add EMI-filters and shields to the boards. The LP87702-Q1's register selectable spread-spectrum mode minimizes the need for output filters, ferrite beads, or chokes. In spread spectrum mode, the switching frequency varies between 0.85 × f_{SW} and f_{SW}, where f_{SW} is switching frequency selected in the OTP. This reduces the EMI emissions radiated by the converter and associated passive components and PCB traces (see Figure 3). This feature is available only when internal RC oscillator is used (EN_PLL is 0 in PLL_CTRL register) and it is enabled with the EN_SPREAD_SPEC bit in CONFIG register, and it affects both buck cores and the boost regulator.

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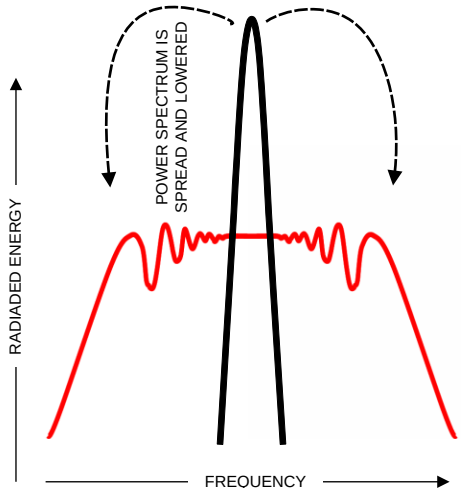
Feature Descriptions (continued)



Where a fixed frequency converter exhibits large amounts of spectral energy at the switching frequency, the spread spectrum architecture of the LP87702-Q1 spreads that energy over a large bandwidth.

Figure 3. Spread Spectrum Modulation

7.3.4 Sync Clock Functionality

The LP87702-Q1 device contains a CLKIN input to synchronize buck and boost regulators' switching clock with the external clock. The block diagram of the clocking and PLL module is shown in Figure 4. Depending on the EN_PLL bit in PLL_CTRL register and the external clock availability, the external clock is selected and interrupt is generated as shown in Table 2. The interrupt can be masked with SYNC_CLK_MASK bit in TOP_MASK_1 register. The nominal frequency of the external input clock is set by EXT_CLK_FREQ[4:0] bits in PLL_CTRL register and it can be from 1 MHz to 24 MHz with 1-MHz steps. The external clock must be inside accuracy limits (–30%/+10%) for valid clock detection.

The SYNC_CLK_INT interrupt in INT_TOP_1 register is also generated in cases the external clock is expected but it is not available. These cases are Startup (Read OTP-to-standby transition) when EN_PLL = 1 and buck or boost regulator is enabled (standby-to-active transition) when EN_PLL = 1.

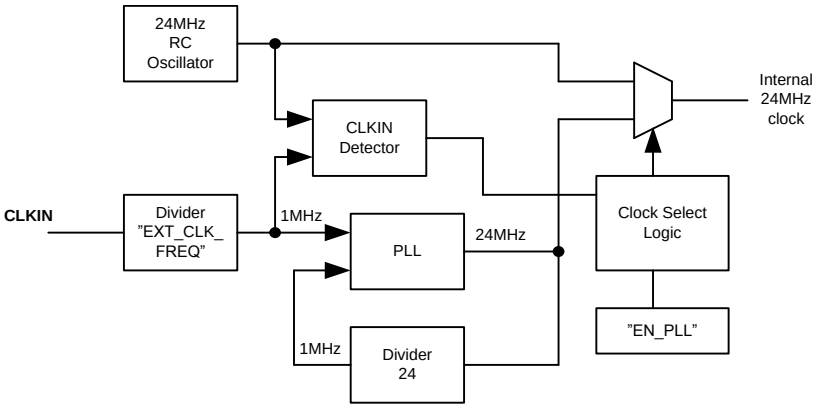


Figure 4. Clock and PLL Module

Table 2. PLL Operation

DEVICE OPERATION MODE	EN_PLL	PLL AND CLOCK DETECTOR STATE	INTERRUPT FOR EXTERNAL CLOCK	CLOCK
STANDBY	0	Disabled	No	Internal RC
ACTIVE	0	Disabled	No	Internal RC

Feature Descriptions (continued)

Table 2. PLL Operation (continued)

DEVICE OPERATION MODE	EN_PLL	PLL AND CLOCK DETECTOR STATE	INTERRUPT FOR EXTERNAL CLOCK	CLOCK
STANDBY	1	Enabled	When external clock disappears or appears	Automatic change to internal RC oscillator when External clock is not available
ACTIVE	1	Enabled	When external clock disappears or appears	Automatic change to internal RC oscillator when External clock is not available

7.3.5 Power-Up

The power-up sequence for the LP87702-Q1 is as follows:

- VANA (and VIN_Bx) reach minimum recommended levels (V_{VANA} > $VANA_{UVLO}$).
- NRST signal is set high. This initiates OTP reading and enables the system I/O interface. The I^2C host allows at least 1.2 ms before writing or reading data to the LP87702-Q1.
- Device enters STANDBY mode. Watchdog operation starts.
- The host can change the default register setting by I^2C if needed.
- The regulators can be enabled/disabled and the GPO signals can be controlled by EN pin and by I^2C interface.

7.3.6 Regulator Control

7.3.6.1 Enabling and Disabling Regulators

The buck regulators can be enabled when the device is in STANDBY or ACTIVE state. There are two ways for enable and disable the buck regulators:

- Using BUCKx_EN bit in BUCKx_CTRL_1 register (BUCKx_EN_PIN_CTRL bit is 00 in BUCKx_CTRL_1 register)
- Using ENx control pin (BUCKx_EN bit is 1 in BUCKx_CTRL_1 register **AND** BUCKx_EN_PIN_CTRL bit is not 00 in BUCKx_CTRL_1 register)

Similarly there are two ways to enable and disable the boost regulator:

- Using BOOST_EN bit in BOOST_CTRL register (BOOST_EN_PIN_CTRL bit is 0 in BOOST_CTRL register)
- Using ENx control pin (BOOST_EN bit is 1 in BOOST_CTRL register **AND** BOOST_EN_PIN_CTRL bit is not 00 in BOOST_CTRL register)

If the ENx control pin is used for enable and disable then the delay from the control signal rising edge to startup is set by BUCKx_STARTUP_DELAY[3:0] bits in BUCKx_DELAY register and BOOST_STARTUP_DELAY[3:0] bits in BOOST_DELAY register and the delay from falling edge of control signal to shutdown is set by BUCKx_SHUTDOWN_DELAY[3:0] bits in BUCKx_DELAY register and BOOST_SHUTDOWN_DELAY[3:0] bits in BOOST_DELAY register. The delays are valid only for ENx signal transitions and not for control with I^2C writings to BUCKx_EN and BOOST_EN bits.

The control of the regulators (with 0-ms delays) is shown in Table 3.

Table 3. Regulator Control

	BUCKx_EN / BOOST_EN	BUCKx_EN_PIN_CTRL / BOOST_EN_PIN_CTRL	EN1 PIN	EN2 PIN	EN3 PIN	BUCKx OUTPUT VOLTAGE / BOOST OUTPUT VOLTAGE
Enable/disable control with BUCKx_EN/BOOST_EN bit	0	Don't Care	Don't Care	Don't Care	Don't Care	Disabled
	1	00	Don't Care	Don't Care	Don't Care	BUCKx_VSET[7:0] / BOOST_VSET[1:0]
Enable/disable control with EN1 pin	1	01	Low	Don't Care	Don't Care	Disabled
	1	01	High	Don't Care	Don't Care	BUCKx_VSET[7:0] / BOOST_VSET[1:0]
Enable/disable control with EN2 pin	1	10	Don't Care	Low	Don't Care	Disabled
	1	10	Don't Care	High	Don't Care	BUCKx_VSET[7:0] / BOOST_VSET[1:0]

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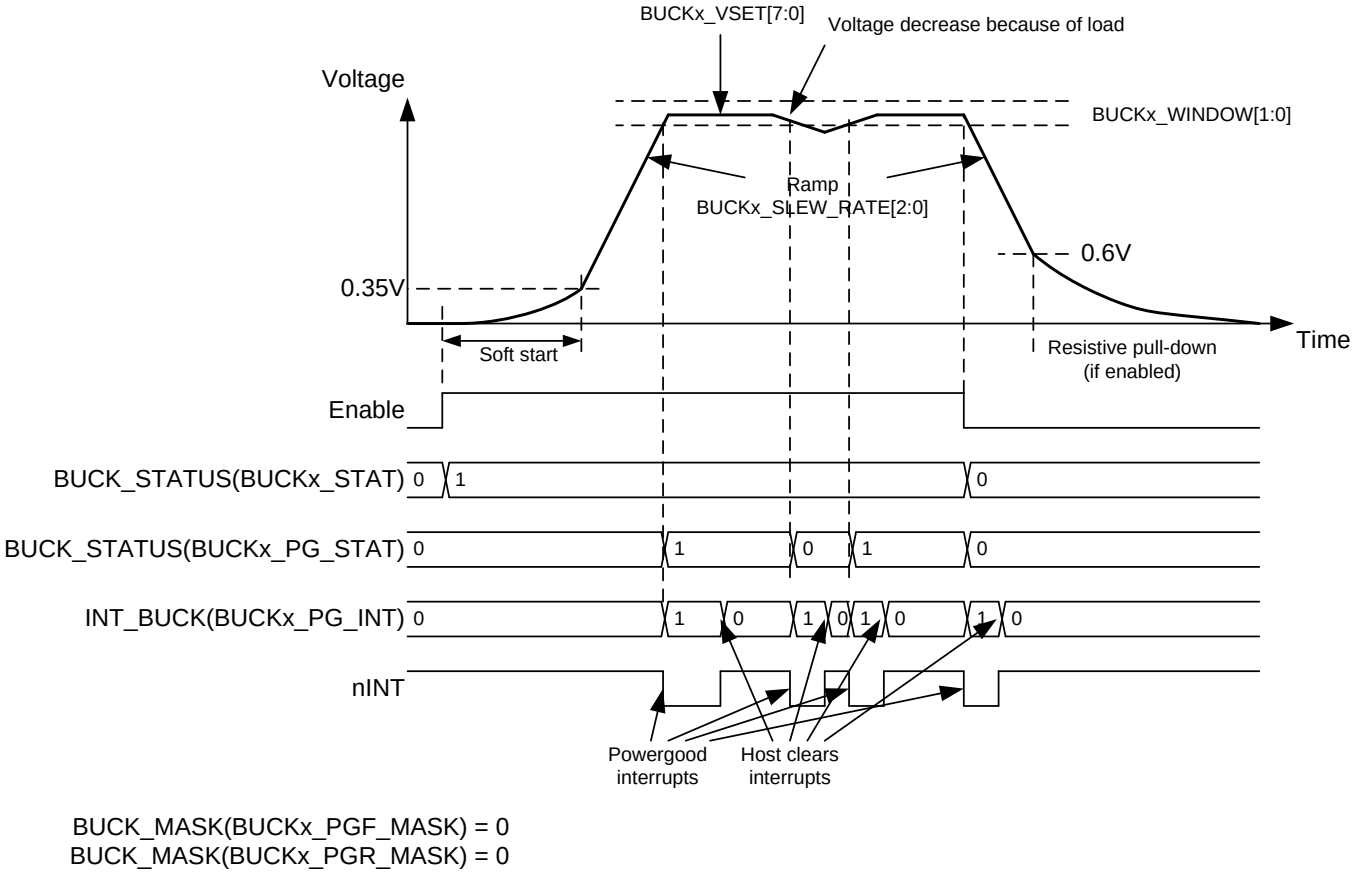
Table 3. Regulator Control (continued)

	BUCKx_EN / BOOST_EN	BUCKx_EN_PIN_CTRL / BOOST_EN_PIN_CTRL	EN1 PIN	EN2 PIN	EN3 PIN	BUCKx OUTPUT VOLTAGE / BOOST OUTPUT VOLTAGE
Enable/disable control with EN3 pin	1	11	Don't Care	Don't Care	Low	Disabled
	1	11	Don't Care	Don't Care	High	BUCKx_VSET[7:0] / BOOST_VSET[1:0]

The Buck regulator is enabled by the EN pin or by I^2C writing as shown in Figure 5. The soft-start circuit limits the in-rush current during start-up. Output voltage increase rate is typically 30 mV/µsec during soft-start. When the output voltage rises to 0.35-V level, the output voltage becomes slew-rate controlled. If there is a short circuit at the output and the output voltage does not increase above a 0.35-V level in 1 ms, the regulator is disabled, and interrupt is set. When the output voltage rises above the undervoltage power-good threshold level the BUCKx_PG_INT interrupt flag in INT_BUCK register is set.

Powergood thresholds are defined by BUCKx_WINDOW bits. A PGOOD_WINDOW bit in PGOOD_CTRL register sets the detection method for the valid buck output voltage, either undervoltage detection or undervoltage and overvoltage detection. The powergood interrupt flag when reaching valid output voltage can be masked using BUCKx_PGR_MASK bit in BUCK_MASK register. The powergood interrupt flag can be also generated when the output voltage becomes invalid. The interrupt mask for invalid output voltage detection is set by BUCKx_PGF_MASK bit in BUCK_MASK register. When window monitoring (under and overvoltage monitoring) is selected, mask bits apply when voltage is crossing either threshold. A BUCKx_PG_STAT bit in BUCK_STAT register shows always the validity of the output voltage; '1' means valid and '0' means invalid output voltage.



BUCK_MASK(BUCKx_PGF_MASK) = 0
BUCK_MASK(BUCKx_PGR_MASK) = 0

Figure 5. Buck Regulator Enable and Disable

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The boost regulator is enabled by the EN pin or by I²C writing as shown in Figure 6. The soft-start circuit limits the in-rush current during start-up. Output voltage increase rate is less than 100 mV/µsec during soft-start. If there is a short circuit at the output and the output voltage does not reach 2.5-V level in 1 ms, the regulator is disabled, and interrupt is set. When the output voltage reaches the powergood threshold level the BOOST_PG_INT interrupt flag in INT_BOOST register is set.

Powergood thresholds are defined by BOOST_WINDOW bits. A PGOOD_WINDOW bit in PGOOD_CTRL register sets the detection method for the valid boost output voltage, either undervoltage detection or undervoltage and overvoltage detection. The powergood interrupt flag when reaching valid output voltage can be masked using BOOST_PGR_MASK bit in BOOST_MASK register. The powergood interrupt flag can be also generated when the output voltage becomes invalid. The interrupt mask for invalid output voltage detection is set by BOOST_PGF_MASK bit in BOOST_MASK register. A BOOST_PG_STAT bit in BOOST_STAT register shows always the validity of the output voltage; '1' means valid and '0' means invalid output voltage.

The ENx input pins have integrated pulldown resistors. The pulldown resistors are enabled by default and host can disable those with ENx_PD bits in CONFIG register.

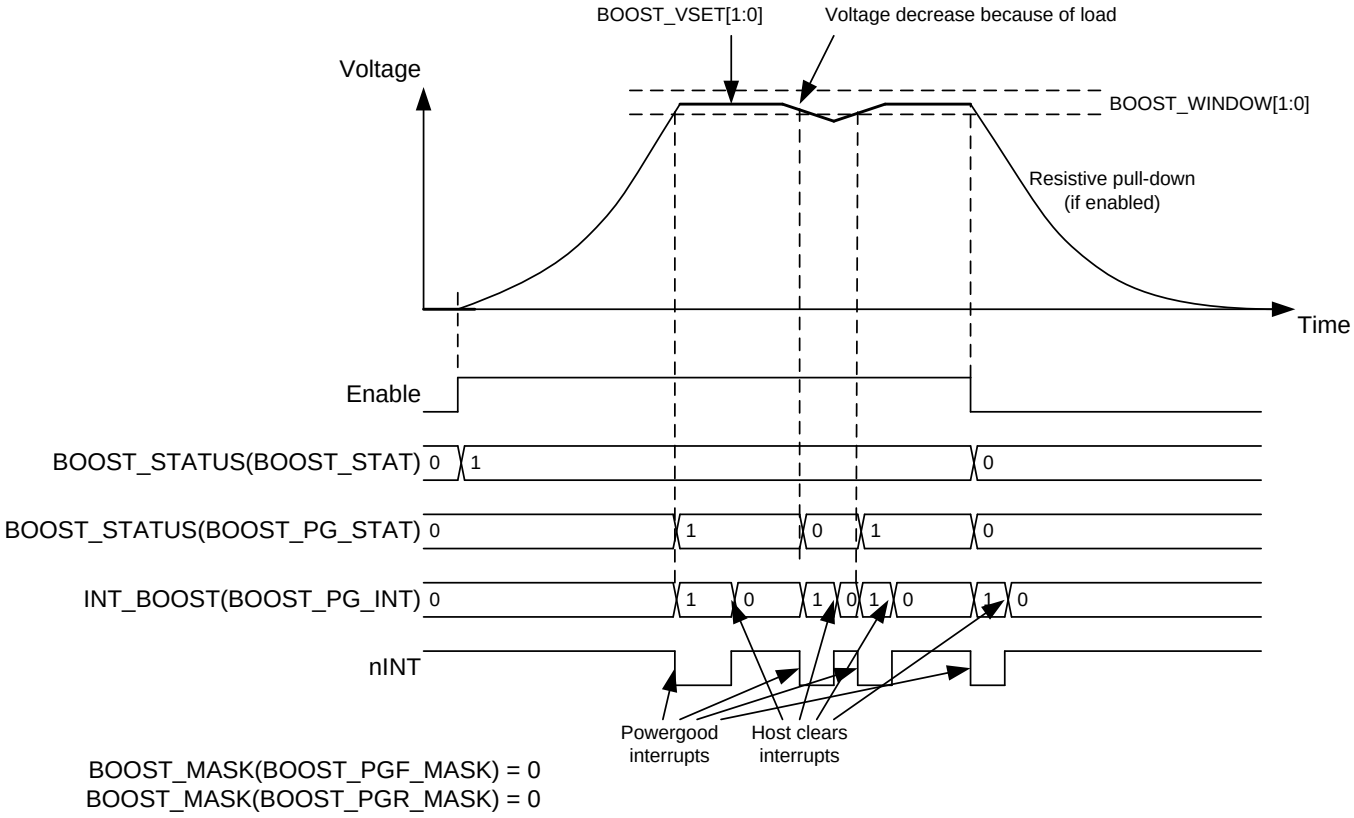

Figure 6. Boost Regulator Enable and Disable

7.3.6.2 Changing Buck Output Voltage

The output voltage of the buck regulator can be changed by writing to the BUCKx_VOUT register. The voltage change for buck regulator is always slew-rate controlled, and the slew-rate is defined by the BUCKx_CTRL_2(BUCKx_SLEW_RATE[2:0]) bits. During voltage change the forced PWM mode is used automatically. When the programmed output voltage is achieved, the mode becomes the one defined by load current, and the BUCKx_FPWM bit.

The voltage change and powergood interrupts are shown in Figure 7.

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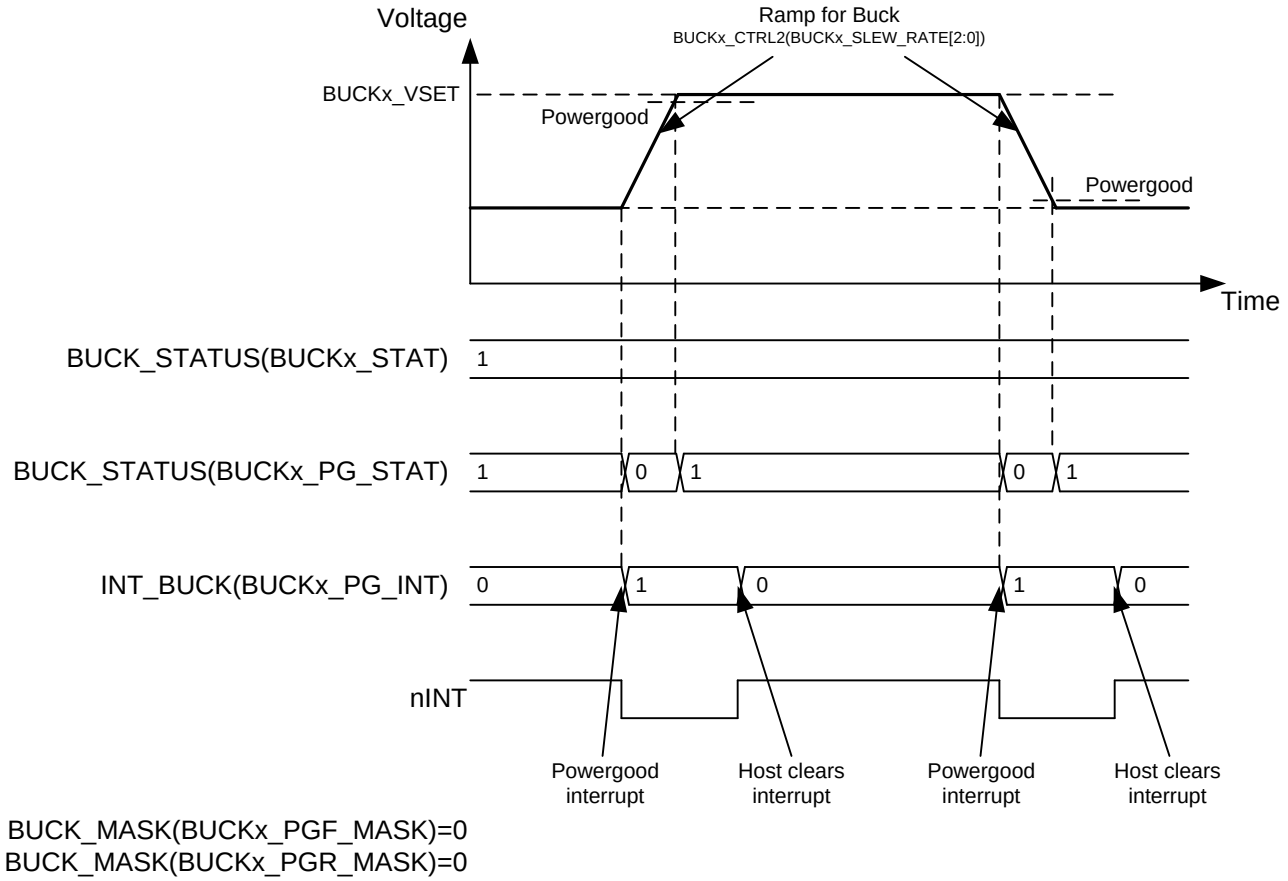

Figure 7. Regulator Output Voltage Change

7.3.7 Enable and Disable Sequences

The LP87702-Q1 device supports programmable start-up and shutdown sequencing. An EN control signal is used to initiate the start-up sequence and to turn off the device according to the programmed shutdown sequence. The buck regulator is selected for sequence control with:

- BUCKx_CTRL_1(BUCKx_EN) = 1
- BUCKx_CTRL_1(BUCKx_EN_PIN_CTRL) = 0x1 or 0x2 or 0x3, for EN1 or EN2 or EN3 control, respectively
- BUCKx_VOUT.(BUCKx_VSET[7:0]) = Required voltage when EN pin is high
- The delay from rising edge of EN pin to the regulator enable is set by BUCKx_DELAY(BUCKx_STARTUP_DELAY[3:0]) bits and
- The delay from falling edge of EN pin to the regulator disable is set by BUCKx_DELAY(BUCKx_SHUTDOWN_DELAY[3:0])

In the same way the boost regulator is selected for delayed control with:

- BOOST_CTRL(BOOST_EN) = 1
- BOOST_CTRL(BOOST_EN_PIN_CTRL) = 0x1 or 0x2 or 0x3, for EN1 or EN2 or EN3 control, respectively
- BOOST_CTRL(BOOST_VSET[2:0]) = Required voltage when EN pin is high
- The delay from rising edge of EN pin to the regulator enable is set by BOOST_DELAY(BOOST_STARTUP_DELAY[3:0]) bits and
- The delay from falling edge of EN pin to the regulator disable is set by BOOST_DELAY(BOOST_SHUTDOWN_DELAY[3:0])

An example of start-up and shutdown sequences for buck regulators are shown in Figure 8. The start-up and shutdown delays for Buck0 regulator are 1 ms and 4 ms and for Buck1 regulator 3 ms and 1 ms. The delay settings are used only for enable/disable control with EN signal.

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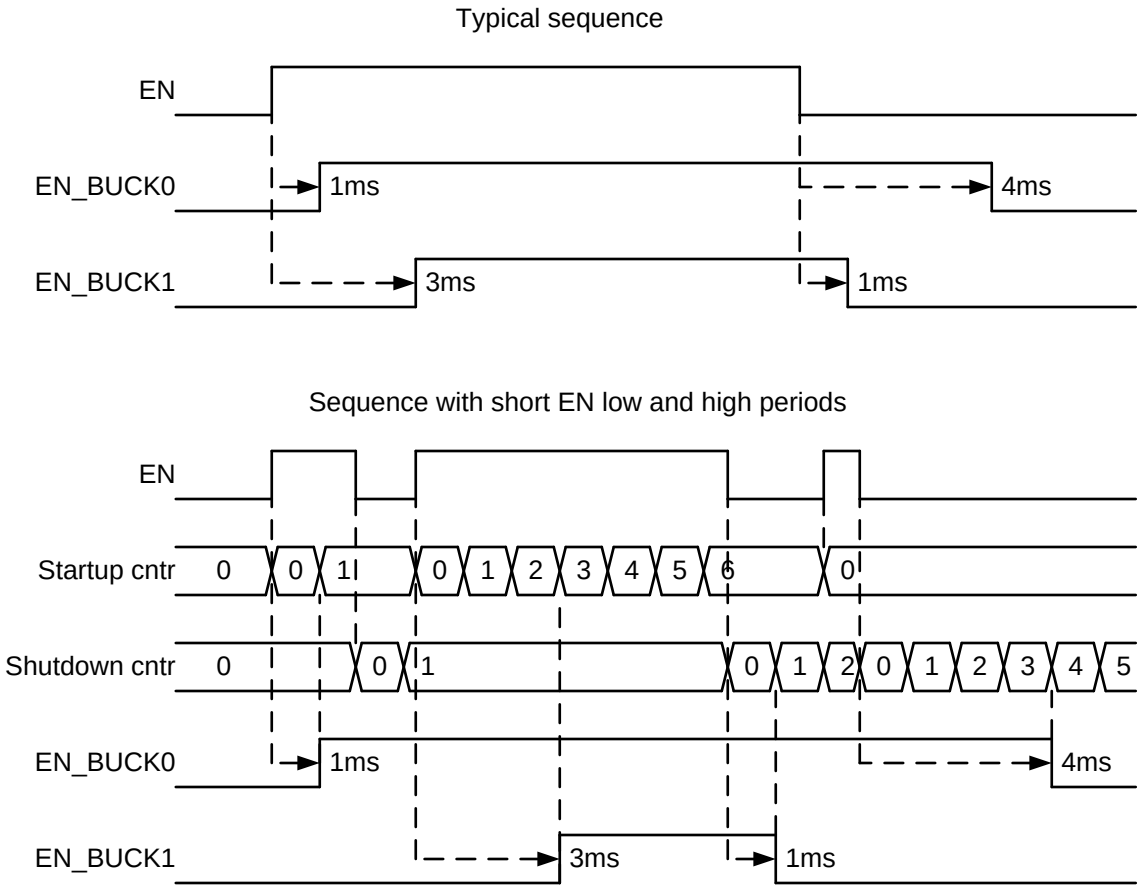

Figure 8. Startup and Shutdown Sequencing

7.3.8 Window Watchdog

Operation of the LP87702-Q1 watchdog is shown in Figure 9. Operation is shown for a case where ENx pin is used for controlling power sequence and ENx pin is active.

WDI is the external input pin for the watchdog and WD_RESET is the reset output. WD_RESET output polarity and mode, push-pull or open drain, are programmable. During device start-up the OTP settings are read, including watchdog defaults. Watchdog default settings in WD_CTRL_1 and WD_CTRL_2 register can be over-written via I2C (until WD_LOCK bit is set). This can be used to extend the Long Open -period: I2C write to either of these registers initializes the Long Open counter and the Long Open period restarts (except in Stop mode). Writing WD_LOCK = 1 in WD_CTRL_2 register locks watchdog settings until next NRST, power cycle or register reset SW_RESET.

Long Open, Close and Open window periods are independently programmable as shown in Table 4. When Long Open or Open window expires before WDI input is received, watchdog enters WD Reset state. Also when WDI is received during Close window, watchdog enters WD Reset.

LP87702-Q1 behavior after WD expiration is programmable :

- When WD_RESET_CNTR_SEL = 00, system restart is disabled and regulators are maintained ON. WD_RESET pin is active for 10 ms. Watchdog returns to Long Open mode.
- When WD_RESET_CNTR_SEL = 01 (restart after first reset pulse), LP87702-Q1 performs shutdown sequence followed by startup sequence so the regulators are disabled and re-enabled according to the OTP programmed sequences. During startup, device reloads OTP defaults when WD_EN_OTP_READ = 1. Settings valid before shutdown are maintained when WD_EN_OTP_READ = 0. WD_RESET output pin is active for a period of (10 ms + maximum shutdown delay). Maximum shutdown delay can be selected as 7.5 ms (SHUTDOWN_DELAY_SEL = 0) or 15 ms (SHUTDOWN_DELAY_SEL = 1). After the restart watchdog returns to Long Open mode.

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- Status bit WD_SYSTEM_RESTART_FLAG is set to indicate that system restart has happened. Status can be cleared by writing "1" to WD_CLR_SYSTEM_RESTART_FLAG. WD_RESET_CNTR_SEL can be set to 10 or 11 to select restart after 2 or 4 WD expirations, respectively. Current status of reset counter is available in WD_RESET_CNTR_STATUS. Reset counter can be cleared by writing WD_CLR_RESET_CNTR to 1.
- Watchdog can also be programmed to perform shutdown sequence and enter STOP mode after the second WD expiration. In STOP mode regulators are OFF. WD_RESET output pin is activated for a period of (10 ms + maximum shutdown delay), in STOP mode WD_RESET is inactive. NRST, power cycle, register reset SW_RESET, writing WD_CLR_SYSTEM_RESTART_FLAG = 1 or writing WD_SYSTEM_RESTART_FLAG_MODE = 0 is required to recover. This WD operating mode is selected by setting OTP bit WD_SYS_RESTART_FLAG_MODE = 1.

Watchdog settings in WD_CTRL_1 and WD_CTRL_2 registers are locked by setting WD_LOCK bit. WD_SYSTEM_RESTART_FLAG and WD_RESET_CNTR_STATUS can be cleared even if WD_LOCK = 1.

Description above is for a case where ENx pin is used for controlling power sequence and ENx pin is active. Depending on OTP settings and ENx pin state watchdog behavior can be slightly different:

- When ENx pin is used for controlling power sequence and ENx pin is not active, shutdown sequence can not be performed. WD_RESET pulse length is fixed 31 ms.
- When ENx pins are not used for power sequence control and all regulators and GPOs enabled via I2C, there is no OTP defined power sequence. WD expiration does not cause regulator disable/enable sequence even when OTP settings for watchdog are such that restart is enabled. In this case WD_RESET pulse is 11 ms.

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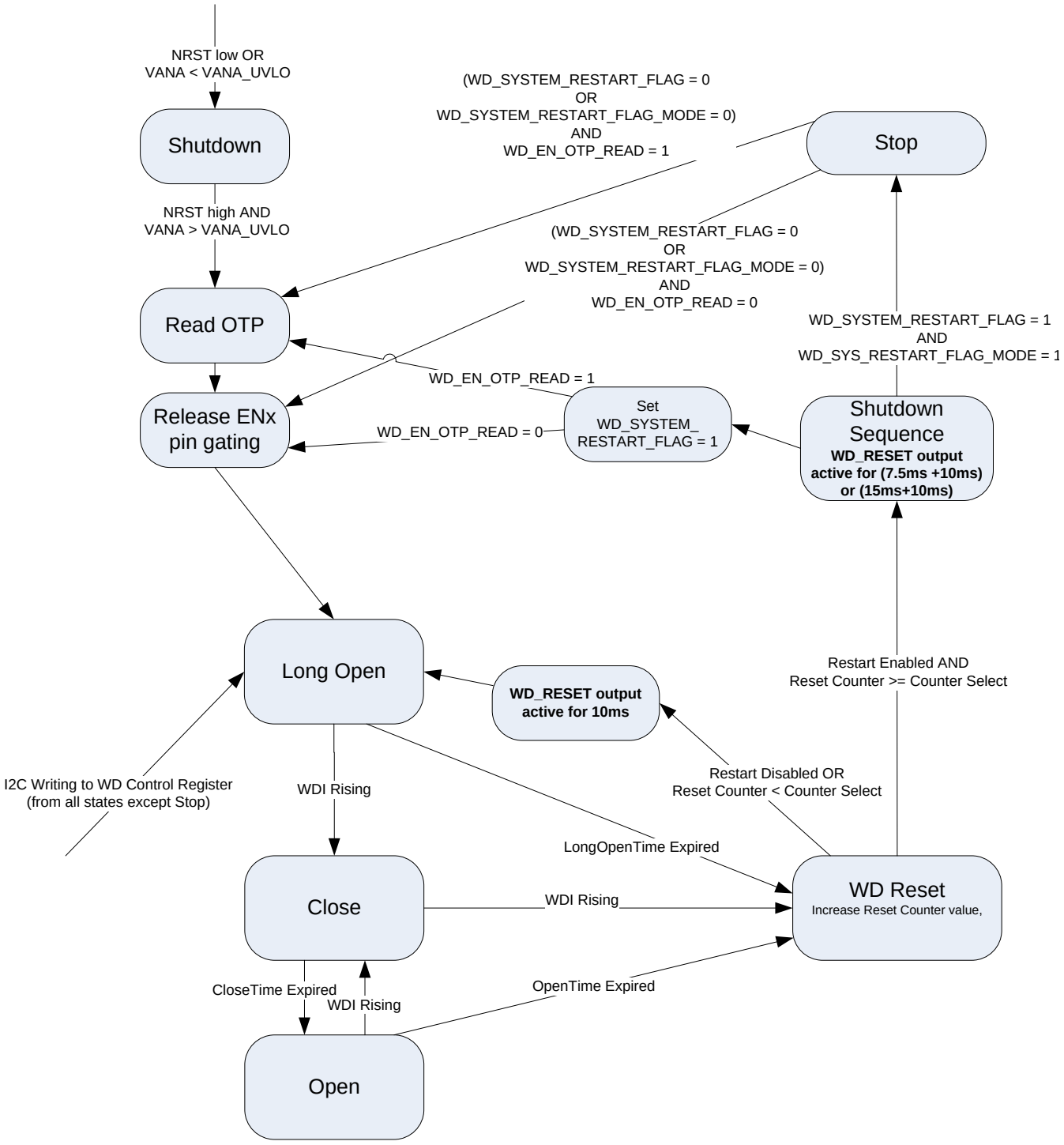

Figure 9. Watchdog Operation

Table 4. Watchdog Window Periods

CONTROL BIT	DEFAULT	VALUES
WD_LONG_OPEN_TIME	OTP	00 - 200 ms 01 - 600 ms 10 - 2000 ms 11 - 5000 ms

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Table 4. Watchdog Window Periods (continued)

CONTROL BIT	DEFAULT	VALUES
WD_CLOSE_TIME	OTP	00 - 10 ms 01 - 20 ms 10 - 50 ms 11 - 100 ms
WD_OPEN_TIME	OTP	00 - 20 ms 01 - 100 ms 10 - 600 ms 11 - 2000 ms

LP87702-Q1 supports option to disable watchdog. WD_DIS pin function is multiplexed with CLKIN/GPIO2 functions. Watchdog disable is not supported by P87702D.

7.3.9 Device Reset Scenarios

There are four reset methods implemented on the LP87702-Q1:

- Software reset with SW_RESET bit in RESET register
- NRST input signal low
- Undervoltage lockout (UVLO) reset from VANA supply
- Watchdog expiration (depending on watchdog settings)

A SW reset occurs when SW_RESET bit is written 1. The bit is automatically cleared after writing. This event disables all the regulators immediately, drives GPO signals low, resets all the register bits to the default values and OTP bits are loaded (see Figure 15). I^2C interface is not reset during software reset. The host must wait at least 1.2 ms after writing SW reset until making a new I2C read or write to the device.

If VANA supply voltage falls below UVLO threshold level or NRST signal is set low then all the regulators are disabled immediately, GPO signals are driven low and all the register bits are reset to the default values. When the VANA supply voltage rises above UVLO threshold level AND NRST signal rises above threshold level, OTP bits are loaded to the registers and a start-up is initiated according to the register settings. The host must wait at least 1.2 ms before reading or writing to I2C interface.

Depending on watchdog settings, watchdog expiration can reset the device to OTP default values.

7.3.10 Diagnostics and Protection Features

The LP87702-Q1 is capable of providing four levels of protection features:

- Information of input and output voltage which sets interrupt or PGx signal;
  - Validity of the output voltage of BUCK or BOOST regulators
  - Validity of VANA, VMON1 and VMON2 input voltages
- Warnings for diagnosis which sets interrupt
  - Peak current limit detection in BUCK or BOOST regulators
  - Thermal warning
- Protection events which are disabling the regulators
  - Short-circuit and overload protection for BUCK and BOOST regulators
  - Input overvoltage protection ($VANA_{OVP}$)
  - Watchdog expiration
  - Thermal shutdown
- Faults which are causing the device to shutdown
  - Undervoltage lockout ($VANA_{UVLO}$)

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7.3.10.1 Voltage Monitorings

The LP87702-Q1 device has programmable voltage monitoring for the BUCK and BOOST regulator output voltages and for VANA, VMON1 and VMON2 inputs. Monitoring of each signal is independently enabled in PGOOD_CTRL register. Voltage monitoring can be under-voltage monitoring only (PGOOD_WINDOW = 0) or overvoltage and undervoltage monitoring (PGOOD_WINDOW = 1). This selection is common for all enabled monitorings. Enabled monitoring signals are combined to generate powergood (PG0, PG1) and/or interrupts as described in Power-Good Information to Interrupt and PG0 and PG1 pins. Monitoring comparators have a dedicated reference and bias block, which is independent of the main reference and bias block.

Nominal level for the output voltage of BUCKx regulator is set with BUCKx_VSET. Overvoltage and undervoltage detection levels, with respect to nominal level, are selected with BUCKx_WINDOW as ± 30 mV, ± 50 mV, ± 70 mV or ± 90 mV. Nominal level for the output voltage of BOOST regulator is set with BOOST_VSET. Available levels are 4.9 V, 5 V, 5.1 V and 5.2 V. Overvoltage and undervoltage detection levels, with respect to nominal level, are selected with BOOST_WINDOW as 2%, ± 4%, ± 6% or ± 8%.

Input voltage of LP87702-Q1 is monitored at VANA pin. Nominal level can be selected as 3.3 V or 5 V with VANA_THRESHOLD bit. Overvoltage and undervoltage detection levels are selected with VANA_WINDOW as ± 5% or ± 10% (nominal).

VMON1 and VMON2 inputs can be used for monitoring external rails in system. Nominal value for the input level of VMONx is selected with VMONx_THRESHOLD, between 0.65 V to 1.8 V. Higher voltage levels or levels not directly supported can be monitored using an external resistor divider. In this case VMONx_THRESHOLD must be set as 0.65V to have high-impedance input and the resistor divider must scale the monitored level down to 0.65V at VMONx pin. Overvoltage and undervoltage detection levels are selected with VMONx_WINDOW as ± 2%, ± 3%, ± 4% or ± 6%.

For more details on the accuracy of the monitoring windows and deglitch filtering see Specifications.

7.3.10.2 Interrupts

The LP87702-Q1 sets the flag bits indicating what protection or warning conditions have occurred, and the nINT pin is pulled low. nINT is released again after a clear of flags is complete. The nINT signal stays low until all the pending interrupts are cleared.

When a fault is detected, it is indicated by a RESET_REG_INT interrupt flag in INT_TOP_2 register after next start-up.

Table 5. Summary of Interrupt Signals

EVENT	SAFE STATE	INTERRUPT BIT	INTERRUPT MASK	STATUS BIT	RECOVERY/INTERRUPT CLEAR
Buck current limit triggered (20-µs debounce)	No effect	BUCK_INT = 1 BUCKx_ILIM_INT = 1	BUCKx_ILIM_MASK	BUCKx_ILIM_STAT	Write 1 to BUCKx_ILIM_INT bit Interrupt is not cleared if current limit is active
Boost current limit triggered	No effect	BOOST_INT = 1 BOOST_ILIM_INT = 1	BOOST_ILIM_MASK	BOOST_ILIM_STAT	Write 1 to BOOST_ILIM_INT bit Interrupt is not cleared if current limit is active
Buck short circuit (V_{VOUT} < 0.35V at 1 ms after enable) or Overload (V_{VOUT} decreasing below 0.35 V during operation, 1 ms debounce)	Regulator disable	BUCKx_INT = 1 BUCKx_SC_INT = 1	N/A	N/A	Write 1 to BUCKx_SC_INT bit
Boost short circuit	Regulator disable	BOOST_INT = 1 BOOST_SC_INT = 1	N/A	N/A	Write 1 to BOOST_SC_INT bit
Thermal Warning	No effect	TDIE_WARN_INT) = 1	TDIE_WARN_MASK	TDIE_WARN_STAT	Write 1 to TDIE_WARN_INT bit Interrupt is not cleared if temperature is above thermal warning level
Thermal Shutdown	All regulators disabled immediately and GPOx set to low	TDIE_SD_INT = 1	N/A	TDIE_SD_STAT	Write 1 to TDIE_SD_INT bit Interrupt is not cleared if temperature is above thermal shutdown level
VANA Overvoltage ($VANA_{OVP}$)	All regulators disabled immediately and GPOx set to low	OVP_INT	N/A	OVP_STAT	Write 1 to OVP_INT bit Interrupt is not cleared if VANA voltage is above $VANA_{OVP}$ level

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Table 5. Summary of Interrupt Signals (continued)

EVENT	SAFE STATE	INTERRUPT BIT	INTERRUPT MASK	STATUS BIT	RECOVERY/INTERRUPT CLEAR
Buck Powergood, output voltage becomes valid	No effect	BUCK_INT = 1 BUCKx_PG_INT = 1	BUCKx_PGR_MASK	BUCKx_PG_STAT	Write 1 to BUCKx_PG_INT bit
Buck Powergood, output voltage becomes invalid	No effect	BUCK_INT = 1 BUCKx_PG_INT = 1	BUCKx_PGF_MASK	BUCKx_PG_STAT	Write 1 to BUCKx_PG_INT bit
Boost Powergood, output voltage becomes valid	No effect	BOOST_INT = 1 BOOST_PG_INT = 1	BOOST_PGR_MASK	BOOST_PG_STAT	Write 1 to BOOST_PG_INT bit
Boost Powergood, output voltage becomes invalid	No effect	BOOST_INT = 1 BOOST_PG_INT = 1	BOOST_PGF_MASK	BOOST_PG_STAT	Write 1 to BOOST_PG_INT bit
VMON1 Powergood, input voltage becomes valid	No effect	DIAG_INT = 1 VMON1_PG_INT = 1	VMON1_PGR_MASK	VMON1_PG_STAT	Write 1 to VMON1_PG_INT bit
VMON1 Powergood, input voltage becomes invalid	No effect	DIAG_INT = 1 VMON1_PG_INT = 1	VMON1_PGF_MASK	VMON1_PG_STAT	Write 1 to VMON1_PG_INT bit
VMON2 Powergood, input voltage becomes valid	No effect	DIAG_INT = 1 VMON2_PG_INT = 1	VMON2_PGR_MASK	VMON2_PG_STAT	Write 1 to VMON2_PG_INT bit
VMON2 Powergood, input voltage becomes invalid	No effect	DIAG_INT = 1 VMON2_PG_INT = 1	VMON2_PGF_MASK	VMON2_PG_STAT	Write 1 to VMON2_PG_INT bit
PGx pin changing from active to inactive state(1)	No effect	PGOOD_INT = 1	PGOOD_MASK	PGOOD_STAT	Write 1 to PGOOD_INT bit
External clock appears or disappears	No effect to regulators	SYNC_CLK_INT(2)	SYNC_CLK_MASK	SYNC_CLK_STAT	Write 1 to SYNC_CLK_INT bit
Load current measurement ready	No effect	I_MEAS_INT = 1	I_MEAS_MASK	N/A	Write 1 to I_MEAS_INT bit
Supply voltage $VANA_{UVLO}$ triggered (VANA falling)	Immediate shutdown, registers reset to default values	N/A	N/A	N/A	N/A
Supply voltage $VANA_{UVLO}$ triggered (VANA rising)	Startup, registers reset to default values and OTP bits loaded	RESET_REG_INT = 1	RESET_REG_MASK	N/A	Write 1 to RESET_REG_INT bit
Software requested reset	Immediate shutdown followed by powerup, registers reset to default values	RESET_REG_INT = 1	RESET_REG_MASK	N/A	Write 1 to RESET_REG_INT bit

(1) PGx_POL bit in PGOOD_CTRL_1 register affects only PGx pin polarity, not PGx interrupt polarity.
(2) Interrupt generated during Clock Detector operation and in case Clock is not available when Clock Detector is enabled.

7.3.10.3 Power-Good Information to Interrupt and PG0 and PG1 pins

LP87702-Q1 supports both interrupt based indication of power-good levels in various voltages and two power-good signals, PG0 and PG1. The selection of monitored signals is independent for the interrupt (nINT) and PG0, PG1 signals. Each signal can include:

- The output voltage of one or both BUCKx regulators
- The output voltage of the BOOST regulator
- Input voltage of VANA
- Input voltage of VMON1 and/or VMON2
- Thermal warning
- Thermal shutdown

The block diagram for powergood connections to PG0 and PG1 pins and interrupt is shown in Figure 10.

Monitored signals are enabled in PGOOD_CTRL register. Regulator output voltage monitoring (not current limit monitoring) can be selected for the indication. Monitoring is enabled by PGOOD_CTRL(EN_PGOOD_BUCKx) and PGOOD_CTRL(EN_PGOOD_BOOST) bits. When a regulator is disabled, the monitoring is automatically masked to prevent it forcing PGx inactive or causing an interrupt. Also monitoring of VANA, VMON1 and VMON2 inputs can be independently enabled via PGOOD_CTRL register. The type of voltage monitoring for PGx signals and nINT is selected by PGOOD_CTRL_1(PGOOD_WINDOW_x) bit. If the bit is 0, only undervoltage is monitored and if the bit is 1 both undervoltage and overvoltage are monitored. For voltage monitoring thresholds see Voltage Monitorings. Monitoring of thermal warning and thermal shutdown monitoring is always enabled.

Monitoring interrupts from all the output rails, input rails, thermal warning and thermal shutdown are combined to nINT pin. Dedicated mask bits are used to select which interrupts control the state of nINT pin. See Table 5 for summary of powergood interrups, mask bits and interrupt clearing.

Similarly, enabled monitoring signals from all the output rails, input rails, thermal warning and thermal shutdown are combined to PG0 and PG1 output pins. Register bits SEL_PGx_x in PG0_CTRL and PG1_CTRL select which of the signals control the state of PG0 and PG1, respectively. The polarity and the output type (push-pull or open-drain) of PG0 and PG1 are selected by PG_CTRL(PGx_POL) and PG_CTRL(PGx_OD) bits.

PGx is only *active* or *asserted* when all enabled power resource output voltages are within specified tolerance for each requested/programmed output voltage.

PGx is *inactive* or *de-asserted* if any enabled power resource output voltages is outside specified tolerance for each requested/programmed output voltage.

When PGx_RISE_DELAY = 1, PGx is set as *active* or *asserted* with 11 ms delay from the point of time where all enabled power resource output voltages are within specified tolerance for each requested/programmed output voltage.

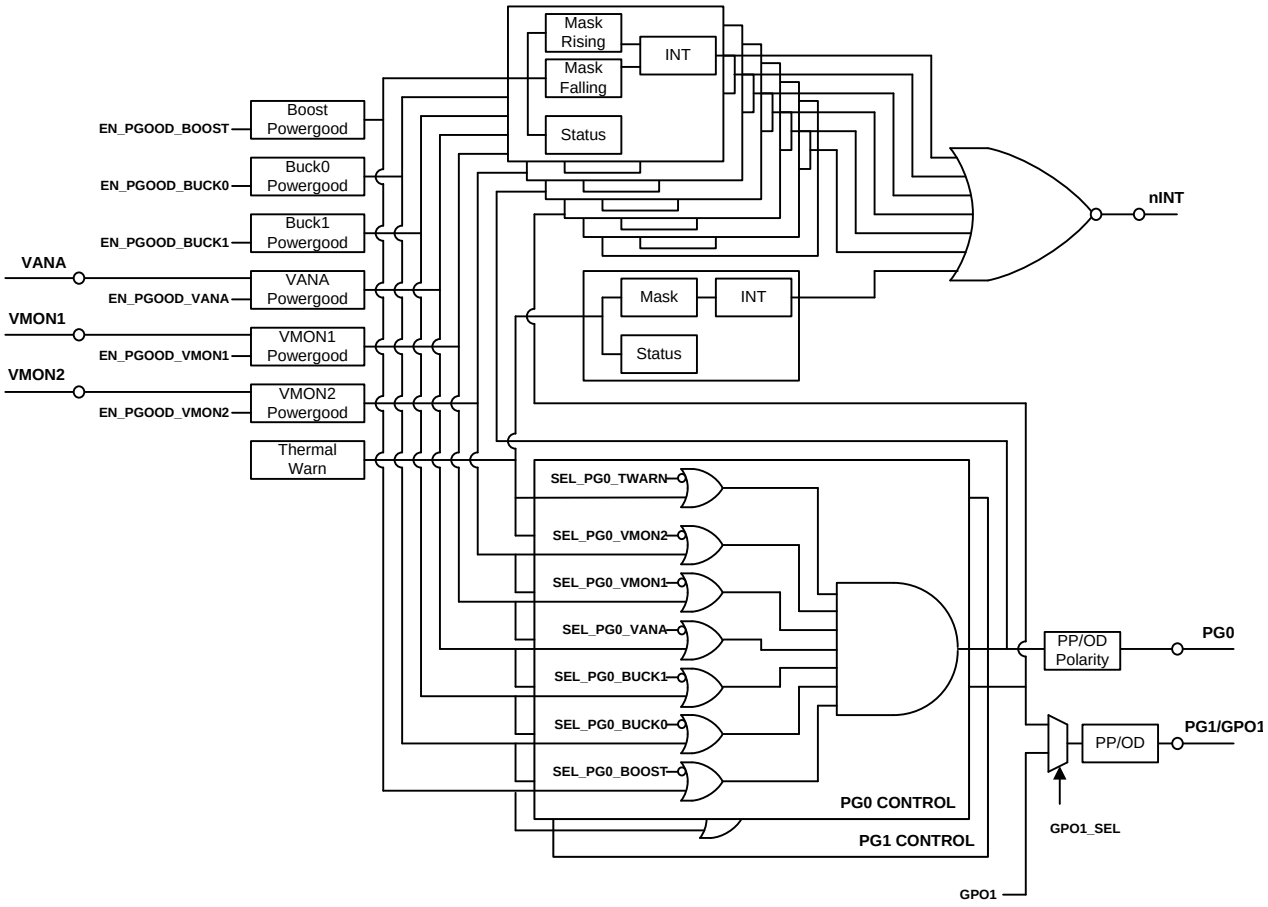

Figure 10. Block Diagram of Power-Good Connections

LP87702-Q1 power-good detection has two operating modes, selected in OTP: gated (that is, *unusual*) or continuous (that is, *invalid*) mode of operation. These modes are described in PGx Pin Gated (Unusual) Mode and in PGx pin Operation in Continuous Mode.

7.3.10.3.1 PGx Pin Gated (Unusual) Mode

In this mode the PGx signal detects unexpected or unusual situations. Mode is selected by setting PGx_MODE bit to 0 in PG_CTRL register.

For the gated mode of operation, PGx behaves as follows:

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- PGx is set to active or asserted state upon exiting OTP configuration as an initial default state.
- For each enabled rail PGx status is suspended or unchanged during an 800-µs gated time period from the enable activation, thereby *gating-off* the status indication.
- During normal power-up sequencing and requested voltage changes, PGx state typically remains *active* or *asserted* for normal conditions.
- During an abnormal power-up sequencing and requested voltage changes, PGx status could change to *inactive* or *de-asserted* after an 800-µs gated time period if any output voltage is outside of regulation range.
- Using the gated mode of operation could allow the PGx signal to initiate an immediate power shutdown sequence if the PGx signal is wired-OR with signal connected to EN input. This type of circuit configuration provides a smart PORz function for processor that eliminates the need for additional components to generate PORz upon start-up and to monitor voltage levels of key voltage domains.

PGx signal is set inactive if the output voltage of a monitored Buck or Boost regulator is invalid or the output voltage is not valid at 800 µs from the enable of the regulator. This should be considered when selecting the BUCKx_SLEW_RATE setting. To avoid PGx triggering at start-up keep the sum of soft start time and slew rate controlled part of voltage ramp below 800 µs. In addition when invalid input voltage at VANA, VMON1 or VMON2 pin is detected PGx is inactive.

Mode 0 is selected by setting PG_CTRL(PGx_MODE) bit to 0. Detected fault sets the corresponding fault bit in PG0_FAULT or in PG0_FAULT register. The detected fault must be cleared to continue the PGx monitoring. The over-voltage and thermal shutdown are cleared by writing 1 to the OVP_INT and TDIE_SD_INT interrupt bits in INT_TOP_1 register. The regulator fault is cleared by writing 1 to the corresponding register bit in PGx_FAULT register. An example of PGx pin operation in Mode 0 is shown in and the different use cases for PGx signal operation are summarized in Table 6.

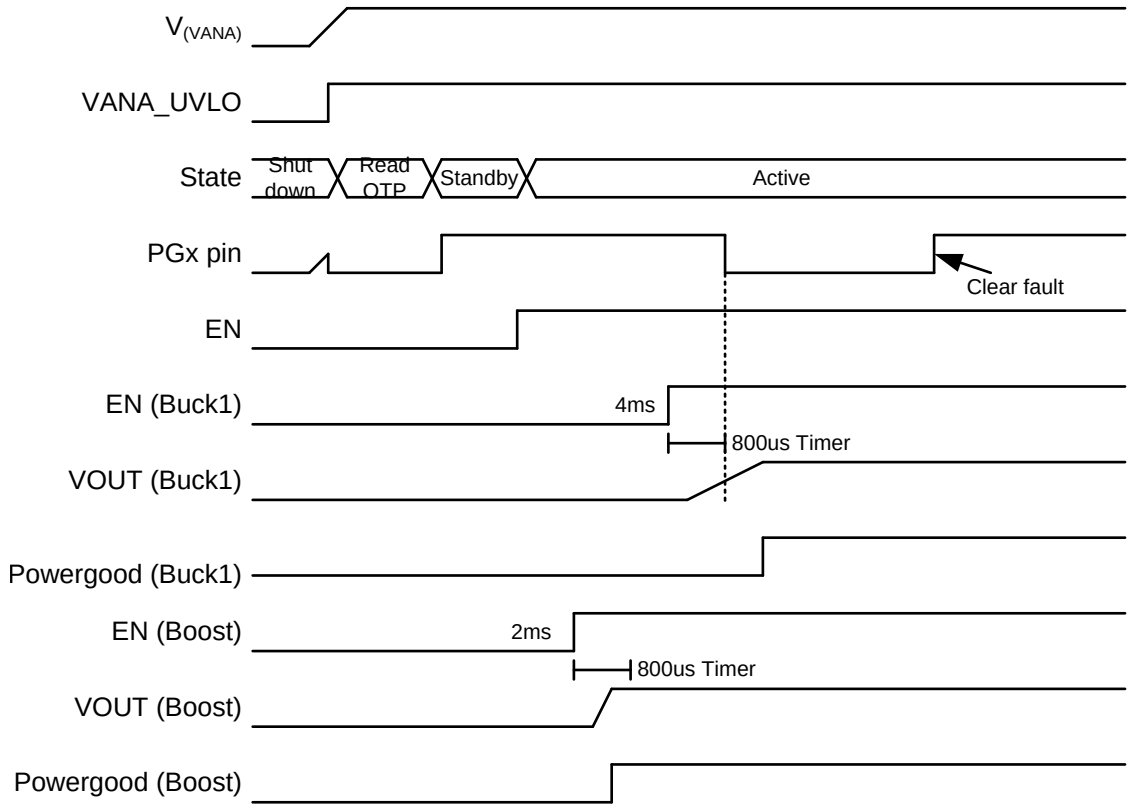

Figure 11. PGx Pin Operation in Gated Mode.

7.3.10.3.2 PGx pin Operation in Continuous Mode

In this mode the PGx signal shows the validity of the requested voltages continuously. Mode is selected by setting PGx_MODE bit to 1 in PG_CTRL register.

For the continuous mode of operation, PGx behaves as follows:

- PGx is set to *active* or *asserted* state upon exiting OTP configuration as an initial default state.
- PGx is set to *inactive* or *de-asserted* as soon as regulator is enabled.
- PGx status begins indicating output voltage regulation status immediately and continuously.
- During power-up sequencing and requested voltage changes, PGx will toggle between *inactive* or *deasserted* while output voltages are outside of regulation ranges and active or asserted when inside of regulation ranges.

When invalid output voltage of monitored regulator is detected, corresponding PG0_FAULT_x or PG1_FAULT_x bit is set to 1 and PGx signal becomes inactive. The PG0_FAULT and PG1_FAULT register bits are latched and maintain the fault information until host clears the fault bit by writing 1 to the bit. The PGx signal indicates also interrupts from VANA, VMON1 and VMON2 inputs and thermal warning and shutdown. All are cleared by clearing the interrupt bits.

When regulator voltage is transitioning from one target voltage to another, the PGx signal is set inactive.

When PGx signal becomes inactive, the source for the fault can be read from PG_FAULT register. If the invalid output voltage becomes valid again the PGx signal becomes active. Thus the PGx signal shows all the time if the monitored output voltages are valid. The block diagram for this operation is shown in Figure 12.

The PGx signal can be also configured so that it maintains inactive state even when the monitored outputs are valid but there are PG_FAULT_x bits pending clearance. This type of operation is selected by setting PGFAULT_GATES_PGOOD bit to 1.

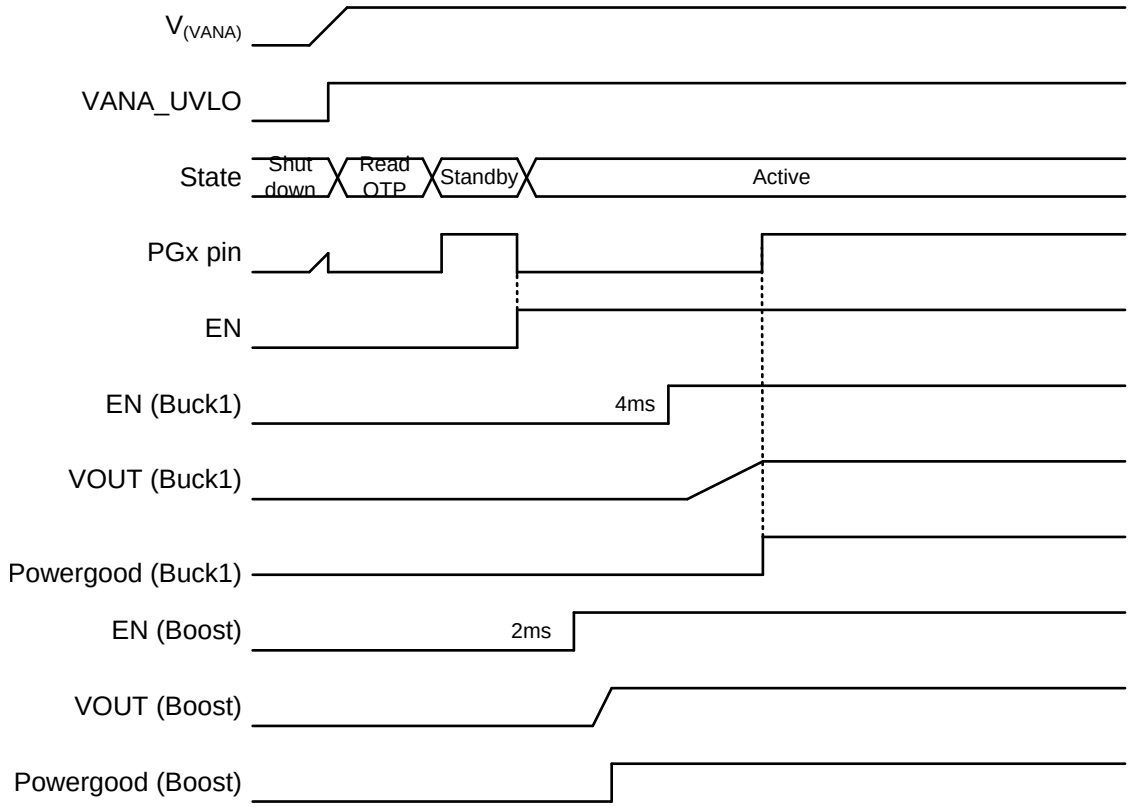

Figure 12. PGx Pin Operation in Continuous Mode

7.3.10.3.3 Summary of PG0, PG1 Gated and Continuous Operating Modes

Table 6summarizes the PGx behavior in different application scenarios, for the gated and continuous operating modes.

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Table 6. PGx Operation

STATUS / USE CASE	CONDITION	PGx SIGNAL (1) (2)	
		Gated mode PGOOD_MODE = 0	Continuous mode PGOOD_MODE
Device startup	Until device state is STANDBY	Low	Low
Regulator not selected for PGx monitoring	EN_PGOOD_x = 0	OK	OK
Regulator selected for PGx monitoring and disabled by host	BUCKx_EN / BOOST_EN = 0 OR (Pin ctrl AND EN = 0)	OK	OK
Regulator start-up delay ongoing	EN = 1	OK	NOK
Regulator start-up until valid output voltage reached	Valid output voltage reached in 800 µs	OK	NOK
Regulator startup until valid output voltage reached	Valid output voltage not reached at 800 µs	NOK	NOK
Output voltage within window limits after start-up	Must be inside limits longer than debounce time	OK	OK
Output voltage spikes (over/undervoltage)	If spikes are outside voltage monitoring threshold(s) longer than debounce time	NOK	NOK
Voltage setting change, output voltage ramp		OK (if new voltage reached in 800 µs) NOK after 800 µs (if new voltage not reached at 800 µs)	NOK
Output voltage within window limits after voltage change	Must be inside limits longer than debounce time	OK	OK
Regulator shutdown delay ongoing		OK	OK
Buck regulator disabled by host, slew-rate controlled ramp down ongoing		OK	OK
Regulator disabled by host, pulldown resistor active (if selected)		OK	OK
Regulator short-circuit interrupt pending (regulator selected for PGx monitoring)	Faulty regulator disabled by short-circuit detection BUCKx_SC_INT / BOOST_SC_INT = 1	NOK	NOK
Thermal shutdown interrupt pending	Regulators disabled by thermal shutdown detection TDIE_SD_INT = 1	NOK	NOK
Input (VANA) overvoltage interrupt pending	Regulators disabled by overvoltage detection OVP_INT = 1	NOK	NOK
Supply voltage below $VANA_{UVLO}$		Low	Low

(1) NOK (Not OK) means faulty situation. PGx pin is inactive if at least one NOK situation is detected.
(2) PGx pin is generated from PG_FAULT register bits and INT_TOP_1 register bits TDIE_SD_INT, OVP_INT and INT_TOP_2(RESET_REG_INT) bit.

7.3.10.4 Warnings for Diagnosis (Interrupt)

7.3.10.4.1 Output Power Limit

The Buck regulators have programmable output peak current limits. The limits are individually programmed for both regulators with BUCKx_ILIM[2:0] bits. If the load current is increased so that the current limit is triggered, the regulator continues to regulate to the limit current level (current peak regulation). The voltage may decrease if the load current is higher than limit current. If the current regulation continues for 20 µs, the LP87702-Q1 device sets the BUCKx_ILIM_INT bit and pulls the nINT pin low. The host processor can read BUCKx_ILIM_STAT bits to see if the regulator is still in peak current regulation mode.

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If the load is so high that the output voltage decreases below a 350-mV level, the LP87702-Q1 device disables the regulator and sets the BUCKx_SC_INT bit. In addition the BUCKx_STAT bit is set to 0. The interrupt is cleared when the host processor writes 1 to BUCKx_SC_INT bit. The Buck overload situation is shown in Figure 13.

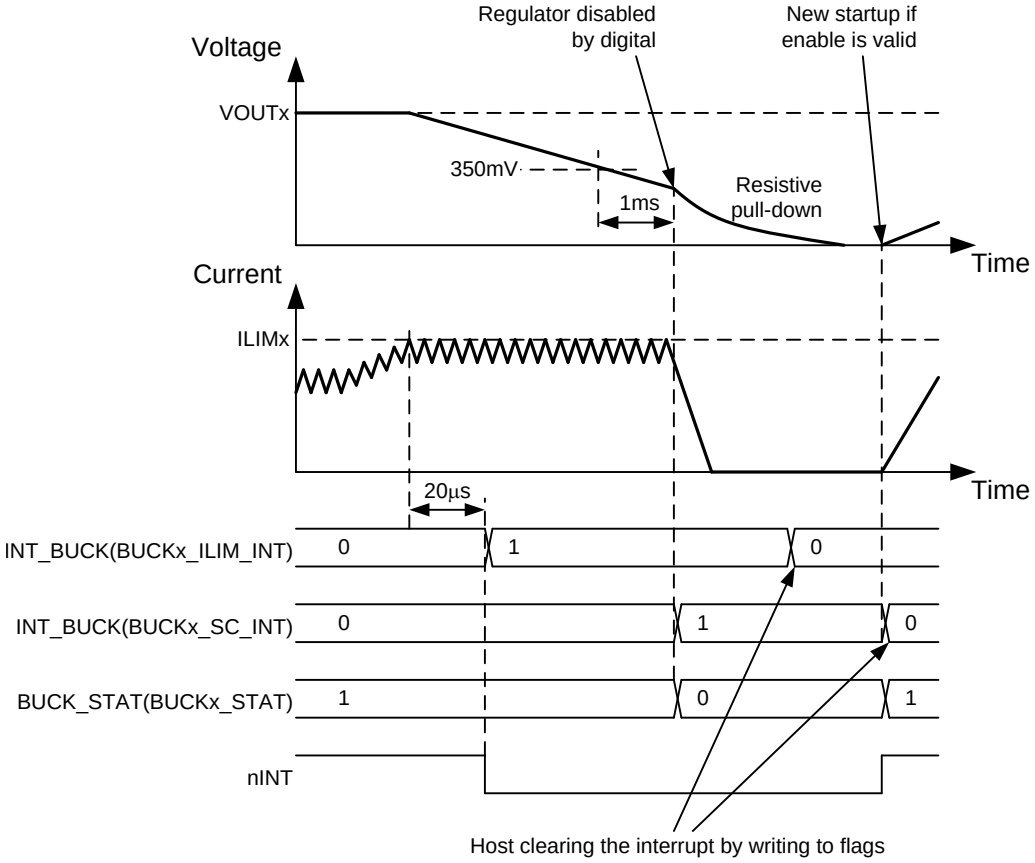

Figure 13. Buck Regulator Overload Situation

The Boost regulator has programmable output peak current limits. The limits are programmed with BOOST_ILIM bits. If the load current is increased so that the current limit is triggered, the regulator continues to regulate to the limit current level (current peak regulation). The voltage may decrease if the load current is higher than limit current. If the current regulation continues for 64 µs, the LP87702-Q1 device sets the BOOST_ILIM_INT bit and pulls the nINT pin low. The host processor can read BOOST_ILIM_STAT bits to see if the regulator is still in peak current regulation mode.

If the load is so high that the output voltage decreases below 2.5 V, the LP87702-Q1 device disables the regulator and sets the BOOST_SC_INT bit. In addition the BOOST_STAT bit is set to 0. The interrupt is cleared when the host processor writes 1 to BOOST_SC_INT bit. The Boost overload situation is shown in Figure 14.

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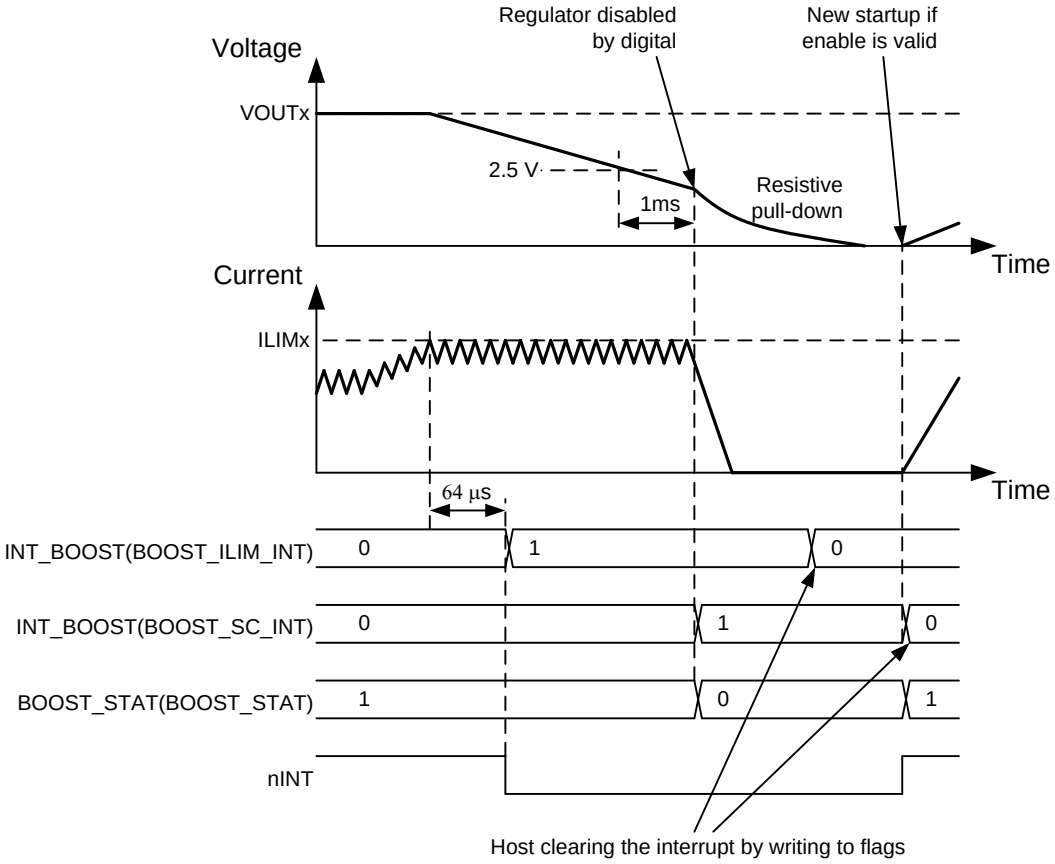

Figure 14. Boost Regulator Overload Situation

7.3.10.4.2 Thermal Warning

The LP87702-Q1 device includes a protection feature against over-temperature by setting an interrupt for host processor. The threshold level of the thermal warning is selected with TDIE_WARN_LEVEL bit.

If the LP87702-Q1 device temperature increases above thermal warning level the device sets TDIE_WARN_INT bit and pulls nINT pin low. The status of the thermal warning can be read from TDIE_WARN_STAT bit and the interrupt is cleared by writing 1 to TDIE_WARN_INT bit. The thermal warning interrupt can be masked by setting TDIE_WARN_MASK bit to 1.

7.3.10.5 Protection (Regulator Disable)

If the regulator is disabled because of protection or fault (short-circuit protection, thermal shutdown, overvoltage protection, or undervoltage lockout), the output power FETs are set to high-impedance mode, and the output pulldown resistor is enabled (if enabled with BUCKx_RDIS_EN and BOOST_RDIS_EN bits). The turnoff time of the output voltage is defined by the output capacitance, load current, and the resistance of the integrated pulldown resistor. The pulldown resistors are active as long as VANA voltage is above approximately 1.2-V level.

7.3.10.5.1 Short-Circuit and Overload Protection

A short-circuit protection feature allows the LP87702-Q1 to protect itself and external components against short circuit at the output or against overload during start-up. For buck regulators the fault threshold is 350 mV, the protection is triggered, and the buck regulator is disabled if the output voltage is below the threshold level 1 ms after the buck regulator is enabled. For boost the fault threshold is 2.5 V. Boost regulator is disabled if the output voltage is below the threshold level 1 ms after the boost regulator is enabled.

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In a similar way the overload situation is protected during normal operation. If the feedback-pin voltage of the buck regulator falls below 0.35 V and remains below the threshold level for 1 ms the buck regulator is disabled. If the output voltage of the boost regulator falls below 2.5 V and remains below the threshold level for 1 ms the boost regulator is disabled.

In the Buck regulator short-circuit and overload situations the BUCKx_SC_INT and the INT_BUCKx bits are set to 1, the BUCKx_STAT bit is set to 0 and the nINT signal is pulled low. In the boost regulator short-circuit and overload situations the BOOST_SC_INT and the BOOST_INT bits are set to 1, the BOOST_STAT bit is set to 0 and the nINT signal is pulled low. The host processor clears the interrupt by writing 1 to the BUCKx_SC_INT or BOOST_SC_INT bit. Upon clearing the interrupt the regulator makes a new start-up attempt if the regulator is in enabled state.

7.3.10.5.2 Overvoltage Protection

The LP87702-Q1 device monitors the input voltage from VANA pin in standby and active operation modes. If the input voltage rises above $VANA_{OVP}$ voltage level, all the regulators are disabled immediately (without switching ramp, no shutdown delays) pulldown resistors discharge the output voltages (BUCKx_RDIS_EN = 1 and BOOST_RDIS_EN = 1), GPOs are set to logic low level, nINT signal is pulled low, OVP_INT bit is set to 1 and BUCKx_STAT and BOOST_STAT bits are set to 0. The host processor clears the interrupt by writing 1 to the OVP_INT bit. If the input voltage is above over-voltage detection level the interrupt is not cleared. The host can read the status of the overvoltage from the OVP_STAT bit. Regulators cannot be enabled as long as the input voltage is above over-voltage detection level or the overvoltage interrupt is pending.

7.3.10.5.3 Thermal Shutdown

The LP87702-Q1 has an overtemperature protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the regulators are disabled immediately (without switching ramp, no shutdown delays), the TDIE_SD_INT bit is set to 1, the nINT signal is pulled low, and the device enters STANDBY. nINT is cleared by writing 1 to the TDIE_SD_INT bit. If the temperature is above thermal shutdown level the interrupt is not cleared. The host can read the status of the thermal shutdown from the TDIE_SD_STAT bit. Regulators cannot be enabled as long as the junction temperature is above thermal shutdown level or the thermal shutdown interrupt is pending.

7.3.10.6 Fault (Power Down)

7.3.10.6.1 Undervoltage Lockout

When the input voltage falls below $VANA_{UVLO}$ at the VANA pin, the buck and boost regulators are disabled immediately (without switching ramp, no shutdown delays), and the output capacitor is discharged using the pulldown resistor, and the LP87702-Q1 device enters SHUTDOWN. When $V_{(VANA)}$ voltage is above $VANA_{UVLO}$ threshold level, the device powers up to STANDBY state.

If the reset interrupt is unmasked by default (TOP_MASK_2(RESET_REG_MASK) = 0) the INT_TOP_2(RESET_REG_INT) interrupt indicates that the device has been in SHUTDOWN. The host processor must clear the interrupt by writing 1 to the INT_TOP_2(RESET_REG_INT) bit. If the host processor reads the INT_TOP_2(RESET_REG_INT) flag after detecting an nINT low signal, it knows that the input supply voltage has been below $VANA_{UVLO}$ level (or the host has requested reset with RESET(SW_RESET) bit), and the registers are reset to default values.

7.3.11 OTP Error Correction

LP87702-Q1 supports OTP bit error detection and 1-bit error correction per five registers. ECC_STATUS register bit SED is set if a single bit error was detected and corrected. In case two bit errors have been detected in any bank of five registers, DED bit is set.

7.3.12 GPO Signals' Operation

The LP87702-Q1 device supports up to 3 General Purpose Output (GPO) signals. The GPO1 signal is multiplexed with PG1 signal and the GPO2 signal is multiplexed with CLKIN signal. The selection between signal use are set with GPO1_SEL and GPO2_SEL bits in GPO_CONTROL_2 register.

The type of the output, either push-pull with $V_{(VANA)}$ level or open drain, are set with GPO0_OD and GPO1_PG1_OD bits in GPO_CONTROL_1 register and GPO2_OD bit in GPO_CONTROL_2 register

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The logic level of the GPOx pins are is set by GPO0_OUT and GPO1_OUT bits in GPO_CONTROL_1 register and GPO2_OUT bit in GPO_CONTROL_2 register.

The control of the GPOs can be included to start-up and shutdown sequences. The GPO control for a sequence with ENx pin is selected by GPOx_EN_PIN_CTRL bits. The delays during start-up and shutdown are set by bits in GPOx_DELAY registers.

7.3.13 Digital Signal Filtering

The digital signals have a debounce filtering. The signal/supply is sampled with a clock signal and a counter. This results as an accuracy of one clock period for the debounce window.

Table 7. Digital Signal Filtering

EVENT	SIGNAL/SUPPLY	RISING EDGE	FALLING EDGE
		LENGTH	LENGTH
Enable/Disable for BUCKx, BOOST or GPOx	ENx	3 µs (1)	3 µs (1)
VANA undervoltage lockout	VANA	Immediate (VANA voltage rising)	Immediate (VANA voltage falling)
VANA overvoltage	VANA	1 µs (VANA voltage rising)	1 µs (VANA voltage falling)
Thermal warning	TDIE_WARN_INT	20 µs	20 µs
Thermal shutdown	TDIE_SD_INT	20 µs	20 µs
Current limit, BUCKx		20 µs	20 µs
Current limit, BOOST		64 µs	64 µs
Overload	FB_B0, FB_B1, VOUT_BST	1 ms	N/V
PGx pin and powergood interrupt (voltage monitoring)	PG0, PG1 / FB_B0, FB_B1	6 µs	6 µs
PGx pin and powergood interrupt (voltage monitoring)	PG0, PG1 / VOUT_BST, VANA, VMON1, VMON2	15 µs	15 µs

(1) No glitch filtering, only synchronization.

7.4 Device Functional Modes

7.4.1 Modes of Operation

SHUTDOWN: The $V_{(VANA)}$ voltage is below $VANA_{UVLO}$ threshold level or NRST signal is low. All switch, reference, control and bias circuitry of the LP87702-Q1 device are turned off.

READ OTP: The main supply voltage $V_{(VANA)}$ is above $VANA_{UVLO}$ level and NRST signal is high. The regulators are disabled and the reference and bias circuitry of the LP87702-Q1 are enabled. The OTP bits are loaded to registers. I2C access is not allowed during OTP read. This applies also to watchdog (see Window Watchdog.

STANDBY: The main supply voltage $V_{(VANA)}$ is above $VANA_{UVLO}$ level and NRST signal is high. All registers can be read or written by the host processor via the system serial interface. Watchdog is active and WDI input is expected to toggle to avoid watchdog expiration. The regulators are disabled and the reference, control and bias circuitry of the LP87702-Q1 are enabled. The regulators can be enabled if needed.

ACTIVE: The main supply voltage $V_{(VANA)}$ is above $VANA_{UVLO}$ level and NRST signal is high. At least one regulator is enabled. All registers can be read or written by the host processor via the system serial interface. Watchdog is active and WDI input is expected to toggle to avoid watchdog expiration.

The operating modes and transitions between the modes are shown in Figure 15. For the window watchdog detailed operation see Window Watchdog.

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Device Functional Modes (continued)

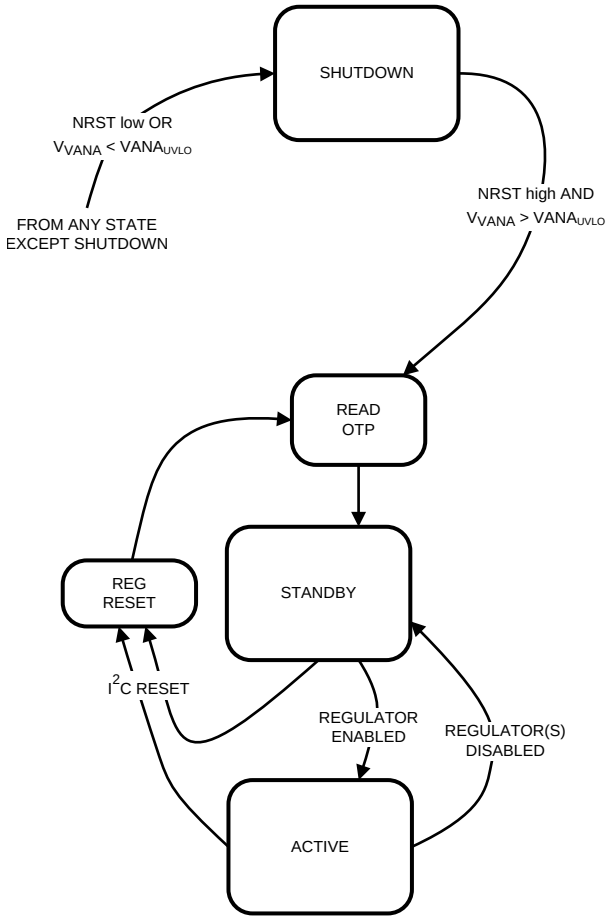

Figure 15. Device Operation Modes.

7.5 Programming

7.5.1 I²C-Compatible Interface

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the ICs connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines should each have a pull-up resistor placed somewhere on the line and remain HIGH even when the bus is idle. The LP87702-Q1 supports standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz), and high-speed mode (3.4 MHz).

7.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when clock signal is LOW.

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Programming (continued)

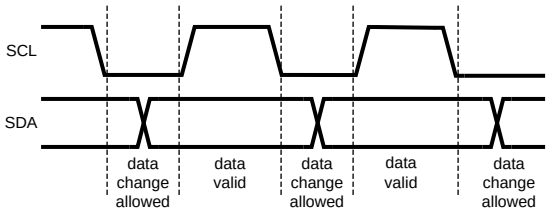

Figure 16. Data Validity Diagram

7.5.1.2 Start and Stop Conditions

The LP87702-Q1 is controlled via an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as SDA transitions from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transition from LOW to HIGH while SCL is HIGH. The I²C master always generates the START and STOP conditions.

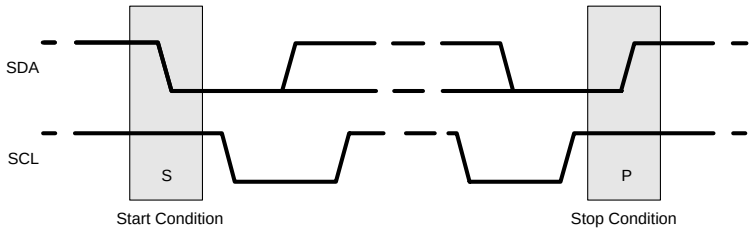

Figure 17. Start and Stop Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I²C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. Figure 18 shows the SDA and SCL signal timing for the I²C-Compatible Bus. See the Figure 1 for timing values.

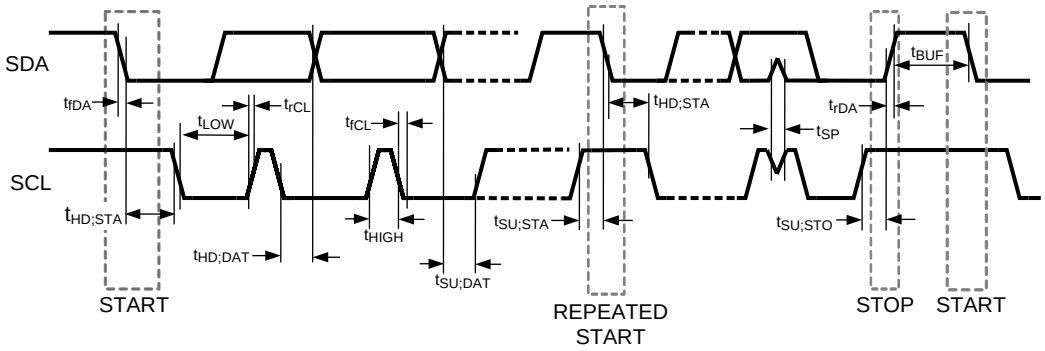

Figure 18. I²C-Compatible Timing

7.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LP87702-Q1 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LP87702-Q1 generates an acknowledge after each byte has been received.

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Programming (continued)

There is one exception to the *acknowledge after every byte* rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*) the last byte clocked out of the slave. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

NOTE

If the $V_{(VANA)}$ voltage is below $VANA_{UVLO}$ threshold level during I^2C communication the LP87702-Q1 device does not drive SDA line. The ACK signal and data transfer to the master is disabled at that time.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE and a 1 indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

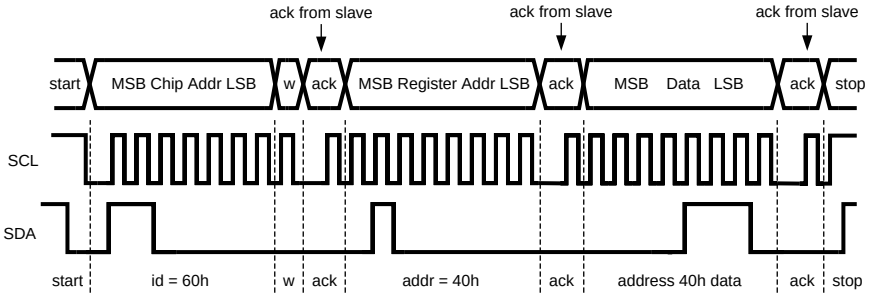
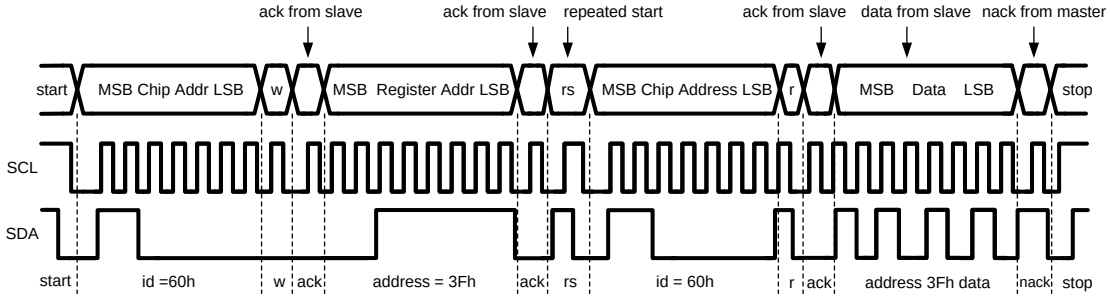


Figure 19. Write Cycle (w = write; SDA = 0), id = Device Address = 60Hex for LP87702-Q1



When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

Figure 20. Read Cycle (r = read; SDA = 1), id = Device Address = 60Hex for LP87702-Q1

7.5.1.4 I^2C-Compatible Chip Address

The device address for the LP87702-Q1 is 0x60. After the START condition, the I^2C master sends the 7-bit address followed by an eighth bit, read or write (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data will be written. The third byte contains the data for the selected register.

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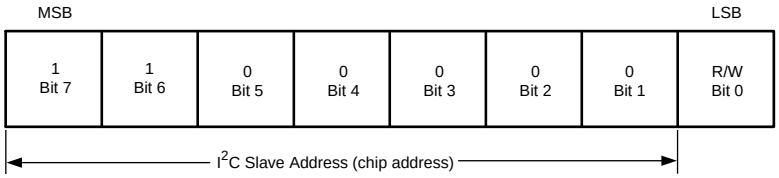
Programming (continued)



A. Here device address is 1100000Bin = 60Hex.

Figure 21. Device Address

7.5.1.5 Auto Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the LP87702-Q1, the internal address index counter will be incremented by one and the next register will be written. Table 8 below shows writing sequence to two consecutive registers. Note that auto increment feature does not work for read.

Table 8. Auto-Increment Example

MASTER ACTION	START	DEVICE ADDRESS = 60H	WRITE		REGISTER ADDRESS		DATA		DATA		STOP
LP87702-Q1				ACK		ACK		ACK		ACK	

7.6 Register Maps

7.6.1 Register Descriptions

The LP87702-Q1 is controlled by a set of registers through the system serial interface port. This register map describes the default values for bits which are not read from OTP memory. The asterisk (*) marking indicates register bits which are updated from OTP memory during READ OTP state. OTP values for each orderable part number are described in a separate Technical Reference Manual.

7.6.1.1 LP8770_MAP Registers

Table 9 lists the memory-mapped registers for the LP8770_MAP. All register offset addresses not listed in Table 9 should be considered as reserved locations and the register contents should not be modified.

Table 9. LP8770_MAP Registers

Offset	Acronym	Register Name	Section
0h	DEV_REV		DEV_REV Register (Offset = 0h)
1h	OTP_CODE		OTP_CODE Register (Offset = 1h)
2h	BUCK0_CTRL_1		BUCK0_CTRL_1 Register (Offset = 2h)
3h	BUCK0_CTRL_2		BUCK0_CTRL_2 Register (Offset = 3h)
4h	BUCK1_CTRL_1		BUCK1_CTRL_1 Register (Offset = 4h)
5h	BUCK1_CTRL_2		BUCK1_CTRL_2 Register (Offset = 5h)
6h	BUCK0_VOUT		BUCK0_VOUT Register (Offset = 6h)
7h	BUCK1_VOUT		BUCK1_VOUT Register (Offset = 7h)

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Table 9. LP8770_MAP Registers (continued)

Offset	Acronym	Register Name	Section
8h	BOOST_CTRL		BOOST_CTRL Register (Offset = 8h)
9h	BUCK0_DELAY		BUCK0_DELAY Register (Offset = 9h)
Ah	BUCK1_DELAY		BUCK1_DELAY Register (Offset = Ah)
Bh	BOOST_DELAY		BOOST_DELAY Register (Offset = Bh)
Ch	GPO0_DELAY		GPO0_DELAY Register (Offset = Ch)
Dh	GPO1_DELAY		GPO1_DELAY Register (Offset = Dh)
Eh	GPO2_DELAY		GPO2_DELAY Register (Offset = Eh)
Fh	GPO_CONTROL_1		GPO_CONTROL_1 Register (Offset = Fh)
10h	GPO_CONTROL_2		GPO_CONTROL_2 Register (Offset = 10h)
11h	CONFIG		CONFIG Register (Offset = 11h)
12h	PLL_CTRL		PLL_CTRL Register (Offset = 12h)
13h	PGOOD_CTRL		PGOOD_CTRL Register (Offset = 13h)
14h	PGOOD_LEVEL_1		PGOOD_LEVEL_1 Register (Offset = 14h)
15h	PGOOD_LEVEL_2		PGOOD_LEVEL_2 Register (Offset = 15h)
16h	PGOOD_LEVEL_3		PGOOD_LEVEL_3 Register (Offset = 16h)
17h	PG_CTRL		PG_CTRL Register (Offset = 17h)
18h	PG0_CTRL		PG0_CTRL Register (Offset = 18h)
19h	PG0_FAULT		PG0_FAULT Register (Offset = 19h)
1Ah	PG1_CTRL		PG1_CTRL Register (Offset = 1Ah)
1Bh	PG1_FAULT		PG1_FAULT Register (Offset = 1Bh)
1Ch	WD_CTRL_1		WD_CTRL_1 Register (Offset = 1Ch)
1Dh	WD_CTRL_2		WD_CTRL_2 Register (Offset = 1Dh)
1Eh	WD_STATUS		WD_STATUS Register (Offset = 1Eh)
1Fh	RESET		RESET Register (Offset = 1Fh)
20h	INT_TOP_1		INT_TOP_1 Register (Offset = 20h)
21h	INT_TOP_2		INT_TOP_2 Register (Offset = 21h)
22h	INT_BUCK		INT_BUCK Register (Offset = 22h)
23h	INT_BOOST		INT_BOOST Register (Offset = 23h)

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Table 9. LP8770_MAP Registers (continued)

Offset	Acronym	Register Name	Section
24h	INT_DIAG		INT_DIAG Register (Offset = 24h)
25h	TOP_STATUS		TOP_STATUS Register (Offset = 25h)
26h	BUCK_STATUS		BUCK_STATUS Register (Offset = 26h)
27h	BOOST_STATUS		BOOST_STATUS Register (Offset = 27h)
28h	DIAG_STATUS		DIAG_STATUS Register (Offset = 28h)
29h	TOP_MASK_1		TOP_MASK_1 Register (Offset = 29h)
2Ah	TOP_MASK_2		TOP_MASK_2 Register (Offset = 2Ah)
2Bh	BUCK_MASK		BUCK_MASK Register (Offset = 2Bh)
2Ch	BOOST_MASK		BOOST_MASK Register (Offset = 2Ch)
2Dh	DIAG_MASK		DIAG_MASK Register (Offset = 2Dh)
2Eh	SEL_I_LOAD		SEL_I_LOAD Register (Offset = 2Eh)
2Fh	I_LOAD_2		I_LOAD_2 Register (Offset = 2Fh)
30h	I_LOAD_1		I_LOAD_1 Register (Offset = 30h)
31h	FREQ_SEL		FREQ_SEL Register (Offset = 31h)
32h	BOOST_ILIM_CTRL		BOOST_ILIM_CTRL Register (Offset = 32h)
33h	ECC_STATUS		ECC_STATUS Register (Offset = 33h)

Complex bit access types are encoded to fit into small table cells. Table 10 shows the codes that are used for access types in this section.

Table 10. LP8770_MAP Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.

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Table 10. LP8770_MAP Access Type Codes (continued)

Access Type	Code	Description
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

7.6.1.1.1 DEV_REV Register (Offset = 0h)

DEV_REV is shown in Figure 22 and described in Table 11.

Return to Summary Table.

Figure 22. DEV_REV Register

7	6	5	4	3	2	1	0
RESERVED		DEVICE_ID			RESERVED		
R/W-0h		R/W			R/W		

Table 11. DEV_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	DEVICE_ID	R/W	*	Device specific ID code. (Default from OTP memory)
2-0	RESERVED			

7.6.1.1.2 OTP_CODE Register (Offset = 1h)

OTP_CODE is shown in Figure 23 and described in Table 12.

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Figure 23. OTP_CODE Register

7	6	5	4	3	2	1	0
OTP_ID						OTP_REV	
R/W						R/W	

Table 12. OTP_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	OTP_ID	R/W	*	Identification Code of the OTP EPROM. (Default from OTP memory)
1-0	OTP_REV	R/W	*	Version number of the OTP ID. (Default from OTP memory)

7.6.1.1.3 BUCK0_CTRL_1 Register (Offset = 2h)

BUCK0_CTRL_1 is shown in Figure 24 and described in Table 13.

Return to Summary Table.

Figure 24. BUCK0_CTRL_1 Register

7	6	5	4	3	2	1	0
RESERVED		BUCK0_FPWM_MP	BUCK0_FPWM	BUCK0_RDIS_EN	BUCK0_EN_PIN_CTRL		BUCK0_EN
R/W-0h		R/W	R/W	R/W-1h	R/W		R/W

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Table 13. BUCK0_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	BUCK0_FPWM_MP	R/W	*	Forces the BUCK0 regulator to operate always in multi-phase and forced PWM operation mode: 0 - Automatic phase adding and shedding. 1 - Forced to multi-phase operation, 2 phases in the 2-phase configuration. (Default from OTP memory)
4	BUCK0_FPWM	R/W	*	Forces the BUCK0 regulator to operate in PWM mode: 0 - Automatic transitions between PFM and PWM modes (AUTO mode). 1 - Forced to PWM operation. (Default from OTP memory)
3	BUCK0_RDIS_EN	R/W	1h	Enable output discharge resistor when BUCK0 is disabled: 0 - Discharge resistor disabled 1 - Discharge resistor enabled.
2-1	BUCK0_EN_PIN_CTRL	R/W	*	Enable/disable control for BUCK0: 0x0 - only BUCK0_EN bit controls BUCK0 0x1 - BUCK0_EN bit AND EN1 pin control BUCK0 0x2 - BUCK0_EN bit AND EN2 pin control BUCK0 0x3 - BUCK0_EN bit AND EN3 pin control BUCK0 (Default from OTP memory)
0	BUCK0_EN	R/W	*	Enable BUCK0 regulator: 0 - BUCK0 regulator is disabled 1 - BUCK0 regulator is enabled. (Default from OTP memory)

7.6.1.1.4 BUCK0_CTRL_2 Register (Offset = 3h)

BUCK0_CTRL_2 is shown in Figure 25 and described in Table 14.

Return to Summary Table.

Figure 25. BUCK0_CTRL_2 Register

7	6	5	4	3	2	1	0
RESERVED		BUCK0_ILIM			BUCK0_SLEW_RATE		
R/W-0h		R/W			R/W		

Table 14. BUCK0_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK0_ILIM	R/W	*	Sets the switch peak current limit of BUCK0. Can be programmed at any time during operation: 0x0 - 1.5 A 0x1 - 2.0 A 0x2 - 2.5 A 0x3 - 3.0 A 0x4 - 3.5 A 0x5 - 4.0 A 0x6 - Reserved 0x7 - Reserved (Default from OTP memory)

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Table 14. BUCK0_CTRL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BUCK0_SLEW_RATE	R/W	*	Sets the output voltage slew rate for BUCK0 regulator (rising and falling edges): 0x0 - 30 mV/µs 0x1 - 15 mV/µs 0x2 - 10 mV/µs 0x3 - 7.5 mV/µs 0x4 - 3.8 mV/µs 0x5 - 1.9 mV/µs 0x6 - 0.94 mV/µs 0x7 - 0.47 mV/µs (Default from OTP memory)

7.6.1.1.5 BUCK1_CTRL_1 Register (Offset = 4h)

BUCK1_CTRL_1 is shown in Figure 26 and described in Table 15.

Return to Summary Table.

Figure 26. BUCK1_CTRL_1 Register

7	6	5	4	3	2	1	0
RESERVED			BUCK1_FPWM	BUCK1_RDIS_EN	BUCK1_EN_PIN_CTRL		BUCK1_EN
R/W-0h			R/W	R/W-1h	R/W		R/W

Table 15. BUCK1_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	BUCK1_FPWM	R/W	*	Forces the BUCK1 regulator to operate in PWM mode: 0 - Automatic transitions between PFM and PWM modes (AUTO mode). 1 - Forced to PWM operation. (Default from OTP memory)
3	BUCK1_RDIS_EN	R/W	1h	Enable output discharge resistor when BUCK1 is disabled: 0 - Discharge resistor disabled 1 - Discharge resistor enabled.
2-1	BUCK1_EN_PIN_CTRL	R/W	*	Enable/disable control for BUCK1: 0x0 - only BUCK1_EN bit controls BUCK1 0x1 - BUCK1_EN bit AND EN1 pin control BUCK1 0x2 - BUCK1_EN bit AND EN2 pin control BUCK1 0x3 - BUCK1_EN bit AND EN3 pin control BUCK1 (Default from OTP memory)
0	BUCK1_EN	R/W	*	Enable BUCK1 regulator: 0 - BUCK1 regulator is disabled 1 - BUCK1 regulator is enabled. (Default from OTP memory)

7.6.1.1.6 BUCK1_CTRL_2 Register (Offset = 5h)

BUCK1_CTRL_2 is shown in Figure 27 and described in Table 16.

Return to Summary Table.

Figure 27. BUCK1_CTRL_2 Register

7	6	5	4	3	2	1	0
RESERVED			BUCK1_ILIM			BUCK1_SLEW_RATE	
R/W-0h			R/W			R/W	

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Table 16. BUCK1_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5-3	BUCK1_ILIM	R/W	*	Sets the switch peak current limit of BUCK1. Can be programmed at any time during operation: 0x0 - 1.5 A 0x1 - 2.0 A 0x2 - 2.5 A 0x3 - 3.0 A 0x4 - 3.5 A 0x5 - 4.0 A 0x6 - Reserved 0x7 - Reserved (Default from OTP memory)
2-0	BUCK1_SLEW_RATE	R/W	*	Sets the output voltage slew rate for BUCK1 regulator (rising and falling edges): 0x0 - 30 mV/µs 0x1 - 15 mV/µs 0x2 - 10 mV/µs 0x3 - 7.5 mV/µs 0x4 - 3.8 mV/µs 0x5 - 1.9 mV/µs 0x6 - 0.94 mV/µs 0x7 - 0.47 mV/µs (Default from OTP memory)

7.6.1.1.7 BUCK0_VOUT Register (Offset = 6h)

BUCK0_VOUT is shown in Figure 28 and described in Table 17.

Return to Summary Table.

Figure 28. BUCK0_VOUT Register

7	6	5	4	3	2	1	0
BUCK0_VSET							
R/W							

Table 17. BUCK0_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK0_VSET	R/W	*	Output voltage of BUCK0 regulator: 0x00 ... 0x13, Reserved, DO NOT USE 0.7 V - 0.73 V, 10 mV steps 0x14 - 0.7V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V (Default from OTP memory)

7.6.1.1.8 BUCK1_VOUT Register (Offset = 7h)

BUCK1_VOUT is shown in Figure 29 and described in Table 18.

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Figure 29. BUCK1_VOUT Register

7	6	5	4	3	2	1	0
BUCK1_VSET							
R/W							

Table 18. BUCK1_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK1_VSET	R/W	*	Output voltage of BUCK1 regulator 0x00 ... 0x13, Reserved, DO NOT USE 0.7 V - 0.73 V, 10 mV steps 0x14 - 0.7V ... 0x17 - 0.73 V 0.73 V - 1.4 V, 5 mV steps 0x18 - 0.735 V ... 0x9D - 1.4 V 1.4 V - 3.36 V, 20 mV steps 0x9E - 1.42 V ... 0xFF - 3.36 V (Default from OTP memory)

7.6.1.1.9 BOOST_CTRL Register (Offset = 8h)

BOOST_CTRL is shown in Figure 30 and described in Table 19.

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Figure 30. BOOST_CTRL Register

7	6	5	4	3	2	1	0
BOOST_VSET		RESERVED	BOOST_FPWM	BOOST_RDIS_EN	BOOST_EN_PIN_CTRL		BOOST_EN
R/W		R/W-0h	R/W	R/W-1h	R/W		R/W

Table 19. BOOST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BOOST_VSET	R/W	*	Output voltage of Boost: 0x0 - 4.9V 0x1 - 5.0V 0x2 - 5.1V 0x3 - 5.2V (Default from OTP memory)
5	RESERVED	R/W	0h	
4	BOOST_FPWM	R/W	*	Forces the Boost regulator to operate in PWM mode: 0 - Automatic transitions between PFM and PWM modes (AUTO mode). 1 - Forced to PWM operation. (Default from OTP memory)
3	BOOST_RDIS_EN	R/W	1h	Enable output discharge resistor when BOOST is disabled: 0 - Discharge resistor disabled 1 - Discharge resistor enabled.

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Table 19. BOOST_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	BOOST_EN_PIN_CTRL	R/W	*	Enable/disable control for Boost: 0x0 - only BOOST_EN bit controls Boost 0x1 - BOOST_EN bit AND EN1 pin control Boost 0x2 - BOOST_EN bit AND EN2 pin control Boost 0x3 - BOOST_EN bit AND EN3 pin control Boost (Default from OTP memory)
0	BOOST_EN	R/W	*	Enable Boost regulator: 0 - Boost regulator is disabled 1 - Boost regulator is enabled. (Default from OTP memory)

7.6.1.1.10 BUCK0_DELAY Register (Offset = 9h)

BUCK0_DELAY is shown in Figure 31 and described in Table 20.

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Figure 31. BUCK0_DELAY Register

7	6	5	4	3	2	1	0
BUCK0_SHUTDOWN_DELAY				BUCK0_STARTUP_DELAY			
R/W				R/W			

Table 20. BUCK0_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BUCK0_SHUTDOWN_DELAY	R/W	*	Shutdown delay of BUCK0 from falling edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	BUCK0_STARTUP_DELAY	R/W	*	Startup delay of BUCK0 from rising edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.11 BUCK1_DELAY Register (Offset = Ah)

BUCK1_DELAY is shown in Figure 32 and described in Table 21.

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Figure 32. BUCK1_DELAY Register

7	6	5	4	3	2	1	0
BUCK1_SHUTDOWN_DELAY				BUCK1_STARTUP_DELAY			
R/W				R/W			

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Table 21. BUCK1_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BUCK1_SHUTDOWN_DELAY	R/W	*	Shutdown delay of BUCK1 from falling edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	BUCK1_STARTUP_DELAY	R/W	*	Startup delay of BUCK1 from rising edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.12 BOOST_DELAY Register (Offset = Bh)

BOOST_DELAY is shown in Figure 33 and described in Table 22.

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Figure 33. BOOST_DELAY Register

7	6	5	4	3	2	1	0
BOOST_SHUTDOWN_DELAY				BOOST_STARTUP_DELAY			
R/W				R/W			

Table 22. BOOST_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BOOST_SHUTDOWN_DELAY	R/W	*	Shutdown delay of Boost from falling edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	BOOST_STARTUP_DELAY	R/W	*	Startup delay of Boost from rising edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.13 GPO0_DELAY Register (Offset = Ch)

GPO0_DELAY is shown in Figure 34 and described in Table 23.

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Figure 34. GPO0_DELAY Register

7	6	5	4	3	2	1	0
GPO0_SHUTDOWN_DELAY				GPO0_STARTUP_DELAY			
R/W				R/W			

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Table 23. GPO0_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO0_SHUTDOWN_DELAY	R/W	*	Shutdown delay of GPO0 from falling edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	GPO0_STARTUP_DELAY	R/W	*	Startup delay of GPO0 from rising edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.14 GPO1_DELAY Register (Offset = Dh)

GPO1_DELAY is shown in Figure 35 and described in Table 24.

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Figure 35. GPO1_DELAY Register

7	6	5	4	3	2	1	0
GPO1_SHUTDOWN_DELAY				GPO1_STARTUP_DELAY			
R/W				R/W			

Table 24. GPO1_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO1_SHUTDOWN_DELAY	R/W	*	Shutdown delay of GPO1 from falling edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	GPO1_STARTUP_DELAY	R/W	*	Startup delay of GPO1 from rising edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.15 GPO2_DELAY Register (Offset = Eh)

GPO2_DELAY is shown in Figure 36 and described in Table 25.

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Figure 36. GPO2_DELAY Register

7	6	5	4	3	2	1	0
GPO2_SHUTDOWN_DELAY				GPO2_STARTUP_DELAY			
R/W				R/W			

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Table 25. GPO2_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO2_SHUTDOWN_DELAY	R/W	*	Shutdown delay of GPO2 from falling edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)
3-0	GPO2_STARTUP_DELAY	R/W	*	Startup delay of GPO2 from rising edge of control signal: 0000 - 0 ms 0001 - 0.5 ms (1ms if CONFIG(STARTUP_DELAY_SEL)=1) ... 1111 - 7.5 ms (15ms if CONFIG(STARTUP_DELAY_SEL)=1) (Default from OTP memory)

7.6.1.1.16 GPO_CONTROL_1 Register (Offset = Fh)

GPO_CONTROL_1 is shown in Figure 37 and described in Table 26.

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Figure 37. GPO_CONTROL_1 Register

7	6	5	4	3	2	1	0
GPO1_PG1_OD	GPO1_EN_PIN_CTRL		GPO1_OUT	GPO0_OD	GPO0_EN_PIN_CTRL		GPO0_OUT
R/W	R/W		R/W	R/W	R/W		R/W

Table 26. GPO_CONTROL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPO1_PG1_OD	R/W	*	GPO1 / PG1 signal type: 0 - Push-pull output (VANA level) 1 - Open-drain output (Default from OTP memory)
6-5	GPO1_EN_PIN_CTRL	R/W	*	Control for GPO1 output: 0x0 - only GPO1_OUT bit controls GPO1 0x1 - GPO1_OUT bit AND EN1 pin control GPO1 0x2 - GPO1_OUT bit AND EN2 pin control GPO1 0x3 - GPO1_OUT bit AND EN3 pin control GPO1 (Default from OTP memory)
4	GPO1_OUT	R/W	*	Control for GPO1 signal (when configured to GPO1): 0 - Logic low level 1 - Logic high level (Default from OTP memory)
3	GPO0_OD	R/W	*	GPO0 signal type: 0 - Push-pull output (VANA level) 1 - Open-drain output (Default from OTP memory)
2-1	GPO0_EN_PIN_CTRL	R/W	*	Control for GPO0 output: 0x0 - only GPO0_OUT bit controls GPO0 0x1 - GPO0_OUT bit AND EN1 pin control GPO0 0x2 - GPO0_OUT bit AND EN2 pin control GPO0 0x3 - GPO0_OUT bit AND EN3 pin control GPO0 (Default from OTP memory)

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Table 26. GPO_CONTROL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GPO0_OUT	R/W	*	Control for GPO0 signal: 0 - Logic low level 1 - Logic high level (Default from OTP memory)

7.6.1.1.17 GPO_CONTROL_2 Register (Offset = 10h)

GPO_CONTROL_2 is shown in Figure 38 and described in Table 27.

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Figure 38. GPO_CONTROL_2 Register

7	6	5	4	3	2	1	0
RESERVED		GPO2_SEL	GPO1_SEL	GPO2_OD	GPO2_EN_PIN_CTRL		GPO2_OUT
R/W-0h		R/W	R/W	R/W	R/W		R/W

Table 27. GPO_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	GPO2_SEL	R/W	*	CLKIN/GPO2 pin function: 0 - CLKIN 1 - GPO2 (Default from OTP memory)
4	GPO1_SEL	R/W	*	PG1/GPO1 pin function: 0 - PG1 1 - GPO1 (Default from OTP memory)
3	GPO2_OD	R/W	*	GPO2 signal type (when configured to GPO2): 0 - Push-pull output (VANA level) 1 - Open-drain output (Default from OTP memory)
2-1	GPO2_EN_PIN_CTRL	R/W	*	Control for GPO2 output: 0x0 - only GPO2_OUT bit controls GPO2 0x1 - GPO2_OUT bit AND EN1 pin control GPO2 0x2 - GPO2_OUT bit AND EN2 pin control GPO2 0x3 - GPO2_OUT bit AND EN3 pin control GPO2 (Default from OTP memory)
0	GPO2_OUT	R/W	*	Control for GPO2 signal (when configured to GPO2): 0 - Logic low level 1 - Logic high level (Default from OTP memory)

7.6.1.1.18 CONFIG Register (Offset = 11h)

CONFIG is shown in Figure 39 and described in Table 28.

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Figure 39. CONFIG Register

7	6	5	4	3	2	1	0
STARTUP_DELAY_SEL	SHUTDOWN_DELAY_SEL	CLKIN_PD	EN3_PD	EN2_PD	EN1_PD	TDIE_WARN_LEVEL	EN_SPREAD_SPEC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 28. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STARTUP_DELAY_SEL	R/W	*	Startup delays from control signal: 0 - 0ms - 7.5ms with 0.5ms steps 1 - 0ms - 15ms with 1ms steps (Default from OTP memory)
6	SHUTDOWN_DELAY_SEL	R/W	*	Shutdown delays from from signal: 0 - 0ms - 7.5ms with 0.5ms steps 1 - 0ms - 15ms with 1ms steps (Default from OTP memory)
5	CLKIN_PD	R/W	*	Selects the pull down resistor on the CLKIN input pin. 0 - Pull-down resistor is disabled. 1 - Pull-down resistor is enabled. (Default from OTP memory)
4	EN3_PD	R/W	*	Selects the pull down resistor on the EN3 pin: 0 - Pull-down resistor is disabled 1 - Pull-down resistor is enabled (Default from OTP memory)
3	EN2_PD	R/W	*	Selects the pull down resistor on the EN2 pin: 0 - Pull-down resistor is disabled 1 - Pull-down resistor is enabled (Default from OTP memory)
2	EN1_PD	R/W	*	Selects the pull down resistor on the EN1 pin: 0 - Pull-down resistor is disabled 1 - Pull-down resistor is enabled (Default from OTP memory)
1	TDIE_WARN_LEVEL	R/W	*	Thermal warning threshold level. 0 - 125C 1 - 140C. (Default from OTP memory)
0	EN_SPREAD_SPEC	R/W	*	Enable spread spectrum feature for Buck and Boost regulators. 0 - Disabled 1 - Enabled (Default from OTP memory)

7.6.1.1.19 PLL_CTRL Register (Offset = 12h)

PLL_CTRL is shown in Figure 40 and described in Table 29.

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Figure 40. PLL_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	EN_PLL	RESERVED	EXT_CLK_FREQ				
R/W-0h	R/W	R/W-0h	R/W				

Table 29. PLL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	EN_PLL	R/W	*	Selection of external clock and PLL operation: 0 - Forced to internal RC oscillator. PLL disabled. 1 - PLL is enabled in STANDBY and ACTIVE modes. Automatic external clock use when available, interrupt generated if external clock appears or disappears. (Default from OTP memory)

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Table 29. PLL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RESERVED	R/W	0h	This bit must be set to '0'.
4-0	EXT_CLK_FREQ	R/W	*	Frequency of the external clock (CLKIN): 0x00 - 1 MHz 0x01 - 2 MHz 0x02 - 3 MHz ... 0x16 - 23 MHz 0x17 - 24 MHz 0x18...0x1F - Reserved See electrical specification for input clock frequency tolerance. (Default from OTP memory)

7.6.1.1.20 PGOOD_CTRL Register (Offset = 13h)

PGOOD_CTRL is shown in Figure 41 and described in Table 30.

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Figure 41. PGOOD_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	PGOOD_WINDOW	EN_PGOOD_VANA	EN_PGOOD_VMON2	EN_PGOOD_VMON1	EN_PGOOD_BOOST	EN_PGOOD_BUCK1	EN_PGOOD_BUCK0
R/W-0h	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 30. PGOOD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	PGOOD_WINDOW	R/W	*	Voltage monitoring method for PG0 and PG1 signals: 0 - Only undervoltage monitoring. 1 - Overvoltage and undervoltage monitoring. (Default from OTP memory)
5	EN_PGOOD_VANA	R/W	*	Enable powergood diagnostics for VANA 0 - Disabled 1 - Enabled (Default from OTP memory)
4	EN_PGOOD_VMON2	R/W	*	Enable powergood diagnostics for VMON2 0 - Disabled 1 - Enabled (Default from OTP memory)
3	EN_PGOOD_VMON1	R/W	*	Enable powergood diagnostics for VMON1 0 - Disabled 1 - Enabled (Default from OTP memory)
2	EN_PGOOD_BOOST	R/W	*	Enable powergood diagnostics for Boost 0 - Disabled 1 - Enabled (Default from OTP memory)
1	EN_PGOOD_BUCK1	R/W	*	Enable powergood diagnostics for Buck1 0 - Disabled 1 - Enabled (Default from OTP memory)

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Table 30. PGOOD_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EN_PGOOD_BUCK0	R/W	*	Enable powergood diagnostics for Buck0 0 - Disabled 1 - Enabled (Default from OTP memory)

7.6.1.1.21 PGOOD_LEVEL_1 Register (Offset = 14h)

PGOOD_LEVEL_1 is shown in Figure 42 and described in Table 31.

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Figure 42. PGOOD_LEVEL_1 Register

7	6	5	4	3	2	1	0
RESERVED			VMON1_WINDOW		VMON1_THRESHOLD		
R/W-0h			R/W		R/W		

Table 31. PGOOD_LEVEL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-3	VMON1_WINDOW	R/W	*	Overvoltage and undervoltage threshold levels for VMON1: 0x0 - +/-2% 0x1 - +/-3% 0x2 - +/-4% 0x3 - +/-6% (Default from OTP memory)
2-0	VMON1_THRESHOLD	R/W	*	Threshold voltage for VMON1 input: 0x0 - 0.65V 0x1 - 0.8V (low ohmic input, no resistor divider) 0x2 - 1.0V 0x3 - 1.1V 0x4 - 1.2V 0x5 - 1.3V 0x6 - 1.8V 0x7 - Reserved (Default from OTP memory)

7.6.1.1.22 PGOOD_LEVEL_2 Register (Offset = 15h)

PGOOD_LEVEL_2 is shown in Figure 43 and described in Table 32.

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Figure 43. PGOOD_LEVEL_2 Register

7	6	5	4	3	2	1	0
RESERVED			VMON2_WINDOW		VMON2_THRESHOLD		
R/W-0h			R/W		R/W		

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Table 32. PGOOD_LEVEL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-3	VMON2_WINDOW	R/W	*	Overvoltage and undervoltage threshold levels for VMON2: 0x0 - +/-2% 0x1 - +/-3% 0x2 - +/-4% 0x3 - +/-6% (Default from OTP memory)
2-0	VMON2_THRESHOLD	R/W	*	Threshold voltage for VMON2 input: 0x0 - 0.65V 0x1 - 0.8V (low ohmic input, no resistor divider) 0x2 - 1.0V 0x3 - 1.1V 0x4 - 1.2V 0x5 - 1.3V 0x6 - 1.8V 0x7 - (Default from OTP memory)

7.6.1.1.23 PGOOD_LEVEL_3 Register (Offset = 16h)

PGOOD_LEVEL_3 is shown in Figure 44 and described in Table 33.

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Figure 44. PGOOD_LEVEL_3 Register

7	6	5	4	3	2	1	0
BOOST_WINDOW		BUCK1_WINDOW		BUCK0_WINDOW		VANA_WINDOW	VANA_THRESHOLD
R/W		R/W		R/W		R/W	R/W

Table 33. PGOOD_LEVEL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BOOST_WINDOW	R/W	*	Undervoltage/overvoltage threshold levels for Boost: 0x0 - 4.9V/5.1V 0x1 - 4.8V/5.2V 0x2 - 4.7V/5.3V 0x3 - 4.6V/5.4V (Default from OTP memory)
5-4	BUCK1_WINDOW	R/W	*	Overvoltage and undervoltage threshold levels for Buck1: 0x0 - +/-30 mV 0x1 - +/-50 mV 0x2 - +/-70 mV 0x3 - +/-90 mV (Default from OTP memory)
3-2	BUCK0_WINDOW	R/W	*	Overvoltage and undervoltage threshold levels for Buck0: 0x0 - +/-30 mV 0x1 - +/-50 mV 0x2 - +/-70 mV 0x3 - +/-90 mV (Default from OTP memory)
1	VANA_WINDOW	R/W	*	Overvoltage and undervoltage threshold levels for VANA: 0 - +/-5% 1 - +/-10% (Default from OTP memory)

Table 33. PGOOD_LEVEL_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	VANA_THRESHOLD	R/W	*	Threshold voltage for VANA input: 0 - 3.3V 1 - 5.0V (Default from OTP memory)

7.6.1.1.24 PG_CTRL Register (Offset = 17h)

PG_CTRL is shown in Figure 45 and described in Table 34.

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Figure 45. PG_CTRL Register

7	6	5	4	3	2	1	0
PG1_MODE	PGOOD_FAULT_GATES_PG1	RESERVED	PG1_POL	PG0_MODE	PGOOD_FAULT_GATES_PG0	PG0_OD	PG0_POL
R/W	R/W	R/W-0h	R/W	R/W	R/W	R/W	R/W

Table 34. PG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG1_MODE	R/W	*	Operating mode for PG1 signal: 0 - Detecting unusual situations 1 - Showing when requested outputs are not valid. (Default from OTP memory)
6	PGOOD_FAULT_GATES_PG1	R/W	*	Type of operation for PG1 signal: 0 - Indicates live status of monitored voltage outputs. 1 - Indicates status of PG1_FAULT register, inactive if at least one of PG1_FAULT_x bit is inactive. (Default from OTP memory)
5	RESERVED	R/W	0h	
4	PG1_POL	R/W	*	PG1 signal polarity. 0 - PG1 signal high when monitored outputs are valid 1 - PG1 signal low when monitored outputs are valid (Default from OTP memory)
3	PG0_MODE	R/W	*	Operating mode for PG0 signal: 0 - Detecting unusual situations 1 - Showing when requested outputs are not valid. (Default from OTP memory)
2	PGOOD_FAULT_GATES_PG0	R/W	*	Type of operation for PG0 signal: 0 - Indicates live status of monitored voltage outputs. 1 - Indicates status of PG0_FAULT register, inactive if at least one of PG0_FAULT_x bit is inactive. (Default from OTP memory)
1	PG0_OD	R/W	*	PG0 signal type: 0 - Push-pull output (VANA level) 1 - Open-drain output (Default from OTP memory)
0	PG0_POL	R/W	*	PG0 signal polarity. 0 - PG0 signal high when monitored outputs are valid 1 - PG0 signal low when monitored outputs are valid (Default from OTP memory)

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7.6.1.1.25 PG0_CTRL Register (Offset = 18h)

PG0_CTRL is shown in Figure 46 and described in Table 35.

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Figure 46. PG0_CTRL Register

7	6	5	4	3	2	1	0
PG0_RISE_DELAY	SEL_PG0_TWARN	SEL_PG0_VANA	SEL_PG0_VMON2	SEL_PG0_VMON1	SEL_PG0_BOOST	SEL_PG0_BUCK1	SEL_PG0_BUCK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 35. PG0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG0_RISE_DELAY	R/W	0h	0 - PG0 rise is not delayed 1 - PG0 rise is delayed 11ms
6	SEL_PG0_TWARN	R/W	*	PG0 control from thermal warning: 0 - Masked 1 - Affecting PGOOD (Default from OTP memory)
5	SEL_PG0_VANA	R/W	*	PG0 signal source control from VANA 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
4	SEL_PG0_VMON2	R/W	*	PG0 signal source control from VMON2 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
3	SEL_PG0_VMON1	R/W	*	PG0 signal source control from VMON1 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
2	SEL_PG0_BOOST	R/W	*	PG0 signal source control from Boost 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
1	SEL_PG0_BUCK1	R/W	*	PG0 signal source control from Buck1 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
0	SEL_PG0_BUCK0	R/W	*	PG0 signal source control from Buck0 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)

7.6.1.1.26 PG0_FAULT Register (Offset = 19h)

PG0_FAULT is shown in Figure 47 and described in Table 36.

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Figure 47. PG0_FAULT Register

7	6	5	4	3	2	1	0
RESERVED	PG0_FAULT_TWARN	PG0_FAULT_VANA	PG0_FAULT_VMON2	PG0_FAULT_VMON1	PG0_FAULT_BOOST	PG0_FAULT_BUCK1	PG0_FAULT_BUCK0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 36. PG0_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	PG0_FAULT_TWARN	R	0h	Source for PG0 inactive signal: 0 - TWARN has not set PG0 signal inactive. 1 - TWARN is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when TWARN is valid.
5	PG0_FAULT_VANA	R	0h	Source for PG0 inactive signal: 0 - VANA has not set PG0 signal inactive. 1 - VANA is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when VANA input is valid.
4	PG0_FAULT_VMON2	R	0h	Source for PG0 inactive signal: 0 - VMON2 has not set PG0 signal inactive. 1 - VMON2 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when VMON2 input is valid.
3	PG0_FAULT_VMON1	R	0h	Source for PG0 inactive signal: 0 - VMON1 has not set PG0 signal inactive. 1 - VMON1 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when VMON1 input is valid.
2	PG0_FAULT_BOOST	R	0h	Source for PG0 inactive signal: 0 - Boost has not set PG0 signal inactive. 1 - Boost is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when Boost output is valid.
1	PG0_FAULT_BUCK1	R	0h	Source for PG0 inactive signal: 0 - Buck1 has not set PG0 signal inactive. 1 - Buck1 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when Buck1 output is valid.
0	PG0_FAULT_BUCK0	R	0h	Source for PG0 inactive signal: 0 - Buck0 has not set PG0 signal inactive. 1 - Buck0 is selected for PG0 signal and it has set PG0 signal inactive. This bit can be cleared by writing '1' to this bit when Buck0 output is valid.

7.6.1.1.27 PG1_CTRL Register (Offset = 1Ah)

PG1_CTRL is shown in Figure 48 and described in Table 37.

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Figure 48. PG1_CTRL Register

7	6	5	4	3	2	1	0
PG1_RISE_DELAY	SEL_PG1_TWARN	SEL_PG1_VANA	SEL_PG1_VMON2	SEL_PG1_VMON1	SEL_PG1_BOOST	SEL_PG1_BUCK1	SEL_PG1_BUCK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Table 37. PG1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PG1_RISE_DELAY	R/W	0h	0 - PG1 rise is not delayed 1 - PG1 rise is delayed 11ms
6	SEL_PG1_TWARN	R/W	*	PG1 control from thermal warning: 0 - Masked 1 - Affecting PGOOD (Default from OTP memory)
5	SEL_PG1_VANA	R/W	*	PG1 signal source control from VANA 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
4	SEL_PG1_VMON2	R/W	*	PG1 signal source control from VMON2 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
3	SEL_PG1_VMON1	R/W	*	PG1 signal source control from VMON1 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
2	SEL_PG1_BOOST	R/W	*	PG1 signal source control from Boost 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
1	SEL_PG1_BUCK1	R/W	*	PG1 signal source control from Buck1 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)
0	SEL_PG1_BUCK0	R/W	*	PG1 signal source control from Buck0 0 - Masked 1 - Powergood threshold voltage (Default from OTP memory)

7.6.1.1.28 PG1_FAULT Register (Offset = 1Bh)

PG1_FAULT is shown in Figure 49 and described in Table 38.

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Figure 49. PG1_FAULT Register

7	6	5	4	3	2	1	0
RESERVED	PG1_FAULT_TWARN	PG1_FAULT_VANA	PG1_FAULT_VMON2	PG1_FAULT_VMON1	PG1_FAULT_BOOST	PG1_FAULT_BUCK1	PG1_FAULT_BUCK0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 38. PG1_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	PG1_FAULT_TWARN	R	0h	Source for PG1 inactive signal: 0 - TWARN has not set PG1 signal inactive. 1 - TWARN is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when TWARN is valid.

Table 38. PG1_FAULT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PG1_FAULT_VANA	R	0h	Source for PG1 inactive signal: 0 - VANA has not set PG1 signal inactive. 1 - VANA is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when VANA input is valid.
4	PG1_FAULT_VMON2	R	0h	Source for PG1 inactive signal: 0 - VMON2 has not set PG1 signal inactive. 1 - VMON2 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when VMON2 input is valid.
3	PG1_FAULT_VMON1	R	0h	Source for PG1 inactive signal: 0 - VMON1 has not set PG1 signal inactive. 1 - VMON1 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when VMON1 input is valid.
2	PG1_FAULT_BOOST	R	0h	Source for PG1 inactive signal: 0 - Boost has not set PG1 signal inactive. 1 - Boost is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when Boost output is valid.
1	PG1_FAULT_BUCK1	R	0h	Source for PG1 inactive signal: 0 - Buck1 has not set PG1 signal inactive. 1 - Buck1 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when Buck1 output is valid.
0	PG1_FAULT_BUCK0	R	0h	Source for PG1 inactive signal: 0 - Buck0 has not set PG1 signal inactive. 1 - Buck0 is selected for PG1 signal and it has set PG1 signal inactive. This bit can be cleared by writing '1' to this bit when Buck0 output is valid.

7.6.1.1.29 WD_CTRL_1 Register (Offset = 1Ch)

WD_CTRL_1 is shown in Figure 50 and described in Table 39.

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Figure 50. WD_CTRL_1 Register

7	6	5	4	3	2	1	0
WD_CLOSE_TIME		WD_OPEN_TIME		WD_LONG_OPEN_TIME		WD_RESET_CNTR_SEL	
R/W		R/W		R/W		R/W	

Table 39. WD_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_CLOSE_TIME	R/W	*	Watchdog close window time select. 00 - 10ms 01 - 20ms 10 - 50ms 11 - 100ms (Default from OTP memory)
5-4	WD_OPEN_TIME	R/W	*	Watchdog open window time select. 00 - 20ms 01 - 100ms 10 - 600ms 11 - 2000ms (Default from OTP memory)
3-2	WD_LONG_OPEN_TIME	R/W	*	Watchdog long open window time select. 00 - 200ms 01 - 600ms 10 - 2000ms 11 - 5000ms (Default from OTP memory)
1-0	WD_RESET_CNTR_SEL	R/W	*	Watchdog reset counter threshold select. After the selected number of reset (WDR) pulses system restart sequence is initiated. 00 - system restart disabled 01 - 1 10 - 2 11 - 4 (Default from OTP memory)

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7.6.1.1.30 WD_CTRL_2 Register (Offset = 1Dh)

WD_CTRL_2 is shown in Figure 51 and described in Table 40.

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Figure 51. WD_CTRL_2 Register

7	6	5	4	3	2	1	0
WD_LOCK	RESERVED		WD_SYS_RESTART_FLAG_MODE	WD_EN_OTP_READ	WDI_PD	WDR_POL	WDR_OD
R-0h	R/W-0h		R/W	R/W	R/W	R/W	R/W

Table 40. WD_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_LOCK	R	0h	Lock bit for watchdog controls. Locks all controls to watchdog in registers WD_CTRL_1, WD_CTRL_2. Lock bit also locks itself. Once lock bit is written 1 it cannot be written 0. Only reset can clear it. 0 - Not locked 1 - Locked WD_STATUS register is not affected by WD_LOCK bit. WD_SYSTEM_RESTART_FLAG and WD_RESET_CNTR_STATUS can be cleared even if WD_LOCK=1.
6-5	RESERVED	R/W	0h	
4	WD_SYS_RESTART_FLAG_MODE	R/W	*	WD_SYSTEM_RESTART_FLAG mode select. 0 - WD_SYSTEM_RESTART_FLAG is only a status bit. 1 - WD_SYSTEM_RESTART_FLAG prevents further system restarts until it is cleared. (Default from OTP memory)
3	WD_EN_OTP_READ	R/W	*	Read OTP during system restart sequence 0 - OTP read not enabled during system restart sequence 1 - OTP read enabled during system restart sequence (Default from OTP memory)
2	WDI_PD	R/W	*	Selects the pull down resistor on the WDI pin: 0 - Pull-down resistor is disabled 1 - Pull-down resistor is enabled (Default from OTP memory)
1	WDR_POL	R/W	*	Watchdog reset output (WDR) polarity select 0 - Active high 1 - Active low (Default from OTP memory)
0	WDR_OD	R/W	*	Watchdog reset output (WDR) signal type 0 - Push-pull output (VANA level) 1 - Open-drain output (Default from OTP memory)

7.6.1.1.31 WD_STATUS Register (Offset = 1Eh)

WD_STATUS is shown in Figure 52 and described in Table 41.

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Figure 52. WD_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			WD_CLR_SYSTEM_RESTART_FLAG	WD_SYSTEM_RESTART_FLAG	WD_CLR_RESET_CNTR	WD_RESET_CNTR_STATUS	
R/W-0h			R-0h	R-0h	R-0h	R-0h	

Table 41. WD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	WD_CLR_SYSTEM_RESTART_FLAG	R	0h	Clear bit for WD_SYSTEM_RESTART_FLAG. Write 1 to generate a clear pulse. Reg bit value returns to 0 after clearing is finished.
3	WD_SYSTEM_RESTART_FLAG	R	0h	Watchdog requested system restart has occurred. Can be cleared by writing WD_CLR_SYSTEM_RESTART_FLAG bit 1.

Table 41. WD_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	WD_CLR_RESET_CNTR	R	0h	Watchdog reset counter clear. Write 1 to generate a clear pulse.
1-0	WD_RESET_CNTR_STATUS	R	0h	Current status of watchdog reset counter.

7.6.1.1.32 RESET Register (Offset = 1Fh)

RESET is shown in Figure 53 and described in Table 42.

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Figure 53. RESET Register

7	6	5	4	3	2	1	0
RESERVED							SW_RESET
R/W-0h							R-0h

Table 42. RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	SW_RESET	R	0h	Software commanded reset. When written to 1, the registers will be reset to default values, OTP memory is read, and the I2C interface is reset. The bit is automatically cleared.

7.6.1.1.33 INT_TOP_1 Register (Offset = 20h)

INT_TOP_1 is shown in Figure 54 and described in Table 43.

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Figure 54. INT_TOP_1 Register

7	6	5	4	3	2	1	0
I_MEAS_INT	DIAG_INT	BOOST_INT	BUCK_INT	SYNC_CLK_INT	TDIE_SD_INT	TDIE_WARN_INT	OVP_INT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 43. INT_TOP_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I_MEAS_INT	R	0h	Latched status bit indicating that the load current measurement result is available in I_LOAD_1 and I_LOAD_2 registers. Write 1 to clear interrupt.
6	DIAG_INT	R	0h	Interrupt indicating that INT_DIAG register has a pending interrupt. The reason for the interrupt is indicated in INT_DIAG register. This bit is cleared automatically when INT_DIAG register is cleared to 0x00.
5	BOOST_INT	R	0h	Interrupt indicating that BOOST have a pending interrupt. The reason for the interrupt is indicated in INT_BOOST register. This bit is cleared automatically when INT_BOOST register is cleared to 0x00.
4	BUCK_INT	R	0h	Interrupt indicating that BUCK0 and/or BUCK1 have a pending interrupt. The reason for the interrupt is indicated in INT_BUCK register. This bit is cleared automatically when INT_BUCK register is cleared to 0x00.

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Table 43. INT_TOP_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SYNC_CLK_INT	R	0h	Latched status bit indicating that the external clock frequency became valid or invalid. Write 1 to clear interrupt.
2	TDIE_SD_INT	R	0h	Latched status bit indicating that the die junction temperature has exceeded the thermal shutdown level. The regulators have been disabled if they were enabled. The regulators cannot be enabled if this bit is active. The actual status of the thermal warning is indicated by TDIE_SD_INT_STAT bit in TOP_STAT register. Write 1 to clear interrupt.
1	TDIE_WARN_INT	R	0h	Latched status bit indicating that the die junction temperature has exceeded the thermal warning level. The actual status of the thermal warning is indicated by TDIE_WARN_INT_STAT bit in TOP_STAT register. Write 1 to clear interrupt.
0	OVP_INT	R	0h	Latched status bit indicating that the input voltage has exceeded the over-voltage detection level. The actual status of the over-voltage is indicated by OVP bit in TOP_STAT register. Write 1 to clear interrupt.

7.6.1.1.34 INT_TOP_2 Register (Offset = 21h)

INT_TOP_2 is shown in Figure 55 and described in Table 44.

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Figure 55. INT_TOP_2 Register

7	6	5	4	3	2	1	0
RESERVED							RESET_REG_INT
R/W-0h							R-0h

Table 44. INT_TOP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	RESET_REG_INT	R	0h	Latched status bit indicating that either VBAT supply voltage has been below undervoltage threshold level or the host has requested a reset (SW_RESET bit in RESET register). The regulators have been disabled, and registers are reset to default values and the normal startup procedure is done. Write 1 to clear interrupt.

7.6.1.1.35 INT_BUCK Register (Offset = 22h)

INT_BUCK is shown in Figure 56 and described in Table 45.

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Figure 56. INT_BUCK Register

7	6	5	4	3	2	1	0
RESERVED	BUCK1_PG_INT	BUCK1_SC_INT	BUCK1_ILIM_INT	RESERVED	BUCK0_PG_INT	BUCK0_SC_INT	BUCK0_ILIM_INT
R/W-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h	R-0h	R-0h

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Table 45. INT_BUCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	
6	BUCK1_PG_INT	R	0h	Latched status bit indicating that BUCK1 powergood event has been detected. Write 1 to clear.
5	BUCK1_SC_INT	R	0h	Latched status bit indicating that the BUCK1 output voltage has fallen below 0.35 V level during operation or BUCK1 output didn't reach 0.35 V level in 1 ms from enable. Write 1 to clear.
4	BUCK1_ILIM_INT	R	0h	Latched status bit indicating that BUCK1 output current limit has been triggered. Write 1 to clear.
3	RESERVED	R/W	0h	
2	BUCK0_PG_INT	R	0h	Latched status bit indicating that BUCK0 powergood event has been detected. Write 1 to clear.
1	BUCK0_SC_INT	R	0h	Latched status bit indicating that the BUCK0 output voltage has fallen below 0.35 V level during operation or BUCK0 output didn't reach 0.35 V level in 1 ms from enable. Write 1 to clear.
0	BUCK0_ILIM_INT	R	0h	Latched status bit indicating that BUCK0 output current limit has been triggered. Write 1 to clear.

7.6.1.1.36 INT_BOOST Register (Offset = 23h)

INT_BOOST is shown in Figure 57 and described in Table 46.

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Figure 57. INT_BOOST Register

7	6	5	4	3	2	1	0
RESERVED					BOOST_PG_INT	BOOST_SC_INT	BOOST_ILIM_INT
R/W-0h					R-0h	R-0h	R-0h

Table 46. INT_BOOST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	BOOST_PG_INT	R	0h	Latched status bit indicating that Boost powergood event has been detected. Write 1 to clear.
1	BOOST_SC_INT	R	0h	Latched status bit indicating that the Boost output voltage has fallen below 2.5V level during operation or BOOST output didn't reach 2.5 V level in 1 ms from enable. Write 1 to clear.
0	BOOST_ILIM_INT	R	0h	Latched status bit indicating that Boost output current limit has been triggered. Write 1 to clear.

7.6.1.1.37 INT_DIAG Register (Offset = 24h)

INT_DIAG is shown in Figure 58 and described in Table 47.

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Figure 58. INT_DIAG Register

7	6	5	4	3	2	1	0
RESERVED			VMON2_PG_INT	RESERVED	VMON1_PG_INT	RESERVED	VANA_PG_INT
R/W-0h			R-0h	R/W-0h	R-0h	R/W-0h	R-0h

Table 47. INT_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4	VMON2_PG_INT	R	0h	Latched status bit indicating that VMON2 powergood event has been detected. Write 1 to clear.
3	RESERVED	R/W	0h	
2	VMON1_PG_INT	R	0h	Latched status bit indicating that VMON1 powergood event has been detected. Write 1 to clear.
1	RESERVED	R/W	0h	
0	VANA_PG_INT	R	0h	Latched status bit indicating that VANA powergood event has been detected. Write 1 to clear.

7.6.1.1.38 TOP_STATUS Register (Offset = 25h)

TOP_STATUS is shown in Figure 59 and described in Table 48.

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Figure 59. TOP_STATUS Register

7	6	5	4	3	2	1	0
RESERVED				SYNC_CLK_STAT	TDIE_SD_STAT	TDIE_WARN_STAT	OVP_STAT
R-0h				R-0h	R-0h	R-0h	R-0h

Table 48. TOP_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	SYNC_CLK_STAT	R	0h	Status bit indicating the status of external clock (CLKIN): 0 - External clock frequency is valid 1 - External clock frequency is not valid.
2	TDIE_SD_STAT	R	0h	Status bit indicating the status of thermal shutdown: 0 - Die temperature below thermal shutdown level 1 - Die temperature above thermal shutdown level.
1	TDIE_WARN_STAT	R	0h	Status bit indicating the status of thermal warning: 0 - Die temperature below thermal warning level 1 - Die temperature above thermal warning level.
0	OVP_STAT	R	0h	Status bit indicating the status of input overvoltage monitoring: 0 - Input voltage below overvoltage threshold level 1 - Input voltage above overvoltage threshold level.

7.6.1.1.39 BUCK_STATUS Register (Offset = 26h)

BUCK_STATUS is shown in Figure 60 and described in Table 49.

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Figure 60. BUCK_STATUS Register

7	6	5	4	3	2	1	0
BUCK1_STAT	BUCK1_PG_STAT	RESERVED	BUCK1_ILIM_STAT	BUCK0_STAT	BUCK0_PG_STAT	RESERVED	BUCK0_ILIM_STAT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 49. BUCK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK1_STAT	R	0h	Status bit indicating the enable/disable status of BUCK1: 0 - BUCK1 regulator is disabled 1 - BUCK1 regulator is enabled.
6	BUCK1_PG_STAT	R	0h	Status bit indicating BUCK1 output voltage validity (raw status) 0 - BUCK1 output is not valid 1 - BUCK1 output is valid.
5	RESERVED	R	0h	Reserved
4	BUCK1_ILIM_STAT	R	0h	Status bit indicating BUCK1 current limit status (raw status) 0 - BUCK1 output current is below current limit threshold level 1 - BUCK1 output current is at current limit threshold level.
3	BUCK0_STAT	R	0h	Status bit indicating the enable/disable status of BUCK0: 0 - BUCK0 regulator is disabled 1 - BUCK0 regulator is enabled.
2	BUCK0_PG_STAT	R	0h	Status bit indicating BUCK0 output voltage validity (raw status) 0 - BUCK0 output is not valid 1 - BUCK0 output is valid.
1	RESERVED	R	0h	Reserved
0	BUCK0_ILIM_STAT	R	0h	Status bit indicating BUCK0 current limit status (raw status) 0 - BUCK0 output current is below current limit threshold level 1 - BUCK0 output current is at current limit threshold level.

7.6.1.1.40 BOOST_STATUS Register (Offset = 27h)

BOOST_STATUS is shown in Figure 61 and described in Table 50.

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Figure 61. BOOST_STATUS Register

7	6	5	4	3	2	1	0
RESERVED				BOOST_STAT	BOOST_PG_STAT	RESERVED	BOOST_ILIM_STAT
R-0h				R-0h	R-0h	R-0h	R-0h

Table 50. BOOST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	
3	BOOST_STAT	R	0h	Status bit indicating the enable/disable status of Boost: 0 - Boost regulator is disabled 1 - Boost regulator is enabled.
2	BOOST_PG_STAT	R	0h	Status bit indicating Boost output voltage validity (raw status) 0 - Boost output is not valid 1 - Boost output is valid.
1	RESERVED	R	0h	Reserved
0	BOOST_ILIM_STAT	R	0h	Status bit indicating Boost current limit status (raw status) 0 - Boost output current is below current limit threshold level 1 - Boost output current is at current limit threshold level.

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7.6.1.1.41 DIAG_STATUS Register (Offset = 28h)

DIAG_STATUS is shown in Figure 62 and described in Table 51.

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Figure 62. DIAG_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			VMON2_PG_STAT	RESERVED	VMON1_PG_STAT	RESERVED	VANA_PG_STAT
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h

Table 51. DIAG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	
4	VMON2_PG_STAT	R	0h	Status bit indicating VMON2 input voltage validity (raw status) 0 - VMON2 voltage is not valid 1 - VMON2 voltage is valid.
3	RESERVED	R	0h	
2	VMON1_PG_STAT	R	0h	Status bit indicating VMON1 input voltage validity (raw status) 0 - VMON1 voltage is not valid 1 - VMON1 voltage is valid.
1	RESERVED	R	0h	
0	VANA_PG_STAT	R	0h	Status bit indicating VANA input voltage validity (raw status) 0 - VANA voltage is not valid 1 - VANA voltage is valid.

7.6.1.1.42 TOP_MASK_1 Register (Offset = 29h)

TOP_MASK_1 is shown in Figure 63 and described in Table 52.

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Figure 63. TOP_MASK_1 Register

7	6	5	4	3	2	1	0
I_MEAS_MASK	RESERVED			SYNC_CLK_MASK	RESERVED	TDIE_WARN_MASK	RESERVED
R/W	R/W-0h			R/W	R/W-0h	R/W	R/W-0h

Table 52. TOP_MASK_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I_MEAS_MASK	R/W	*	Masking for load current measurement ready interrupt MEAS_INT in INT_TOP_1 register. 0 - Interrupt generated 1 - Interrupt not generated. (Default from OTP memory)
6-4	RESERVED	R/W	0h	
3	SYNC_CLK_MASK	R/W	*	Masking for external clock detection interrupt SYNC_CLK_INT in INT_TOP_1 register: 0 - Interrupt generated 1 - Interrupt not generated. (Default from OTP memory)
2	RESERVED	R/W	0h	

Table 52. TOP_MASK_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TDIE_WARN_MASK	R/W	*	Masking for thermal warning interrupt TDIE_WARN_INT in INT_TOP_1 register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect TDIE_WARN_STAT status bit in TOP_STAT register. (Default from OTP memory)
0	RESERVED	R/W	0h	

7.6.1.1.43 TOP_MASK_2 Register (Offset = 2Ah)

TOP_MASK_2 is shown in Figure 64 and described in Table 53.

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Figure 64. TOP_MASK_2 Register

7	6	5	4	3	2	1	0
RESERVED							RESET_REG_MASK
R/W-0h							R/W

Table 53. TOP_MASK_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	
0	RESET_REG_MASK	R/W	*	Masking for register reset interrupt RESET_REG_INT in INT_TOP_2 register: 0 - Interrupt generated 1 - Interrupt not generated. (Default from OTP memory)

7.6.1.1.44 BUCK_MASK Register (Offset = 2Bh)

BUCK_MASK is shown in Figure 65 and described in Table 54.

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Figure 65. BUCK_MASK Register

7	6	5	4	3	2	1	0
BUCK1_PGF_MASK	BUCK1_PGR_MASK	RESERVED	BUCK1_ILIM_MASK	BUCK0_PGF_MASK	BUCK0_PGR_MASK	RESERVED	BUCK0_ILIM_MASK
R/W	R/W	R/W-0h	R/W	R/W	R/W	R/W-0h	R/W

Table 54. BUCK_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK1_PGF_MASK	R/W	*	Masking of powergood invalid detection for BUCK1 power good interrupt BUCK1_PG_INT in INT_BUCK register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK1_PG_STAT status bit in BUCK_STAT register. (Default from OTP memory)

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Table 54. BUCK_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	BUCK1_PGR_MASK	R/W	*	Masking of powergood valid detection for BUCK1 power good interrupt BUCK1_PG_INT in INT_BUCK register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK1_PG_STAT status bit in BUCK_STAT register. (Default from OTP memory)
5	RESERVED	R/W	0h	
4	BUCK1_ILIM_MASK	R/W	*	Masking for BUCK1 current monitoring interrupt BUCK1_IMON_INT in INT_BUCK register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK1_IMON_STAT status bit in BUCK_STAT register. (Default from OTP memory)
3	BUCK0_PGF_MASK	R/W	*	Masking of powergood invalid detection for BUCK0 power good interrupt BUCK0_PG_INT in INT_BUCK register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK0_PG_STAT status bit in BUCK_STAT register. (Default from OTP memory)
2	BUCK0_PGR_MASK	R/W	*	Masking of powergood valid detection for BUCK0 power good interrupt BUCK0_PG_INT in INT_BUCK register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK0_PG_STAT status bit in BUCK_STAT register. (Default from OTP memory)
1	RESERVED	R/W	0h	
0	BUCK0_ILIM_MASK	R/W	*	Masking for BUCK0 current monitoring interrupt BUCK0_IMON_INT in INT_BUCK register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK0_IMON_STAT status bit in BUCK_STAT register. (Default from OTP memory)

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7.6.1.1.45 BOOST_MASK Register (Offset = 2Ch)

BOOST_MASK is shown in Figure 66 and described in Table 55.

Return to Summary Table.

Figure 66. BOOST_MASK Register

7	6	5	4	3	2	1	0
RESERVED				BOOST_PGF_MASK	BOOST_PGR_MASK	RESERVED	BOOST_ILIM_MASK
R/W-0h				R/W	R/W	R/W-0h	R/W

Table 55. BOOST_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	
3	BOOST_PGF_MASK	R/W	*	Masking of powergood invalid detection for Boost power good interrupt BOOST_PG_INT in INT_BOOST register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BOOST_PG_STAT status bit in BOOST_STAT register. (Default from OTP memory)
2	BOOST_PGR_MASK	R/W	*	Masking of powergood valid detection for Boost power good interrupt BOOST_PG_INT in INT_BOOST register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BOOST_PG_STAT status bit in BOOST_STAT register. (Default from OTP memory)
1	RESERVED	R/W	0h	
0	BOOST_ILIM_MASK	R/W	*	Masking for Boost current monitoring interrupt BOOST_IMON_INT in INT_BOOST register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BOOST_IMON_STAT status bit in BOOST_STAT register. (Default from OTP memory)

7.6.1.1.46 DIAG_MASK Register (Offset = 2Dh)

DIAG_MASK is shown in Figure 67 and described in Table 56.

Return to Summary Table.

Figure 67. DIAG_MASK Register

7	6	5	4	3	2	1	0
RESERVED		VMON2_PGF_MASK	VMON2_PGR_MASK	VMON1_PGF_MASK	VMON1_PGR_MASK	VANA_PGF_MASK	VANA_PGR_MASK
R/W-0h		R/W	R/W	R/W	R/W	R/W	R/W

Table 56. DIAG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	
5	VMON2_PGF_MASK	R/W	*	Masking of VMON2 invalid detection for powergood interrupt VMON2_PG_INT in INT_MON register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect VMON2_PG_STAT status bit in VMON_STAT register. (Default from OTP memory)
4	VMON2_PGR_MASK	R/W	*	Masking of VMON2 valid detection for powergood interrupt VMON2_PG_INT in INT_MON register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect VMON2_PG_STAT status bit in VMON_STAT register. (Default from OTP memory)

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Table 56. DIAG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	VMON1_PGF_MASK	R/W	*	Masking of VMON1 invalid detection for powergood interrupt VMON1_PG_INT in INT_MON register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect VMON1_PG_STAT status bit in VMON_STAT register. (Default from OTP memory)
2	VMON1_PGR_MASK	R/W	*	Masking of VMON1 valid detection for powergood interrupt VMON1_PG_INT in INT_MON register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect VMON1_PG_STAT status bit in VMON_STAT register. (Default from OTP memory)
1	VANA_PGF_MASK	R/W	*	Masking of VANA invalid detection for powergood interrupt VANA_PG_INT in INT_MON register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect VANA_PG_STAT status bit in VMON_STAT register. (Default from OTP memory)
0	VANA_PGR_MASK	R/W	*	Masking of VANA valid detection for powergood interrupt VANA_PG_INT in INT_MON register: 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect VANA_PG_STAT status bit in VMON_STAT register. (Default from OTP memory)

7.6.1.1.47 SEL_I_LOAD Register (Offset = 2Eh)

SEL_I_LOAD is shown in Figure 68 and described in Table 57.

Return to Summary Table.

Figure 68. SEL_I_LOAD Register

7	6	5	4	3	2	1	0
RESERVED						LOAD_CURRENT_BUCK_SELECT	
R/W-0h						R/W-0h	

Table 57. SEL_I_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1-0	LOAD_CURRENT_BUCK_SELECT	R/W	0h	Start the current measurement on the selected Buck regulator: 0 - BUCK0 1 - BUCK1 The measurement is started when register is written.

7.6.1.1.48 I_LOAD_2 Register (Offset = 2Fh)

I_LOAD_2 is shown in Figure 69 and described in Table 58.

Return to Summary Table.

Figure 69. I_LOAD_2 Register

7	6	5	4	3	2	1	0
RESERVED							BUCK_LOAD_CURRENT_8
R-0h							R-0h

Table 58. I_LOAD_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	
0	BUCK_LOAD_CURRENT_8	R	0h	This register describes the MSB bit of the average load current on selected regulator with a resolution of 10 mA per LSB and max 10 A current.

7.6.1.1.49 I_LOAD_1 Register (Offset = 30h)

I_LOAD_1 is shown in Figure 70 and described in Table 59.

Return to Summary Table.

Figure 70. I_LOAD_1 Register

7	6	5	4	3	2	1	0
BUCK_LOAD_CURRENT_7_0							
R-0h							

Table 59. I_LOAD_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BUCK_LOAD_CURRENT_7_0	R	0h	This register describes 8 LSB bits of the average load current on selected regulator with a resolution of 10 mA per LSB and max 10 A current.

7.6.1.1.50 FREQ_SEL Register (Offset = 31h)

FREQ_SEL is shown in Figure 71 and described in Table 60.

Return to Summary Table.

Figure 71. FREQ_SEL Register

7	6	5	4	3	2	1	0
RESERVED					BOOST_FREQ_SEL	BUCK_FREQ_SEL	
R/W-0h					R/W	R/W	

Table 60. FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	
2	BOOST_FREQ_SEL	R/W	*	Boost switching frequency: 0 - 2 MHz 1 - 4 MHz (Deafault from OTP memory)
1-0	BUCK_FREQ_SEL	R/W	*	Buck0 and Buck1 switching frequency: 0x0 - 2 MHz 0x1 - 3 MHz 0x2 - 4 MHz 0x3 - 4 MHz (Default from OTP memory)

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7.6.1.1.51 BOOST_ILIM_CTRL Register (Offset = 32h)

BOOST_ILIM_CTRL is shown in Figure 72 and described in Table 61.

Return to Summary Table.

Figure 72. BOOST_ILIM_CTRL Register

7	6	5	4	3	2	1	0
RESERVED						BOOST_ILIM1	BOOST_ILIM0
R/W-0h						R/W	R/W

Table 61. BOOST_ILIM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	
1	BOOST_ILIM1	R/W	*	BOOST_ILIM[1] Boost ilim selection bit 1. Sets the current limit of Boost. 00 - 1.0 A 01 - 1.4 A 10 - 1.9 A 11 - 2.8 A (Default from OTP memory)
0	BOOST_ILIM0	R/W	*	BOOST_ILIM[0] Boost ilim selection bit 0. Sets the current limit of Boost. 00 - 1.0 A 01 - 1.4 A 10 - 1.9 A 11 - 2.8 A (Default from OTP memory)

7.6.1.1.52 ECC_STATUS Register (Offset = 33h)

ECC_STATUS is shown in Figure 73 and described in Table 62.

Return to Summary Table.

Figure 73. ECC_STATUS Register

7	6	5	4	3	2	1	0
RESERVED						DED	SED
R-0h						R-0h	R-0h

Table 62. ECC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	
1	DED	R	0h	OTP error correction status: 0 - No dual errors detected 1 - Dual errors detected and not corrected
0	SED	R	0h	OTP error correction status: 0 - No single errors detected 1 - Single errors detected and corrected

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP87702-Q1 is a power management unit including a boost regulator, two step-down converters and three general-purpose digital output signals.

8.2 Typical Application

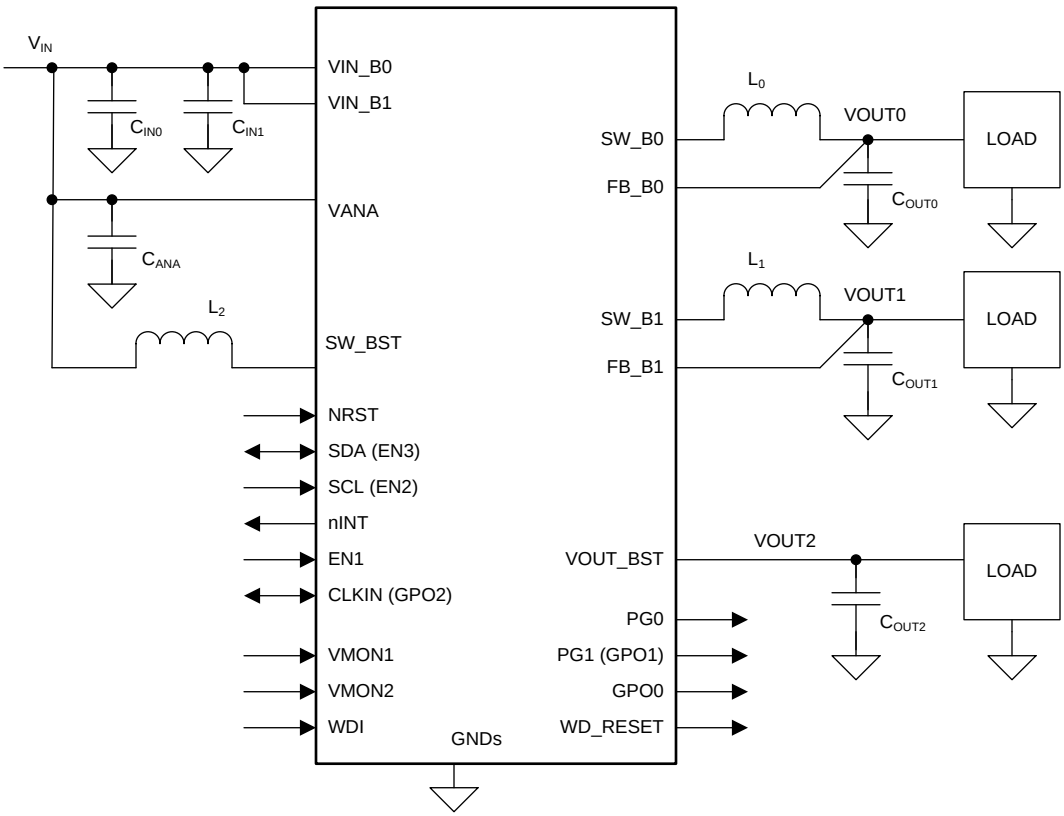

Figure 74. LP87702-Q1 Typical Application

8.2.1 Design Requirements

Table 63. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.3 V
Output voltages	1.8 V, 1.24 V, 5 V
Forward current limit settings	4 A, 4 A, 1.4 A
Switching frequency	4 MHz

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8.2.2 Detailed Design Procedure

The performance of the LP87702-Q1 device depends greatly on the care taken in designing the printed circuit board (PCB). The use of low-inductance and low serial-resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention should be given to decoupling the power supplies. Decoupling capacitors must be connected close to the device and between the power and ground pins to support high peak currents being drawn from system power rail during turnon of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance, and capacitance can easily become the performance limiting items. The separate buck regulator power pins VIN_Bx are not connected together internally. The VIN_Bx power connections shall be connected together outside the package using power plane construction.

8.2.2.1 Application Components

8.2.2.1.1 Inductor Selection

The inductors are L_0, L_1, and L_2 are shown in the Typical Application. The inductance and DCR of the inductor affects the control loop of the buck and boost regulator. It is recommended to use inductors or similar ones listed in Table 64. Pay attention to the saturation current and temperature rise current of the inductor. Check that the saturation current is higher than the peak current limit and the temperature rise current is higher than the maximum expected rms output current. For minimum effective inductance to ensure good performance refer to Specifications . DC resistance of the inductor should be less than 0.05 Ω for good efficiency at high-current condition. The inductor AC loss (resistance) also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle load. Shielded inductors are preferred as they radiate less noise.

Table 64. Recommended Inductors

MANUFACTURER	PART NUMBER	VALUE	DIMENSIONS LxWxH (mm)	RATED DC CURRENT, I_{SAT} max (typ) / I_{TEMP} max (typ) (A)	DCR typ / max (mΩ)
TOKO	DFE252012PD-R47M	0.47 µH (20%)	2.5 × 2 × 1.2	5.2 (-) / 4.0 (-)(1)	- / 27
TOKO	DFE252012PD-1R0M	1.0 µH (20%)	2.5 × 2 × 1.2	3.8 (4.5) / 3.2 (3.8)(1)	35 / 42
Tayo Yuden	MDMK2020TR47MMV	0.47 µH (20%)	2 × 2 × 1.2	4.2 (4.8) / 2.3 (2.45)	40 / 46
TDK	TFM252012ALMA1R0MTAA	0.47 µH (20%)	2.5 × 2 × 1.2	5.8 (6.5) / 4.9 (5.6)	19 / 24

(1) Operating temperature range is up to 125°C including self temperature rise.

8.2.2.1.2 Buck Input Capacitor Selection

The input capacitors C_{IN0} and C_{IN1} are shown in the Typical Application. A ceramic input bypass capacitor of 10 µF is required for both regulators. Place the input capacitor as close as possible to the VIN_Bx pin and PGND_Bx pin of the device. A larger value or higher voltage rating improves the input voltage filtering. Use X7R type of capacitors, not Y5V or F. DC bias characteristics of the capacitors must also be considered. Minimum effective input capacitance to ensure good performance is 1.9 µF per buck input at maximum input voltage including tolerances and ambient temperature range. In addition there must be at least 22 µF of additional capacitance common for all the power input pins on the system power rail. See Table 65.

The input filter capacitor supplies current to the high-side FET switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating. In addition ferrite can be used in front of the input capacitor to reduce the EMI.

Table 65. Recommended Buck Input Capacitors (X7R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GCM21BR71A106KE22	10 µF (10%)	0805	2.0 x 1.25 x 1.25	10 V
TDK	CGA4J3X7S1A106K125AB	10 µF (10%)	0805	2.0 x 1.25 x 1.25	10 V

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8.2.2.1.3 Buck Output Capacitor Selection

The output capacitor C_{OUT0} and C_{OUT1} are shown in Typical Application. A ceramic local output capacitor of 22 µF is required for both outputs. Use ceramic capacitors, X7R or X7T types; do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to perform these functions. Minimum effective output capacitance to ensure good performance is 15 µF per including the DC voltage roll-off, tolerances, aging and temperature effects.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its RESR. The RESR is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the switching frequency of the part. See Table 66.

POL capacitors can be used to improve load transient performance and to decrease the ripple voltage. A higher output capacitance improves the load step behavior and reduces the output voltage ripple as well as decreases the PFM switching frequency. Note that the output capacitor may be the limiting factor in the output voltage ramp, especially for very large (100-µF range) output capacitors. For large output capacitors, the output voltage might be slower than the programmed ramp rate at voltage transitions, because of the higher energy stored on the output capacitance. Also at start-up, the time required to charge the output capacitor to target value might be longer. At shutdown the output voltage is discharged to 0.6 V level using forced-PWM operation. This can increase the input voltage if the load current is small and the output capacitor is large compared to input capacitor. Below 0.6 V level the output capacitor is discharged by the internal discharge resistor and with large capacitor more time is required to settle VOUT down as a consequence of the increased time constant.

Table 66. Recommended Buck Output Capacitors (X7R or X7T Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GCM31CR71A226KE02	22 µF (10%)	1206	3.2 × 1.6 × 1.6	10 V
TDK	CGA5L1X7S1A226M160AC	22 µF (20%)	1206	3.2 × 1.6 × 1.6	10 V

8.2.2.1.4 Boost Input Capacitor Selection

A ceramic input capacitor of 10 µF is sufficient for most applications. Place the input capacitor close to the SW_BST pin of the device. Use X7R types, do not use Y5V or F. See Table 67.

Table 67. Recommended Boost Input Capacitors (X7R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GCM21BR71A106KE22	10 µF (10%)	0805	2.0 x 1.25 x 1.25	10 V

8.2.2.1.5 Boost Output Capacitor Selection

Use ceramic capacitors, X7R or X7T types; do not use Y5V or F. Place the output capacitor as close as possible to the VOUT_BST pin and PGND_BST pin of the device. DC bias voltage characteristics of ceramic capacitors must be considered. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them as part of the capacitor selection process. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to support load transients. See Table 68.

Table 68. Recommended Boost Output Capacitors (X7R or X7T Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GCM31CR71A226KE02	22 µF (10%)	1206	3.2 x 1.6 x 1.6	10 V

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8.2.2.1.6 Supply Filtering Components

The VANA input is used to supply analog and digital circuits in the device. See Table 69 recommended components from for VANA input supply filtering.

Table 69. Recommended Supply Filtering Components

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GCM188R71C104KA37D	100 nF (10%)	0603	1.6 x 0.8 x 0.8	16 V
Murata	GCM155R71C104KA55D	100 nF (10%)	0402	1.0 x 0.5 x 0.5	16 V

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.8 V and 5.5 V. This input supply must be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail should be low enough that the input current transient does not cause too high drop in the LP87702-Q1 supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the LP87702-Q1 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

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10 Layout

10.1 Layout Guidelines

The high frequency and large switching currents of the LP87702-Q1 make the choice of layout important. Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamps to several amps, good power supply layout is much more difficult than most general PCB design. The following steps should be used as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range.

1. Place C_{IN} as close as possible to the VIN_Bx pin and the PGND_Bx pin. Route the V_{IN} trace wide and thick to avoid IR drops. The trace between the positive node of the input capacitor and device VIN_Bx pin(s) as well as the trace between the negative node of the input capacitor and power PGND_Bx pin(s) must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The inductance of the connection is the most important parameter of a local decoupling capacitor - parasitic inductance on these traces must be kept as tiny as possible for proper device operation.
2. The output filter, consisting of L and C_{OUT}, converts the switching signal at SW_Bx to the noiseless output voltage. It should be placed as close as possible to the device keeping the switch node small, for best EMI behavior. Route the traces between the LP87702-Q1's output capacitors and the load's input capacitors direct and wide to avoid losses due to the IR drop.
3. Input for analog blocks (VANA and AGND) should be isolated from noisy signals. Connect VANA directly to a quiet system voltage node and AGND to a quiet ground point where no IR drop occurs. Place the decoupling capacitor as close as possible to the VANA pin.
4. If remote voltage sensing can be used for the load, connect the device feedback pins FB_Bx to the respective sense pins on the load capacitor. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND_Bx, VIN_Bx, and SW_Bx, as well as high bandwidth signals such as the I^2C. Avoid both capacitive as well as inductive coupling by keeping the sense lines short and direct. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible.
5. PGND_Bx, VIN_Bx and SW_Bx should be routed on thick layers. They must not surround inner signal layers which are not able to withstand interference from noisy PGND_Bx, VIN_Bx and SW_Bx.

Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide power traces come with the ability to sink dissipated heat. This can be improved further on multi-layer PCB designs with vias to different planes. This results in reduced junction-to-ambient ($R_{\theta JA}$) and junction-to-board ($R_{\theta JB}$) thermal resistances and thereby reduces the device junction temperature, T_J. It's strongly recommended to perform a careful system-level 2D or full 3D dynamic thermal analysis at the beginning product design process, by using a thermal modeling analysis software.

ADVANCE INFORMATION

10.2 Layout Example

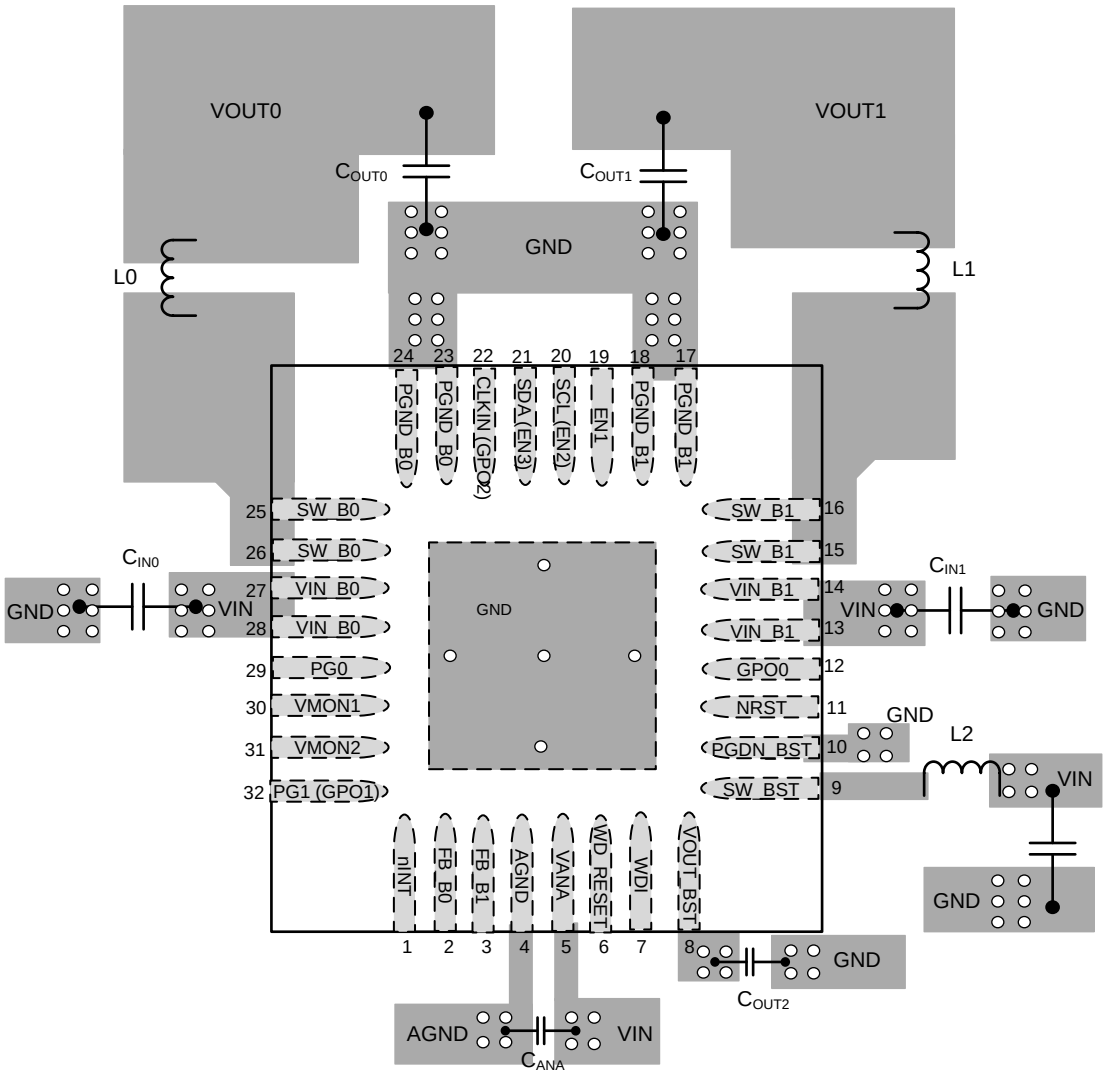

Figure 75. LP87702-Q1 Board Layout Example

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.3 Community Resources

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
P87702DRHBRQ1	ACTIVE	VQFN	RHB	32	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

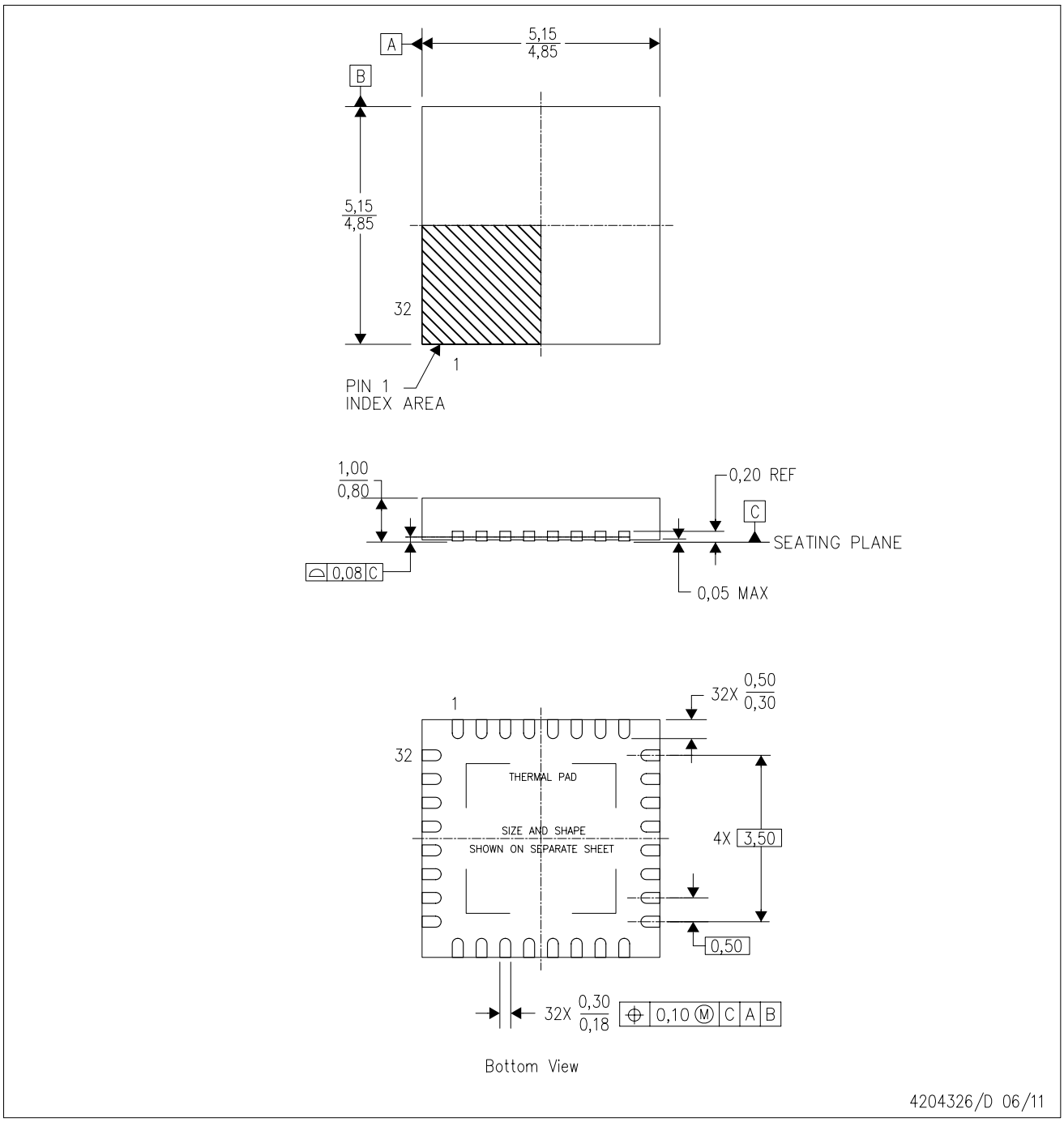
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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