

# PowerMOS transistor

## Voltage clamped logic level FET

**BUK563-48C**

### GENERAL DESCRIPTION

Protected N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.

The device is intended for use in automotive applications. It has built-in zener diodes providing active drain voltage clamping.

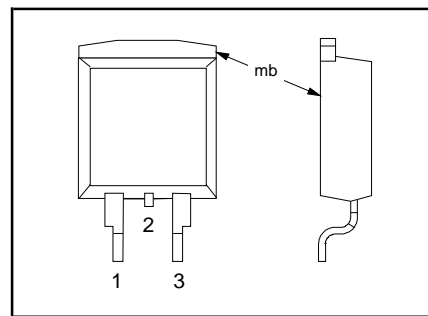
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamp voltage	40	48	58	V
$I_D$	Drain current (DC)			21	A
$P_{tot}$	Total power dissipation			75	W
$T_j$	Junction temperature			175	°C
$W_{DSRR}$	Repetitive clamped turn off energy; $T_j = 150^\circ\text{C}$			50	mJ
$R_{DS(ON)}$	Drain-source on-state resistance; $V_{GS} = 5\text{ V}$			85	mΩ

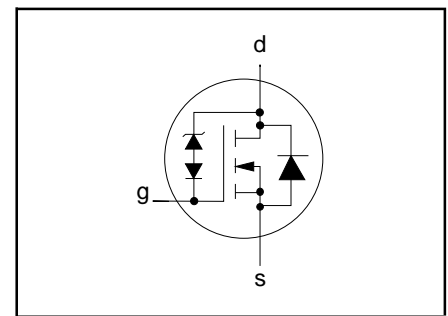
### PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

### PIN CONFIGURATION



### SYMBOL



### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	continuous	-	30	V
$V_{DG}$	Drain-gate voltage	continuous	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$I_D$	Drain current (DC)	$T_{mb} = 25^\circ\text{C}$	-	21	A
$I_D$	Drain current (DC)	$T_{mb} = 100^\circ\text{C}$	-	15	A
$I_{DM}$	Drain current (pulse peak value)	$T_{mb} = 25^\circ\text{C}$	-	84	A
$P_{tot}$	Total power dissipation	$T_{mb} = 25^\circ\text{C}$	-	75	W
$T_{stg}$	Storage temperature	-	-55	175	°C
$T_j$	Junction temperature	-	-55	175	°C

### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	2	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see fig. 18)	-	50	-	K/W

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BUK563-48C

### STATIC CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DG}$	Drain-gate zener voltage	$0.2 \leq -I_G \leq 0.4\text{ mA}$ ; $-55\text{ }^\circ\text{C} \leq T_j \leq 150\text{ }^\circ\text{C}$	38	45	54	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ ; $I_D = 1\text{ mA}$	1.0	1.5	2.0	V
$V_{GS(ON)}$	Gate voltage	$V_{DS} = 10\text{ V}$ ; $I_D = 10\text{ A}$ ; $-55\text{ }^\circ\text{C} \leq T_j \leq 150\text{ }^\circ\text{C}$	2.0	3.1	4.0	V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 30\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 150\text{ }^\circ\text{C}$	-	0.01	1.0	mA
$I_{GSS}$	Gate source leakage current	$V_{GS} = \pm 15\text{ V}$ ; $V_{DS} = 0\text{ V}$ ; $T_j = 150\text{ }^\circ\text{C}$	-	0.1	10	$\mu\text{A}$
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5\text{ V}$ ; $I_D = 10\text{ A}$	-	65	85	m $\Omega$

### DYNAMIC CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain source clamp voltage (peak value)	$R_G = 10\text{ k}\Omega$ ; $I_D = 10\text{ A}$ ; $-55 \leq T_j \leq 150\text{ }^\circ\text{C}$ ; Inductive load.	40	48	58	V
$g_{fs}$	Forward transconductance	$V_{DS} = 25\text{ V}$ ; $I_D = 10\text{ A}$	7	12	-	S
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 25\text{ V}$ ; $f = 1\text{ MHz}$	-	550	825	pF
$C_{oss}$	Output capacitance		-	240	350	pF
$C_{rss}$	Feedback capacitance		-	100	160	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 12\text{ V}$ ; $I_D = 5\text{ A}$ ; $V_{GS} = 5\text{ V}$ ; $R_G = 10\text{ k}\Omega$ ;	-	3.5	-	$\mu\text{s}$
$t_r$	Turn-on rise time		-	22	-	$\mu\text{s}$
$t_{d\ off}$	Turn-off delay time		-	16	-	$\mu\text{s}$
$t_f$	Turn-off fall time		-	18	-	$\mu\text{s}$
$L_d$	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
$L_s$	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

### REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

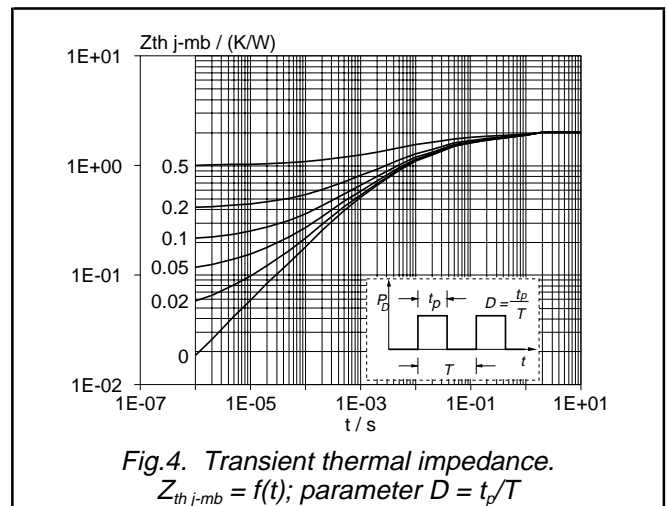
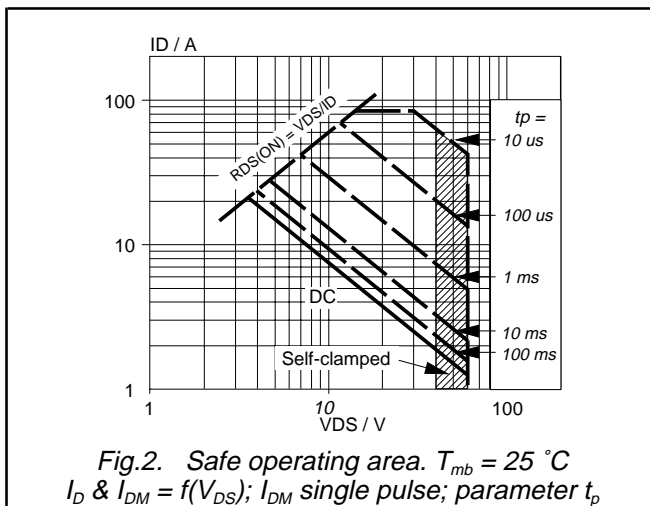
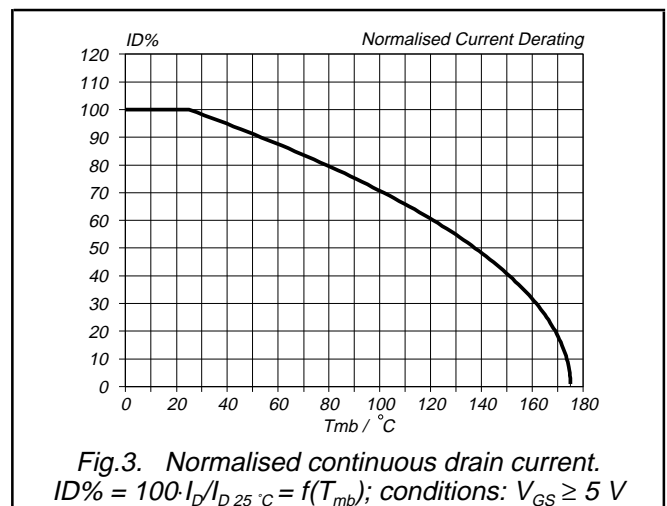
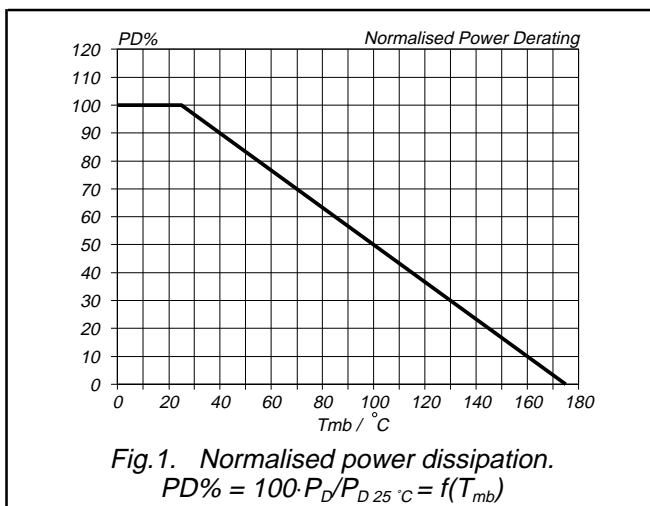
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DR}$	Continuous reverse drain current	-	-	-	21	A
$I_{DRM}$	Pulsed reverse drain current	-	-	-	84	A
$V_{SD}$	Diode forward voltage	$I_F = 21\text{ A}$ ; $V_{GS} = 0\text{ V}$	-	1.3	1.7	V

PowerMOS transistor  
Voltage clamped logic level FET

BUK563-48C

**CLAMPED ENERGY LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$W_{DSRS}$	Non-repetitive drain-source clamped inductive turn off energy	$T_j = 25^\circ\text{C}$ prior to clamping; $I_D = 10\text{ A}$ ; $V_{DD} \leq 16\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $R_G = 10\text{ k}\Omega$ ; inductive load	-	200	mJ
$W_{DSRR}$	Drain-source repetitive clamped inductive turn off energy	$T_j = 150^\circ\text{C}$ prior to clamping; $I_D = 10\text{ A}$ ; $V_{DD} \leq 16\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $R_G = 10\text{ k}\Omega$ ; inductive load	-	50	mJ



PowerMOS transistor  
Voltage clamped logic level FET

BUK563-48C

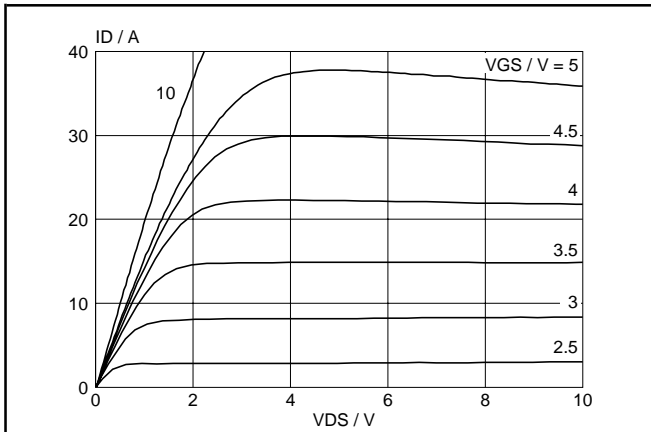


Fig. 5. Typical output characteristics,  $T_j = 25\text{ }^\circ\text{C}$ .  
 $I_D = f(V_{DS})$ ; parameter  $V_{GS}$

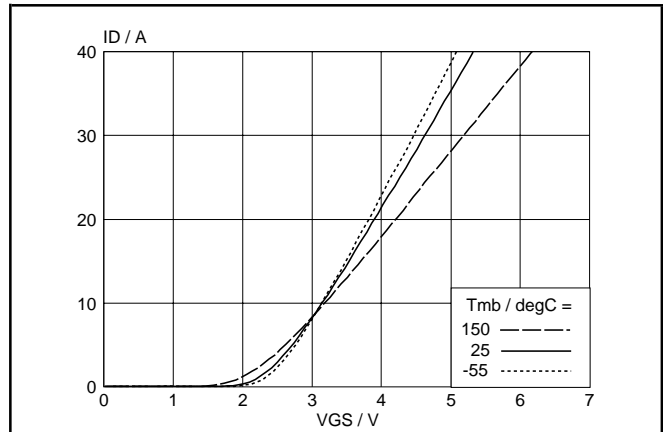


Fig. 8. Typical transfer characteristics.  
 $I_D = f(V_{GS})$ ; conditions:  $V_{DS} = 25\text{ V}$ .

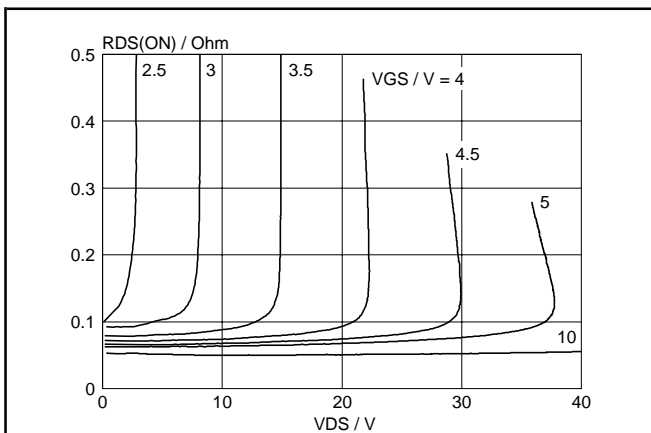


Fig. 6. Typical on-state resistance,  $T_j = 25\text{ }^\circ\text{C}$ .  
 $R_{DS(ON)} = f(I_D)$ ; parameter  $V_{GS}$

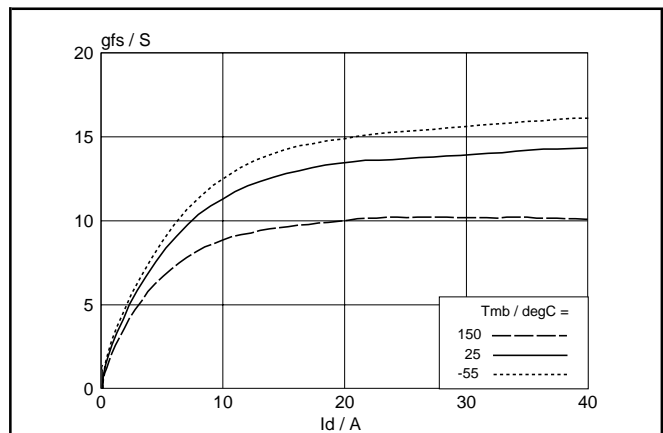


Fig. 9. Typical transconductance.  
 $g_{fs} = f(I_D)$ ; conditions:  $V_{DS} = 25\text{ V}$

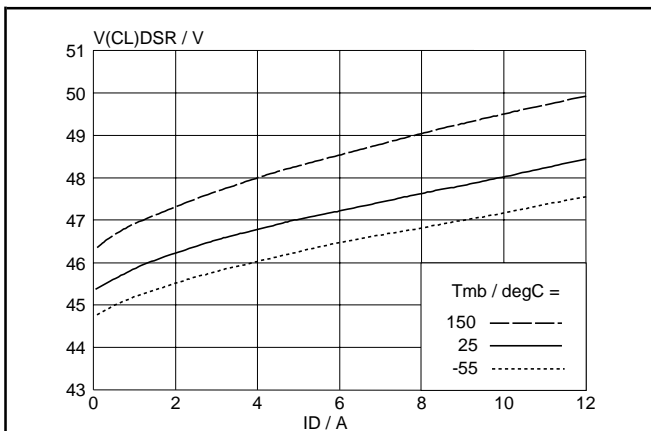


Fig. 7. Typical clamping voltage  
 $V_{(CL)DSR} = f(I_D)$ ; conditions:  $R_G = 10\text{ k}\Omega$

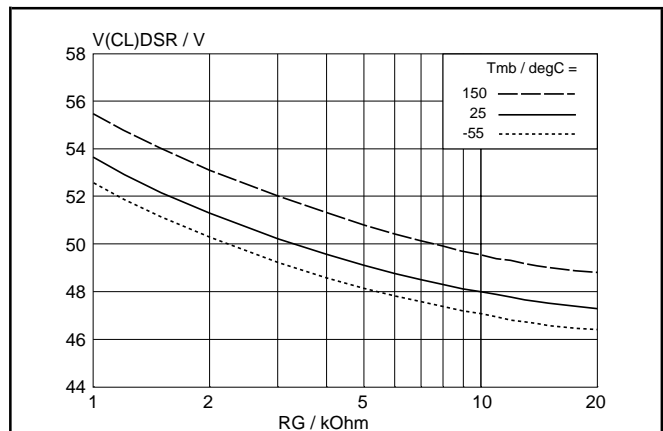


Fig. 10. Typical clamping voltage  
 $V_{(CL)DSR} = f(R_G)$ ; conditions:  $I_D = 10\text{ A}$ .

PowerMOS transistor  
Voltage clamped logic level FET

BUK563-48C

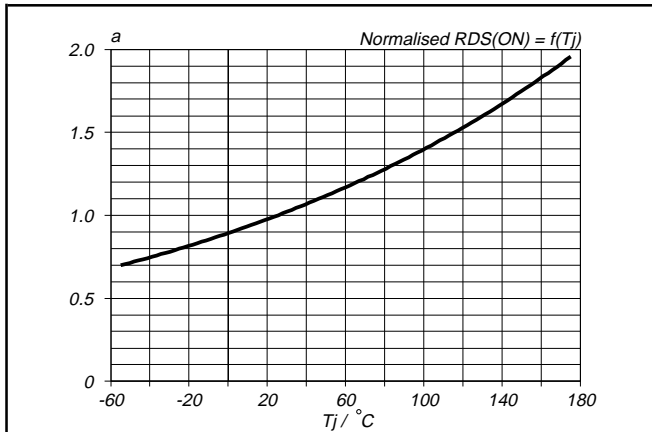


Fig. 11. Normalised drain-source on-state resistance.  
 $a = R_{DS(ON)}/R_{DS(ON)25^\circ C} = f(T_j)$ ;  $I_D = 10\text{ A}$ ;  $V_{GS} = 5\text{ V}$

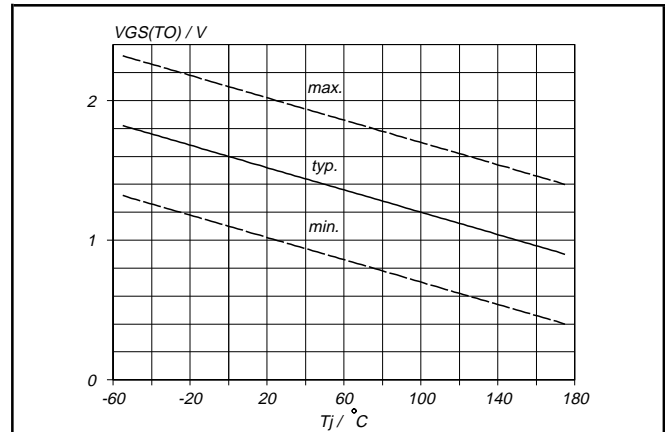


Fig. 14. Gate threshold voltage.  
 $V_{GS(T0)} = f(T_j)$ ; conditions:  $I_D = 1\text{ mA}$ ;  $V_{DS} = V_{GS}$

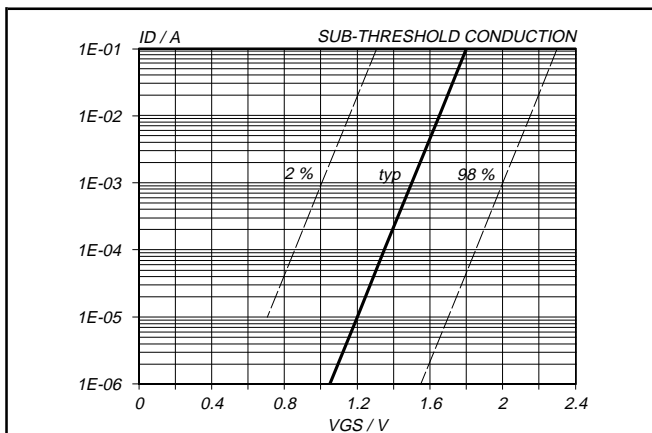


Fig. 12. Sub-threshold drain current.  
 $I_D = f(V_{GS})$ ; conditions:  $T_j = 25^\circ\text{C}$ ;  $V_{DS} = V_{GS}$

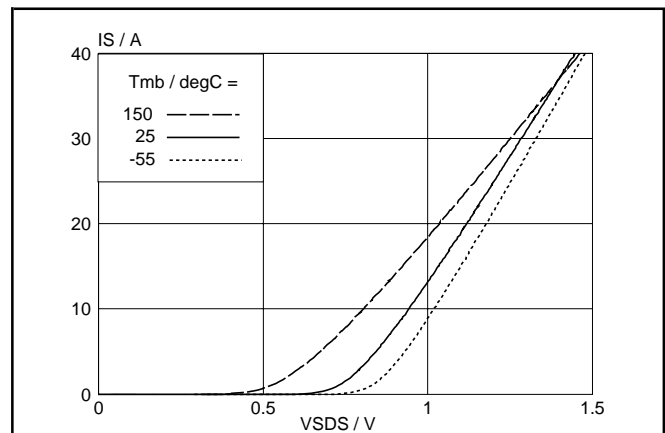


Fig. 15. Typical reverse diode current.  
 $I_F = f(V_{SDS})$ ; conditions:  $V_{GS} = 0\text{ V}$ ; parameter  $T_j$

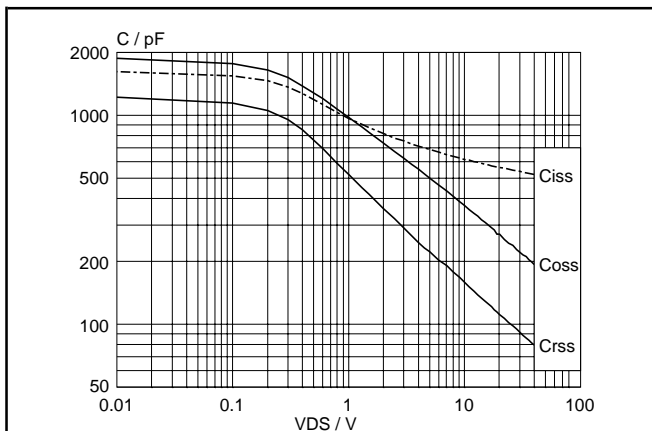


Fig. 13. Typical capacitances,  $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$ .  
 $C = f(V_{DS})$ ; conditions:  $V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

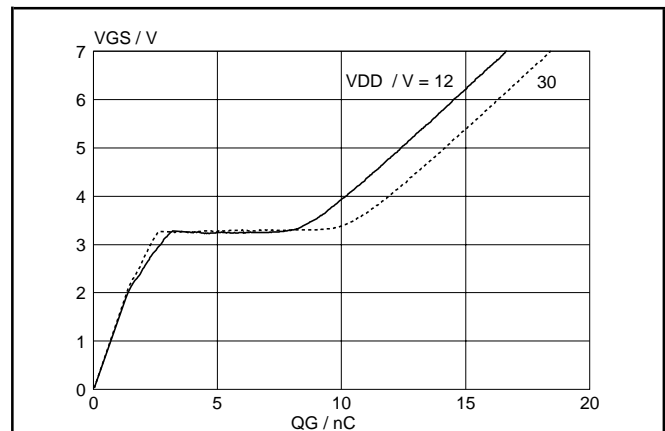
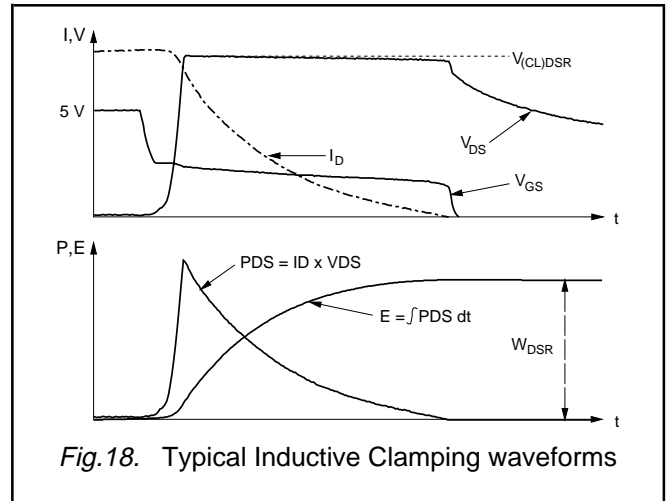
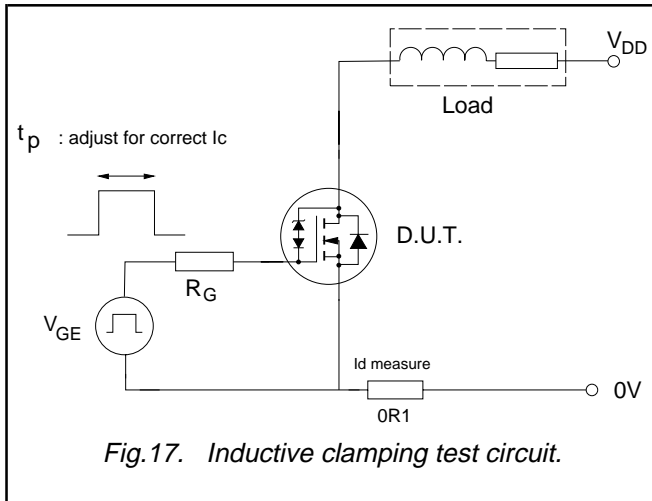


Fig. 16. Typical turn-on gate-charge characteristics.  
 $V_{GS} = f(Q_G)$ ; conditions:  $I_D = 10\text{ A}$ ; parameter  $V_{DS}$

PowerMOS transistor  
Voltage clamped logic level FET

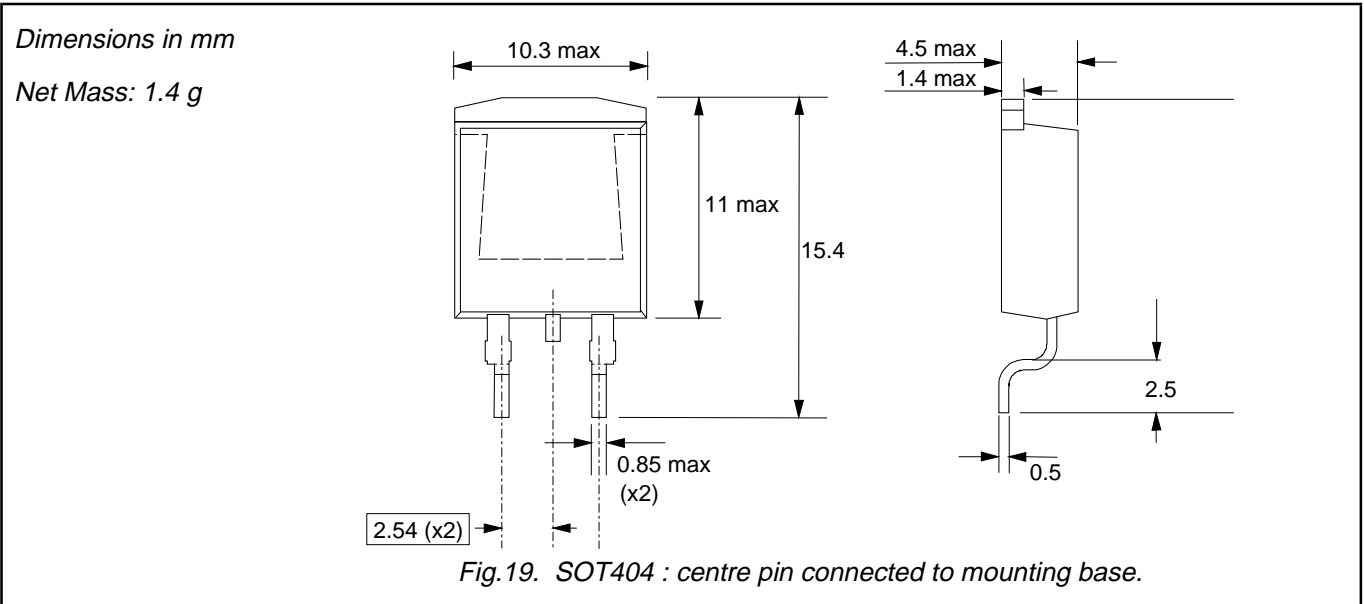
BUK563-48C



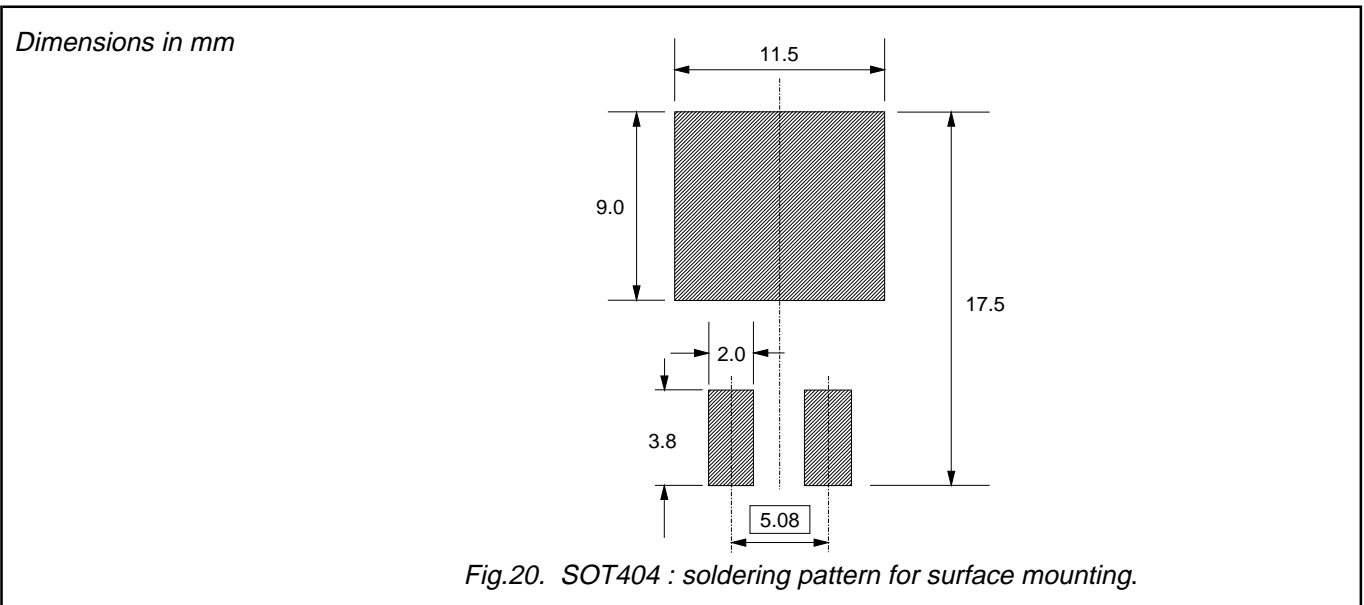
PowerMOS transistor  
Voltage clamped logic level FET

BUK563-48C

**MECHANICAL DATA**



**MOUNTING INSTRUCTIONS**



**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

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# BUK563-48C

### DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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