Half-Duplex, *i*Coupler Isolated RS-485 Transceiver

Data Sheet

ADM2483

FEATURES

- **RS-485 transceiver with electrical data isolation**
- **Complies with ANSI TIA/EIA RS-485-A and ISO 8482: 1987(E)**
- **500 kbps data rate**
- **Slew rate-limited driver outputs**
- **Low power operation: 2.5 mA max**
- **Suitable for 5 V or 3 V operations (V_{DD1})**
- **High common-mode transient immunity: >25 kV/μs**
- **True fail-safe receiver inputs**
- **Chatter-free power-up/power-down protection**
- **256 nodes on bus**
- **Thermal shutdown protection**
- **Safety and regulatory approvals**
    - **UL recognition: 2500 V rms for 1 minute per UL 1577**
    - **CSA Component Acceptance Notice 5A**
        - **IEC 60950-1 800 V rms (basic), 400 V rms (reinforced)**
    - **VDE Certificate of Conformity**
        - **DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12**
        - **V_{IORM} = 560 V peak (reinforced)**
        - **$V_{IORM(DC)}$ = 1500 V dc**
    - **CQC certification per GB4943.1-2011**
- **Operating temperature range: −40°C to +85°C**

APPLICATIONS

- **Low power RS-485/RS-422 networks**
- **Isolated interfaces**
- **Building control networks**
- **Multipoint data transmission systems**

FUNCTIONAL BLOCK DIAGRAM

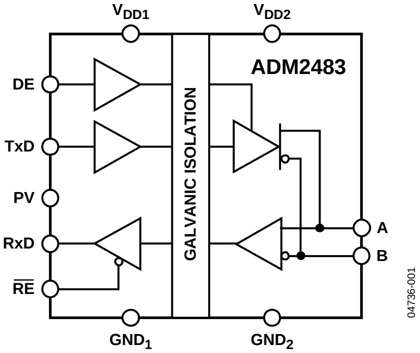

Figure 1.

GENERAL DESCRIPTION

The ADM2483 differential bus transceiver is an integrated, galvanically isolated component designed for bidirectional data communication on balanced, multipoint bus transmission lines. It complies with ANSI EIA/TIA-485-A and ISO 8482: 1987(E). Using the *i*Coupler technology from Analog Devices, Inc., the ADM2483 combines a 3-channel isolator, a three-state differential line driver, and a differential input receiver into a single package. The logic side of the device is powered with either a 5 V or 3 V supply, and the bus side uses a 5 V supply only.

The ADM2483 is slew-limited to reduce reflections with improperly terminated transmission lines. The controlled slew rate limits the data rate to 500 kbps. The device's input impedance is 96 kΩ, allowing up to 256 transceivers on the bus. Its driver has an active-high enable feature. The driver differential outputs and receiver differential inputs are connected internally to form a differential input/output (I/O) port.

When the driver is disabled or when V_{DD1} or V_{DD2} = 0 V, this imposes minimal loading on the bus. An active-high receiver disable feature, which causes the receive output to enter a high impedance state, is provided as well.

The receiver inputs have a true fail-safe feature that ensures a logic-high receiver output level when the inputs are open or shorted. This guarantees that the receiver outputs are in a known state before communication begins and at the point when communication ends.

Current limiting and thermal shutdown features protect against output short circuits and bus contention situations that might cause excessive power dissipation. The part is fully specified over the industrial temperature range and is available in a 16-lead, wide body SOIC package.

Rev. F
Document Feedback

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10/2004—Revision 0: Initial Version

SPECIFICATIONS

2.7 V ≤ V_{DD1} ≤ 5.5 V, 4.75 V ≤ V_{DD2} ≤ 5.25 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Outputs					
Differential Output Voltage, V_{OD}			5	V	R = ∞, see Figure 3
	2.0		5	V	R = 50 Ω (RS-422), see Figure 3
	1.5		5	V	R = 27 Ω (RS-485), see Figure 3
	1.5		5	V	V_{TST} = −7 V to +12 V, V_{DD1} ≥ 4.75, see Figure 4
Δ |V_{OD}| for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, see Figure 3
Common-Mode Output Voltage, V_{OC}			3	V	R = 27 Ω or 50 Ω, see Figure 3
Δ |V_{OC}| for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, see Figure 3
Output Short-Circuit Current, V_{OUT} = High	−250		+250	mA	−7 V ≤ V_{OUT} ≤ +12 V
Output Short-Circuit Current, V_{OUT} = Low	−250		+250	mA	−7 V ≤ V_{OUT} ≤ +12 V
Logic Inputs					
Input High Voltage	0.7 V_{DD1}			V	TxD, DE, $\overline{RE}$, PV
Input Low Voltage			0.25 V_{DD1}	V	TxD, DE, $\overline{RE}$, PV
CMOS Logic Input Current (TxD, DE, $\overline{RE}$, PV)	−10	+0.01	+10	µA	TxD, DE, $\overline{RE}$, PV = V_{DD1} or 0 V
RECEIVER					
Differential Inputs					
Differential Input Threshold Voltage, V_{TH}	−200	−125	−30	mV	−7 V ≤ V_{CM} ≤ +12 V
Input Hysteresis		20		mV	−7 V ≤ V_{CM} ≤ +12 V
Input Resistance (A, B)	96	150		kΩ	−7 V ≤ V_{CM} ≤ +12 V
Input Current (A, B)			0.125	mA	V_{IN} = +12 V
			−0.1	mA	V_{IN} = −7 V
RxD Logic Output					
Output High Voltage	V_{DD1} − 0.1			V	I_{OUT} = 20 µA, V_A − V_B = 0.2 V
	V_{DD1} − 0.4	V_{DD1} − 0.2		V	I_{OUT} = 4 mA, V_A − V_B = 0.2 V
Output Low Voltage			0.1	V	I_{OUT} = −20 µA, V_A − V_B = −0.2 V
			0.4	V	I_{OUT} = −4 mA, V_A − V_B = −0.2 V
Output Short-Circuit Current	7		85	mA	V_{OUT} = GND or V_{CC}
Three-State Output Leakage Current			±1	µA	0.4 V ≤ V_{OUT} ≤ 2.4 V
POWER SUPPLY CURRENT					
Logic Side			2.5	mA	4.5 V ≤ V_{DD1} ≤ 5.5 V, outputs unloaded, $\overline{RE}$ = 0 V
			1.3	mA	2.7 V ≤ V_{DD1} ≤ 3.3 V, outputs unloaded, $\overline{RE}$ = 0 V
Bus Side			2.0	mA	Outputs unloaded, DE = 5 V
			1.7	mA	Outputs unloaded, DE = 0 V
COMMON-MODE TRANSIENT IMMUNITY[1]	25			kV/µs	TxD = V_{DD1} or 0 V, V_{CM} = 1 kV, transient magnitude = 800 V

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[1] Common-mode transient immunity is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

2.7 V ≤ V_{DD1} ≤ 5.5 V, 4.75 V ≤ V_{DD2} ≤ 5.25 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Maximum Data Rate	500			kbps	
Propagation Delay, t_{PLH}, t_{PHL}	250		620	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 5 and Figure 9
Skew, t_{SKEW}			40	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 5 and Figure 9
Rise/Fall Time, t_R, t_F	200		600	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 5 and Figure 9
Enable Time			1050	ns	R_L = 500 Ω, C_L = 100 pF, see Figure 6 and Figure 11
Disable Time			1050	ns	R_L = 500 Ω, C_L = 15 pF, see Figure 6 and Figure 11
RECEIVER					
Propagation Delay, t_{PLH}, t_{PHL}	400		1050	ns	C_L = 15 pF, see Figure 7 and Figure 10
Differential Skew, t_{SKEW}			250	ns	C_L = 15 pF, see Figure 7 and Figure 10
Enable Time		25	70	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 8 and Figure 12
Disable Time		40	70	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 8 and Figure 12
POWER VALID INPUT					
Enable Time		1	2	μs	
Disable Time		3	5	μs	

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

Table 3.

Parameter	Rating
V_{DD1}	−0.5 V to +7 V
V_{DD2}	−0.5 V to +6 V
Digital Input Voltage (DE, $\overline{RE}$, TxD)	−0.5 V to V_{DD1} + 0.5 V
Digital Output Voltage	
RxD	−0.5 V to V_{DD1} + 0.5 V
Driver Output/Receiver Input Voltage	−9 V to +14 V
ESD Rating: Contact	
Human Body Model (A, B Pins)	±2 kV
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +150°C
Average Output Current per Pin	−35 mA to +35 mA
θ_{JA} Thermal Impedance	73°C/W
Lead Temperature	
Soldering (10 sec)	260°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 4. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Reference Standard
AC Voltage			
Bipolar Waveform			
Basic Insulation	565	V_{PEAK}	50-year minimum lifetime
Reinforced Insulation	565	V_{PEAK}	50-year minimum lifetime
Unipolar Waveform			
Basic Insulation	1131	V_{PEAK}	50-year minimum lifetime
Reinforced Insulation	1131	V_{PEAK}	50-year minimum lifetime
DC Voltage			
Basic Insulation	1517	V_{PEAK}	Pollution Degree 2, Material Group I
Reinforced Insulation	757	V_{PEAK}	Pollution Degree 2, Material Group I

[1] Refers to continuous voltage magnitude imposed across the isolation barrier.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE CHARACTERISTICS

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-Output)[1]	C_{I-O}		3		pF	f = 1 MHz
Input Capacitance[2]	C_I		4		pF	
Input IC Junction-to-Case Thermal Resistance	θ_{JCI}		33		°C/W	Thermocouple located at center of package underside
Output IC Junction-to-Case Thermal Resistance	θ_{JCO}		28		°C/W	Thermocouple located at center of package underside

[1] Device considered a 2-terminal device: Pins 1, 2, 3, 4, 5, 6, 7, and 8 shorted together, and Pins 9, 10, 11, 12, 13, 14, 15, and 16 shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADM2483 has been approved by the following organizations:

Table 6.

UL[1]	CSA	CQC	VDE[2]
Recognized Under 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Approved Under CQC11-471543-2012	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
	IEC 609501 800 V rms (1131 V_{PEAK}) basic, 400 V rms (565 V_{PEAK}) reinforced	Basic insulation per GB4943.1-2011, 415 V rms (588 V_{PEAK}) maximum working voltage, tropical climate, altitude ≤ 5000 meters	Reinforced insulation, V_{IORM} = 565 V peak, $V_{IORM(DC)}$ = 1500 V dc
File E214100	File 205078	File CQC14001114898	File 2471900-4880-0001

[1] In accordance with UL1577, each ADM2483 is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 5 μA).
[2] In accordance with VDE V 0884-10, each ADM2483 is proof tested by applying an insulation test voltage ≥2813 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 7.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.6 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.6 min	mm	Measured from input terminals to output terminals, shortest distance along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L(PCB)	8.1 min	mm	
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400 or >600	V	DIN IEC 112/VDE 0303 Part 1[1]
Isolation Group		I or II		Material Group (Table 1 in DIN VDE 0110,1/89)[1]

[1] An ampersand (&) on the physical package denotes the CSA attestation of CTI>600 V and isolation of Material Group I.

DIN V VDE V 0884-10 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation only within this safety limit data. Maintenance of this safety data shall be ensured by means of protective circuits.

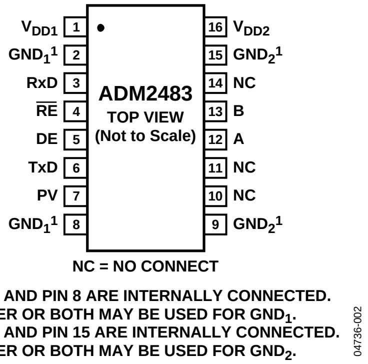
An asterisk (*) on the physical package denotes DIN V VDE V 0884-10 approval.

Table 8.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤150 V rms			I to IV	
For Rated Mains Voltage ≤300 V rms			I to III	
For Rated Mains Voltage ≤400 V rms			I to II	
Climatic Classification			40/100/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage	See Absolute Maximum Ratings[1]			
Reinforced		V_{IORM}	560	V_{PEAK}
DC (Basic)		$V_{IORM(DC)}$	1500	V_{DC}
Input to Output test Voltage, Method b1	$V_{IORM(DC)} \times 1.875 = V_{pd(m)}$, 100% production tested, $t_{ini} = t_m = 1$ sec, partial discharge <5 pC	$V_{pd(m)}$	2813	V_{PEAK}
Input-to-Output Test Voltage, Method a				
After Environmental Tests, Subgroup 1	$V_{IORM(DC)} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge <5 pC	$V_{pd(m)}$	2250	V_{PEAK}
After Input and/or Safety Test, Subgroup 2 and Subgroup 3	$V_{IORM(DC)} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge <5 pC	$V_{pd(m)}$	1800	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	4200	V_{PEAK}
Surge Isolation Voltage Reinforced	$V_{PEAK} = 10$ kV	V_{IOSM}	6250	V_{PEAK}
Safety-Limiting Values	Maximum value allowed in the event of a failure; see Figure 23			
Maximum Junction Temperature		T_S	150	°C
Input Current		$I_{S, INPUT}$	265	mA
Output Current		$I_{S, OUTPUT}$	335	mA
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

[1] The Absolute Maximum Ratings section places limitations on the device due to 50-year lifetime to 1% failure or due to package restrictions (on maximum continuous working voltage for ac bipolar, ac unipolar, and dc voltages, as well as basic and reinforced insulation).

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NC = NO CONNECT

[1] PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED. EITHER OR BOTH MAY BE USED FOR GND_1. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED. EITHER OR BOTH MAY BE USED FOR GND_2.

Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply (Logic Side).
2, 8	GND_1	Ground (Logic Side).
3	RxD	Receiver Output Data. When enabled, if (A – B) ≥ –30 mV, then RxD = high. If (A – B) ≤ –200 mV, then RxD = low. This is a tristate output when the receiver is disabled, that is, when $\overline{RE}$ is driven high.
4	$\overline{RE}$	Receiver Enable Input. This is an active-low input. Driving this input low enables the receiver, and driving it high disables the receiver.
5	DE	Driver Enable Input. Driving the input high enables the driver, and driving it low disables the driver.
6	TxD	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
7	PV	Power_Valid. Used during power-up and power-down. See the Applications Information section.
9, 15	GND_2	Ground (Bus Side).
10, 11, 14	NC	No Connect.
12	A	Noninverting Driver Output/Receiver Input. When the driver is disabled, or when V_{DD1} or V_{DD2} is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
13	B	Inverting Driver Output/Receiver Input. When the driver is disabled, or when V_{DD1} or V_{DD2} is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
16	V_{DD2}	Power Supply (Bus Side).

TEST CIRCUITS

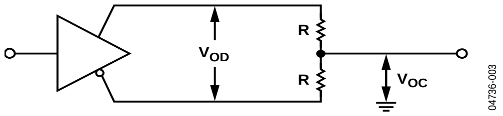


Figure 3. Driver Voltage Measurement

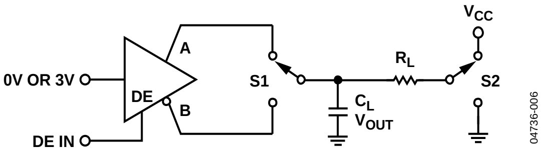


Figure 6. Driver Enable/Disable

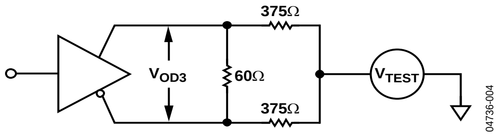


Figure 4. Driver Voltage Measurement

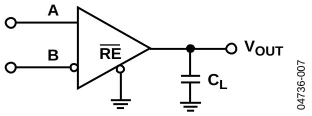


Figure 7. Receiver Propagation Delay

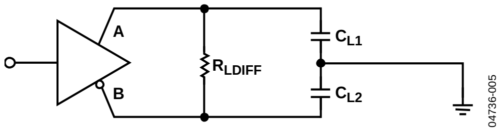


Figure 5. Driver Propagation Delay

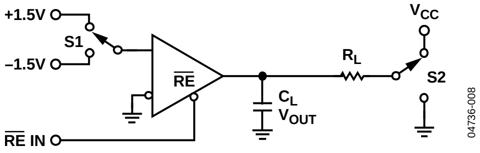


Figure 8. Receiver Enable/Disable

SWITCHING CHARACTERISTICS

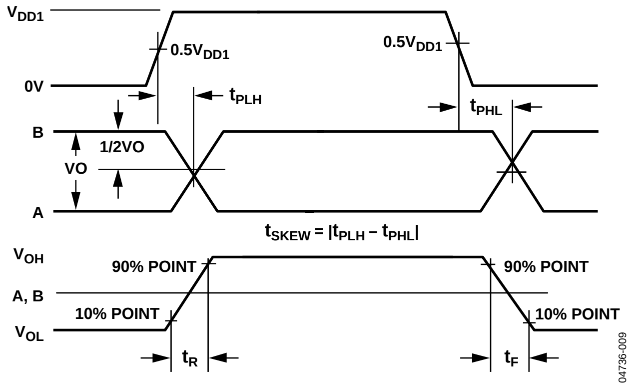


Figure 9. Driver Propagation Delay, Rise/Fall Timing

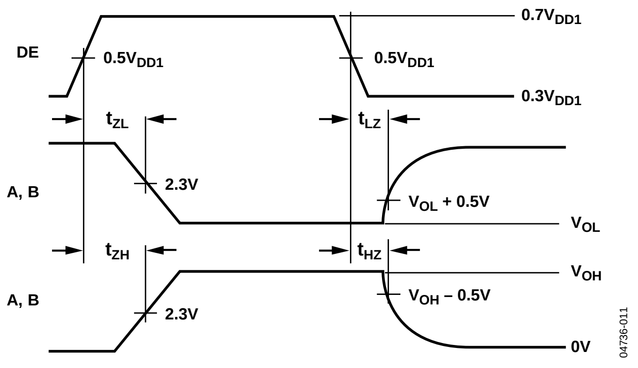


Figure 11. Driver Enable/Disable Timing

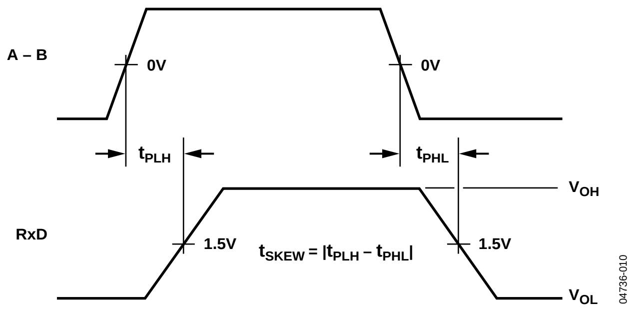


Figure 10. Receiver Propagation Delay

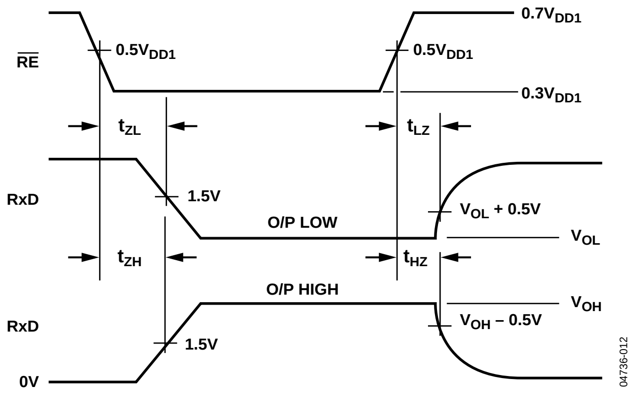


Figure 12. Receiver Enable/Disable Timing

TYPICAL PERFORMANCE CHARACTERISTICS

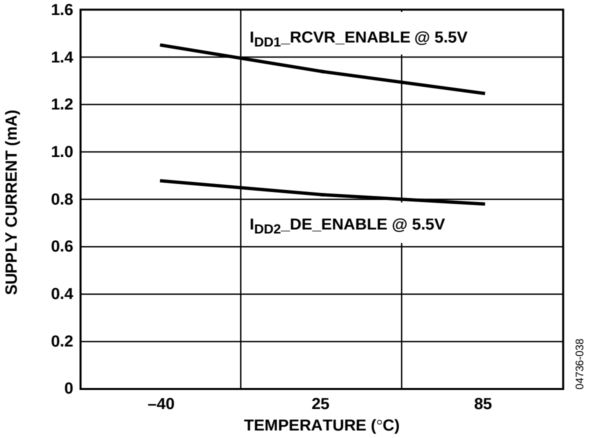


Figure 13. Unloaded Supply Current vs. Temperature

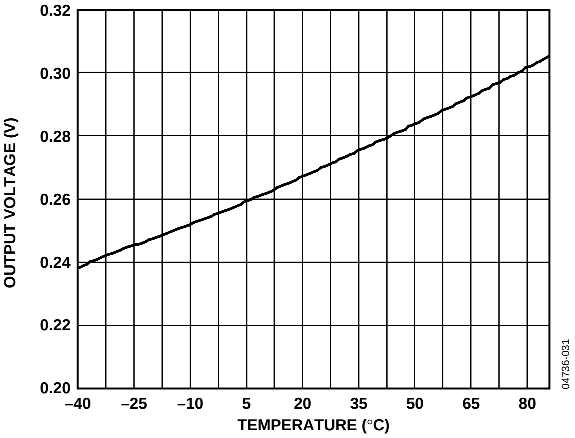


Figure 16. Receiver Output Low Voltage vs. Temperature, I = –4mA

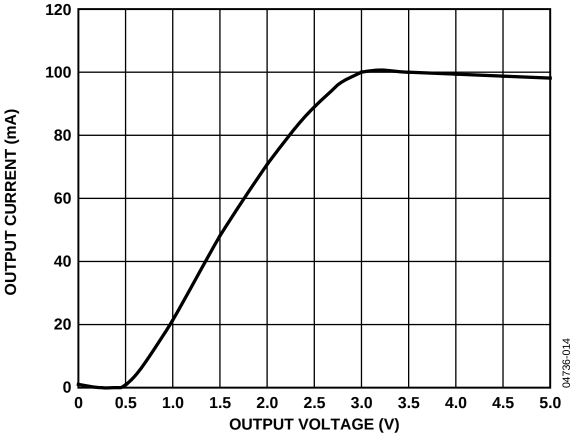


Figure 14. Output Current vs. Driver Output Low Voltage

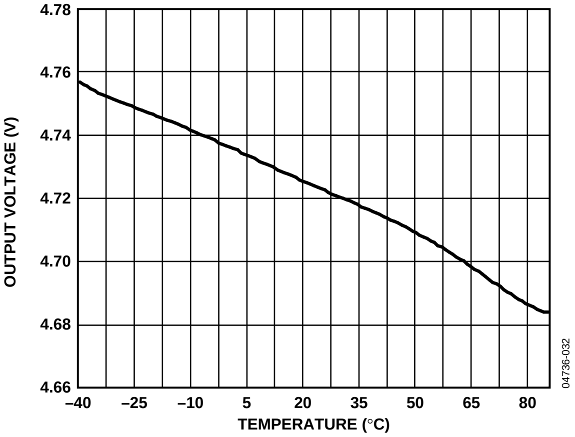


Figure 17. Receiver Output High Voltage vs. Temperature, I = 4 mA

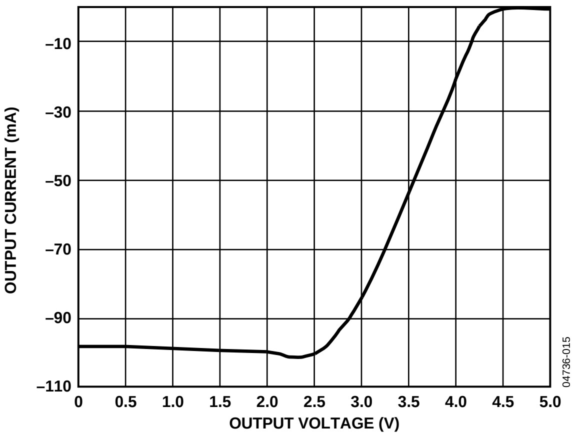


Figure 15. Output Current vs. Driver Output High Voltage

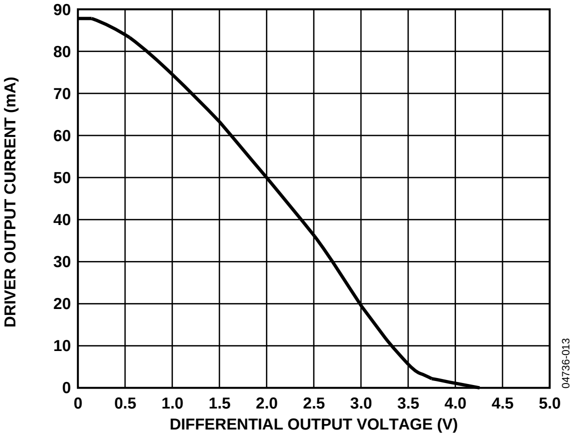


Figure 18. Driver Output Current vs. Differential Output Voltage

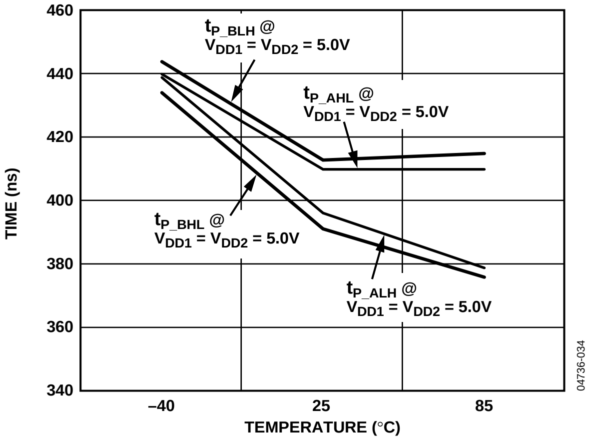


Figure 19. Driver Propagation Delay vs. Temperature

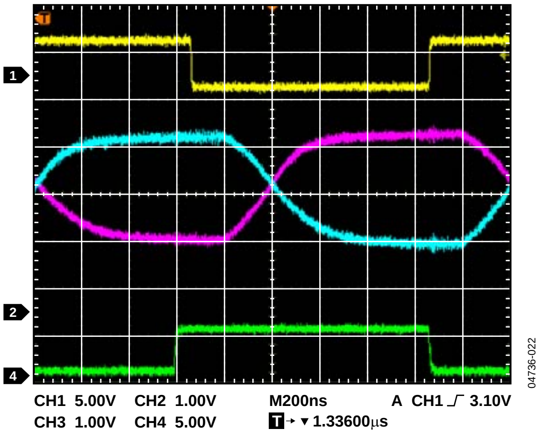


Figure 21. Driver/Receiver Propagation Delay High to Low

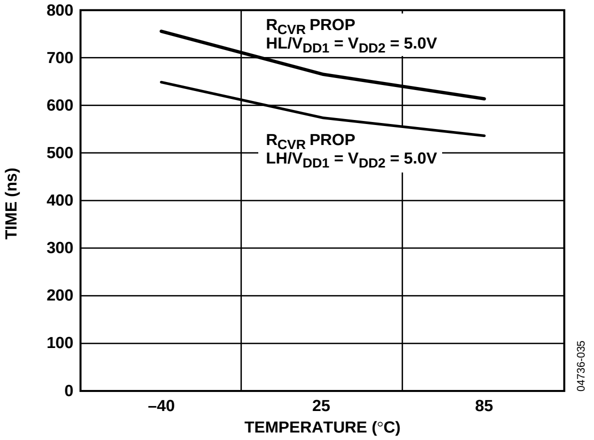


Figure 20. Receiver Propagation Delay vs. Temperature

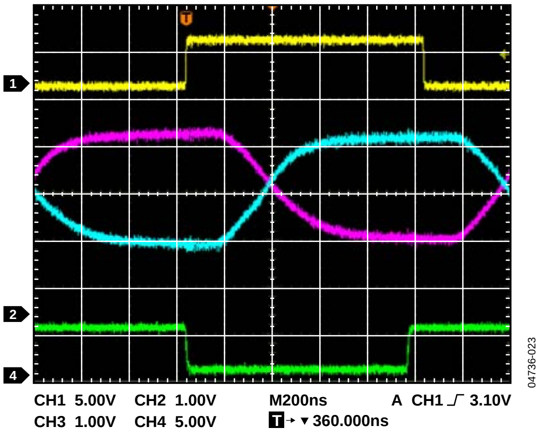


Figure 22. Driver/Receiver Propagation Delay Low to High

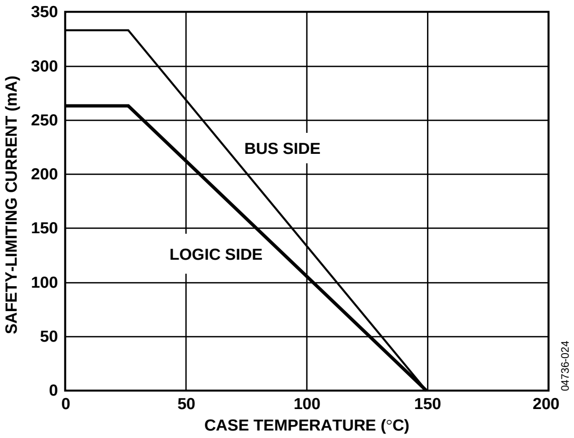


Figure 23. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per VDE V 0884

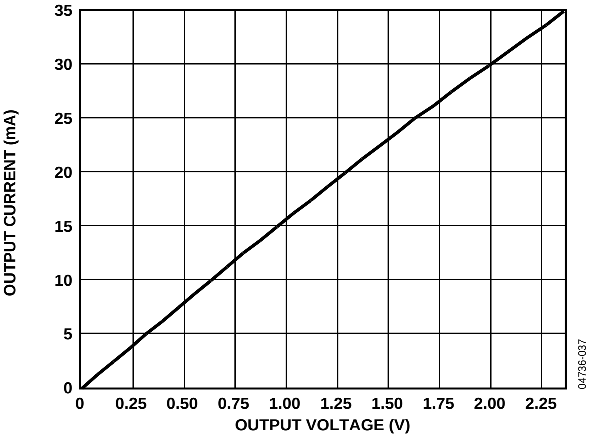


Figure 25. Output Current vs. Receiver Output Low Voltage

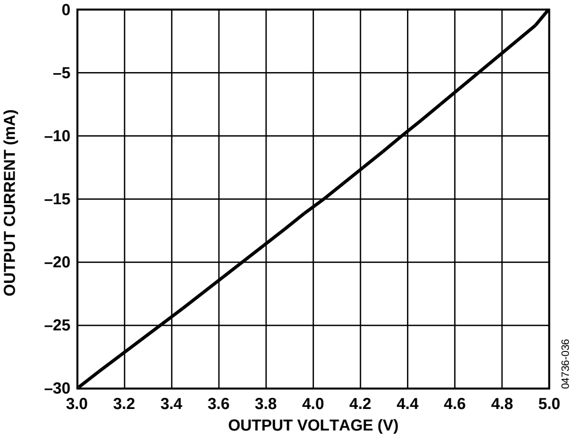


Figure 24. Output Current vs. Receiver Output High Voltage

CIRCUIT DESCRIPTION

ELECTRICAL ISOLATION

In the ADM2483, electrical isolation is implemented on the logic side of the interface. Therefore, the part has two main sections: a digital isolation section and a transceiver section (see Figure 26). Driver input and data enable signals, applied to the TxD and DE pins, respectively, and referenced to logic ground (GND_1), are coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground (GND_2). Similarly, the receiver output, referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to logic ground.

iCoupler Technology

The digital signals are transmitted across the isolation barrier using *i*Coupler technology. This technique uses chip scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are then decoded into the binary value that was originally transmitted.

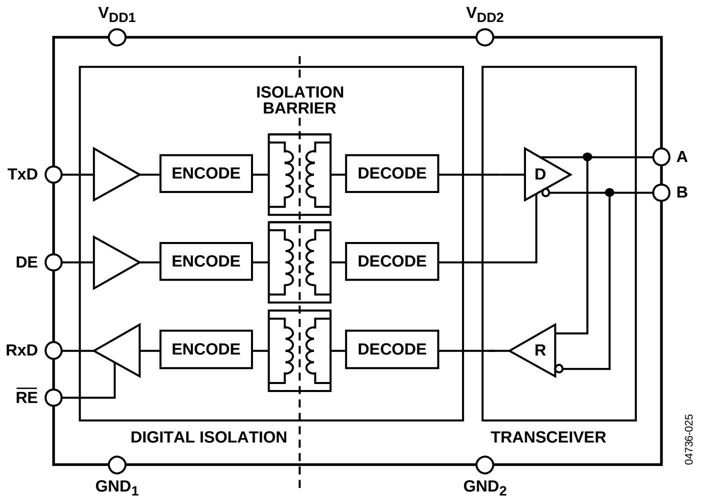


Figure 26. ADM2483 Digital Isolation and Transceiver Sections

TRUTH TABLES

The following truth tables use these abbreviations:

Letter	Description
H	High level
L	Low level
X	Irrelevant
Z	High impedance (off)
NC	Disconnected

Table 10. Transmitting

Supply Status		Inputs		Outputs	
V_{DD1}	V_{DD2}	DE	TxD	A	B
On	On	H	H	H	L
On	On	H	L	L	H
On	On	L	X	Z	Z
On	Off	X	X	Z	Z
Off	On	X	X	Z	Z
Off	Off	X	X	Z	Z

Table 11. Receiving

Supply Status		Inputs		Outputs
V_{DD1}	V_{DD2}	A – B (V)	$\overline{RE}$	RxD
On	On	>−0.03	L or NC	H
On	On	<−0.2	L or NC	L
On	On	−0.2 < A – B < −0.03	L or NC	Indeterminate
On	On	Inputs open	L or NC	H
On	On	X	H	Z
On	Off	X	L or NC	H
Off	On	X	L or NC	H
Off	Off	X	L or NC	L

POWER-UP/POWER-DOWN CHARACTERISTICS

The power-up/power-down characteristics of the ADM2483 are in accordance with the supply thresholds shown in Table 12. Upon power-up, the ADM2483 output signals (A, B, and RxD) reach their correct state once both supplies exceed their thresholds. Upon power-down, the ADM2483 output signals retain their correct state until at least one of the supplies drops below its power-down threshold. When the V_{DD1} power-down threshold is crossed, the ADM2483 output signals reach their unpowered states within 4 µs.

Table 12. Power-Up/Power-Down Thresholds

Supply	Transition	Threshold (V)
V_{DD1}	Power-up	2.0
V_{DD1}	Power-down	1.0
V_{DD2}	Power-up	3.3
V_{DD2}	Power-down	2.4

THERMAL SHUTDOWN

The ADM2483 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

TRUE FAIL-SAFE RECEIVER INPUTS

The receiver inputs have a true fail-safe feature, which ensures that the receiver output is high when the inputs are open or shorted. During line-idle conditions, when no driver on the bus is enabled, the voltage across a terminating resistance at the receiver input decays to 0 V. With traditional transceivers, receiver input thresholds specified between −200 mV and +200 mV mean that external bias resistors are required on the A and B pins to ensure that the receiver outputs are in a known state. The true fail-safe receiver input feature eliminates the need for bias resistors by specifying the receiver input threshold between −30 mV and −200 mV. The guaranteed negative threshold means that when the voltage between A and B decays to 0 V, the receiver output is guaranteed to be high.

MAGNETIC FIELD IMMUNITY

Because *i*Couplers use a coreless technology, no magnetic components are present, and the problem of magnetic saturation of the core material does not exist. Therefore, *i*Couplers have essentially infinite dc field immunity. The analysis that follows defines the conditions under which this might occur. The 3 V operating condition of the ADM2483 is examined because it represents the most susceptible mode of operation.

The limitation on the *i*Coupler's ac magnetic field immunity is set by the condition in which the induced error voltage in the receiving coil (the bottom coil in this case) is made sufficiently large, either to falsely set or reset the decoder. The voltage induced across the bottom coil is given by

$$V = \left(\frac{-d\beta}{dt}\right)\sum \pi r_n^2; \quad n = 1, 2, \ldots, N$$

where if the pulses at the transformer output are greater than 1.0 V in amplitude:

β = magnetic flux density (gauss)

N = number of turns in receiving coil

r_n = radius of nth turn in receiving coil (cm)

The decoder has a sensing threshold of about 0.5 V; therefore, there is a 0.5 V margin in which induced voltages can be tolerated.

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 27.

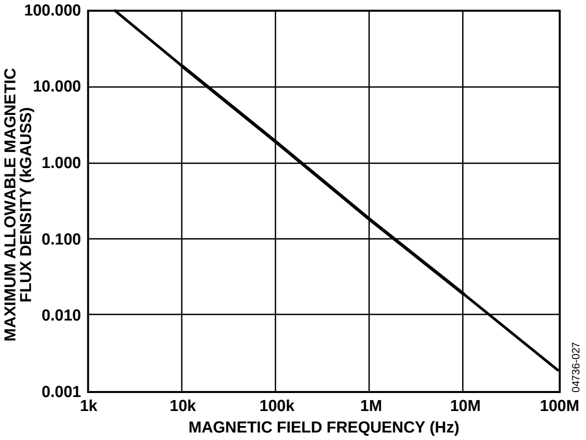


Figure 27. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kGauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V. This is well above the 0.5 V sensing threshold of the decoder.

These magnetic flux density values are shown in Figure 28, using more familiar quantities such as maximum allowable current flow, at given distances away from the ADM2483 transformers.

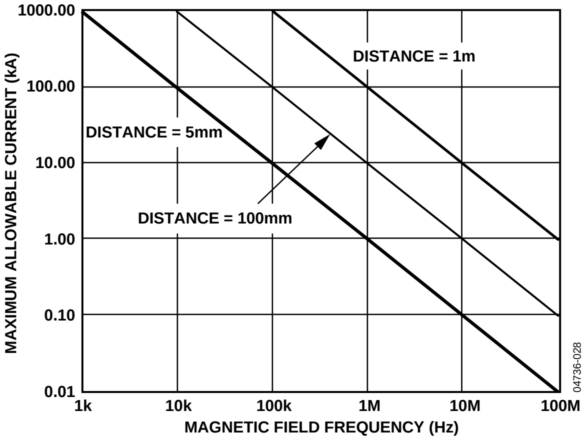


Figure 28. Maximum Allowable Current for Various Current-to-ADM2483 Spacings

At combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce large enough error voltages to trigger the thresholds of succeeding circuitry. To avoid this possibility, care should be taken in the layout of such traces.

APPLICATIONS INFORMATION

POWER_VALID INPUT

To avoid chatter on the A and B outputs caused by slow power-up and power-down transients on V_{DD1} (>100 μs/V), the ADM2483 features a power_valid (PV) digital input. This pin should be driven low until V_{DD1} exceeds 2.0 V. When V_{DD1} is greater than 2.0 V, the pin should be driven high. Conversely, upon power-down, the PV should be driven low before V_{DD1} reaches 2.0 V.

The power_valid input can be driven, for example, by the output of a system reset circuit such as the ADM809Z, which has a threshold voltage of 2.32 V.

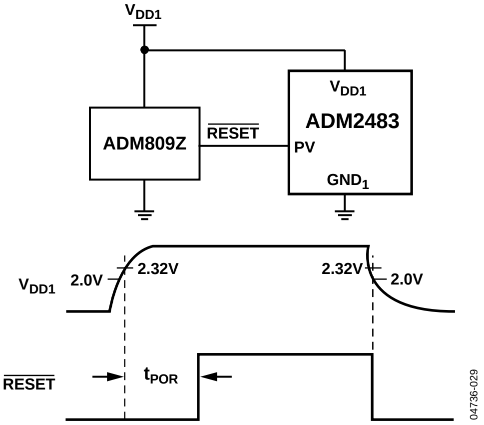


Figure 29. Driving PV with ADM809Z

ISOLATED POWER SUPPLY CIRCUIT

The ADM2483 requires isolated power capable of 5 V at 100 mA to be supplied between the V_{DD2} and GND_2 pins. If no suitable integrated power supply is available, a discrete circuit, such as the one in Figure 30, can be used. A center-tapped transformer provides electrical isolation. The primary winding is excited with a pair of square waveforms that are 180° out of phase with each other. A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP667 linear voltage regulator provides a regulated power supply to the ADM2483's bus-side circuitry.

To create the pair of square waves, a D-type flip-flop with complementary $Q/\overline{Q}$ outputs is used. The flip-flop can be connected so that output Q follows the clock input signal. If no local clock signal is available, a simple digital oscillator can be implemented with a hex-inverting Schmitt trigger and a resistor and capacitor. In this case, values of 3.9 kΩ and 1 nF generate a 364 kHz square wave. A pair of discrete NMOS transistors, switched by the $Q/\overline{Q}$ flip-flop outputs, conduct current through the center tap of the primary transformer, winding in an alternating fashion.

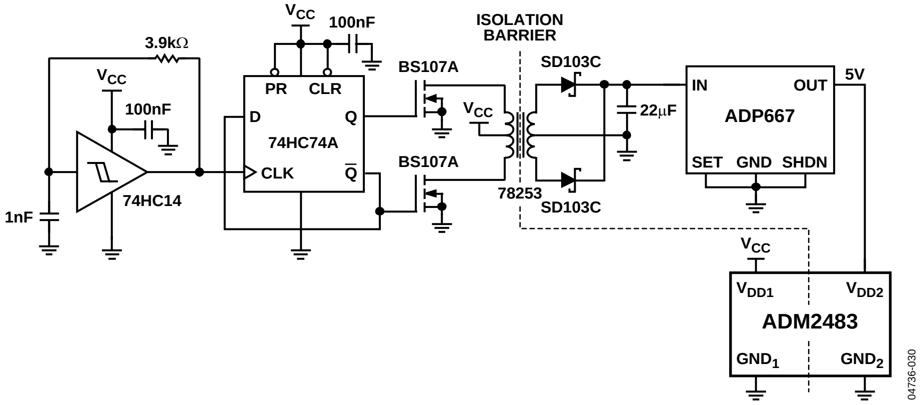
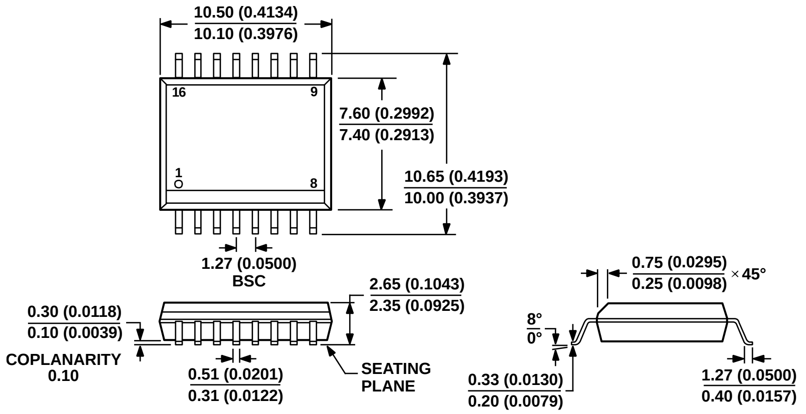


Figure 30. Isolated Power Supply Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 31. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1, 2]	Data Rate (kbps)	Temperature Range	Package Description	Package Option
ADM2483BRW	500	−40°C to +85°C	16-Lead, Wide Body SOIC_W	RW-16
ADM2483BRW-REEL	500	−40°C to +85°C	16-Lead, Wide Body SOIC_W	RW-16
ADM2483BRWZ	500	−40°C to +85°C	16-Lead, Wide Body SOIC_W	RW-16
ADM2483BRWZ-REEL	500	−40°C to +85°C	16-Lead, Wide Body SOIC_W	RW-16
EVAL-ADM2483EBZ			ADM2483 Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] -REEL suffix designates a 13-inch (1,000 units) tape-and-reel option.