# WS7808QD

## 0.1GHz – 3GHz DP8T Diversity Receive Antenna Switch

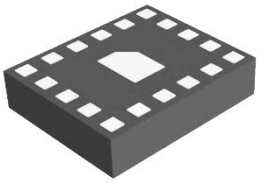
http//:www.sh-willsemi.com

## Descriptions

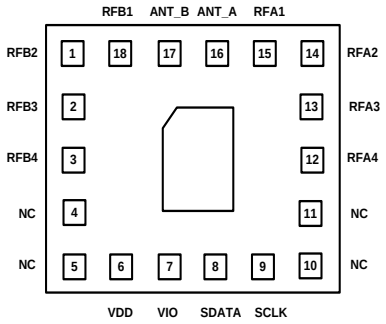
The WS7808QD is a dual single-pole, four-throw (2xSP4T) with Mobile Industry Processor Interface (MIPI) controlled antenna switch designed specifically for receive diversity in carrier aggregation applications. The device is optimized for broadband performance. Using advanced switching technologies, the WS7808QD maintains low insertion loss and high isolation for all switching paths. The high linearity performance and low insertion loss achieved by the WS7808QD makes it an ideal choice for carrier aggregation applications in both main and diversity antenna switching. The switch also exhibits excellent second/third order intermodulation distortion (IMD2/IMD3) performance.

Switching is controlled by an integrated MIPI decoder. The two switches can be configured independently. There are separate registers for each SP4T. No external DC blocking capacitors are required on the RF paths if no DC voltage is applied to those paths.

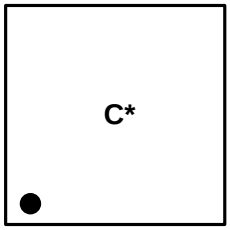
The WS7808QD is manufactured in a compact, 2.0 x 2.4 x 0.55 mm, 18-pin surface-mount Quad Flat No-Lead (QFN) package.



**QFN2.0x2.4-18L（Bottom view）**




**Pin configuration (Top view)**




C = Device code

* = Month code（A~Z）

**Marking (Top view)**

## Features

- Working frequency up to 3 GHz
- Single, positive DC power supply (2.4 to 3.1 V)
- Integrated programmable MIPI interface using separate registers for ANT_A and ANT_B bands
- Dual antenna ports can be connected externally to a diplexer
- Small QFN (18-pin, 2.0 x 2.4 x 0.55 mm) package

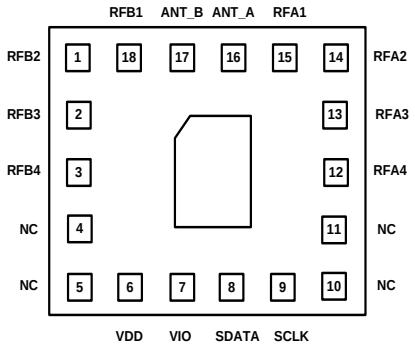
## Applications

- Cell phones
- Tablets
- Other RF front-end modules

## Order information

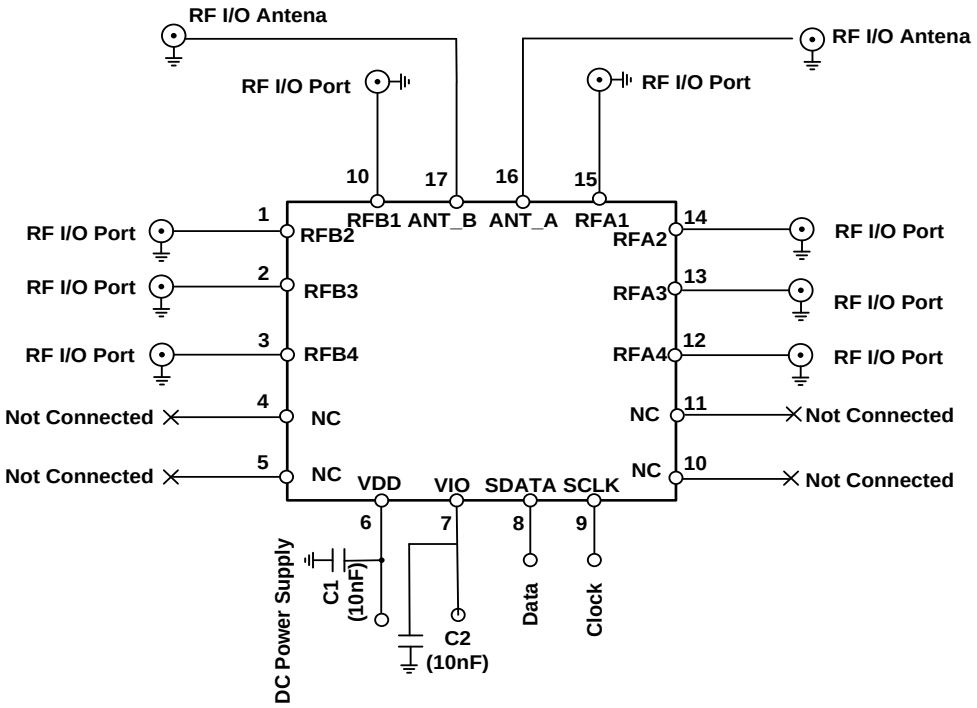
| Device | Package | Shipping |
|---|---|---|
| WS7808QD-18/TR | QFN 2.0x2.4-18Q | 3000/Reel &Tape |

## Pin information

| Pin | Function | Description | Transparent top view |
|---|---|---|---|
| 1 | RFB2 | ANT_B RF arm 2 |  |
| 2 | RFB3 | ANT_B RF arm 3 | |
| 3 | RFB4 | ANT_B RF arm 4 | |
| 4 | NC | Not Connected | |
| 5 | NC | Not Connected | |
| 6 | VDD | DC supply voltage | |
| 7 | VIO | MIPI interface DC voltage | |
| 8 | SDATA | Data | |
| 9 | SCLK | Clock | |
| 10 | NC | Not Connected | |
| 11 | NC | Not Connected | |
| 12 | RFA4 | ANT_A RF arm 4 | |
| 13 | RFA3 | ANT_A RF arm 3 | |
| 14 | RFA2 | ANT_A RF arm 2 | |
| 15 | RFA1 | ANT_A RF arm 1 | |
| 16 | ANT_A | Antenna A port | |
| 17 | ANT_B | Antenna B port | |
| 18 | RFB1 | ANT_B RF arm 1 | |



## Application information




**WS7808QD Evaluation Board Schematic**

**Note 1**: filter capacitor is needed on VDD and VIO respectively.

## Recommended operating conditions

| Parameters | Conditions | Specifications | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| **ESD Rating** | | | | | |
| ESD All Pins | HBM, JESD22-A114 | | | 1500 | V |
| **Power Supply** | | | | | |
| Power Supply Voltage | Operating Voltage | 2.4 | 2.8 | 3.1 | V |
| Power Supply Current | VDD≤3.0V | 25 | 32 | 40 | μA |
| Interface supply voltage level | | 1.65 | 1.8 | 1.95 | V |
| **Control Voltage** | | | | | |
| SCLK port voltage | | 0.8 x VIO | | VIO | V |
| SDATA port voltage | | 0 | | 0.2 x VIO | V |
| **RF Impedance** | | | | | |
| RF Port Input and Output Impedance | | | 50 | | Ω |
| Turn-On Switching Time | 50% of final control voltage to 90% of final RF power, switching between RF ports | | 5 | | μs |

## Absolute maximum ratings

Maximum ratings are absolute ratings, exceeding only one of these values may cause irreversible damage to the integrated circuit.

| Items | Value | Unit |
|---|---|---|
| VDD Voltage | -0.3 to +3.1 | V |
| Control Voltage | -0.3 to +2.0 | V |
| **Maximum Input Power** | | |
| Momentary, infrequent occurrence, 50 ohms | +29 | dBm |
| Momentary, infrequent occurrence, 6:1 | +27 | dBm |
| Continuous Operation, 50 ohms | +28 | dBm |
| Continuous Operation, 6:1 | +26 | dBm |
| Operation Temperature | -40 to +85 | °C |
| Storage Temperature | -65 to +150 | °C |

## Characteristics (RF spec)

Nominal test condition unless otherwise stated. All unused ports are 50Ω terminated.

VDD=2.8V, Temp= +25°C, $P_{IN}$=0dBm.

| Parameters | Conditions | | Specifications | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Insertion Loss<br>(ANT_A to any RFA port，<br>ANT_B to any RFB port) | 0.1GHz to 1.0GHz<br>1.0GHz to 2.0GHz<br>2.0GHz to 2.7GHz | | | 0.50<br>0.65<br>0.90 | | dB |
| Isolation | ANT_A to ANT_B<br>CA mode | 0.1GHz to 1.0GHz<br>1.0GHz to 2.0GHz<br>2.0GHz to 2.7GHz | | 31<br>25<br>22 | | dB |
| | ANT_A to ANT_B<br>non-CA mode | 0.1GHz to 1.0GHz<br>1.0GHz to 2.0GHz<br>2.0GHz to 2.7GHz | | 37<br>28<br>23 | | dB |
| | RFAn to RFBm<br>CA mode | 0.1GHz to 1.0GHz<br>1.0GHz to 2.0GHz<br>2.0GHz to 2.7GHz | | 38<br>33<br>32 | | dB |
| | RFAn to RFBm<br>non-CA mode | 0.1GHz to 1.0GHz<br>1.0GHz to 2.0GHz<br>2.0GHz to 2.7GHz | | 43<br>34<br>29 | | dB |
| | RFAn to RFAm,<br>RFBn to RFBm,<br>RFAn to ANT_A,<br>RFBn to ANT_B<br>non-CA mode | 0.1GHz to 1.0GHz<br>1.0GHz to 2.0GHz<br>2.0GHz to 2.7GHz | | 30<br>21<br>17 | | dB |
| Second Harmonics<br>(ANT to RF) | 0.7GHz to 1.0GHz, $P_{IN}$=+26dBm<br>1.0GHz to 2.0GHz, $P_{IN}$=+26dBm<br>2.0GHz to 2.7GHz, $P_{IN}$=+26dBm | | | 83<br>82<br>81 | | dBc |
| Third Harmonics<br>(ANT to RFX) | 0.7GHz to 1.0GHz, $P_{IN}$=+26dBm<br>1.0GHz to 2.0GHz, $P_{IN}$=+26dBm<br>2.0GHz to 2.7GHz, $P_{IN}$=+26dBm | | | 76<br>75<br>74 | | dBc |
| 0.1dB Compression Point<br>(ANT to RFX) | 0.7GHz to 1.0GHz<br>1.0GHz to 2.0GHz<br>2.0GHz to 2.7GHz | | | 28 | | dBm |
| 3rd Order Input Intercept Point<br>(ANT to RFX) | 0.7GHz to 2.7GHz<br>$P_{IN}$=+26dBm<br>$\Delta f$ =1MHz | | | 60 | | dBm |

**Note 2**：CA means Carrier Aggregation

## IMD2 Test Conditions

Nominal test condition unless otherwise stated. All unused ports are 50Ω terminated.

VDD=2.8V, Temp=+25°C, PIN=0dBm.

| Band | Transmit Frequency (MHz) | Transmit Power (dBm) | Frequency Blocker, Low (MHz) | Frequency Blocker, High (MHz) | Power Blocker (dBm) | Receive Frequency (MHz) |
|---|---|---|---|---|---|---|
| 1 | 1950.0 | +20 | 190 | 4090 | -15 | 2140.0 |
| 2 | 1880.0 | | 80 | 3840 | | 1960.0 |
| 4 | 1732.0 | | 400 | 3864 | | 2132.0 |
| 5 | 836.5 | | 45 | 1718 | | 881.5 |
| 7 | 2535.0 | | 120 | 5187 | | 2655.0 |
| 8 | 897.0 | | 45 | 1839 | | 942.0 |

## IMD3 Test Conditions

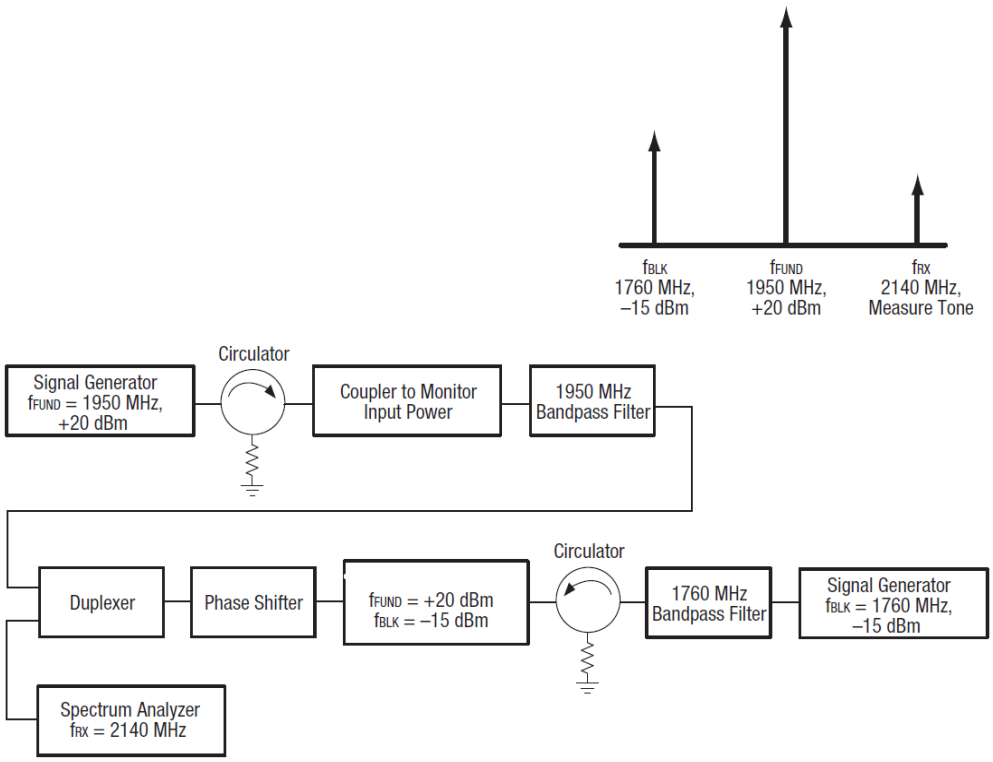
Nominal test condition unless otherwise stated. All unused ports are 50Ω terminated.

VDD=2.8V, Temp=+25°C, PIN=0dBm.

| Band | Transmit Frequency (MHz) | Transmit Power (dBm) | Frequency Blocker, (MHz) | Power Blocker (dBm) | Receive Frequency (MHz) |
|---|---|---|---|---|---|
| 1 | 1950.0 | +20 | 1760.0 | -15 | 2140.0 |
| 2 | 1880.0 | | 1800.0 | | 1960.0 |
| 4 | 1732.0 | | 1332.0 | | 2132.0 |
| 5 | 836.5 | | 791.5 | | 881.5 |
| 7 | 2535.0 | | 2415.0 | | 2655.0 |
| 8 | 897.0 | | 852.0 | | 942.0 |

## Triple Beat Ratio Test Conditions

| Band | Transmit Frequency 1 (MHz) | Transmit Power 1 (dBm) | Transmit Frequency 2 (MHz) | Transmit Power 2 (dBm) | Frequency Blocker @ ANT (MHz) | Power Blocker (dBm) | TBR Product Frequency (MHz) |
|---|---|---|---|---|---|---|---|
| 2 | 1880.0 | +21.5 | 1881.0 | +21.5 | 1960.0 | -30 | 1960.0±1 |
| 5 | 836.5 | | 881.5 | | 881.5 | | 881.5±1 |




**Typical Third Order Intermodulation Test Setup**

## Power ON and OFF sequence

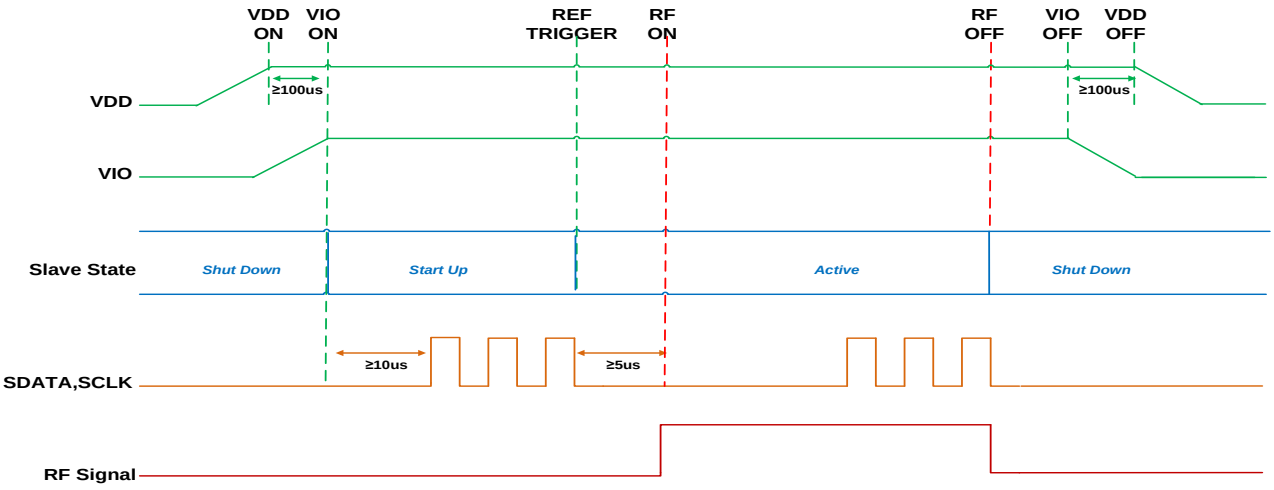
It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device (Note 3).

**Power ON**

1) Apply voltage supply - VDD
2) Wait 100μs or greater and then apply logic supply - VIO
3) Wait 10μs or greater and then apply RFFE
4) Wait 5μs or greater after RFFE Trigger falling edge and then apply the RF Signal

**Power OFF**

1) Remove the RF Signal
2) Remove RFFE
3) Remove logic supply – VIO
4) Remove voltage supply – VDD




**Note 3**: VIO can be applied to the device after VDD or removed before VDD .It is important to wait 10μs after VIO & VDD are applied before sending SDATA to ensure correction data transmission. The minimum time between a power up and power down sequence (and vice versa) is ≥ 100us.

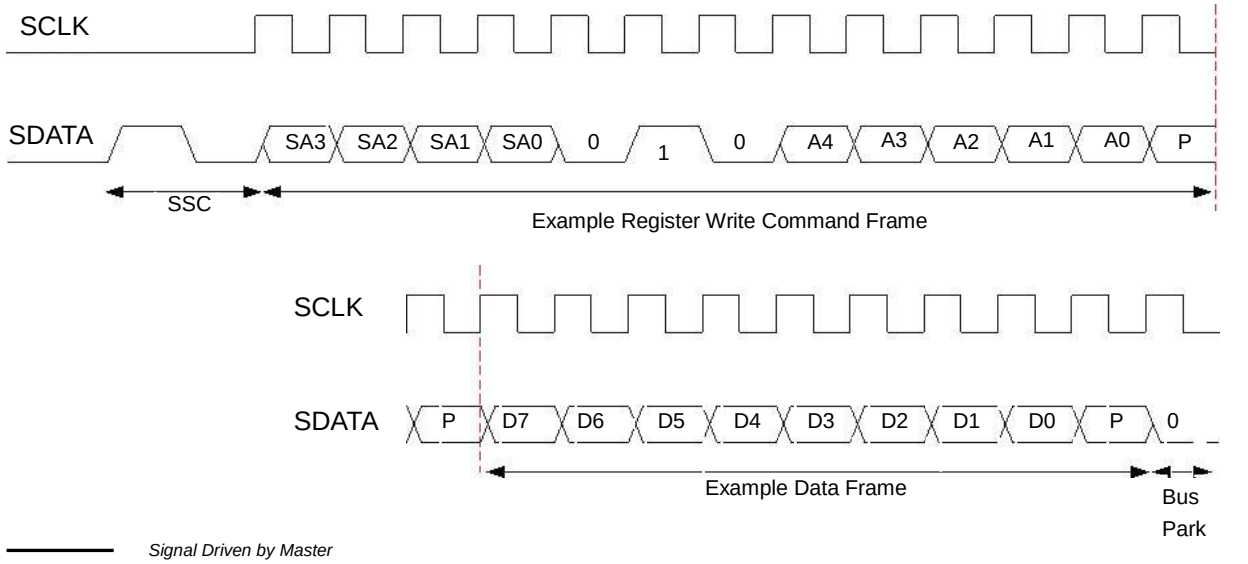
## Command Sequence Bit Definitions

| Type | SSC | C11-C8 | C7 | C6-C5 | C4 | C3-C0 | Parity Bits | BPC | Extended Operation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | DA7(1)-DA0(1) | Parity Bits | BPC | DA7(n)-DA0(n) | Parity Bits | BPC |
| Reg_0 Write, Short Command | Y | SA[3:0] | 1b | Data[6:5] | Data[4] | Data{3:0] | Y | Y | - | - | - | - | - | - |
| Reg_0 Write, Long Command | Y | SA[3:0] | 0 | 10b | Addr[4] | Data{3:0] | Y | - | Data[7:0] | - | - | - | Y | Y |
| Reg_1 Write | Y | SA[3:0] | 0 | 10b | Addr[4] | Data{3:0] | Y | Y | Data[7:0] | - | - | - | Y | Y |
| Reg Read | Y | SA[3:0] | 0 | 11b | Addr[4] | Data{3:0] | Y | Y | Data[7:0] | - | - | - | Y | Y |

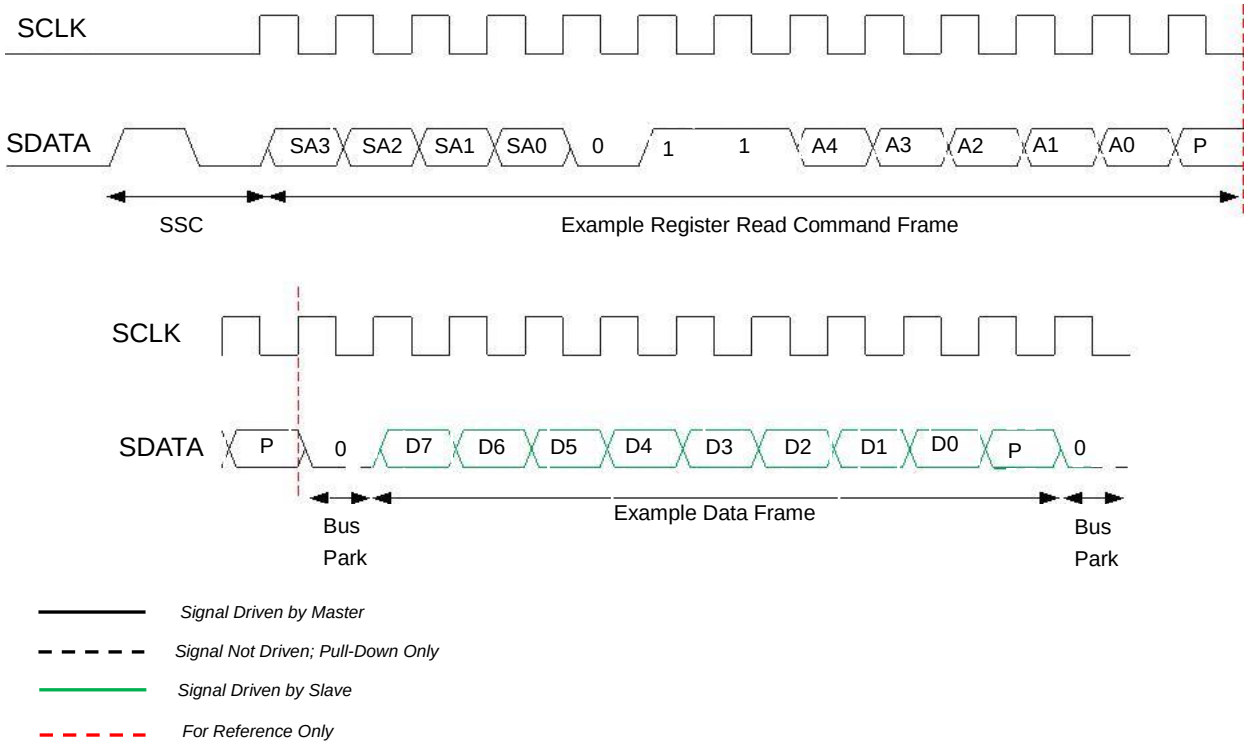
**Legend:**

SSC = Sequence start command DA = Data/address frame bits BC = Byte count (# of consecutive addresses)

C = Command frame bits BPC = Bus park cycle




**Register Write Command Timing Diagram**




**Register Read Command Timing Diagram**

## Register Description and Programming

| Register | | Parameter | Description | Default Name (Binary) |
|---|---|---|---|---|
| Name | Address (Hex) | | | |
| Register_0 | 0000 | MODE_CTRL | Bits[4:0]:<br>See Table B for logic | 00000 |
| Register_1 | 0001 | MODE_CTRL | Bits[4:0]:<br>See Table A for logic | 00000 |
| RFFE_STATUS | 001A | SOFTWARE RESET | Bits[7]:<br>Resets all data to default values except for USID, GSID, or the contents of the PM_TRIG Register.<br>0 = Normal operation (active)<br>1 = Software reset | 0 |
| | | COMMAND_FRAME_PARITY_ERR | Bit[6]:<br>Command sequence received with parity error – discard command. | 0 |
| | | COMMAND_LENGTH_ERR | Bit[5]:<br>Command length error. | 0 |
| | | ADDRESS_FRAME_PARITY_ERR | Bit[4]:<br>Address frame parity error =1. | 0 |
| | | DATA_FRAME_PARITY_ERR | Bit[3]:<br>Data frame with parity error. | 0 |
| | | READ_UNUSED_REG | Bit[2]:<br>Read command to an invalid address. | 0 |
| | | WRITE_UNUSED_REG | Bit[1]:<br>Write command to an invalid address. | 0 |
| | | BID_GID_ERR | Bit[0]:<br>Read command with a BROADCAST_ID (refer to the MIPI Alliance Specification) or GSID. | 0 |
| PM_TRIG (Note 4) | 001C | PWR_MODE | Bits[7:6]:<br>00 = Normal operation (active)<br>01 = Default settings (startup)<br>10 = Low power (low power)<br>11 = Reserved | 00 |
| | | Trigger_Mask_2 | Bit[5]:<br>If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register. | 0 |
| | | Trigger_Mask_1 | Bit[4]:<br>If this bit is set, trigger 1 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register. | 0 |
| | | Trigger_Mask_0 | Bit[3]:<br>If this bit is set, trigger 0 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register. | 0 |
| | | Trigger_2 | Bit[2]:<br>If this bit is set, data is loaded into the trigger 2 | 0 |

| | | | | |
|---|---|---|---|---|
| | | | registers. | |
| | | Trigger_1 | Bit[1]:<br>If this bit is set, data is loaded into the trigger 1 registers. | 0 |
| | | Trigger_0 | Bit[0]:<br>If this bit is set, data is loaded into the trigger 0 registers. | 0 |
| PRODUCT_ID | 001D | PRODUCT_ID | Bits[7:0]:<br>This is a read-only register. However, during the programming of the Unique Slave Identifier (USID), a write command sequence is performed on this register but the value is not changed. | 00011100 |
| MANUFACTURER_ID | 001E | MANUFACTURER_ID | Bits[7:0]:<br>Read-only register | 10111100 |
| MAN_USID | 001F | Reserved | Bits[7:6]:<br>Reserved | 00 |
| | | MANUFACTURER_ID | Bits[5:4]:<br>Read-only register | 11 |
| | | USID | Bits[3:0]:<br>Programmable USID. A write to these bits programs the USID. | 1010 |

**Note 4**: Unlike the complete independence between triggers 0, 1, and 2, and also between the associated trigger masks 0, 1, and 2, respectively, as described in the MIPI RFFE Specification, this device uses additional interactions between the provided trigger functions. The delayed application of updated data to all triggerable registers in this device may be accomplished using any of the three triggers (0, 1, or 2), provided that the particular trigger used is not currently masked off. If multiple triggers are enabled, any or all of those are sufficient to cause the data to be transferred from shadow registers to destination registers for all triggerable registers in the device. It is also necessary to disable all three triggers (i.e., set all three trigger masks) to ensure that data written to any triggerable register will immediately be written to the destination register at the conclusion of the RFFE command sequence where the data is written.

## Register_0 Truth Table B (ANT_B)

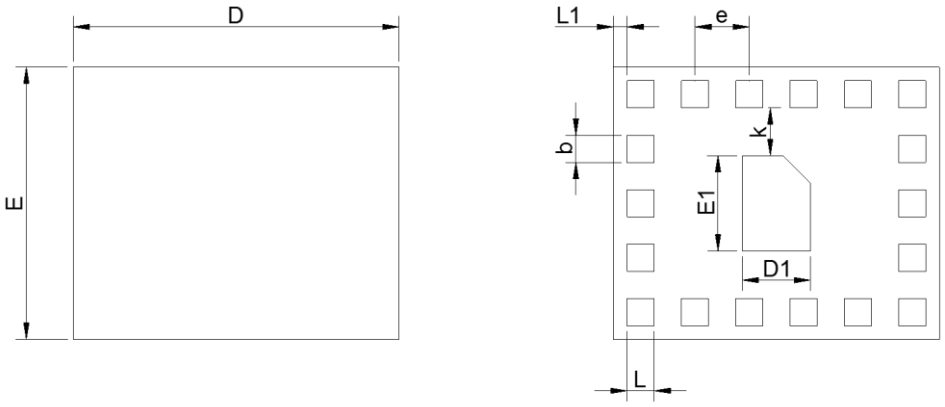
| Mode | Register_0 Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| All isolation | | | | 0 | 0 | 0 | 0 | 0 |
| TRx1 | | | | 0 | 0 | 0 | 0 | 1 |
| TRx2 | | | | 0 | 0 | 0 | 1 | 0 |
| TRx3 | | | | 0 | 0 | 0 | 1 | 1 |
| TRx4 | | | | 0 | 0 | 1 | 0 | 0 |
| TRx4+3 | | | | 1 | 0 | 0 | 0 | 0 |
| TRx4+2 | | | | 1 | 0 | 0 | 0 | 1 |
| TRx4+1 | | | | 1 | 0 | 0 | 1 | 0 |
| TRx3+2 | | | | 1 | 0 | 0 | 1 | 1 |
| TRx3+1 | | | | 1 | 0 | 1 | 0 | 0 |
| TRx2+1 | | | | 1 | 0 | 1 | 0 | 1 |
| All isolation | | | | 1 | 0 | 1 | 1 | 0 |
| All isolation | | | | 1 | 0 | 1 | 1 | 1 |
| All isolation | | | | 1 | 1 | 0 | 0 | 0 |
| All isolation | | | | 1 | 1 | 0 | 0 | 1 |
| All isolation | | | | 1 | 1 | 0 | 1 | 0 |
| All isolation | | | | 1 | 1 | 0 | 1 | 1 |
| All isolation | | | | 1 | 1 | 1 | 0 | 0 |
| All isolation | | | | 1 | 1 | 1 | 0 | 1 |
| All isolation | | | | 1 | 1 | 1 | 1 | 0 |
| All isolation | | | | 1 | 1 | 1 | 1 | 1 |

## Register_1 Truth Table A (ANT_A)

| Mode | Register_1 Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| All isolation | | | | 0 | 0 | 0 | 0 | 0 |
| TRx1 | | | | 0 | 0 | 0 | 0 | 1 |
| TRx2 | | | | 0 | 0 | 0 | 1 | 0 |
| TRx3 | | | | 0 | 0 | 0 | 1 | 1 |
| TRx4 | | | | 0 | 0 | 1 | 0 | 0 |
| TRx4+3 | | | | 1 | 0 | 0 | 0 | 0 |
| TRx4+2 | | | | 1 | 0 | 0 | 0 | 1 |
| TRx4+1 | | | | 1 | 0 | 0 | 1 | 0 |
| TRx3+2 | | | | 1 | 0 | 0 | 1 | 1 |
| TRx3+1 | | | | 1 | 0 | 1 | 0 | 0 |
| TRx2+1 | | | | 1 | 0 | 1 | 0 | 1 |
| All isolation | | | | 1 | 0 | 1 | 1 | 0 |
| All isolation | | | | 1 | 0 | 1 | 1 | 1 |
| All isolation | | | | 1 | 1 | 0 | 0 | 0 |
| All isolation | | | | 1 | 1 | 0 | 0 | 1 |
| All isolation | | | | 1 | 1 | 0 | 1 | 0 |
| All isolation | | | | 1 | 1 | 0 | 1 | 1 |
| All isolation | | | | 1 | 1 | 1 | 0 | 0 |
| All isolation | | | | 1 | 1 | 1 | 0 | 1 |
| All isolation | | | | 1 | 1 | 1 | 1 | 0 |
| All isolation | | | | 1 | 1 | 1 | 1 | 1 |

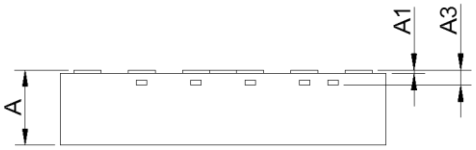
## Package Dimensions

### QFN2420-18L




TOP VIEW

BOTTOM VIEW

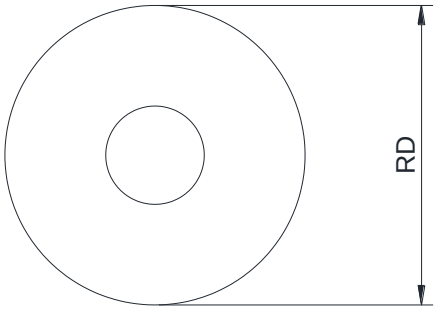



SIDE VIEW

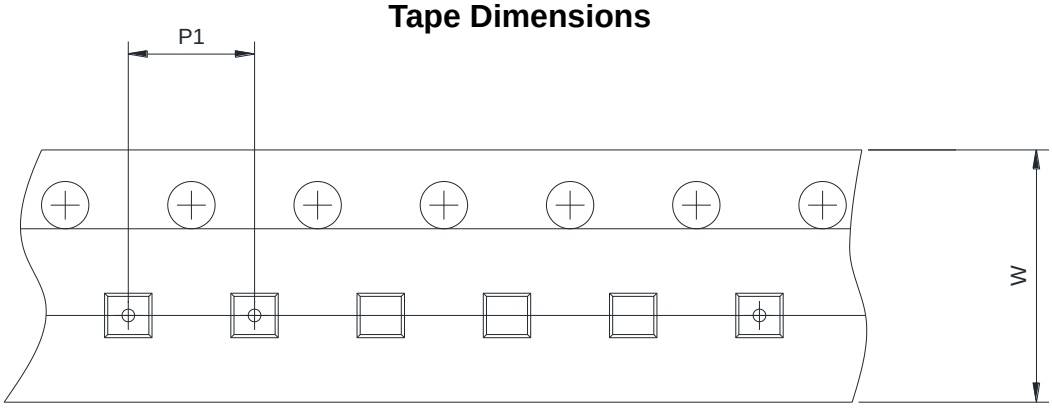
| Symbol | Dimensions in Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.50 | 0.55 | 0.60 |
| A1 | 0.00 | - | 0.046 |
| A3 | 0.11 Ref. | | |
| D | 2.30 | 2.40 | 2.50 |
| E | 1.90 | 2.00 | 2.10 |
| D1 | 0.40 | 0.50 | 0.60 |
| E1 | 0.60 | 0.70 | 0.80 |
| k | 0.35 Ref.. | | |
| b | 0.15 | 0.20 | 0.25 |
| e | 0.40 BSC | | |
| L | 0.15 | 0.20 | 0.25 |
| L1 | 0.10 Ref. | | |

## Tape and Reel Dimensions

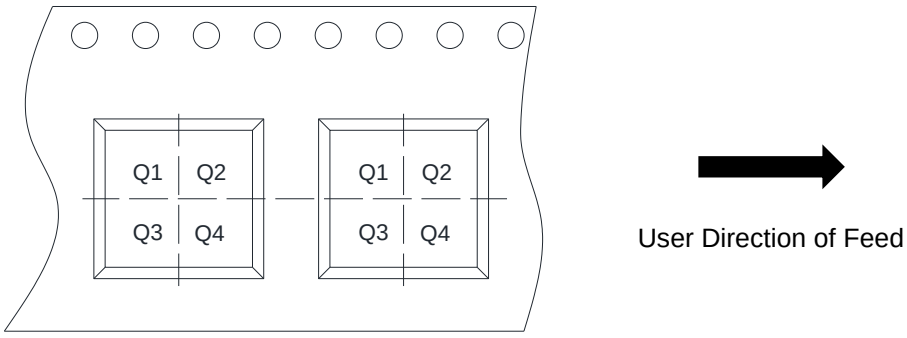
### Reel Dimensions




### Tape Dimensions




### Quadrant Assignments For PIN1 Orientation In Tape




| | | |
|---|---|---|
| RD | Reel Dimension | ☑ 7inch ☐ 13inch |
| W | Overall width of the carrier tape | ☑ 8mm ☐ 12mm ☐ 16mm |
| P1 | Pitch between successive cavity centers | ☐ 2mm ☑ 4mm ☐ 8mm |
| Pin1 | Pin1 Quadrant | ☑ Q1 ☐ Q2 ☐ Q3 ☐ Q4 |