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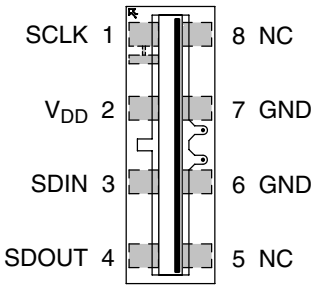
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TSL3301CL
102 × 1 LINEAR OPTICAL SENSOR ARRAY WITH ANALOG-TO-DIGITAL CONVERTER

TAOS141 – JULY 2011

- **102 × 1 Sensor Element Organization**
- **300 Dots-per-Inch Pixel Pitch**
- **High Sensitivity**
- **On-Chip 8-Bit Analog-to-Digital Conversion**
- **Three-Zone Programmable Offset (Dark Level) and Gain**
- **High Speed Serial Interface**
- **1 MHz Pixel Rate**
- **Single 3-V to 5.5-V Supply**
- **Replacement for TSL3301**
- **RoHS Compliant**

CL PACKAGE
(TOP VIEW)



NC – No internal connection

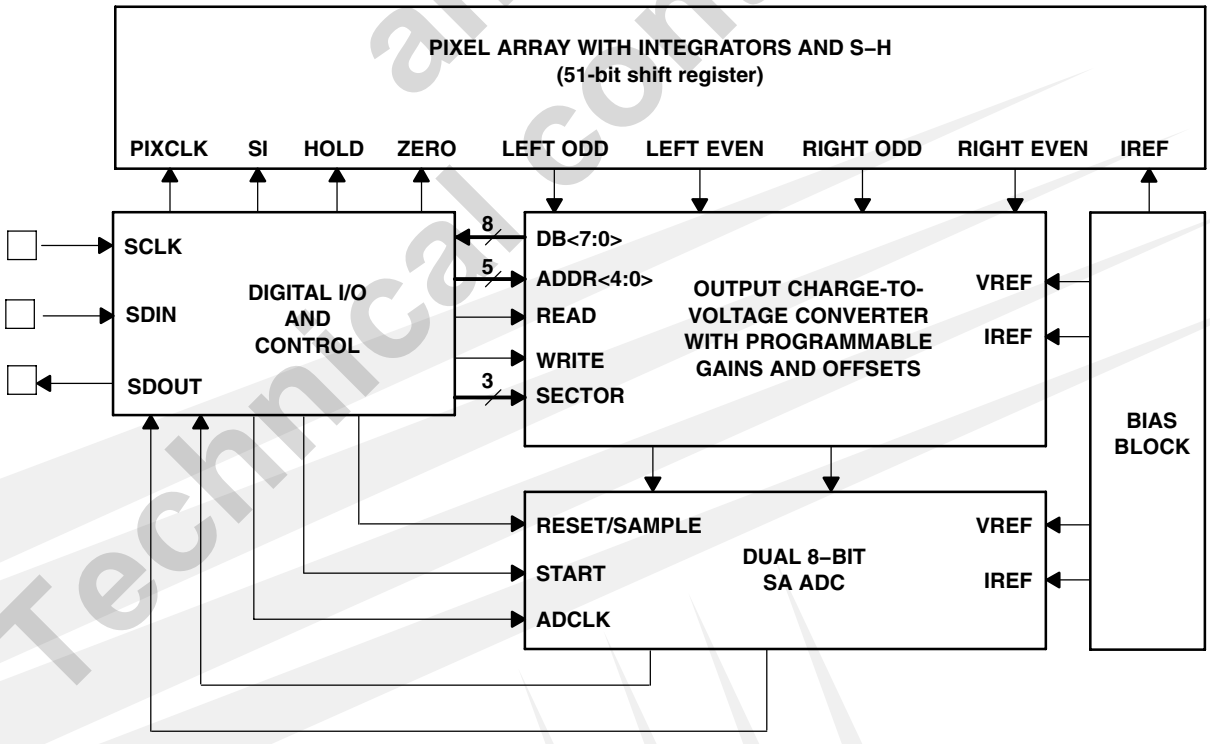
Package Drawing is Not to Scale

Description

The TSL3301CL is a high-sensitivity 300-dpi, linear optical sensor array with integrated 8-bit analog-to-digital converters. The array consists of 102 pixels: 100 inner pixels and 2 end pixels. The inner pixels measure 85 μm (H) by 77 μm (W) on 85-μm centers and the end pixels are 132 μm (H) by 49 μm (W). Associated with each pixel is a charge integrator/amplifier and sample-hold circuit. All pixels have concurrent integration periods and sampling times. The array is split into three 34-pixel zones, with each zone having programmable gain and offset levels. Data communication is accomplished through a three-wire serial interface.

Intended for use in high performance, cost-sensitive scanner applications, the TSL3301CL is based on a linear sensor array die that has expanded capability, including multi-die addressing and cascade options. Please contact TAOS for additional information on die and multi-die package availability.

Functional Block Diagram



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	6, 7		Ground
SCLK	1	I	System clock input for serial I/O and all internal logic.
SDIN	3	I	Serial data input. Data is clocked in on the rising edge of SCLK.
SDOUT	4	O	Serial data output. Data is clocked out on the falling edge of SCLK.
V_{DD}	2		Positive supply voltage.

Detailed Description

The TSL3301CL is a 102 × 1 linear optical array with onboard A/D conversion. It communicates over a serial digital interface and operates over a 3 V to 5.5 V range. The array is divided into three 34-pixel zones (left, center, and right), with each zone having programmable gain and offset (dark signal) correction.

The sensor consists of 102 photodiodes, also called pixels, arranged in a linear array. Light energy impinging on a pixel generates a photocurrent, which is then integrated by the active integration circuitry associated with that pixel. During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity (E_e) on that pixel and to the integration time (t_{int}). At maximum programmed gain, one LSB corresponds to approximately 300 electrons.

Integration, sampling, output, and reset of the integrators are performed by the control logic in response to commands input via the SDIN pin. Data is read out on the SDOUT pin. A normal sequence of operation consists of a pixel reset (*RESET*), start of integration (*STARTInt*), integration period, sampling of integrators (*SAMPLEInt*), and pixel output (*READPixel*). Reset sets all the integrators to zero. Start of integration releases the integrators from the reset state and defines the beginning of the integration period. Sampling the integrators ends the integration period and stores the charge accumulated in each pixel in a sample and hold circuit. Reading the pixels causes the sampled value of each pixel to be converted to 8-bit digital format and output on the SDOUT pin. All 102 pixels are output sequentially unless interrupted by an abort (*ABORTPixel*) command or reset by a *RESET* command.

Gain adjustment is controlled by three 5-bit DACs, one for each of the the three zones. Table 1 lists the gain settings and the corresponding pixel values. Offset is affected by the gain setting and may have to be adjusted after gain changes are made.

Offset correction is controlled by three 8-bit sign-magnitude† DACs and is performed in the analog domain prior to the digital conversion. There is a separate offset DAC for each of the three zones. Codes 0h – 7Fh correspond to positive offset values and codes 80h – FFh correspond to negative offset values.

The offset correction is proportional to the gain setting. At minimal gain, one LSB of the offset DAC corresponds to approximately 1/3 LSB of the device output, and at maximum gain, to about 1 LSB of the device output.

Note that the gain and offset registers are in indeterminate states after power up and must be set by the controller as required.

† Sign-magnitude is a binary representation in which the most significant bit (MSB) is used to represent the sign of the number, with the remaining bits representing the magnitude. An MSB of 1 indicates a negative number.

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Table 1. Gain Settings and Results

GAIN CODE	RELATIVE GAIN	% INCREASE	GAIN CODE	RELATIVE GAIN	% INCREASE
0	1		16	1.52	3.23
1	1.02	2.17	17	1.57	3.33
2	1.05	2.22	18	1.62	3.45
3	1.07	2.27	19	1.68	3.57
4	1.09	2.33	20	1.74	3.70
5	1.12	2.38	21	1.81	3.85
6	1.15	2.44	22	1.88	4.00
7	1.18	2.50	23	1.96	4.17
8	1.21	2.56	24	2.05	4.35
9	1.24	2.63	25	2.14	4.55
10	1.27	2.70	26	2.24	4.76
11	1.31	2.78	27	2.35	5.00
12	1.34	2.86	28	2.48	5.26
13	1.38	2.94	29	2.61	5.56
14	1.43	3.03	30	2.77	5.88
15	1.47	3.13	31	2.94	6.25

Serial Interface

The serial interface follows a USART format, with start bit, 8 data bits, and one or more stop bits. Data is clocked in synchronously on the rising edge of SCLK and clocked out on the falling edge of SCLK. Stop bits are not required on the input. When clocking data out continuously (i.e., reading out pixels) there will be one stop bit between data words.

The receive and transmit state machines are independent, which means commands can be issued while reading data. This feature allows starting new integration cycles while reading data. Note that this allows undefined conditions so care must be taken not to issue commands that will cause outputs (such as register read) while reading out data. For instance, issuing a register read command while reading out image data will result in garbage out. Likewise, it is possible to change offset and gain registers during a readout, which can give unpredictable results.

It is not necessary to have a continuously active clock, but a minimum of 5 clocks after the stop bit is required after any command has been issued to ensure that the corresponding internal logic actions have been completed. When reading register contents, there will be a 4-clock delay from the completion of the *REGRead* command before the register contents are output (see Figure 5). When reading out pixel values, there will be a 44-clock delay from completion of the *READPixel* command until the first pixel data is output. When starting integration (*STARTInt*), it is necessary to have 22 clocks to complete the pixel reset cycle (see *Imaging* below).

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Register Address Map

The TSL3301CL contains seven registers as defined in Table 2. Data in these registers may be written to or read from using the *REGWrite* and *REGRead* commands. Three registers control the gain of the analog-to-digital converters (ADC). Three other registers allow the offset of the system to be adjusted. Together the gain and offset registers are used to maximize the achievable dynamic range.

Table 2. Register Address Map

ADDRESS	REGISTER DESCRIPTION	REGISTER WIDTH
0x00	Left (pixels 0–33) offset	8
0x01	Left (pixels 0–33) gain	5
0x02	Center (pixels 34–67) offset	8
0x03	Center (pixels 34–67) gain	5
0x04	Right (pixels 68–101) offset	8
0x05	Right (pixels 68–101) gain	5
0x1F	Mode	8

The offset registers are 8-bit sign-magnitude values and the gain registers are 5-bit values. The programmed offset correction is applied to the sampled energy, and then the gain is applied. (i.e., the gain will affect the offset correction.) These registers allow the user to maximize the dynamic range achievable in the given system.

The last register is the mode register. Bits in this register select the sleep mode as well as options for multichip arrays and production testing. Note that test and multichip options do not apply to the 8-pin packaged device. Users should always write 0s into the production test and multichip control bits.

	7	6	5	4	3	2	1	0	
0x1F	P2	0	0	SLP	P1	P0	C1	C0	MODE

SLP = Sleep Mode:
1 places device into sleep mode
0 places device in normal operating mode

C1, C0 are Reserved (should be written *0*)

P2 to P0 are factory test bits (should be written *0*)

Figure 1. Mode Register Bit Assignments

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Command Description

The TSL3301CL is a *slave* device that reacts strictly to commands received from the digital controller. These commands cause the device to perform functions such as reset, integrate, sample, etc. Table 3 summarizes the command types and formats and Table 4 lists the command set for the TSL3301CL. Each command is described in more detail below.

Table 3. Command Type and Format Summary

COMMAND TYPE	FORMAT
Action command	< Command byte >
Register write	< Command byte > < Data byte >

Table 4. TSL3301CL Command Set

COMMAND	HEX CODE	DESCRIPTION
IRESET	SDIN held low for 30 clocks	Interface Reset
RESET	0x1B	Reset Integration and read blocks
STARTInt	0x08	Start pixel integration
SAMPLEInt	0x10	Stop light integration and sample results
READPixel	0x02	Dump serial the contents of each sampled integrator
ABORTPixel	0x19	Abort any READPixel operation in progress
READHold	0x12	Combination of SAMPLEInt and READPixel commands
READHoldNStart	0x16	Combination of SAMPLEInt, READPixel and STARTInt commands
REGWrite	0x40 + address	Write a gain, offset, or mode register
REGRead	0x60 + address	Read a gain, offset, or mode register

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A minimum of 5 clock cycles after the stop bit is required after any command to ensure that the internal logic actions have been completed.

Reset Commands

Reset commands are used to put the TSL3301CL into a known state.

IRESET — Interface Initialization

Encoding: Break Character (10 or more consecutive start bits, or zeros)

The commands vary in length from one to three bytes. *IRESET* initializes the internal state machine that keeps track of which command bytes have been received. This command should be first and given only once after power-up to synchronize the TSL3301CL internal command interpreter.

An alternative is to issue three successive *RESET* commands.

RESET — Main Reset

Encoding: 0x1b: <0001_1011>

RESET resets most of the internal control logic of the TSL3301CL and any *READPixel* command currently in progress is aborted. *RESET* puts the pixel integrators into the auto-zero/reset state. Any values that were being held in the array's sample/hold circuits are lost.

NOTE:
The value on the SDOUT pin is not guaranteed from the time power is applied until 30 clocks after the first RESET command is issued.

Pixel Action Commands

Pixel action commands allow the user to control pixel integration and reading of pixel data.

STARTInt — Start Integration

Encoding: 0x08: <0000_1000>

STARTInt causes each pixel to leave the reset state and to start integrating light. The actual execution of *STARTInt* is delayed 22 clock cycles until the pixel reset cycle has been completed. (See *imaging* below.)

SAMPLEInt — Stop Integration

Encoding: 0x10: <0001_0000>

SAMPLEInt causes each pixel to store its integrator's contents into a sample and hold circuit. Also, the Integrator is returned to the reset state.

READPixel — Read Pixel Data

Encoding: 0x02: <0000_0010>

READPixel causes the sampled value of each pixel to be converted to an 8-bit digital value that is clocked out on the SDOUT pin. The LSB is the first data bit, which is preceded by a START bit (logic 0) and followed by a STOP bit (logic 1). Each pixel in the device is presented on SDOUT starting from pixel 00 and completes with pixel 101. There is a 44-clock cycle delay from the completion of the *READPixel* command until the first pixel data is output.

Gain and offset registers are used to adjust the ADC converter to maximize dynamic range and should be programmed prior to invoking the *READPixel* command.

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ABORTPixel — Abort Pixel Data Read

Encoding: 0x19: <0001_1001>

ABORTPixel is an optional command that stops a *READPixel* command during its execution. It also causes pixel integration to terminate and the device to enter the auto-zero/reset state. Any values that were being held in the array's sample/hold circuits are lost.

READHold — Sample and Read Combination

Encoding: 0x12: <0001_0010>

READHold is a macro command that combines both the *SAMPLEInt* and *READPixel* commands into a single command.

READHoldNStart Combination

Encoding: 0x16: <0001_0110>

READHold is a macro command that combines the *SAMPLEInt*, *READPixel,* and *StartInt* commands into a single command. 22 clock cycles are necessary to complete the pixel reset cycle.

Register Commands

The register commands provide the user the capability of setting gain and offset corrections for each of the three zones of pixels. a4–a0 refer to the register address as given in Table 2.

REGWrite — Write a Gain/Offset/Mode Register

Encoding (2 bytes): 0x40 <data>: <010a4_a3a2a1a0> <d7d6d5d4_d3d2d1d0>

REGWrite writes a value into either a gain, offset, or mode register. The 5-bit address of the register is encoded into the lower 5 bits of the command byte (the first byte). A second byte, which contains the data to be written, follows the command byte.

REGRead — Read a Gain/Offset/Mode Register

Encoding: 0x60: <011a4_a3a2a1a0>

REGRead reads the value previously stored in a gain, offset, or mode register. The 5-bit address of the register is encoded into the lower 5 bits of the command byte. Following receipt of the *REGRead* command, the device places the contents of the selected register onto the SDOUT pin, LSB first.

There is a 4-clock cycle delay from the completion of the *REGRead* command until the register contents are output.

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OPERATION

Initialization Sequence

After powering on the device, a minimum of 10 clocks with SDIN held high must be received by the TSL3301CL to clear the receiver logic so that a start bit will be detected correctly. The control logic may then be cleared by either issuing an *IRESET* command (break character) or 3 *RESET* (0x1b) commands. An additional 30 clocks must be received by the device to assure the state of SDOUT.

Sleep Mode

The device can be put into a power down or sleep mode by writing a 0x10 to the mode register. This turns off all the analog circuitry on the chip. Normal operation is restored by writing a 0x00 to the mode register. The analog circuitry will require a minimum of 1 millisecond to recover from the sleep mode.†

Note that putting the device in the sleep mode does not affect the logic states of the machine. If, for example, a *READPixel* command is issued, the device will respond but the resulting data will be meaningless. Also note that 0x00 and 0x10 are the only two legitimate user programmable values for the single-chip version of the TSL3301CL. Other values may put the device into a non-operational mode.

† For minimum sleep mode current consumption, voltage levels on logic inputs must be at either V_{DD} or ground.

Imaging

After powering up the device and completing the initialization sequence, it is necessary to allow a minimum of 1 millisecond for the internal analog circuitry to settle. This delay is also required when coming out of the sleep mode.

Issuing a *STARInt* (0x08) command will release the pixel integrators from the reset state. After an appropriate delay to integrate the image, the pixel data may be sampled by issuing a *SAMPLEInt* (0x10) command and then read out by issuing a *READPixel* (0x02) command.

A *STARTInt* command can be issued anytime after the *SAMPLEInt* command is issued to start another cycle. Thus, it is possible to be reading out one sample while integrating the next. However, the sampled data from the previous *SAMPLEInt* must be completely read out before the next *SAMPLEInt* command is issued.

The compound commands *READHold* (0x12) and *READHoldNStart* ((0x16) are shortcut commands to simplify the imaging sequence.

It is important to note that a pixel reset sequence is initiated with the receipt of a *STARTInt* or *READHoldNStart* command. The next integration sequence cannot start until the pixel reset sequence has been completed, which requires 22 clocks ***AFTER*** the receipt of one of these commands. These clocks can also be used to clock commands or data into or out of the device.

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Absolute Maximum Ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} . . . . . 6 V
Digital output voltage range, V_O . . . . . –0.3 V to V_{DD} +0.3 V
Digital output current . . . . . –10 to +10 mA
Digital input current range, I_I . . . . . –20 mA to 20 mA
Operating free-air temperature range, T_A . . . . . –25°C to 85°C
Storage temperature range . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds‡ . . . . . 260°C
ESD tolerance, human body model . . . . . 2000 V

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Not recommended for solder reflow.

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	5.5	V
High-level input voltage at SCLK, SDIN, V_{IH}	2		V_{DD}	V
Low-level input voltage at SCLK, SDIN, V_{IL}			0.8	V
Power supply ripple, 100 kHz sawtooth waveform			60	mVp-p
Input clock (SCLK) rise time, 10% to 90%			30	ns
Operating junction temperature, T_J	0		70	°C
Maximum clock frequency, f_{SCLK}			10	MHz

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, SDOUT	V_{DD} = 5 V	I_O = 50 µA	4.5	4.95		V
			I_O = 4 mA		4.6		
		V_{DD} = 3.3 V	I_O = 50 µA		2.9		
			I_O = 4 mA		2.7		
V_{OL}	Low-level output voltage, SDOUT	I_O = 50 µA			0.01	0.1	V
		I_O = 4 mA			0.4		
I_{DD}	Supply current	A/D active			11	17	mA
		A/D inactive			6	11	
		Sleep mode				10	µA
V_{IL}	Low-level input voltage (SCLK, SDIN)					0.8	V
V_{IH}	High-level input voltage (SCLK, SDIN)			2			V
I_{IH}	High-level input current (SCLK, SDIN)	V_I = V_{DD}				±10	µA
I_{IL}	Low-level input current (SCLK, SDIN)	V_I = 0				±10	µA

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Light-to-Digital Transfer Characteristics at V_{DD} = 5 V, T_J = 25°C, λ_p = 660 nm, t_{int} = 250 μs (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
A-to-D converter resolution				8		Bits
Full-scale reference	Gain register = 00000b			3.6		nJ/cm^2
	Gain register = 11111b			1.24		
Full-scale reference temperature sensitivity		For converter only, does not include photodiode characteristics		±150		ppm/°C
Average dark-level offset	Gain register = 00000b	Offset register = 00000000b	0	7	30	LSB
	Gain register = 11111b			20		
Dark signal nonuniformity (DSNU)		Gain register = 00000b, see Note 1		5	10	LSB
		Gain register = 11111b, see Note 1			14	
Average white level output	Offset register = 00000000b	Gain register = 00000b Ee = 11.3 μW/cm^2	160	200	240	LSB
		Gain register = 11111b Ee = 3.77 μW/cm^2		200		
Pixel-response non-uniformity (PRNU)		Ee = 11.3 μW/cm^2, See Notes 2 and 3		±8	±10	%
Programmable offset steps				±128		
Programmable offset step size	Gain register = 00000b			0.5		LSB
	Gain register = 11111b			1.5		
Dark-level change with temperature		0°C < T_J < 70°C		2		LSB
Differential nonlinearity				±0.5		LSB
Integral nonlinearity				±1		LSB
Dark level noise	Gain register = 00000b			0.5		LSB
	Gain register = 11111b			1.5		

NOTES: 1. DSNU is the difference between the highest value pixel and the lowest value pixel of the device under test when the array is not illuminated.
2. PRNU does not include DSNU.
3. PRNU is the difference between the highest value pixel and the lowest value pixel of the device under test when the array is uniformly illuminated at nominal white level (typical average output level = 200).

Timing Requirements over recommended operating range (unless otherwise noted) (Figure 2)

		MIN	NOM	MAX	UNIT
f_{max}	Maximum clock frequency	10			MHz
$t_{w(CLKH)}$	Clock high pulse duration	30			ns
$t_{w(CLKL)}$	Clock low pulse duration	30			ns
t_{su}	Input setup time	20			ns
t_h	Input hold time	20			ns

Switching Characteristics over recommended operating range (unless otherwise noted) (Figure 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time, output	C_L = 20 pF		10		ns
t_f	Fall time, output			10		ns
t_d	Delay from clock edge to data-out stable			20		ns
C_i	Input pin capacitance			10		pF

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TYPICAL CHARACTERISTICS

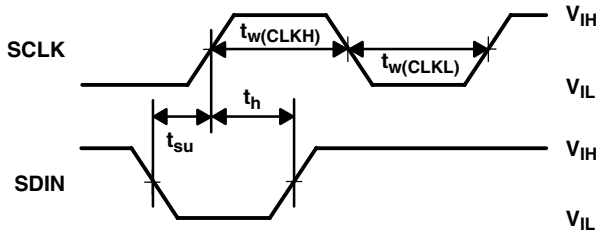


Figure 2. TSL3301CL Input Timing Requirements

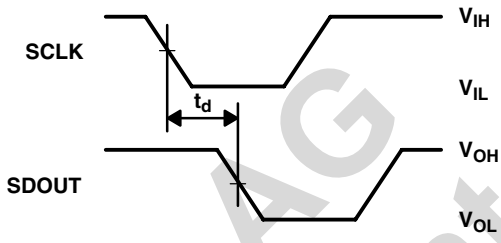


Figure 3. TSL3301CL Output Switching Characteristics

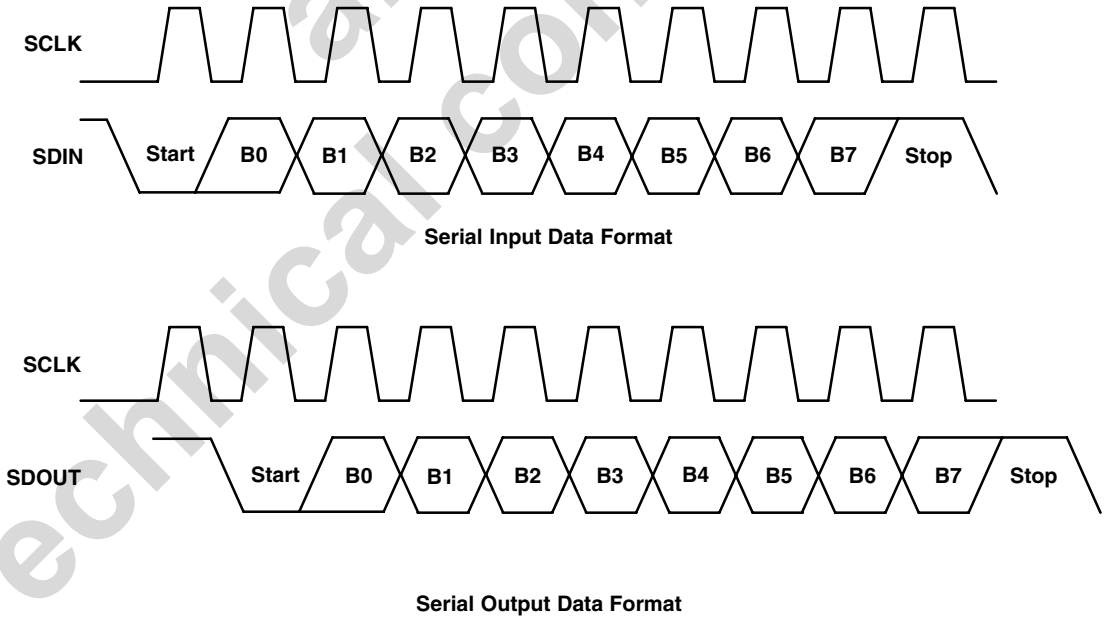


Figure 4. TSL3301CL Serial I/O

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TYPICAL CHARACTERISTICS

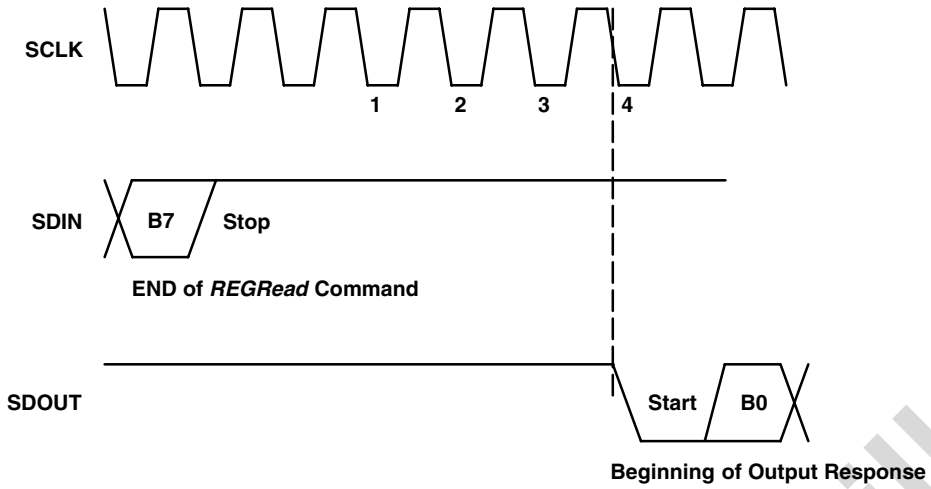


Figure 5. TSL3301CL *REGRead* Output Response Timing

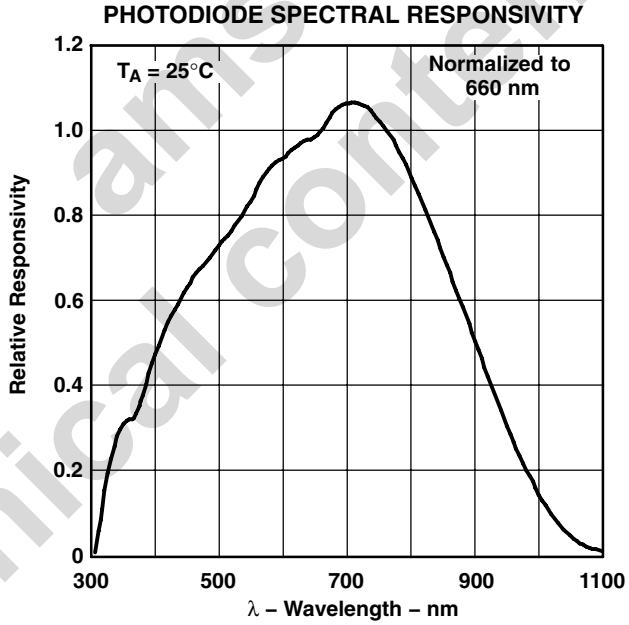


Figure 6. TSL3301CL Photodiode Spectral Response

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APPLICATION INFORMATION

Normal Sequence

A typical programming sequence for the TSL3301CL device appears below:

```
Send(IRESET);
Send(RESET);
Calibration Cycle
 *
 *
while(1) {
   for(i=0;i<=2;i++) {/* for each pixel page */
      Write page gain register
      Write page offset register
      Read page gain register and verify (optional)
      Read page offset register and verify (optional)
   }
}
Send(STARTInt);
DelayIntegrationTime();   /* wait for appropriate time interval to elapse */
Send(SAMPLEInt);
Send(READPixel);
```

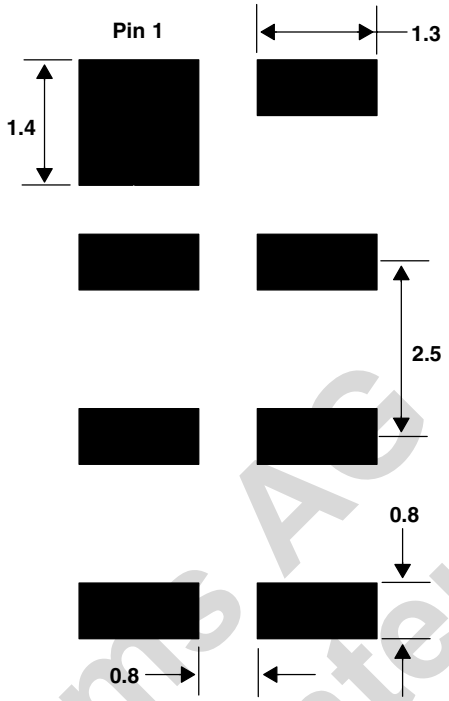
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APPLICATION INFORMATION: HARDWARE

PCB Pad Layout

Suggested PCB pad layout guidelines for the CL package are shown in Figure 7.



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

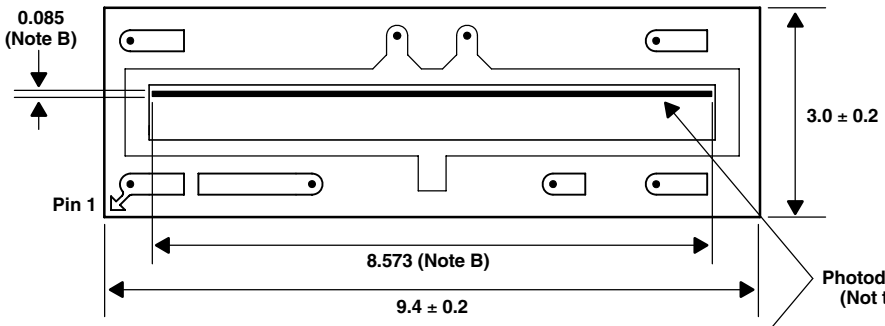
Figure 7. Suggested CL Package PCB Layout

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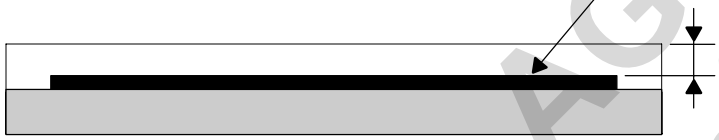
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PACKAGE INFORMATION

TOP VIEW



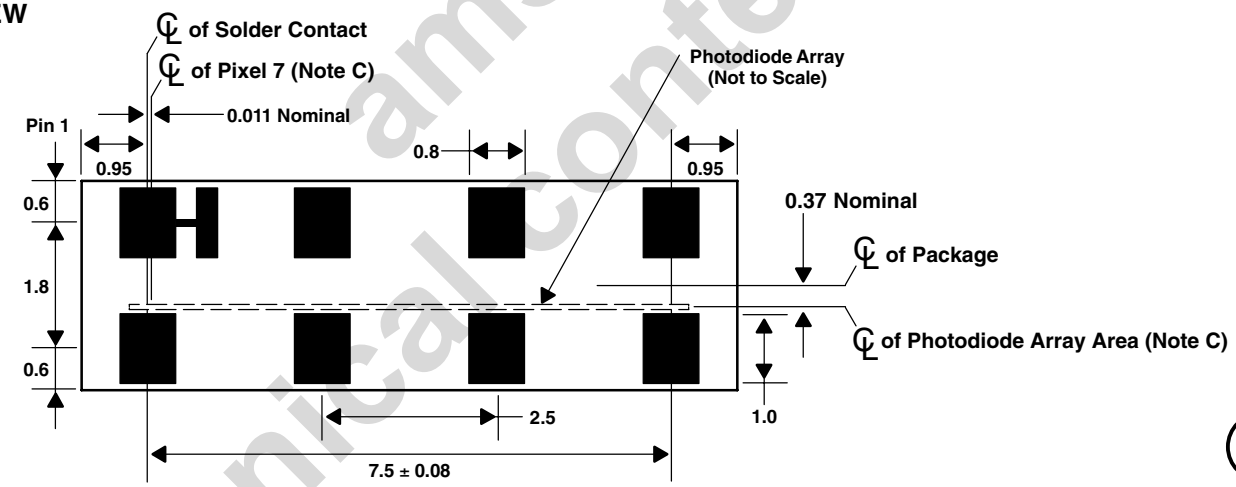
SIDE VIEW



END VIEW



BOTTOM VIEW



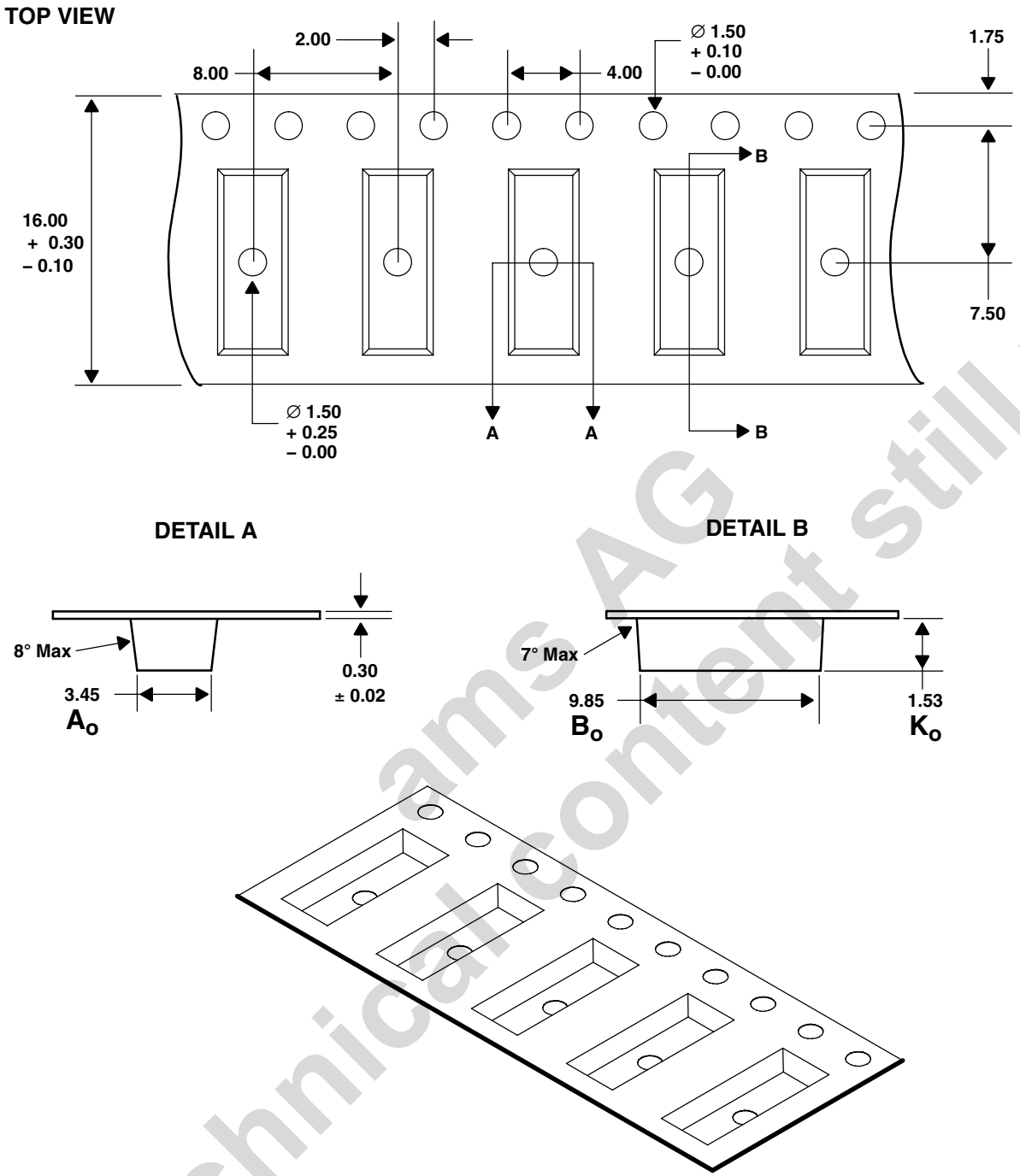
NOTES: A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.05 mm unless otherwise noted.
B. Nominal photodiode array dimension. The array is made up of 100 inner pixels and 2 end pixels with pixel #1 closer to Pin 1. The inner pixel is 77 μm wide by 85 μm high, spaced on 85μm centers. The end pixel is 49μm wide by 132 μm high.
C. The die is centered within the package within a tolerance of ± 0.05 mm.
D. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.56.
E. Contact finish is soft gold plated.
F. This package contains no lead (Pb).
G. This drawing is subject to change without notice.

Figure 8. Package CL Configuration

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CARRIER TAPE AND REEL INFORMATION



NOTES: A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
B. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
C. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481–B 2001.
D. Each reel is 178 millimeters in diameter and contains 1000 parts.
E. TAOS packaging tape and reel conform to the requirements of EIA Standard 481–B.
F. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
G. This drawing is subject to change without notice.

Figure 9. Package CL Carrier Tape

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SOLDERING INFORMATION

The CL package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Table 5. Solder Reflow Profile

PARAMETER	REFERENCE	DEVICE
Average temperature gradient in preheating		2.5°C/sec
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T1)	t_1	Max 60 sec
Time above 230°C (T2)	t_2	Max 50 sec
Time above T_{peak} –10°C (T3)	t_3	Max 10 sec
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max –5°C/sec

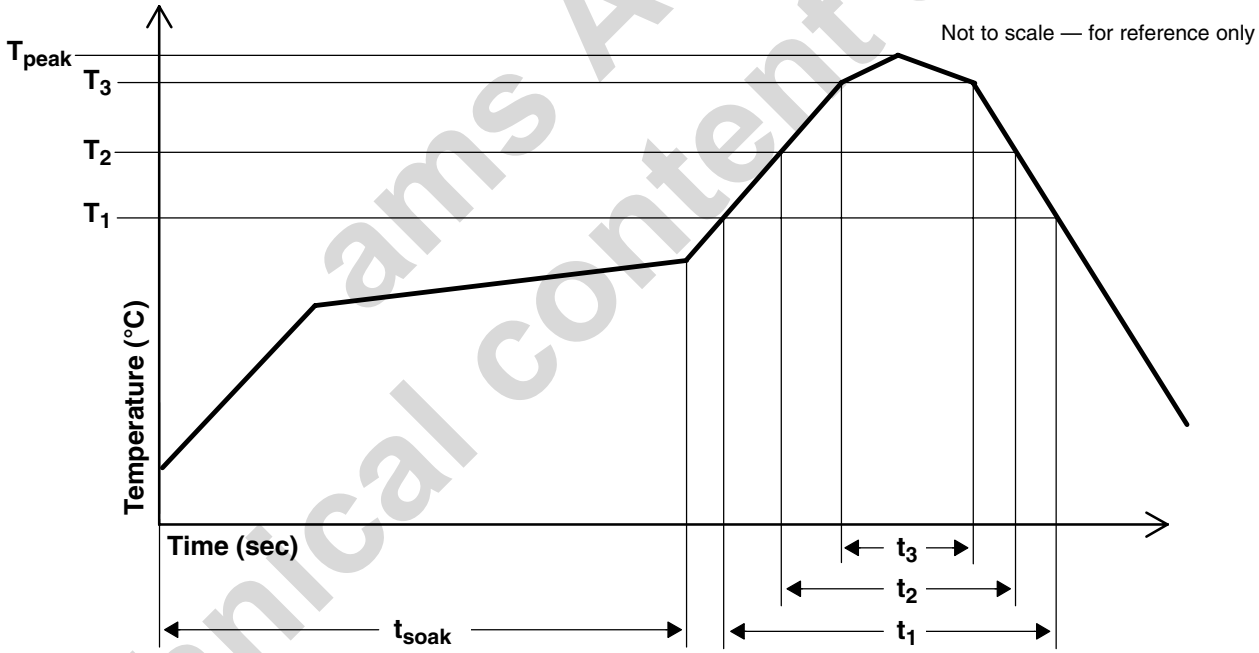


Figure 10. Solder Reflow Profile Graph

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STORAGE INFORMATION

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping. Devices are packed in a sealed aluminized envelope called a moisture barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

The CL package has been assigned a moisture sensitivity level of MSL 5a and the devices should be stored under the following conditions:

Temperature Range	5°C to 50°C
Relative Humidity	60% maximum
Total Time	6 months from the date code on the aluminized envelope — if unopened
Opened Time	24 hours or fewer

Rebaking will be required if the devices have been stored unopened for more than 6 months or if the aluminized envelope has been open for more than 24 hours. If rebaking is required, it should be done at 60°C for 24 hours.

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Green (RoHS & no Sb/Br) TAOS defines *Green* to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

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