Low-Noise, Fixed Output Voltage, 300mA LDO Regulator

General Description

The RT9167B is a 300mA low dropout and low noise micropower regulator suitable for portable applications. The output voltages range from 1.5V to 5V in 100mV increments and 2% accuracy. The RT9167B is designed for use with very low ESR capacitors. The output remains stable even with 1μF ceramic output capacitor.

The RT9167B uses an internal PMOS as the pass device, which does not cause extra GND current in heavy load and dropout conditions. The shutdown mode with nearly zero operation current makes the IC suitable for battery-powered devices. Other features include a reference bypass pin to improve low noise performance, current limiting, and over temperature protection.

Ordering Information

RT9167B-□□□□

- Package Type
  F : MSOP-8
- Lead Plating System
  P : Pb Free
- Output Voltage
  15 : 1.5V
  16 : 1.6V
  :
  49 : 4.9V
  50 : 5.0V
  2H : 2.85V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a RichTek distributor located in your area.

Features

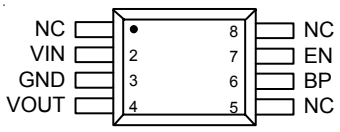
- **Stable with Low-ESR Output Capacitor**
- **Low Dropout Voltage (350mV @ 300mA)**
- **Low Operation Current –80μA Typical**
- **Shutdown Function**
- **Low Noise Output**
- **Low Temperature Coefficient**
- **Current and Thermal Limiting**
- **Custom Voltage Available**
- **MSOP-8 Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Cellular Telephones
- Laptop, Notebook, and Palmtop Computers
- Battery-powered Equipment
- Hand-held Equipment

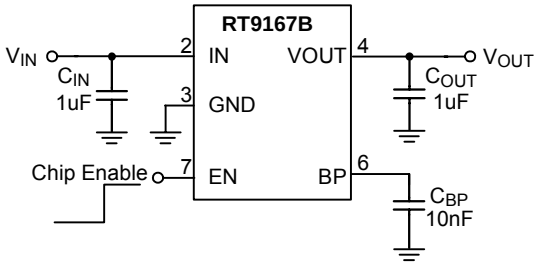
Pin Configurations

(TOP VIEW)



MSOP-8

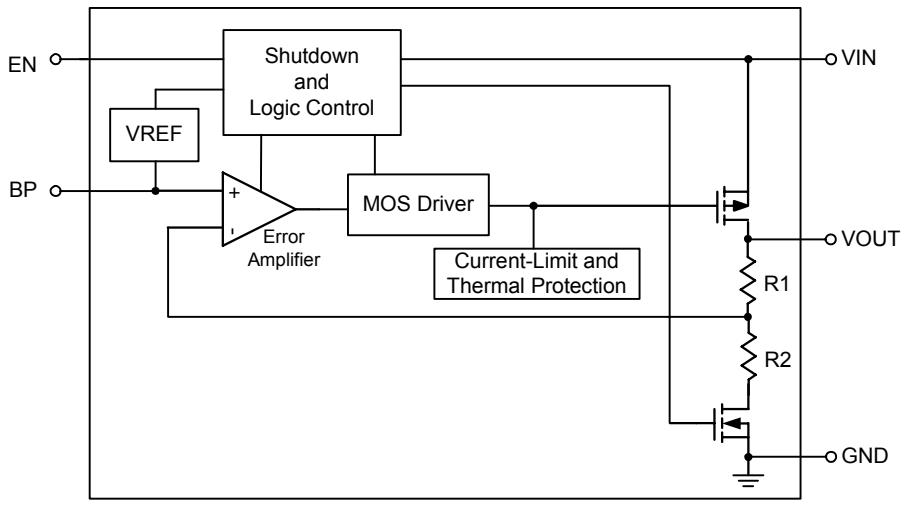
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 5, 8	NC	No Internal Connection.
2	VIN	Power Input Voltage.
3	GND	Ground.
7	EN	Chip Enable (Active High).
6	BP	Reference Noise Bypass.
4	VOUT	Output Voltage.

Function Block Diagram



Absolute Maximum Ratings (Note1)

- Input Voltage ---------- 8V
- EN Input Voltage ---------- 6V
- Power Dissipation, P_D @ T_A = 25°C
  MSOP-8 ---------- 0.823W
- Package Thermal Resistance (Note2)
  MSOP-8, θ_{JA} ---------- 120°C/W
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C

Recommended Operating Conditions (Note 3)

- Supply Input Voltage, V_{IN} ---------- 2.7V to 7V
- EN Input Voltage ---------- 2.7V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 5.0V, C_{IN} = 1μF, C_{OUT} = 1μF, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range		V_{IN}		2.9	--	7	V
			I_L = 50mA	2.7	--	7	
Output Voltage Accuracy		ΔV_{OUT}	I_L = 1mA	–2	--	2	%
Maximum Output Current		I_{MAX}		300	--	--	mA
Current Limit		I_{LIM}	R_{LOAD} = 1Ω	400	--	--	mA
Quiescent Current		I_Q	No Load	--	80	150	μA
			I_{OUT} = 300mA	--	90	150	
Dropout Voltage (Note 4) ($V_{OUT(Normal)}$ = 3V Version)		V_{DROP}	I_{OUT} = 1mA	--	1.1	5	mV
			I_{OUT} = 50mA	--	55	100	
			I_{OUT} = 300mA	--	350	450	
Line Regulation		ΔV_{LINE}	V_{IN}= (V_{OUT} + 0.15) to 7V, I_{OUT} =1mA	--	--	6	mV/V
Load Regulation		ΔV_{LOAD}	I_{OUT} = 0mA to 300mA	--	--	30	mV
EN Input Threshold	Logic-High	V_{IH}	V_{IN}= 3V to 5.5V	1.6	--	--	V
	Logic-Low	V_{IL}	V_{IN} = 3V to 5.5V	--	--	0.4	
EN Bias Current		I_{SD}		--	--	100	nA
Shutdown Supply Current		I_{GSD}	V_{OUT} = 0V	--	0.01	1	μA
Thermal Shutdown Temperature		T_{SD}		--	155	--	°C
Ripple Rejection		PSRR	F = 100Hz, C_{BP} = 10nF, C_{OUT} = 10μF	--	58	--	dB

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

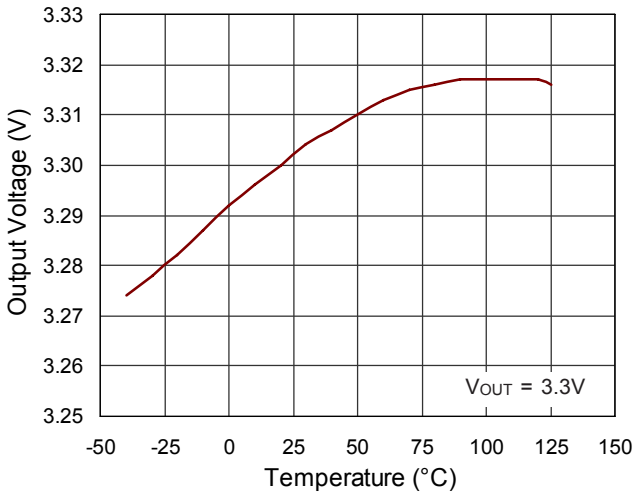
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

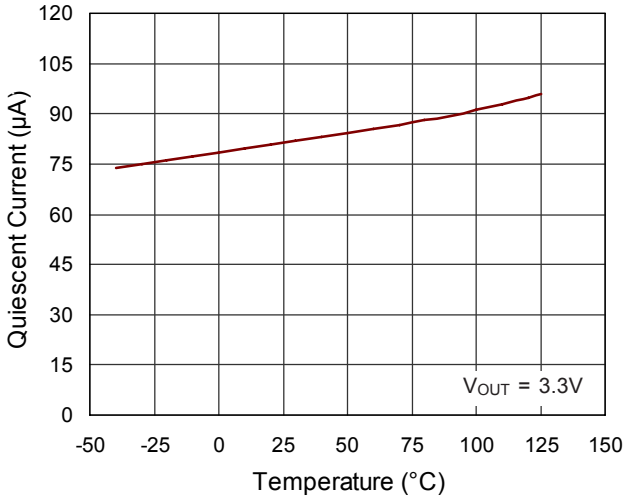
Note 4. The dropott voltage is defined as $V_{IN} - V_{OUT}$, which is measured when V_{OUT} is V_{OUT} (NORMAL) −100mV

Typical Operating Characteristics

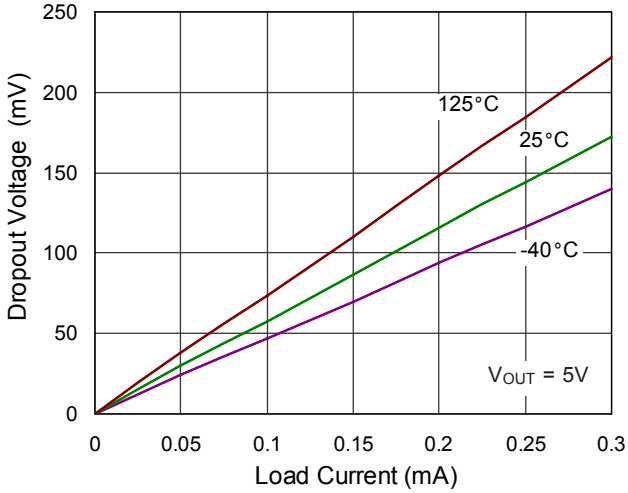
Output Voltage vs. Temperature



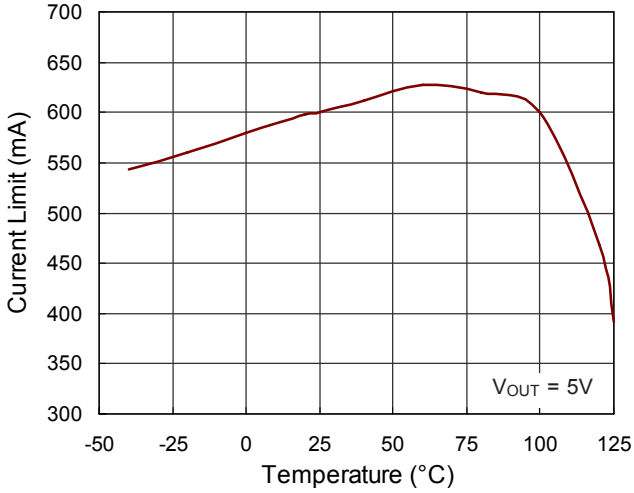
Quiescent Current vs. Temperature



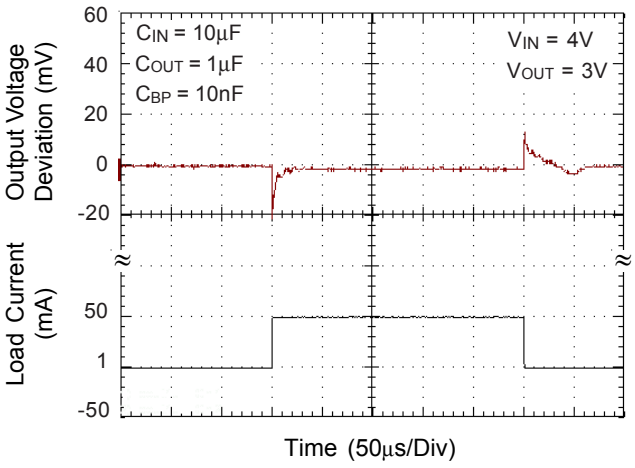
Dropout Voltage vs. Load Current



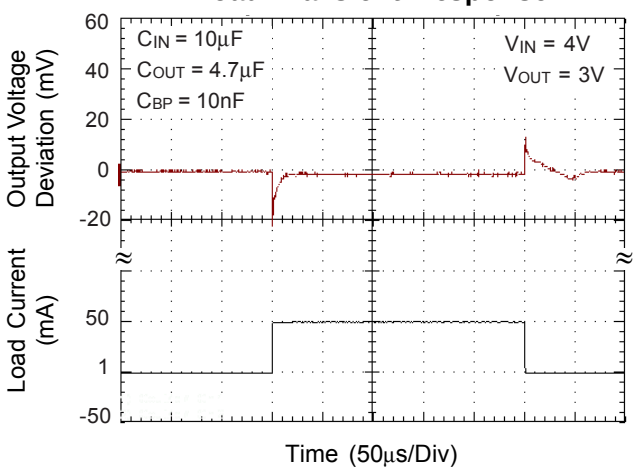
Current Limit vs. Temperature



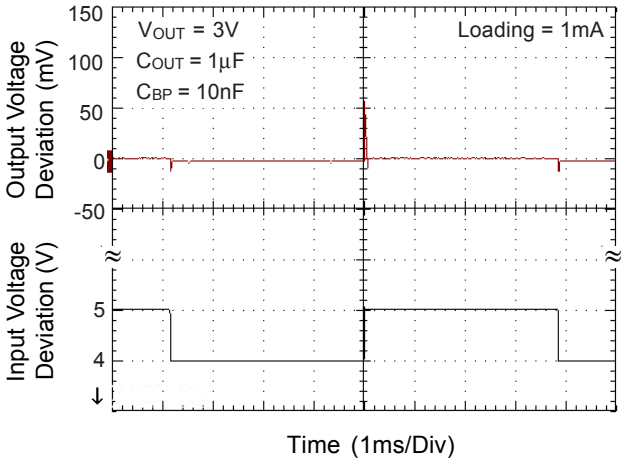
Load Transient Response



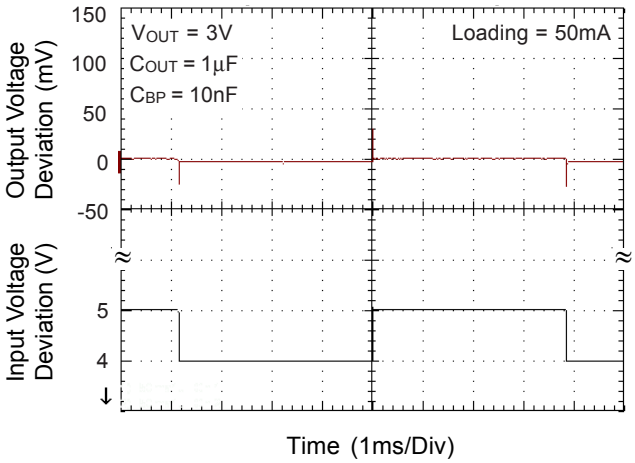
Load Transient Response



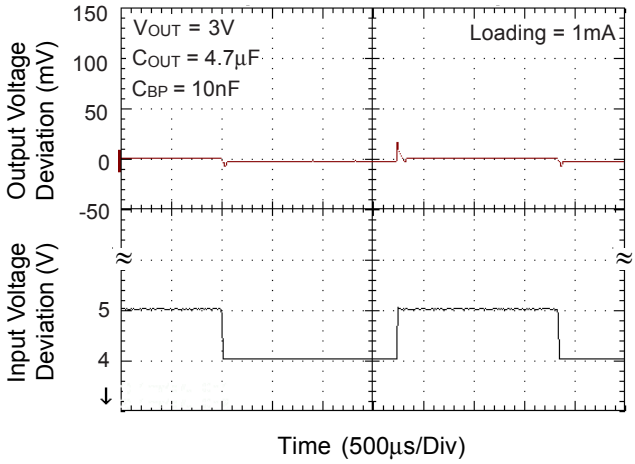
Line Transient Response



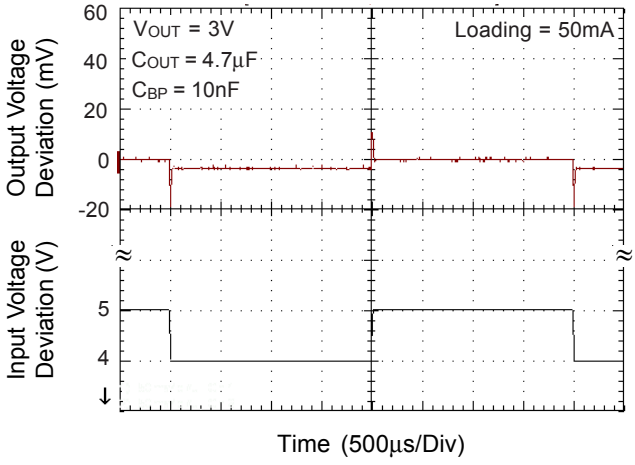
Line Transient Response



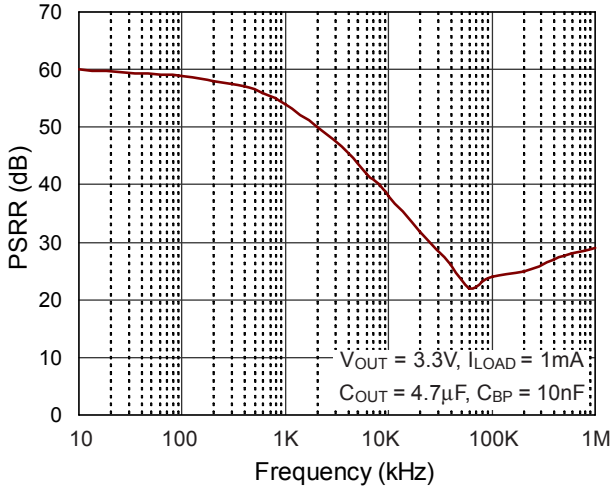
Line Transient Response



Line Transient Response



PSRR



Application Information

Capacitor Selection and Regulator Stability

Like any low-dropout regulator, the external capacitors used with the RT9167B must be carefully selected for regulator stability and performance.

Using a capacitor whose value is > 1μF on the RT9167B input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5" from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9167B is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 5mΩ on the RT9167B output ensures stability. The RT9167B still works well with output capacitor of other types due to the wide stable ESR range. Figure 1. shows the curves of allowable ESR range as a function of load current for various output voltages and capacitor values. Output capacitor of larger capacitance can reduce noise and improve load-transient response, stability, and PSRR. The output capacitor should be located not more than 0.5" from the V_{OUT} pin of the RT9167B and returned to a clean analog ground.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. It may be necessary to use 2.2μF or more to ensure stability at temperatures below −10°C in this case. Also, tantalum capacitors, 2.2μF or more may be needed to maintain capacitance and ESR in the stable region for strict application environment.

Tantalum capacitors maybe suffer failure due to surge current when it is connected to a low-impedance source of power (like a battery or very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed to have a surge current rating sufficient for the application by the manufacture.

Use a 10nF bypass capacitor at BP for low output voltage noise. The capacitor, in conjunction with an internal 200kΩ resistor, which connects bypass pin and the band-gap reference, creates an 80Hz low-pass filter for noise reduction. Increasing the capacitance will slightly decrease the output noise, but increase the start-up time. The capacitor connected to the bypass pin for noise reduction must have very low leakage. This capacitor leakage current causes the output voltage to decline by a proportional amount to the current due to the voltage drop on the internal 200kΩ resistor. Figure 2 shows the power on response.

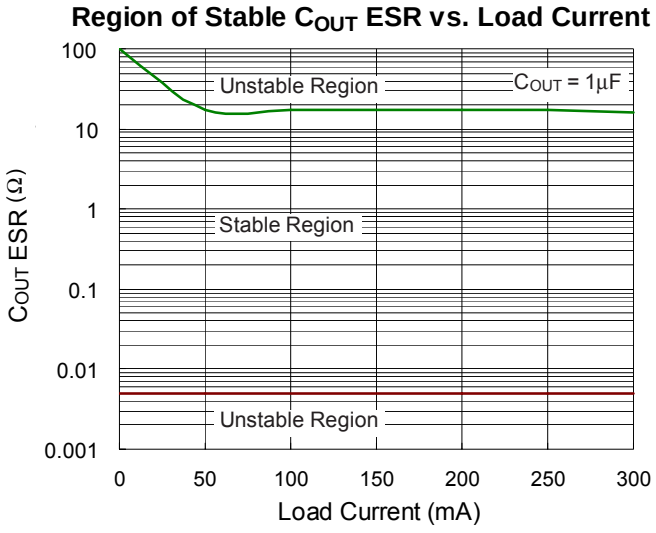


Figure 1

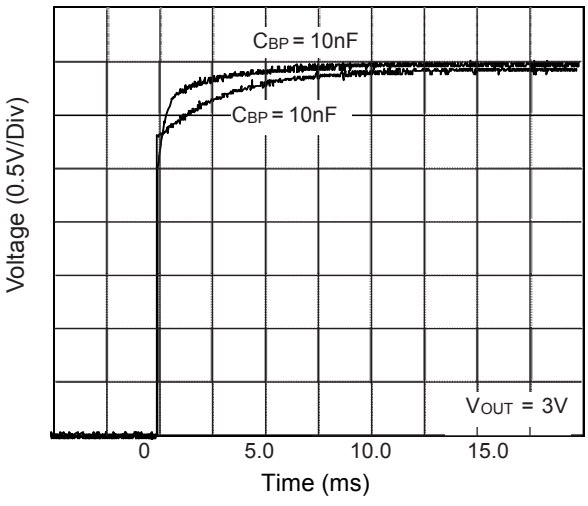


Figure 2

Load-Transient Considerations

The RT9167B load-transient response graphs (see Typical Operating Characteristics) show two components of the output response : a DC shift from the output impedance due to the load current change, and the transient response. The DC shift is quite small due to the excellent load regulation of the IC. Typical output voltage transient spike for a step change in the load current from 0mA to 50mA is tens mV, depending on the ESR of the output capacitor. Increasing the output capacitor's value and decreasing the ESR attenuates the overshoot.

Shutdown Input Operation

The RT9167B is shutdown by pulling the EN input low, and turned on by driving the input high. If this feature is not to be used, the EN input should be tied to VIN to keep the regulator on at all times (the EN input must **not** be left floating).

To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turn-on/turn-off voltage thresholds which guarantee an ON or OFF state (see Electrical Characteristics). The ON/OFF signal may come from either CMOS output, or an open-collector output with pull-up resistor to the RT9167B input voltage or another logic supply. The high-level voltage may exceed the RT9167B input voltage, but must remain within the absolute maximum ratings for the EN pin.

Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this will determine the useful end-of-life battery voltage. Because the RT9167B uses a P-Channel MOSFET pass transistor, the dropout voltage is a function of drain-to-source on-resistance [$R_{DS(ON)}$] multiplied by the load current.

Operating Region and Power Dissipation

The maximum power dissipation of RT9167B depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The power dissipation across the device is $P = I_{OUT} (V_{IN} – V_{OUT})$. The maximum power dissipation is : $PMAX = (T_J – T_A) / \theta_{JA}$

where $T_J – T_A$ is the temperature difference between the RT9167B die junction and the surrounding environment, θ_{JA} is the thermal resistance from the junction to the surrounding environment. The GND pin of the RT9167B performs the dual function of providing an electrical connection to ground and channeling heat away. Connect the GND pin to ground using a large pad or ground plane.

Current Limit and Thermal Protection

The RT9167B includes a current limit which monitors and controls the pass transistor's gate voltage limiting the output current to 400mA min. Thermal-overload protection limits total power dissipation in the RT9167B. When the junction temperature exceeds T_J = 155°C, the thermal sensor signals the shutdown logic turning off the pass transistor and allowing the IC to cool. The thermal sensor will turn the pass transistor on again after the IC's junction temperature cools by 10°C, resulting in a pulsed output during continuous thermal-overload conditions. Thermal-overloaded protection is designed to protect the RT9167B in the event of fault conditions. Do not exceed the absolute maximum junction-temperature rating of T_J = 150°C for continuous operation. The output can be shorted to ground for an indefinite amount of time without damaging the part by cooperation of current limit and thermal protection.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT9167B, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For MSOP-

8 packages, the thermal resistance, θ_{JA}, is 120°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (120°C/W) = 0.833W for MSOP-8 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT9167B package, the derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

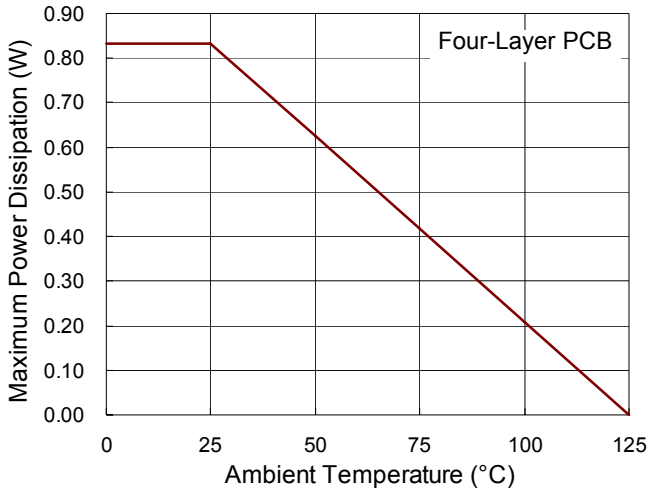
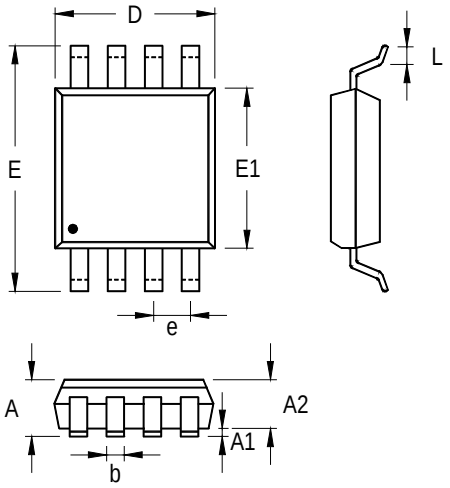


Figure 3. Derating Curves for RT9167B Packages

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.810	1.100	0.032	0.043
A1	0.000	0.150	0.000	0.006
A2	0.750	0.950	0.030	0.037
b	0.220	0.380	0.009	0.015
D	2.900	3.100	0.114	0.122
e	0.650		0.026	
E	4.800	5.000	0.189	0.197
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031

8-Lead MSOP Plastic Package

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