ISL9105

600mA Low Quiescent Current 1.6MHz High Efficiency Synchronous Buck Regulator

FN6415
Rev 2.00
March 28, 2008

ISL9105 is a 600mA, 1.6MHz step-down regulator that is ideal for powering low-voltage microprocessors in handheld devices such as PDAs and cellular phones. It is optimized for generating low output voltages down to 0.8V. The supply voltage range is from 2.7V to 5.5V, allowing for the use of a single Li+ cell, three NiMH cells or a regulated 5V input. It has a guaranteed minimum output current of 600mA. 1.6MHz pulse-width modulation (PWM) switching frequency allows for use of small external components. It has flexible operation mode selection of forced PWM mode and low IQ mode with typical 25µA quiescent current for highest light load efficiency to maximize battery life.

The ISL9105 includes a pair of low ON-resistance P-Channel and N-Channel internal MOSFETs to maximize efficiency and minimize external component count. 100% duty-cycle operation allows less than 200mV dropout voltage at 600mA output current.

The ISL9105 offers a typical 216ms Power-On-Reset (POR) timer at power-up. The timer output can be reset by RSI. When shutdown, ISL9105 discharges the output capacitor. Other features include internal digital soft-start, enable for power sequence, overcurrent protection, and thermal shutdown.

The ISL9105 is offered in a 2mmx3mm 8 Ld DFN package with 1mm maximum height. The complete converter occupies less than $1cm^2$ area.

Ordering Information

PART NUMBER (NOTE)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL9105IRZ-T*	05Z	-40 to +85	8 Ld 2x3 DFN	L8.2x3

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

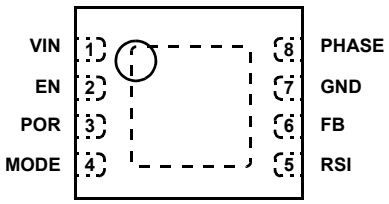
- High Efficiency Synchronous Buck Regulator with up to 95% Efficiency
- Selectable Forced PWM Mode and SKIP Mode
- 25µA Quiescent Supply Current in SKIP Mode
- 2.7V to 5.5V Supply Voltage
- 216ms POR Timer
- 3% Output Accuracy Over Temperature/Line/Load
- 600mA Guaranteed Output Current
- Less than 1µA Logic Controlled Shutdown Current
- 100% Maximum Duty Cycle for Lowest Dropout
- Discharge Output Capacitor when Shutdown
- Internal Loop Compensation
- Internal Digital Soft-Start
- Peak Current Limit Protection, Short Circuit Protection
- Over-Temperature Protection
- Enable
- Small 8 Ld 2mmx3mm DFN
- Pb-free (RoHS Compliant)

Applications

- Single Li-Ion Battery-Powered Equipment
- DSP Core Power
- PDAs and Palmtops

Pinout

ISL9105
(8 LD DFN)
TOP VIEW



Absolute Maximum Ratings (Reference to GND)

Supply Voltage (VIN) . . . . . -0.3V to 6.5V
EN, RSI, MODE, POR . . . . . -0.3V to VIN+0.3V
PHASE. . . . . -1.5V to 6.5V
FB . . . . . -0.3V to 2.7V

Recommended Operating Conditions

VIN Supply Voltage Range . . . . . 2.7V to 5.5V
Load Current Range . . . . . 0mA to 600mA
Ambient Temperature Range . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
2x3 DFN Package	75	6

Junction Temperature Range. . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. θ_{JC}, “case temperature” location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.
3. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

Electrical Specifications

Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specifications are measured at the following conditions: T_A = +25°C, V_{IN} = 3.6V, EN = V_{IN}, RSI = MODE = 0V, L = 3.3µH, C1 = 10µF, C2 = 10µF, I_{OUT} = 0A (see “TYPICAL APPLICATION DIAGRAM” on page 6).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
SUPPLY						
VIN Undervoltage Lockout Threshold	V_{UVLO}	Rising	-	2.5	2.7	V
		Falling	2.2	2.4	-	V
Quiescent Supply Current	I_{VIN}	MODE = V_{IN}, no load at the output	-	25	50	µA
		MODE = GND, no load at the output	-	5	8	mA
Shutdown Supply Current	I_{SD}	V_{IN} = 5.5V, EN = low	-	0.1	2	µA
OUTPUT REGULATION						
FB Regulation Voltage	V_{FB}	T_A = 0°C to +85°C	0.784	0.8	0.816	V
		T_A = -40°C to +85°C	0.78	0.8	0.82	V
FB Bias Current	I_{FB}	FB = 0.75V	-	0.1	-	µA
Output Voltage Accuracy		V_{IN} = V_O + 0.5V to 5.5V, I_O = 0mA to 600mA	-3	-	3	%
Line Regulation		V_{IN} = V_O + 0.5V to 5.5V (minimal 2.7V)	-	0.2	-	%/V
Maximum Output Current			600	-	-	mA
COMPENSATION						
Error Amplifier Trans-Conductance		Design info only	-	20	-	µA/V
PHASE						
P-Channel MOSFET ON-resistance		V_{IN} = 3.6V, I_O = 200mA	-	0.16	0.22	Ω
N-Channel MOSFET ON-resistance		V_{IN} = 3.6V, I_O = 200mA	-	0.14	0.22	Ω
P-Channel MOSFET Peak Current Limit	I_{PK}		0.75	1.0	1.3	A
PHASE Maximum Duty Cycle			-	100	-	%
PWM Switching Frequency	f_S		1.2	1.6	1.8	MHz
PHASE Minimum ON-time		MODE = low (forced PWM mode)	-	-	140	ns
Soft-Start-Up Time			-	1.1	-	ms

Electrical Specifications Unless otherwise noted, all parameter limits are guaranteed over the recommended operating conditions and the typical specifications are measured at the following conditions: T_A = +25°C, V_{IN} = 3.6V, EN = V_{IN}, RSI = MODE = 0V, L = 3.3µH, C1 = 10µF, C2 = 10µF, I_{OUT} = 0A (see "TYPICAL APPLICATION DIAGRAM" on page 6).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
POR						
Output Low Voltage		Sinking 1mA, FB = 0.7V	-	-	0.3	V
Delay Time			150	216	275	ms
POR Pin Leakage Current		POR = V_{IN} = 3.6V	-	0.01	0.1	µA
Minimum Supply Voltage for Valid POR Signal			1.2	-	-	V
Internal PGOOD Low Rising Threshold		Percentage of nominal regulation voltage	89.5	92	94.5	%
Internal PGOOD Low Falling Threshold		Percentage of nominal regulation voltage	85	88	91	%
Internal PGOOD High Rising Threshold		Percentage of nominal regulation voltage	105.5	108	110.5	%
Internal PGOOD High Falling Threshold		Percentage of nominal regulation voltage	102	105	108	%
Internal PGOOD Delay Time			-	64	-	µs
EN, MODE, RSI						
Logic Input Low			-	-	0.4	V
Logic Input High			1.4	-	-	V
Logic Input Leakage Current		Pulled up to 5.5V	-	0.1	1	µA
Thermal Shutdown			-	150	-	°C
Thermal Shutdown Hysteresis			-	25	-	°C

Pin Descriptions

VIN

Input supply voltage. Connect a 10µF ceramic capacitor to power ground.

EN

Regulator enable pin. Enable the output when driven to high. Shutdown the chip and discharge the output capacitor when driven to low. Do not leave this pin floating.

POR

216ms timer output. At power-up or EN HI, this output is a 216ms delayed Power-Good signal for the output voltage. This output can be reset by a low RSI signal. 216ms starts when RSI goes to high.

MODE

Mode Selection pin. Connect to logic high or input voltage VIN for low IQ mode; connect to logic low or ground for forced PWM mode. Do not leave this pin floating.

PHASE

Switching node connection. Connect to one terminal of inductor.

GND

System ground.

FB

Buck regulator output feedback. Connect to the output through a voltage divider resistor.

RSI

This input resets the 216ms timer. When the output voltage is within the PGOOD window, an internal timer is started and generates a POR signal 216ms later when RSI is low. A high RSI resets POR and RSI high to low transition restarts the internal counter if the output voltage is within the window, otherwise the counter is reset by the output voltage condition.

Exposed Pad

The exposed pad must be connected to the GND pin for proper electrical performance. The exposed pad must also be connected to as much as possible for optimal thermal performance.

Typical Operating Performance

(Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 3.6V, EN = VIN, RSI = MODE = 0V, L = 3.3µH, C1 = 10µF, C2 = 10µF, I_{OUT} = 0A).

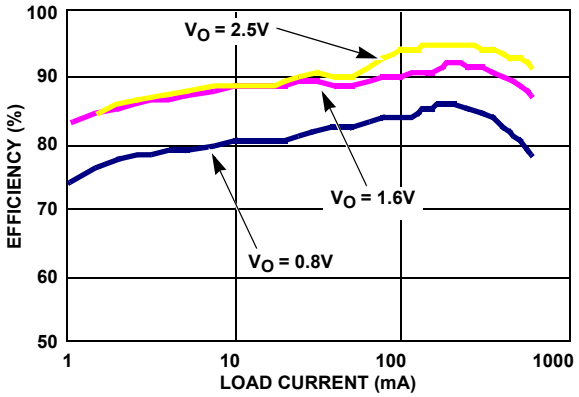


FIGURE 1. EFFICIENCY vs LOAD CURRENT (V_{IN} = 3.6V)

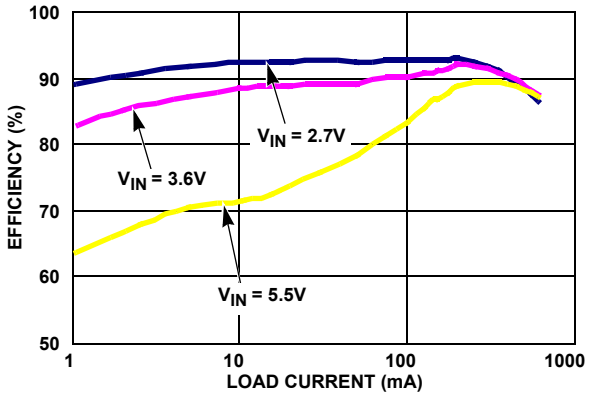


FIGURE 2. EFFICIENCY vs LOAD CURRENT (V_O = 1.6V)

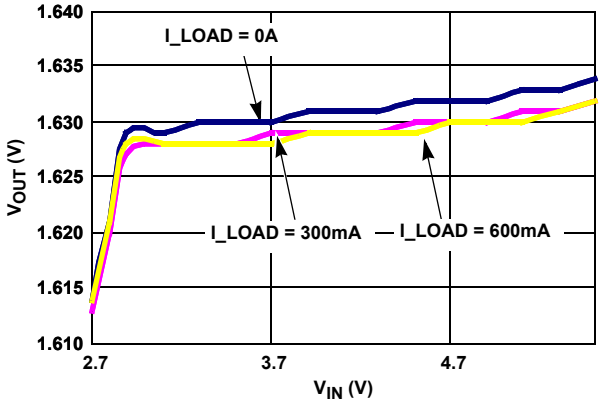


FIGURE 3. LINE REGULATION

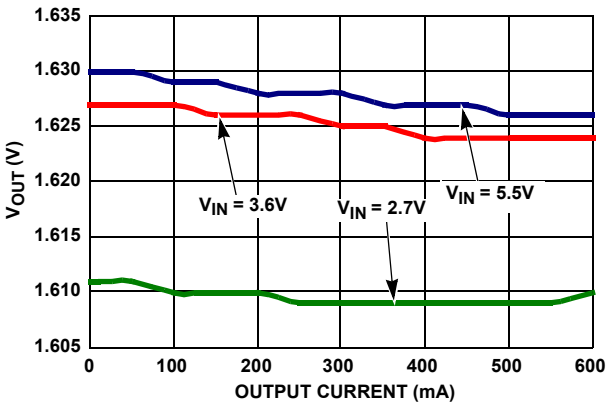


FIGURE 4. LOAD REGULATION

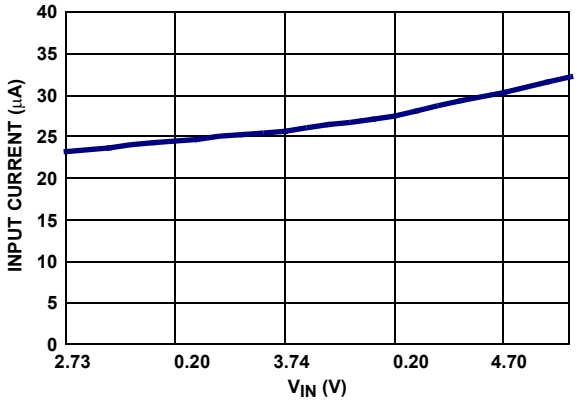


FIGURE 5. I_Q vs V_{IN} (PFM)

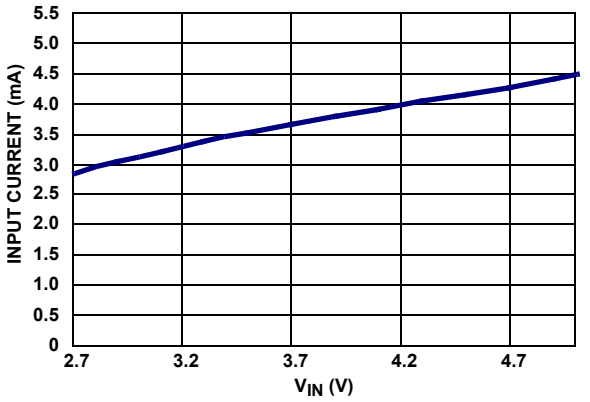


FIGURE 6. I_Q vs V_{IN} (PWM)

Typical Operating Performance (Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 3.6V, EN = VIN, RSI = MODE = 0V, L = 3.3µH, C1 = 10µF, C2 = 10µF, I_{OUT} = 0A). **(Continued)**

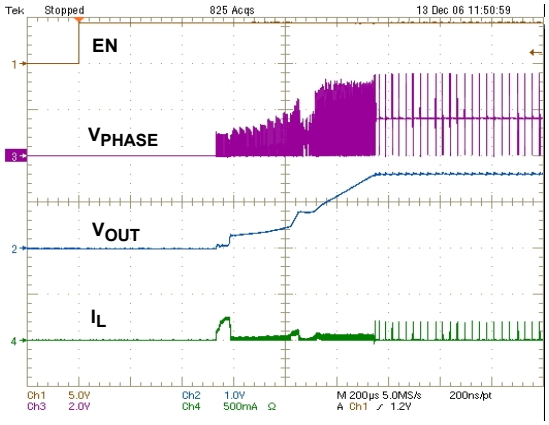


FIGURE 7. SOFT-START (PFM, V_{IN} = 3.6V, V_{OUT} = 1.6V, I_O = 10mA)

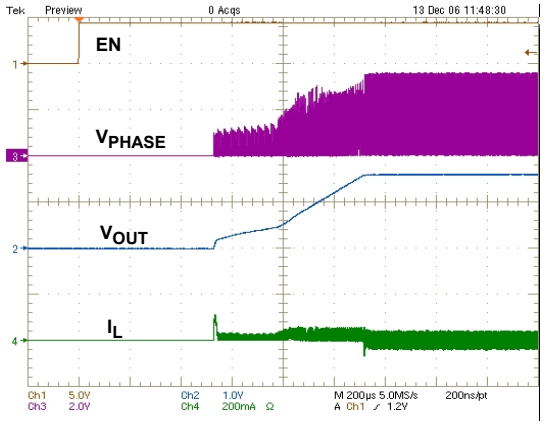


FIGURE 8. SOFT-START (PWM, V_{IN} = 3.6V, V_{OUT} = 1.6V, I_O = 1mA)

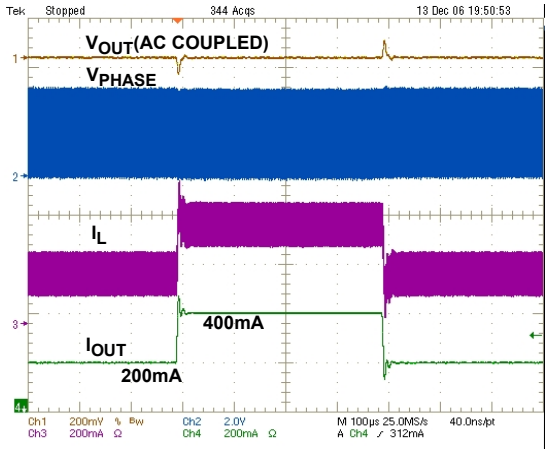


FIGURE 9. LOAD TRANSIENT (PWM, V_{IN} = 3.6V, V_{OUT} = 1.6V)

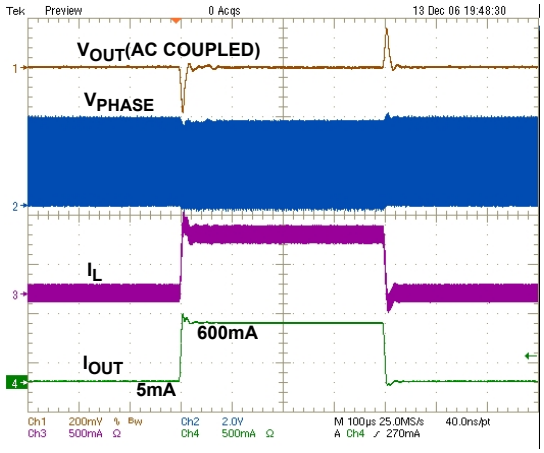


FIGURE 10. LOAD TRANSIENT (PWM, V_{IN} = 3.6V, V_{OUT} = 1.6V)

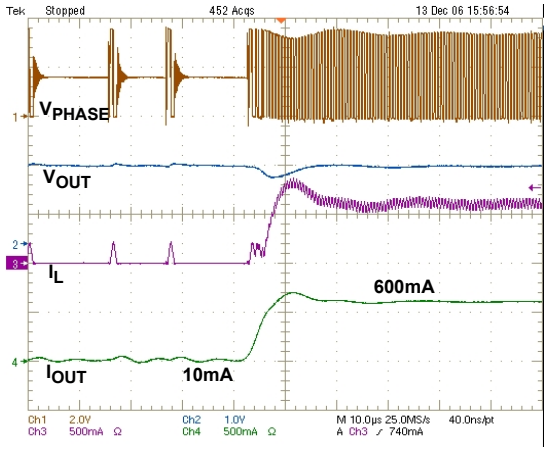


FIGURE 11. LOAD TRANSIENT (PFM, V_{IN} = 3.6V, V_{OUT} = 1.6V)

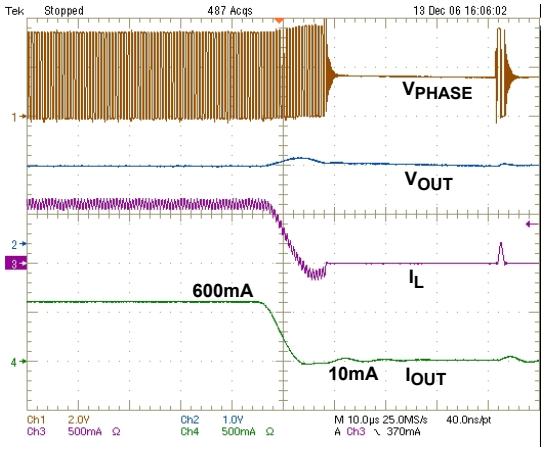


FIGURE 12. LOAD TRANSIENT (PFM, V_{IN} = 3.6V, V_{OUT} = 1.6V)

Typical Operating Performance (Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 3.6V, EN = VIN, RSI = MODE = 0V, L = 3.3µH, C1 = 10µF, C2 = 10µF, I_{OUT} = 0A). **(Continued)**

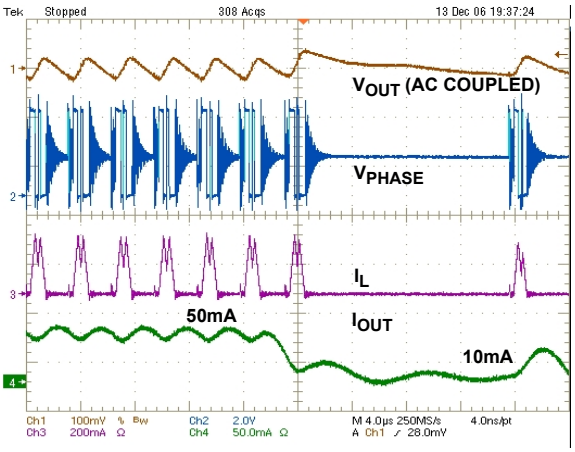


FIGURE 13. (PFM, V_{IN} = 3.6V, V_{OUT} = 1.6V)

Typical Applications

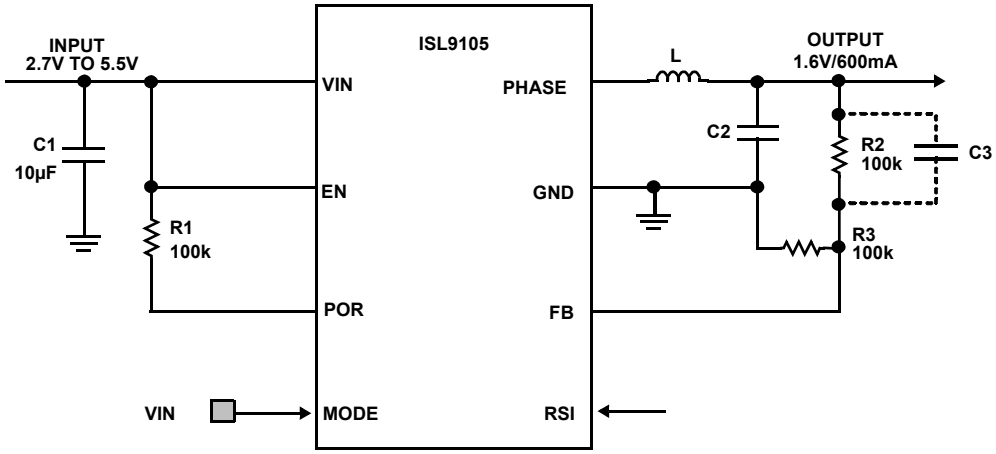
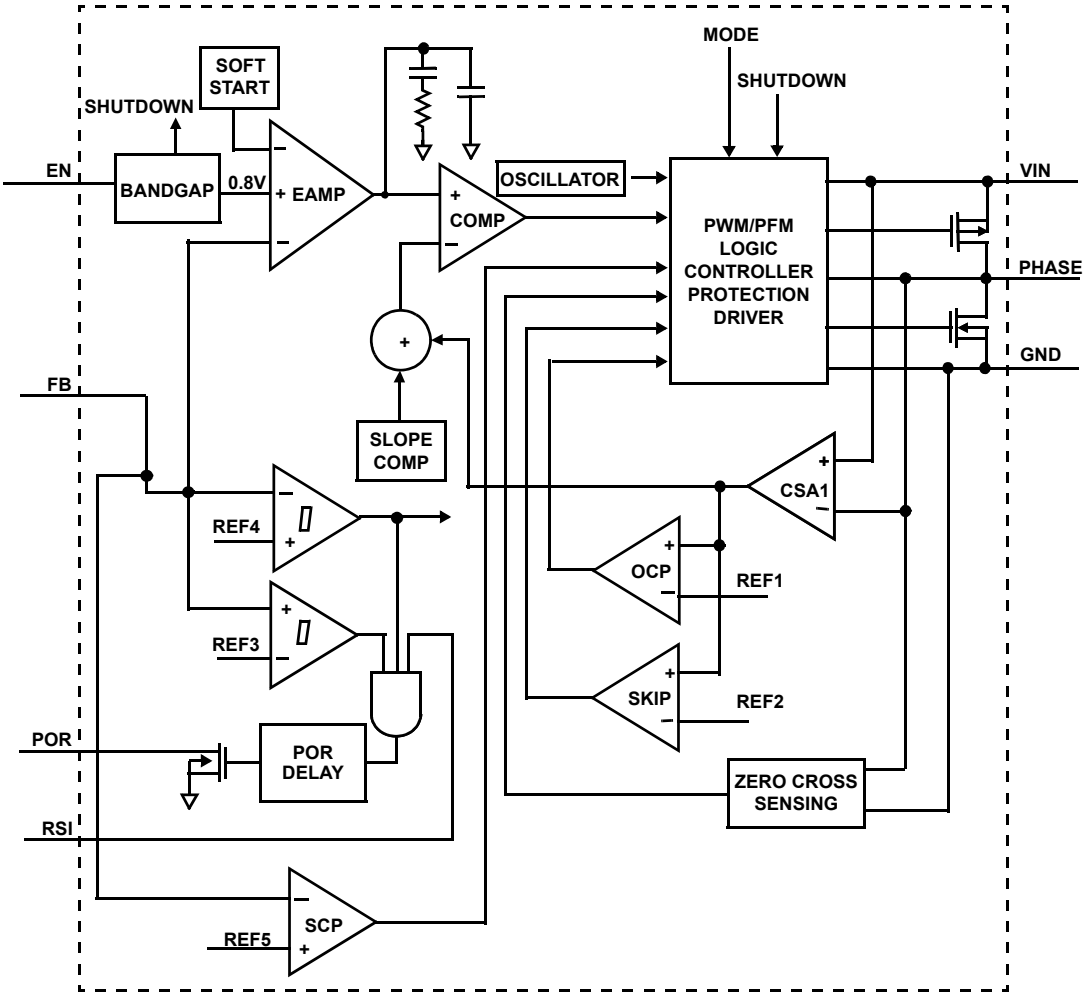


FIGURE 14. TYPICAL APPLICATION DIAGRAM

PARTS	DESCRIPTION	MANUFACTURERS	PART NUMBER	SPECIFICATIONS	SIZE
L	Output inductor	Sumida	CDRH4D14/HP-4R7	4.7µH/1.40A/115mΩ	4.6mmx4.6mmx1.5mm
		Sumida	CDRH2D14NP-3R3	3.3µH/1.20A/100mΩ	3.2mmx3.2mmx1.55mm
		Coilcraft	LPS3015-472MLB	4.7µH/1.10A/200mΩ	3.3mmx3.3mmx1.4mm
C1	Input capacitor	Murata	GRM21BR60J106KE19L	10µF/6.3V	2.0mmx1.25mmx1.25mm (0805)
C2	Output capacitor	Murata	GRM21BR60J475KA11L	4.7µF/6.3V, 10µF/6.3V	2.0mmx1.25x1.25mm (0805)
C3		Panasonic	ECJ-1VC2A100D	10pF/100V	0603
R1	Pull-up resistor	Various		100kΩ	1.6mmx0.8mmx0.45mm (0603)

Block Diagram



Theory of Operation

The ISL9105 is a step-down switching regulator optimized for battery-powered handheld applications. The regulator operates at 1.6MHz fixed switching frequency under heavy load conditions to allow small external inductor and capacitors to be used for minimal printed-circuit board (PCB) area. At light load, the regulator reduces the switching frequency, unless forced to the fixed frequency, to minimize the switching loss and to maximize the battery life. The quiescent current when the output is not loaded is typically only 25µA. The supply current is typically only 0.1µA when the regulator is shut down.

PWM Control Scheme

The ISL9105 employs the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Figure 15 shows the block diagram. The current loop consists of the oscillator, the PWM comparator COMP, current sensing circuit, and the slope compensation for the current loop stability. The current sensing circuit consists of the resistance of the P-Channel MOSFET when it is turned on and the Current Sense Amplifier (CSA). The control reference for the current loops comes from the Error Amplifier (EAMP) of the voltage loop.

The PWM operation is initialized by the clock from the oscillator. The P-Channel MOSFET is turned on at the beginning of a PWM cycle and the current in the P-Channel MOSFET starts ramping up. When the sum of the CSA output and the compensation slope reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-Channel MOSFET and to turn on the N-Channel MOSFET. The N-Channel MOSFET remains on till the end of the PWM cycle. Figure 15 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the compensation ramp and the CSA output.

The output voltage is regulated by controlling the reference voltage to the current loop. The bandgap circuit outputs a 0.8V reference voltage to the voltage control loop. The feedback signal comes from the FB pin. The soft-start block only affects the operation during the start-up and will be

discussed separately in the “Soft-Start-Up” on page 9. The error amplifier is a transconductance amplifier, which converts the voltage error signal to a current output. The voltage loop is internally compensated by a RC network. The maximum EAMP voltage output is precisely clamped to the bandgap voltage (1.172V).

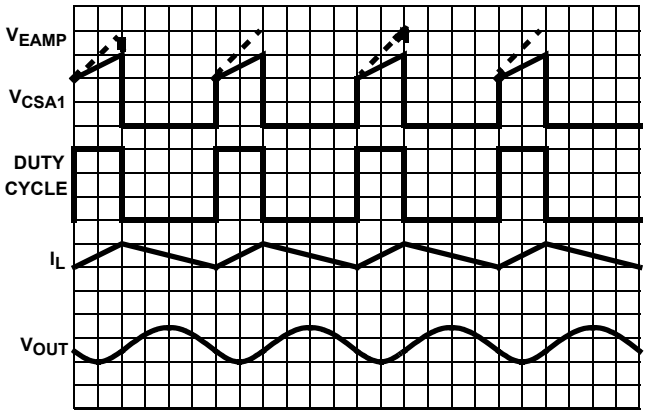


FIGURE 15. PWM OPERATION WAVEFORMS

SKIP Mode

The ISL9105 enters a pulse-skipping mode at light load to minimize the switching loss by reducing the effective switching frequency. Figure 16 illustrates the skip-mode operation. A zero-cross sensing circuit (as shown in Figure 15) monitors the N-Channel MOSFET current for zero crossing. When the N-Channel MOSFET current is detected crossing zero for 8 consecutive cycles, the regulator enters the skip mode. During the 8 consecutive cycles, the inductor current is allowed to be negative. The internal counter is reset to zero when the sensed N-Channel MOSFET current does not cross zero in any cycle within the 8 consecutive cycles.

Once ISL9105 enters SKIP mode, the pulse modulation starts being controlled by the SKIP comparator shown in Figure 15. Each pulse cycle is still synchronized by the PWM clock. The P-Channel MOSFET is turned on at the rising edge of the clock and turned off when its current reaches 20% of the peak current limit. As the average inductor current in each cycle is higher than the average current of the load, the output voltage rises cycle over cycle. When the output voltage reaches 1.5% above the nominal voltage, the P-Channel MOSFET is turned off immediately and the inductor current is fully discharged to zero and remains zero. The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-Channel MOSFET will be turned on again, repeating the previous operations.

The regulator resumes PWM mode operation when the output voltage drops 1.5% below the nominal voltage.

Enable

The enable (EN) input allows user to control the turn-on and turn-off of the regulator for purposes, such as power-up sequencing. When the regulator is enabled, there is a typically a 600µs delay for waking up the internal reference circuit, then the soft start-up begins. When the regulator is disabled, the P-MOSFET is turned off immediately and the output capacitor is discharged.

POR Signal

The ISL9105 offers a Power-On Reset (POR) signal. When the output voltage is not within a power-good window, the POR pin outputs an open-drain low signal (Figure 15), which can be used to reset the microprocessor. When the output voltage is within a power-good window, a power-good signal is issued to turn off the open-drain POR pin. The rising edge of the POR output is delayed by 216ms (typical) from the time the power-good signal is issued.

Mode Selection

MODE pin is provided on ISL9105 to select the operation mode. When it is driven to logic low or shorted to ground, the regulator operates in the forced PWM mode. The forced PWM mode remains the fixed PWM frequency (typically 1.6MHz) at all load conditions.

When the MODE pin is driven to logic high or connected to input voltage V_{IN}, the regulator operates in either SKIP mode or fixed PWM mode depending upon the load condition.

RSI Signal

The RSI signal is an input signal, which can reset the POR signal. As shown in the “Block Diagram” on page 7, the power-

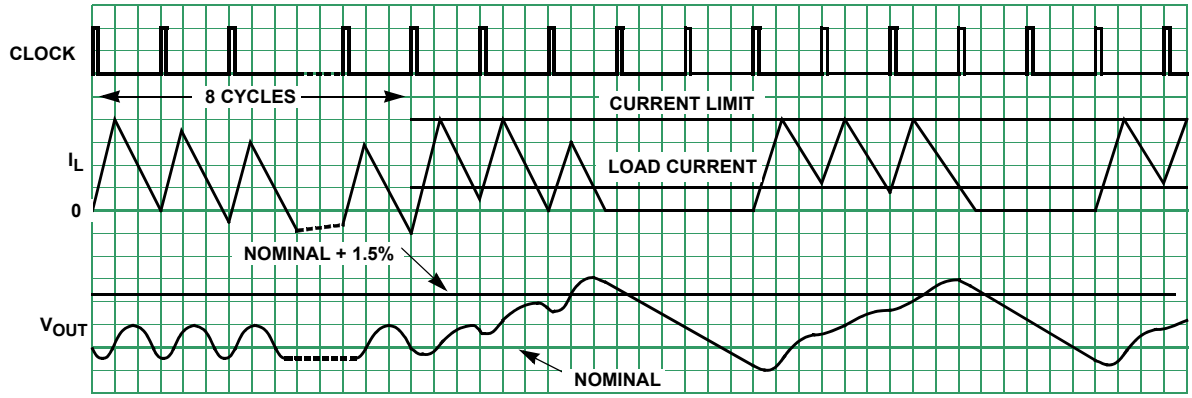


FIGURE 16. SKIP MODE OPERATION WAVEFORMS

good signal is gated by the RSI signal. When the RSI is high, the POR signal will remain low, regardless of the power-good signal.

Overcurrent Protection

The overcurrent protection can protect ISL9105 itself, as well as other external components when over load condition happens. It is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 15. The current sensing circuit has a gain of 0.4V/A. When the CSA output reaches 0.4V, (which means the current at P-Channel MOSFET reaches 1A) the OCP comparator is triggered to turn off the P-Channel MOSFET immediately.

Short-Circuit Protection

ISL9105 has a Short-Circuit Protection (SCP) comparator monitors the FB pin voltage for output short-circuit protection. When the FB is lower than 0.2V, the SCP comparator forces the PWM oscillator frequency to drop to 1/3 of the normal operation value. This comparator is effective during start-up or an output short-circuit event.

UVLO

When the input voltage is below the Undervoltage Lock Out (UVLO) threshold, the regulator is disabled.

Soft-Start-Up

The soft-start-up eliminates the in-rush current during the start-up. The soft-start block outputs a ramp reference to both the voltage loop and the current loop. The two ramps limit the inductor current rising speed as well as the output voltage speed so that the output voltage rises in a controlled fashion. At the very beginning of the start-up, the output voltage is less than 0.2V; hence the PWM operating frequency is 1/3 of the normal frequency.

Power MOSFETs

The two power MOSFETs are optimized to achieve better efficiency. The ON-resistance for the P-Channel MOSFET is typically 160mΩ and the ON-resistance for the N-Channel MOSFET is typically 140mΩ.

100% Duty Cycle Operation

The ISL9105 features 100% duty cycle operation to maximize the battery life. When the input voltage drops to a level that the ISL9105 can no longer maintain the switching regulation at the output, the P-Channel MOSFET is completely turned on. The maximum drop out voltage under the 100% duty-cycle operation is the product of the load current and the ON-resistance of the P-Channel MOSFET. Minimum input voltage V_{IN} under this condition is the sum of output voltage and the voltage drop cross the output inductor and P-Channel MOSFET.

Thermal Shut Down

The ISL9105 provides built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shutdown. As the temperature drops to +125°C, the ISL9105 resumes operation by stepping through a soft-start-up.

Applications Information

Output Inductor and Capacitor Selection

To achieve better steady state and transient operation, ISL9105 typically uses a 4.7µH output inductor. Higher or lower inductor value can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V application, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. The peak-to-peak inductor current ripple can be expressed in Equation 1:

$$\Delta I = \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L \bullet f_S} \quad \text{(EQ. 1)}$$

In Equation 1, the inductance should consider the value with worst case tolerances; and for switching frequency f_S, the minimum f_S from the “Electrical Specifications” table on page 2 can be used.

To select the inductor, its saturation current rating should be at least higher than the sum of the maximum output current and $(\Delta I)/2$ from Equation 1.

ISL9105 uses internal compensation network and the output capacitor value is dependant on the output voltage. The ceramic capacitor is recommended to be X5R or X7R.

Input Capacitor Selection

The main functions of the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current flowing back to the battery rail. A 10µF/6.3V ceramic capacitor (X5R or X7R) is a good starting point for the input capacitor selection.

Output Voltage Setting Resistor Selection

The voltage divider resistors, R_2 and R_3, shown in Figure 14 set the output voltage. The output voltage can be calculated using Equation 2:

$$V_O = 0.8 \bullet \left(1 + \frac{R_2}{R_3}\right) \quad \text{(EQ. 2)}$$

where the 0.8V is the reference voltage. The voltage divider, which consists of R_2 and R_3, increases the quiescent current by $V_O/(R_2 + R_3)$, so larger resistance is desirable. On the other hand, the FB pin has leakage current that will cause error in the output voltage setting. The leakage current is typically 0.1µA. To minimize the accuracy impact on the output voltage, select the R_3 no larger than 200kΩ.

PCB Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well.

For ISL9105, the power loop is composed of the output inductor L, the output capacitor C_{OUT}, the PHASE pin and the GND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide.

The switching node of the converter, the PHASE pin, and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces.

The input capacitor should be placed to VIN pin as close as possible. And the ground of input and output capacitors should be connected as close as possible.

The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance.

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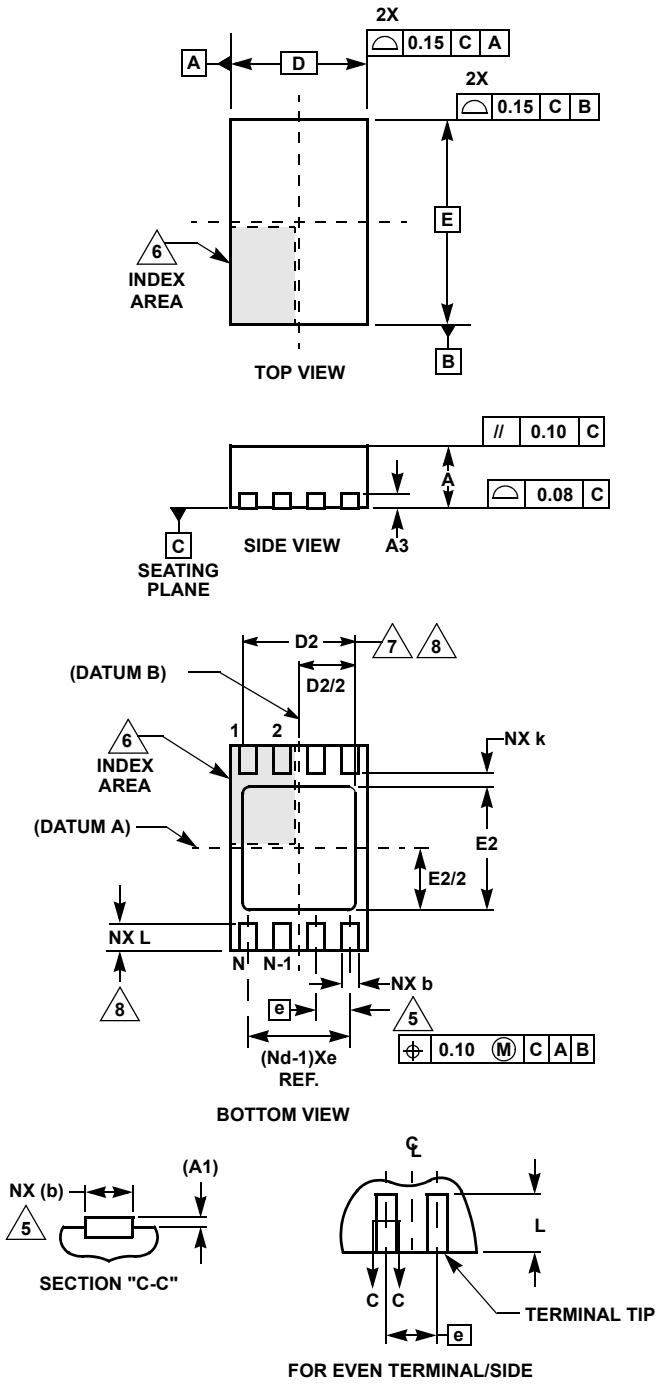
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Dual Flat No-Lead Plastic Package (DFN)



L8.2x3

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.32	5,8
D		2.00 BSC		-
D2	1.50	1.65	1.75	7,8
E		3.00 BSC		-
E2	1.65	1.80	1.90	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		8		2
Nd		4		3

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.