MJD128T4G (PNP)

Preferred Device

Complementary Darlington Power Transistor

DPAK For Surface Mount Applications

ON Semiconductor®

http://onsemi.com

SILICON
POWER TRANSISTOR
8 AMPERES
120 VOLTS, 20 WATTS

Features

Designed for general purpose amplifier and low speed switching applications.

- Monolithic Construction With Built−in Base−Emitter Shunt Resistors
- High DC Current Gain − h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Epoxy Meets UL 94 V−0 @ 0.125 in.
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V
- This is a Pb−Free Device

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	120	Vdc
Collector−Base Voltage	V_{CB}	120	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous Peak	I_C	8 16	Adc
Base Current	I_B	120	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	W W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

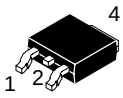
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction−to−Ambient*	$R_{\theta JA}$	71.4	°C/W

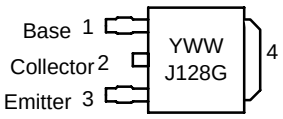
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

MARKING DIAGRAM



DPAK
CASE 369C
STYLE 1



Y = Year
WW = Work Week
J128 = Device Code
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MJD128T4G	DPAK (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	120	−	Vdc
Collector Cutoff Current (V_{CE} = 120 Vdc, I_B = 0)	I_{CEO}	−	5	mA
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	−	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	−	2	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 4 Vdc) (I_C = 8 Adc, V_{CE} = 4 Vdc)	h_{FE}	1000 100	12,000 −	−
Collector−Emitter Saturation Voltage (I_C = 4 Adc, I_B = 16 mAdc) (I_C = 8 Adc, I_B = 80 mAdc)	$V_{CE(sat)}$	− −	2 4	Vdc
Base−Emitter Saturation Voltage (1) (I_C = 8 Adc, I_B = 80 mAdc)	$V_{BE(sat)}$	−	4.5	Vdc
Base−Emitter On Voltage (I_C = 4 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	−	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain−Bandwidth Product (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 MHz)	$\|h_{fe}\|$	4	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	−	300	pF
Small−Signal Current Gain (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	300	−	−

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

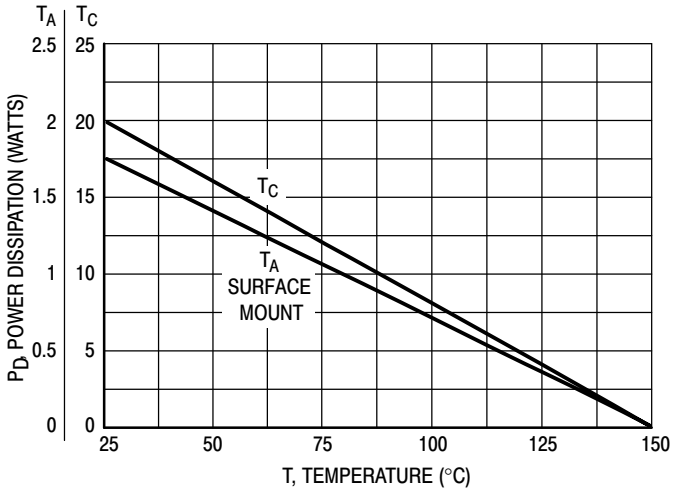


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

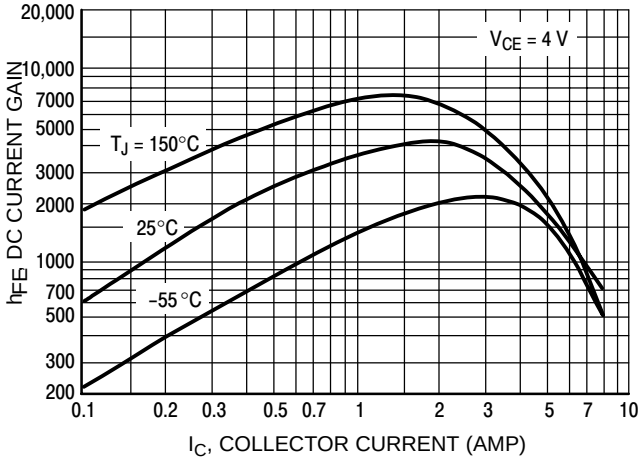


Figure 2. DC Current Gain

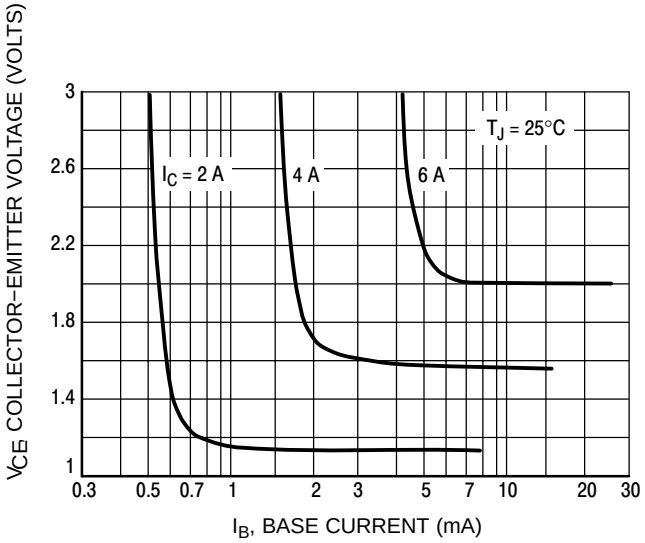


Figure 3. Collector Saturation Region

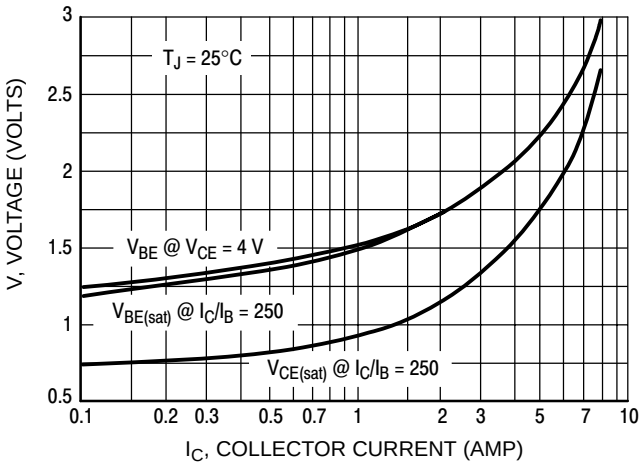


Figure 4. “On” Voltages

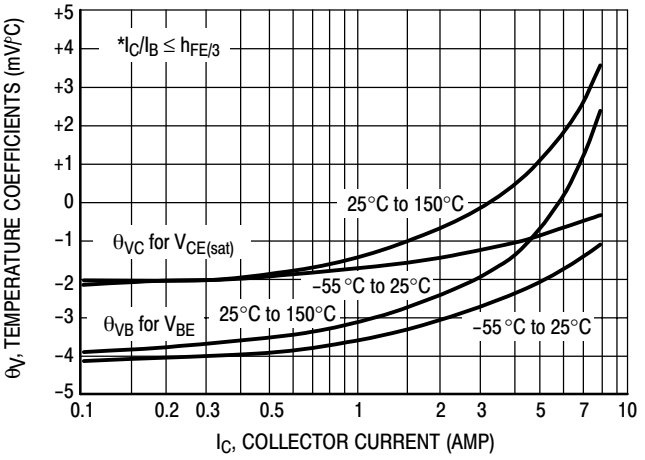


Figure 5. Temperature Coefficients

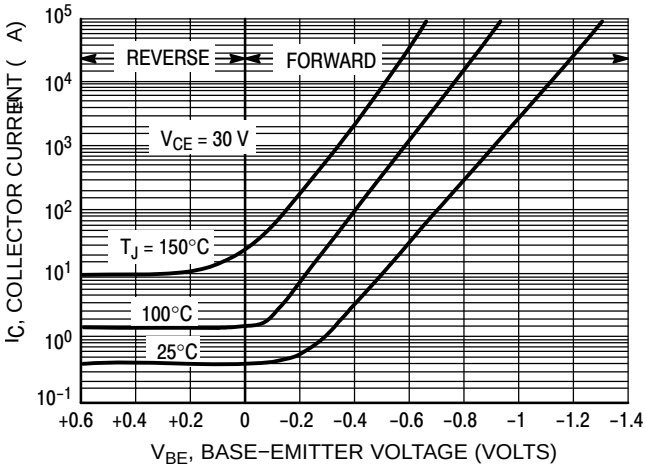


Figure 6. Collector Cut−Off Region

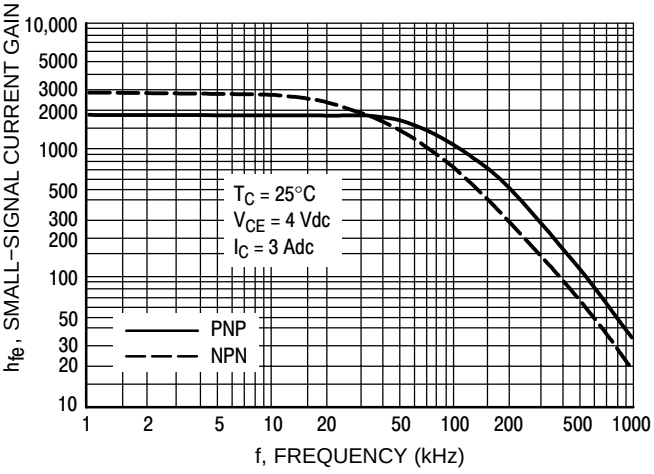


Figure 7. Small−Signal Current Gain

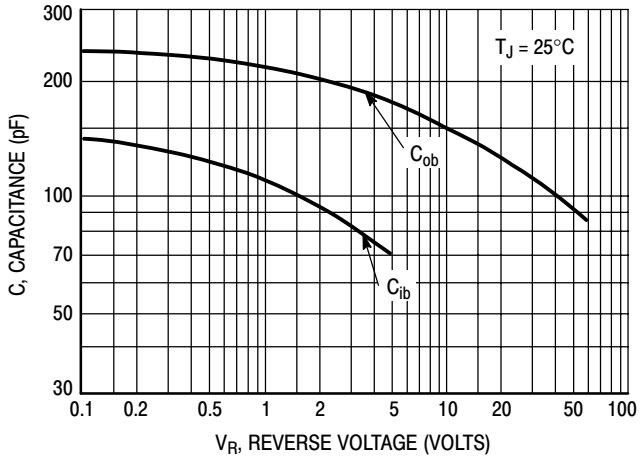


Figure 8. Capacitance

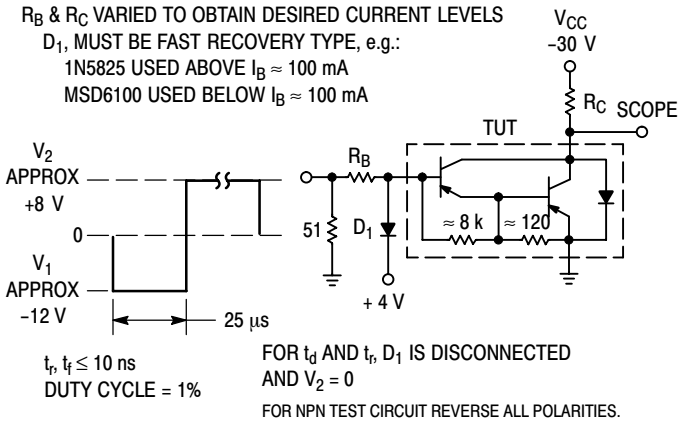


Figure 9. Switching Times Test Circuit

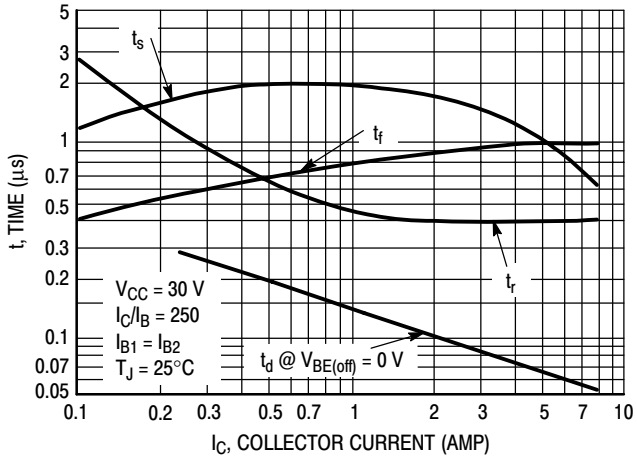


Figure 10. Switching Times

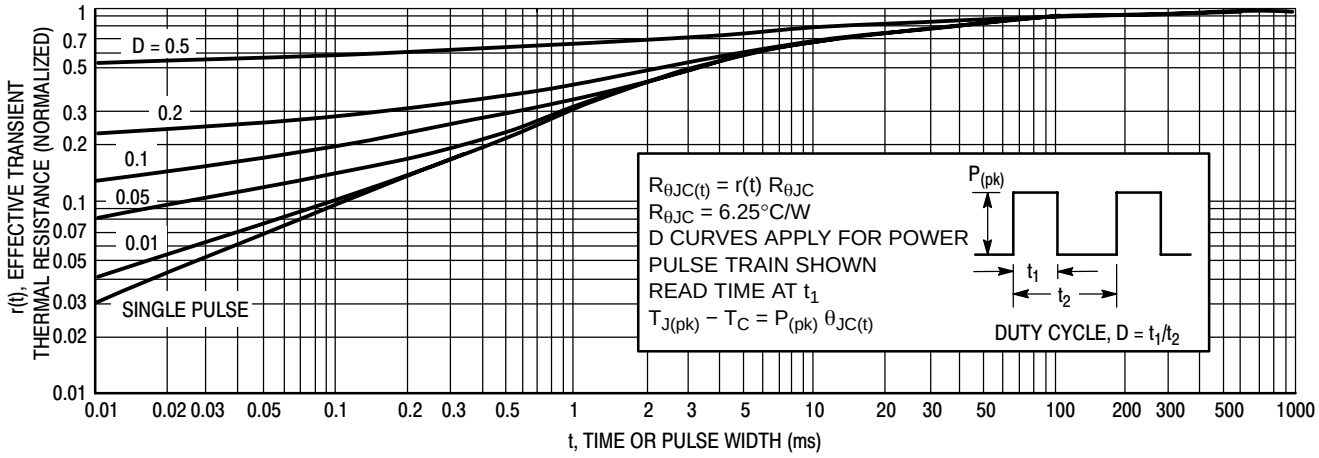


Figure 11. Thermal Response

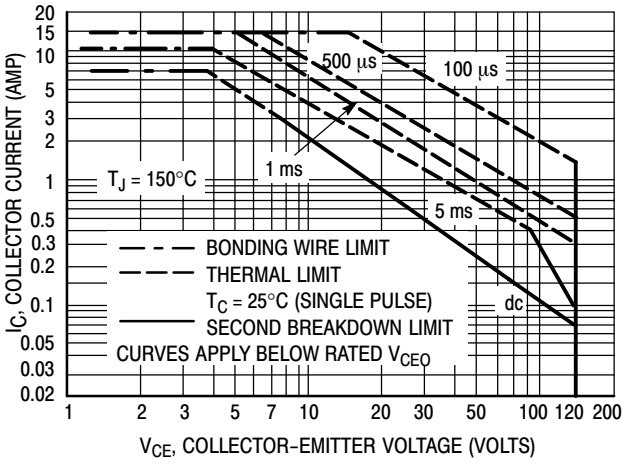


Figure 12. Maximum Forward Bias Safe Operating REA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

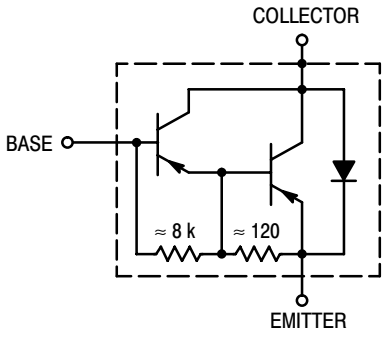
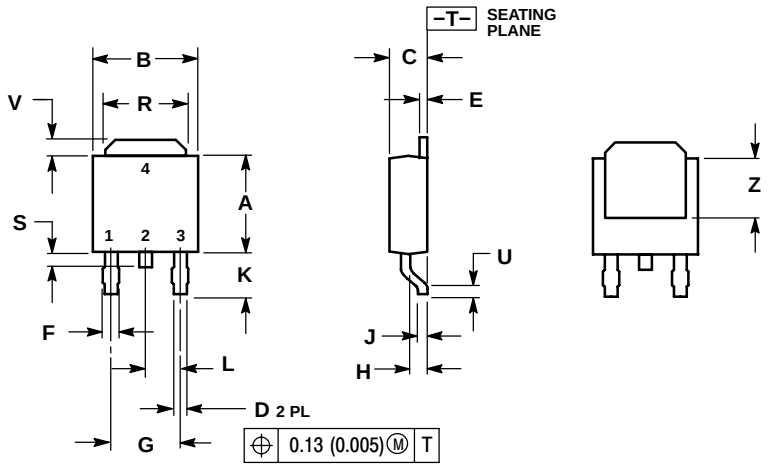


Figure 13. Darlington Schematic

MJD128T4G (PNP)

PACKAGE DIMENSIONS

DPAK
CASE 369C−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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