National Semiconductor

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LM5039

Half-Bridge PWM Controller with Average Current Limit

General Description

The LM5039 Half-Bridge Controller/Gate Driver contains all of the features necessary to implement half-bridge topology power converters using voltage mode control with line voltage feed-forward. The LM5039 is a functional variant of the LM5035B half-bridge PWM controller, featuring average current limit during an overload event to balance the center-point of the half-bridge capacitor divider. The floating high-side gate driver is capable of operating with supply voltages up to 105V. Both the high-side and low-side gate drivers are capable of 2A peak. An internal high voltage startup regulator is included, along with programmable line undervoltage lockout (UVLO). The oscillator is programmed with a single resistor to frequencies up to 2MHz. The oscillator can also be synchronized to an external clock. A current sense input provides peak cycle-by-cycle and average current limit. Other features include adjustable hiccup mode overload protection, soft-start, revision reference, and thermal shutdown.

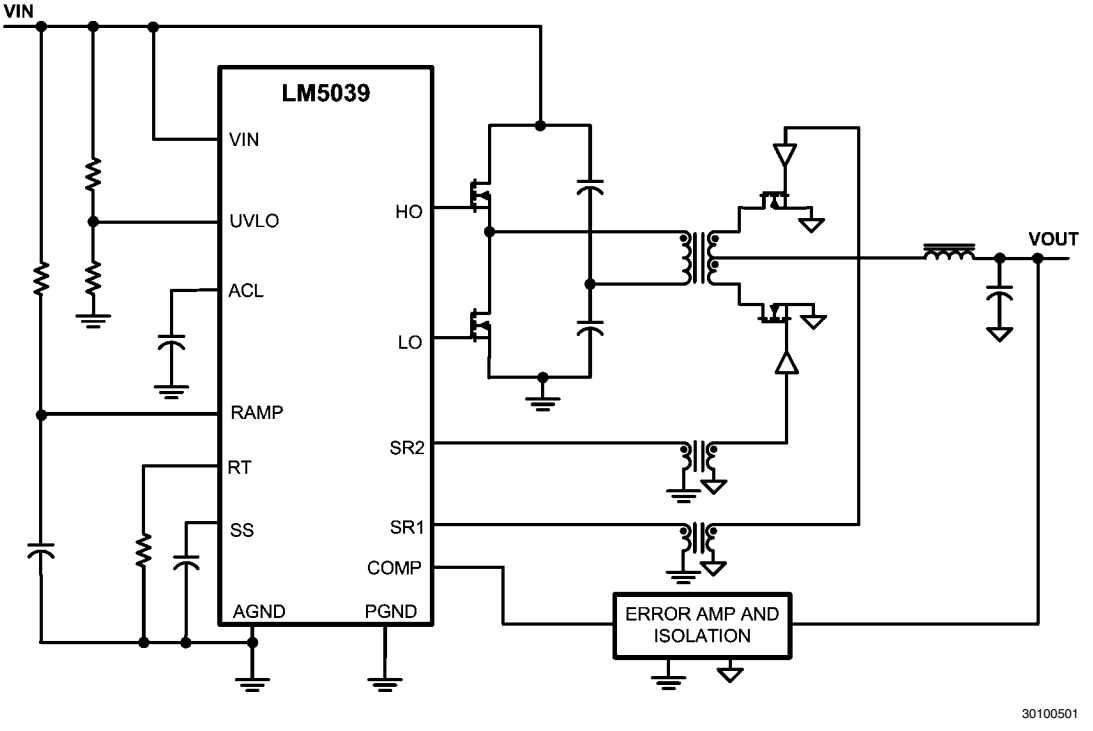
Packages

- TSSOP-20EP (Thermally enhanced)
- LLP-24 (4mm x 5mm) [Coming soon]

Features

- 105V / 2A Half-Bridge Gate Drivers
- Synchronous Rectifier Control Outputs with Programmable Delays
- High Voltage (105V) Start-up Regulator
- Voltage-mode Control with Line Feed-Forward and Volt • Second Limiting
- Programmable average current limit balances the half-bridge capacitor divider voltage in an overload condition
- Programmable hiccup mode timer reduces power dissipation during a continuous overload event
- Adjustable peak cycle-by-cycle over current protection
- Resistor Programmed, 2MHz Capable Oscillator
- Patented Oscillator Synchronization
- Programmable Line Under-Voltage Lockout
- Internal Thermal Shutdown Protection
- Adjustable Soft-Start
- Direct Opto-coupler Interface
- 5V Reference Output

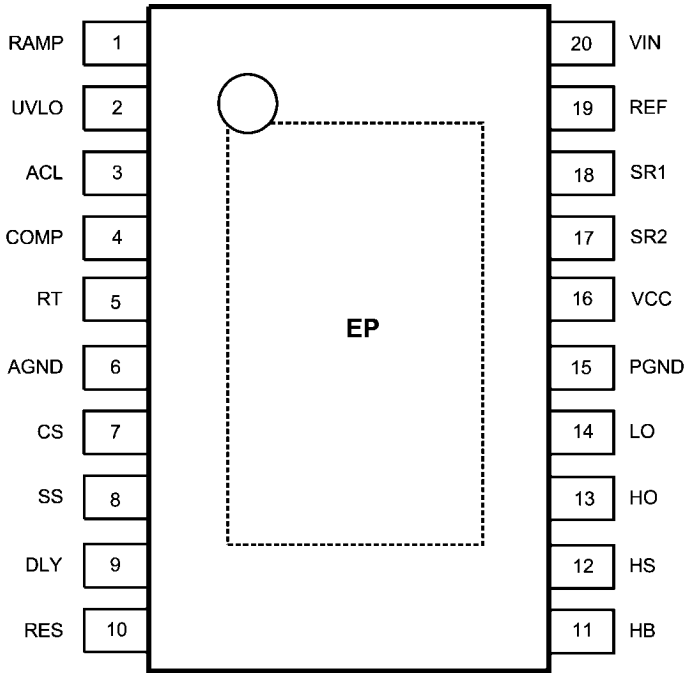
Simplified Application Diagram



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Connection Diagrams

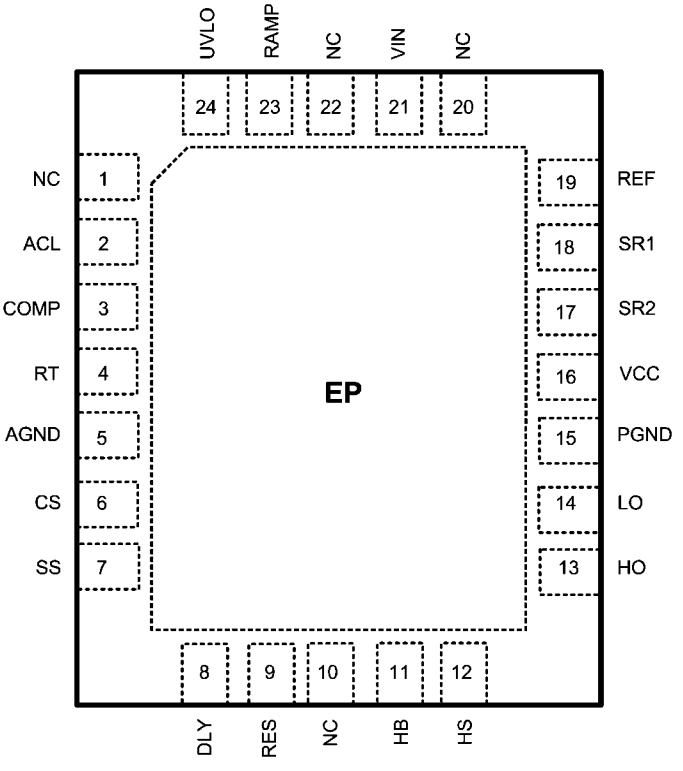
Top View



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20-Lead TSSOP EP

Top View



30100503

LLP-24 Package [Coming soon]

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM5039MH	TSSOP-20EP	MXA20A	73 Units per Rail
LM5039MHX	TSSOP-20EP	MXA20A	2500 Units on Tape and Reel

Pin Descriptions

TSSOP Pin	LLP Pin	Name	Description	Application Information
1	23	RAMP	Modulator ramp signal	An external RC circuit from VIN sets the ramp slope. This pin is discharged at the conclusion of every cycle by an internal FET. Discharge is initiated by either the internal clock or the Volt • Second clamp comparator.
2	24	UVLO	Line Under-Voltage Lockout	An external voltage divider from the power source sets the shutdown and standby comparator levels. When UVLO reaches the 0.4V threshold the VCC and REF regulators are enabled. When UVLO reaches the 1.25V threshold, the SS pin is released and the device enters the active mode. Hysteresis is set by an internal current source that sources 23 µA into the external resistor divider.
3	2	ACL	Average Current Limit	A capacitor connected between the ACL pin and GND operates as an integrator in the average current limit circuitry. The ACL capacitor is charged during current limit condition. As the ACL pin voltage rises, it terminates the cycle through the PWM comparator by pulling down the input of the comparator that is normally controlled through the COMP pin. This maintains equal pulse-widths in both the phases of the half-bridge and thereby maintains balance of the half-bridge capacitor voltages.
4	3	COMP	Input to the Pulse Width Modulator	An external opto-coupler connected to the COMP pin sources current into an internal NPN current mirror. The PWM duty cycle is maximum with zero input current, while 1mA reduces the duty cycle to zero. The current mirror improves the frequency response by reducing the AC voltage across the opto-coupler detector.
5	4	RT	Oscillator Frequency Control and Sync Clock Input.	Normally regulated at 2V. An external resistor connected between RT and AGND sets the internal oscillator frequency. The internal oscillator can be synchronized to an external clock with a frequency higher than the free running frequency set by the RT resistor.
6	5	AGND	Analog Ground	Connect directly to Power Ground.
7	6	CS	Current Sense input for current limit	The CS pin is driven by a signal representative of the primary current. A higher threshold (600mV) comparator is used to implement a fast peak cycle-by-cycle current limit to provide instant protection to the power converter. A lower threshold (500mV) comparator is used to implement a slower average current limit that maintains the balance of the half-bridge capacitor divider voltage. A 50ns blanking time at the CS pin avoids false tripping the current limit comparators due to leading edge transients.
8	7	SS	Soft-start Input	An internal 110µA current source charges an external capacitor to set the soft-start rate. During a current limit restart sequence, the internal current source is reduced to 1.2µA to increase the delay before retry.

TSSOP Pin	LLP Pin	Name	Description	Application Information
9	8	DLY	Timing programming pin for the LO and HO to SR1 and SR2 outputs.	An external resistor to ground sets the timing for the non-overlap time of HO to SR1 and LO to SR2.
10	9	RES	Restart Timer	If the current limit is exceeded during any cycle, a 22µA current is sourced to the RES pin capacitor. If the RES capacitor voltage reaches 2.5V, the soft-start capacitor will be fully discharged and then released with a pull-up current of 1.2µA. After the first output pulse at LO (when SS > COMP offset, typically 1V), the SS pin charging current will revert to 110µA.
11	11	HB	Boost voltage for the HO driver	An external diode is required from VCC to HB and an external capacitor is required from HS to HB to power the HO gate driver.
12	12	HS	Switch node	Connection common to the transformer and both power switches. Provides a return path for the HO gate driver.
13	13	HO	High side gate drive output.	Output of the high side PWM gate driver. Capable of sinking 2A peak current.
14	14	LO	Low side gate drive output.	Output of the low side PWM gate driver. Capable of sinking 2A peak current.
15	15	PGND	Power Ground	Connect directly to Analog Ground.
16	16	VCC	Output of the high voltage start-up regulator. The VCC voltage is regulated to 7.6V.	If an auxiliary winding raises the voltage on this pin above the regulation setpoint, the Start-up Regulator will shutdown, thus reducing the internal power dissipation.
17	17	SR2	Synchronous rectifier driver output.	Control output of the synchronous FET gate. Capable of 0.5A peak current.
18	18	SR1	Synchronous rectifier driver output.	Control output of the synchronous FET gate. Capable of 0.5A peak current.
19	19	REF	Output of 5V Reference	Typical output current is 20mA. Locally decoupled with a 0.1µF capacitor.
20	21	VIN	Input voltage source	Input to the Start-up Regulator. Operating input range is 13V to 100V with transient capability to 105V. For power sources outside of this range, the LM5039 can be biased directly at VCC by an external regulator.
EP	EP	EP	Exposed Pad, underside of package	No electrical contact. Connect to system ground plane for reduced thermal resistance.
	1	NC	No connection	No electrical contact.
	10	NC	No connection	No electrical contact.
	20	NC	No connection	No electrical contact.
	22	NC	No connection	No electrical contact.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN to GND	-0.3V to 105V
HS to GND	-1V to 105V
HB to GND	-0.3V to 118V
HB to HS	-0.3V to 18V
VCC to GND	-0.3V to 16V
CS, RT, DLY, SS, to GND	-0.3V to 5.5V
COMP Input Current	10mA
ACL Input Current	500 µA
All other inputs to GND	-0.3V to 7V
ESD Rating (*Note 4*)	
Human Body Model	2kV
Storage Temperature Range	-65°C to 150°C
Junction Temperature	150°C

Operating Ratings (*Note 1*)

VIN Voltage	13V to 105V
External Voltage Applied to VCC	8V to 15V
Operating Junction Temperature	-40°C to +125°C

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{VIN} = 48V, V_{VCC} = 10V externally applied, R_{RT} = 20.0 kΩ, R_{DLY} = 27.4kΩ, V_{UVLO} = 3V unless otherwise stated. See (*Note 2*) and (*Note 3*).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Startup Regulator (VCC pin)						
V_{VCC}	VCC voltage	I_{VCC} = 10mA	**7.3**	7.6	**7.9**	V
$I_{VCC(LIM)}$	VCC current limit	V_{VCC} = 7V	**57**	65		mA
V_{VCCUV}	VCC Under-voltage threshold (VCC increasing)	VIN = VCC, ΔV_{VCC} from the regulation setpoint	**0.2**	0.1		V
	VCC decreasing	VCC – PGND	**5.5**	6.2	**6.9**	V
I_{VIN}	Startup regulator current	VIN = 90V, UVLO = 0V		35	**70**	µA
	Supply current into VCC from external source	Outputs & COMP open, V_{VCC} = 10V, Outputs Switching		4	**6**	mA
Voltage Reference Regulator (REF pin)						
V_{REF}	REF Voltage	I_{REF} = 0mA	**4.85**	5	**5.15**	V
	REF Voltage Regulation	I_{REF} = 0 to 10mA		25	**50**	mV
	REF Current Limit	REF = 4.5V	**15**	20		mA
Under-Voltage Lock Out and shutdown (UVLO pin)						
V_{UVLO}	Under-voltage threshold		**1.212**	1.25	**1.288**	V
I_{UVLO}	Hysteresis current	UVLO pin sourcing	**19**	23	**27**	µA
	Under-voltage Shutdown Threshold	UVLO voltage falling		0.3		V
	Under-voltage Standby Enable Threshold	UVLO voltage rising		0.4		V
Current Sense Input (CS Pin)						
$V_{CS(th1)}$	Current Limit Threshold for Peak cycle-by-cycle limiting		**0.570**	0.6	**0.630**	V
$V_{CS(th2)}$	Current Limit Threshold for Average current limiting		**0.475**	0.5	**0.525**	V
	CS delay to output (peak cycle-by-cycle only)	CS from zero to 1V. Time for HO and LO to fall to 90% of VCC. Output load = 0 pF.		65		ns
	Leading edge blanking time at CS			50		ns
	CS sink impedance (clocked)	Internal FET on resistance		36	**65**	Ω
Average Current (ACL Pin)						
I_{ACL}	Pull-down sink Impedance			28		Ω
	Source Current	V_{CS} > 0.525	**7.3**	9.3	**11.3**	mA
Current Limit Restart (RES Pin)						
V_{RES}	RES Threshold		**2.4**	2.5	**2.6**	V
	Charge source current	V_{RES} = 1.5V	**16**	22	**28**	µA
	Discharge sink current	V_{RES} = 1V	**8**	12	**16**	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Soft-Start (SS Pin)						
I_{SS}	Charging current in normal operation	V_{SS} = 0	**80**	110	**140**	µA
	Charging current during a hiccup mode restart	V_{SS} = 0	**0.6**	1.2	**1.8**	µA
Oscillator (RT Pin)						
F_{SW1}	Frequency 1(at HO, half oscillator frequency)	R_{RT} = 25 kΩ	**180**	200	**220**	
F_{SW2}	Frequency 2 (at HO, half oscillator frequency)	R_{RT} = 8.76 kΩ	**430**	500	**570**	kHz
$F_{Foldback}$	Foldback frequency in current limit	R_{RT} = 25 kΩ, 0.570<V_{CS} > 0.525 I_{ACL}>35 µA		66.7		kHz
	DC level			2		V
	Input Sync threshold		**2.5**	3	**3.4**	V
PWM Controller (Comp Pin)						
	Delay to output			110		ns
V_{PWM-OS}	SS to RAMP offset		**0.7**	1	**1.2**	V
	Minimum duty cycle	SS = 0V			**0**	%
	Small signal impedance	I_{COMP} = 400µA, COMP current to PWM voltage		6000		Ω
Main Output Drivers (HO and LO Pins)						
	Output high voltage	I_{OUT} = 50mA, V_{HB} - V_{HO}, V_{VCC} - V_{LO}	**0.5**	0.25		V
	Output low voltage	I_{OUT} = 100 mA		0.2	**0.5**	V
	Rise time	C_{LOAD} = 1 nF		15		ns
	Fall time	C_{LOAD} = 1 nF		13		ns
	Peak source current	$V_{HO,LO}$ = 0V, V_{VCC} = 10V		1.25		A
	Peak sink current	$V_{HO,LO}$ = 10V, V_{VCC} = 10V		2		A
	HB Threshold	V_{CC} rising		3.8		V
Voltage Feed-Forward (RAMP Pin)						
	RAMP comparator threshold	COMP current = 0	**2.0**	2.2	**2.4**	V
Synchronous Rectifier Drivers (SR1, SR2)						
	Output high voltage	I_{OUT} = 10mA, V_{VCC} - V_{SR1}, V_{VCC} - V_{SR2}	**0.25**	0.1		V
	Output low voltage	I_{OUT} = 20 mA (sink)		0.07	**0.2**	V
	Rise time	C_{LOAD} = 1 nF		40		ns
	Fall time	C_{LOAD} = 1 nF		20		ns
	Peak source current	V_{SR} = 0, V_{VCC} = 10V		0.5		A
	Peak sink current	V_{SR} = V_{VCC}, V_{VCC} = 10V		0.5		A
T1	Deadtime, SR1 falling to HO rising, SR2 falling to LO rising	R_{DLY} = 10k		33		ns
		R_{DLY} = 27.4k	**65**	88	**118**	ns
		R_{DLY} = 100k		300		ns
T2	Deadtime, HO falling to SR1 rising, LO falling to SR2 rising	R_{DLY} = 10k		12		ns
		R_{DLY} = 27.4k	**20**	29	**42**	ns
		R_{DLY} = 100k		80		ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Thermal Shutdown						
T_{SD}	Shutdown temperature			165		°C
	Hysteresis			20		°C
Thermal Resistance						
θ_{JA}	Junction to ambient, 0 LFPM Air Flow	TSSOP-20_EP package		40		°C/W
θ_{JC}	Junction to Case (EP) Thermal resistance	TSSOP-20_EP package		4		°C/W
θ_{JA}	Junction to ambient, 0 LFM Air Flow	LLP-24 (4 mm x 5 mm)		40		°C/W
θ_{JC}	Junction to Case Thermal resistance	LLP-24 (4 mm x 5 mm)		6		°C/W

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

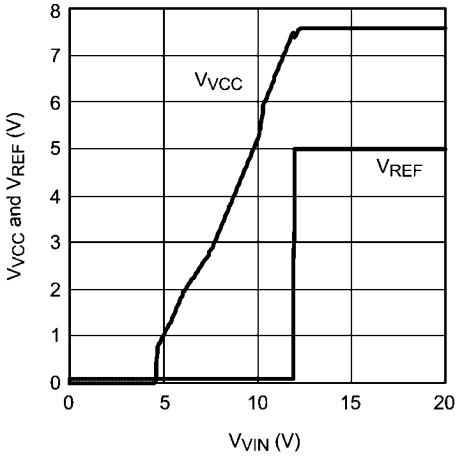
Note 2: All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production with T_A = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 3: Typical specifications represent the most likely parametric norm at 25°C operation

Note 4: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. 2kV for all pins except HB, HO and HS which are rated at 1.5kV.

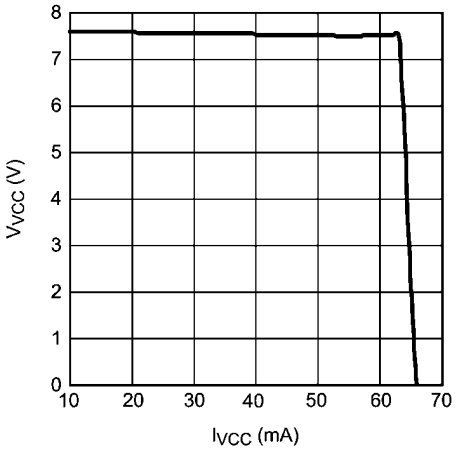
Typical Performance Characteristics

V_{VCC} and V_{REF} vs V_{VIN}



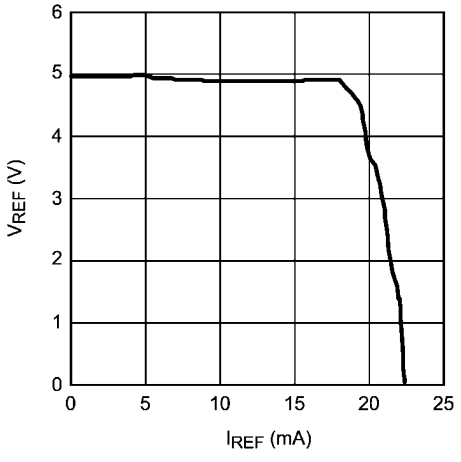
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V_{VCC} vs I_{VCC}



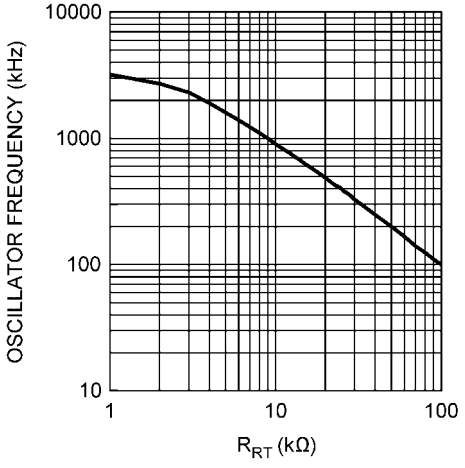
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V_{REF} vs I_{REF}



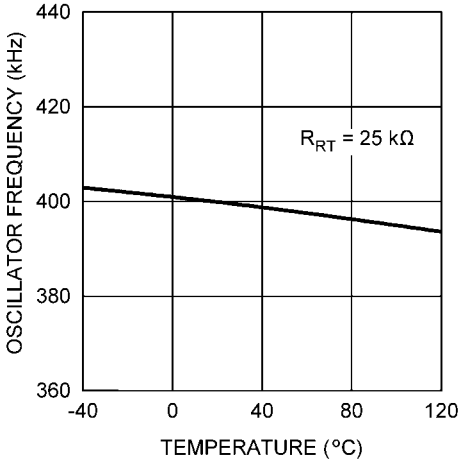
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Oscillator Frequency vs RT



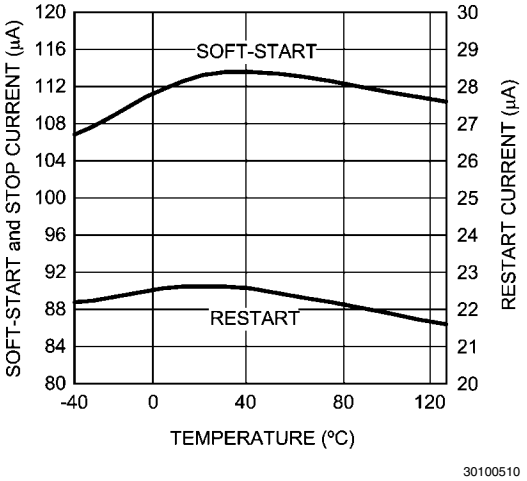
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Oscillator Frequency vs Temperature



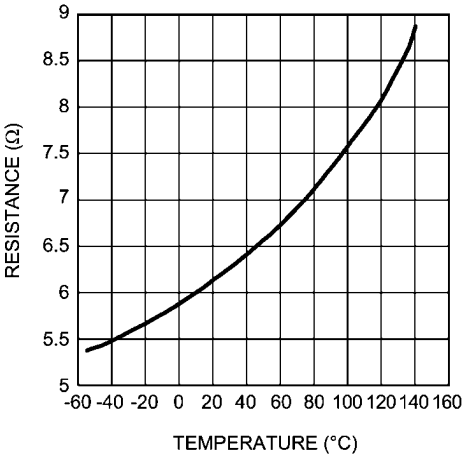
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Soft-Start & Stop Current vs Temperature



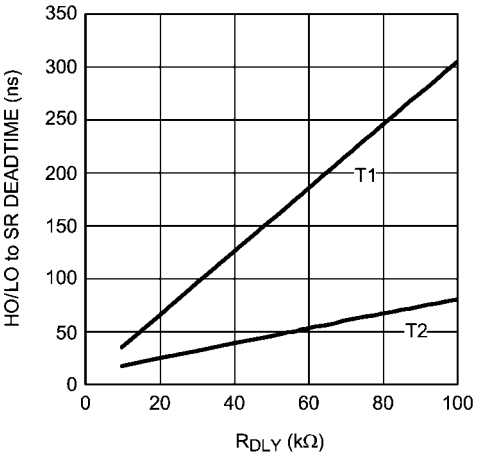
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Effective Comp Input Impedance



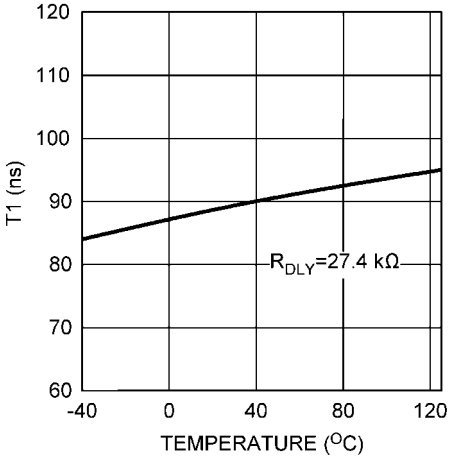
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R_{DLY} vs SR Deadtime



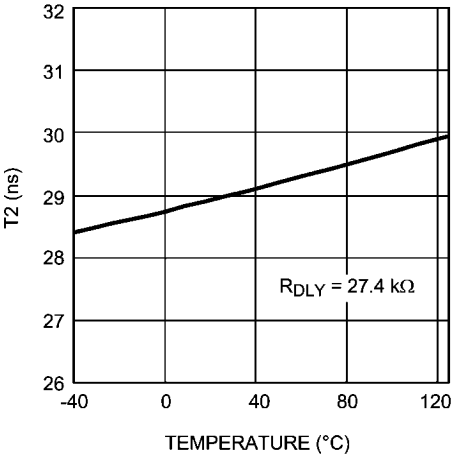
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SR "T1" Parameter vs Temperature



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SR "T2" Parameter vs Temperature



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Block Diagram

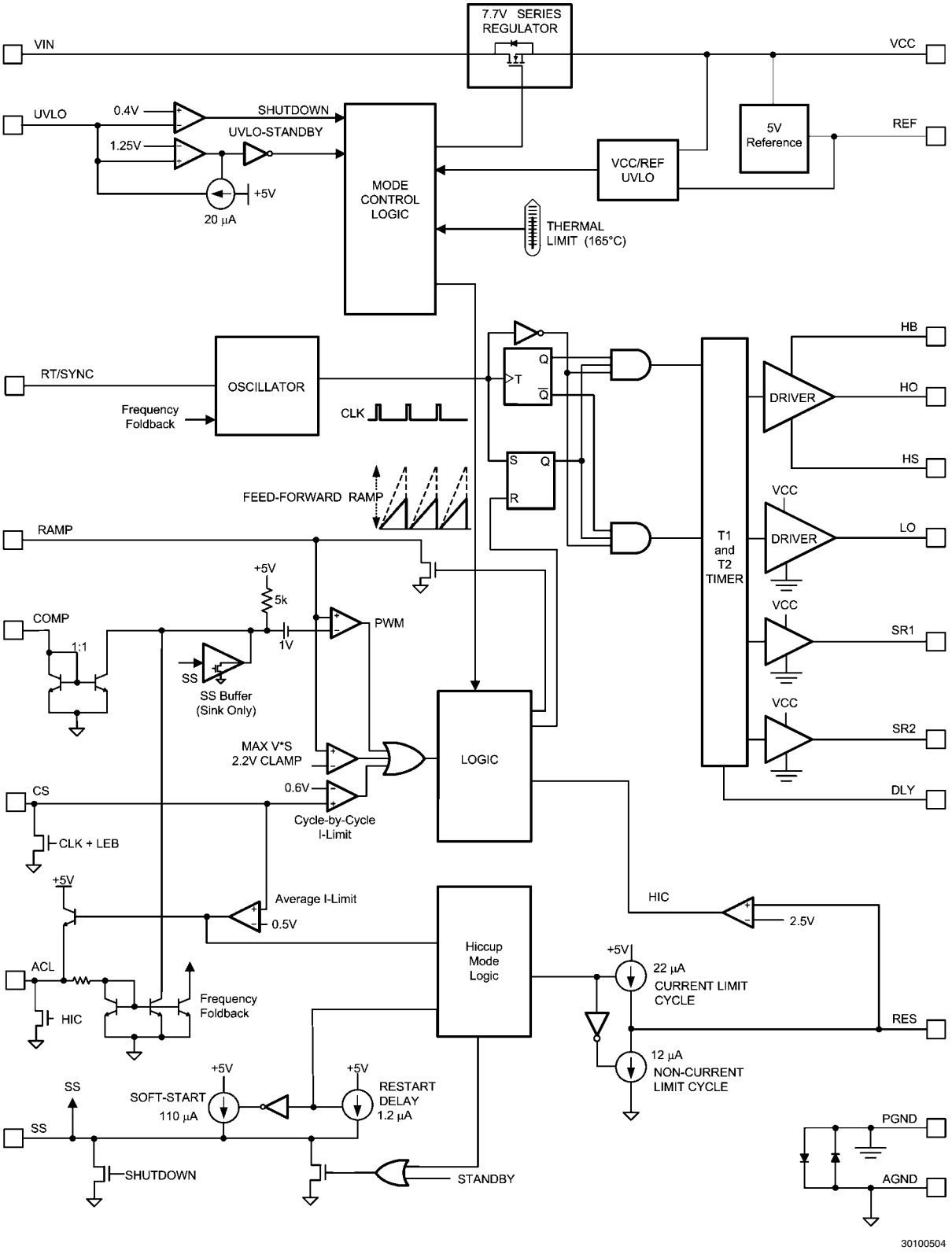


FIGURE 1.

Functional Description

The LM5039 PWM controller contains all of the features necessary to implement half-bridge voltage-mode controlled power converters. The LM5039 provides two gate driver outputs to directly drive the primary side power MOSFETs and two signal level outputs to control secondary synchronous rectifiers through an isolation interface. Secondary side drivers, such as the LM5110, are typically used to provide the necessary gate drive current to control the sync MOSFETs. Synchronous rectification allows higher conversion efficiency and greater power density than conventional PN or Schottky rectifier techniques. The LM5039 can be configured to operate with bias voltages ranging from 8V to 105V. Additional features include line under-voltage lockout, peak cycle-by-cycle current limit, average current limit to balance half-bridge capacitor voltage, voltage feed-forward compensation, hiccup mode fault protection with adjustable delays, soft-start, a 2MHz capable oscillator with synchronization capability, precision reference, thermal shutdown, and programmable volt•second clamping. These features simplify the design of voltage-mode half-bridge DC-DC power converters. The Functional Block Diagram is shown in *Figure 1*.

High-Voltage Start-Up Regulator

The LM5039 contains an internal high voltage start-up regulator that allows the input pin (VIN) to be connected directly to a nominal 48 VDC input voltage. The regulator input can withstand transients up to 105V. The regulator output at VCC (7.6V) is internally current limited to 65mA typical. When the UVLO pin potential is greater than 0.4V, the VCC regulator is enabled to charge an external capacitor connected to the VCC pin. The VCC regulator provides power to the voltage reference (REF) and the output drivers (LO, SR1 and SR2). When the voltage on the VCC pin exceeds the UVLO threshold, the internal voltage reference (REF) reaches its regulation setpoint of 5V and the UVLO voltage is greater than 1.25V, the controller outputs are enabled. The value of the VCC capacitor depends on the total system design, and its start-up characteristics. The recommended range of values for the VCC capacitor is 0.1 µF to 100 µF.

The VCC under-voltage comparator threshold is lowered to 6.2V (typical) after VCC reaches the regulation set-point. If VCC falls below this value, the outputs are disabled, and the soft-start capacitor is discharged. If VCC increases above 7.6V, the outputs will be enabled and a soft-start sequence will commence.

The internal power dissipation of the LM5039 can be reduced by powering VCC from an external supply. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8.3V to shut off the internal start-up regulator. Powering VCC from an auxiliary winding improves efficiency while reducing the controller's power dissipation. The under-voltage comparator circuit will still function in this mode, requiring that VCC never falls below 6.2V during the start-up sequence.

During a fault mode, when the converter auxiliary winding is inactive, external current drawn on the VCC line should be limited such that the power dissipated in the start-up regulator does not exceed the maximum power dissipation of the IC package.

An external DC bias voltage can be used instead of the internal regulator by connecting the external bias voltage to both the VCC and the VIN pins. The external bias must be greater than 8.3V to exceed the VCC UVLO threshold and less than the VCC maximum operating voltage rating (15V).

Line Under-Voltage Detector

The LM5039 contains a dual level Under-Voltage Lockout (UVLO) circuit. When the UVLO pin voltage is below 0.4V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.4V but less than 1.25V, the controller is in standby mode. In standby mode the VCC and REF bias regulators are active while the controller outputs are disabled. When the VCC and REF outputs exceed the VCC and REF under-voltage thresholds and the UVLO pin voltage is greater than 1.25V, the outputs are enabled and normal operation begins. An external set-point voltage divider from VIN to GND can be used to set the minimum operating voltage of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 1.25V when VIN enters the desired operating range. UVLO hysteresis is accomplished with an internal 23 µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 1.25V threshold, the current source is deactivated. The hysteresis of the 0.4V shutdown comparator is internally fixed at 100 mV.

The UVLO pin can also be used to implement various remote enable / disable functions. See the Soft Start section for more details.

Reference

The REF pin is the output of a 5V linear regulator that can be used to bias an opto-coupler transistor and external housekeeping circuits. The regulator output is internally current limited to 20mA (typical).

Current Limit

The LM5039 utilizes two high-speed comparators to implement a current limiting in an overload condition: A higher threshold (600mV) comparator is used to implement a fast peak cycle-by-cycle current limit to provide instantaneous protection to the power converter and a lower threshold (500mV) comparator is used to implement a slower average current limit that balances the half-bridge capacitor divider voltage. During an overload event, average current limit scheme allows the power converter to act as a constant current source with the duty cycle maintained such that the average output current is:

$$I_{OUT} = \left(\frac{N_{PRI}}{N_{SEC}}\right) \times \frac{500\ mV}{Rcs} \times CT_{Turns}$$

This scheme is often known as “brickwall” current limiting or constant current limiting and its response is same whether the load is a soft-short or a hard-short. Typically, in an overload condition, the PWM cycle is terminated by the peak cycle-by-cycle comparator instead of the PWM comparator. This is similar to peak current mode control, which inherently results in an on-time imbalance between the two phases of a half-bridge topology. Any such imbalance, for an extended period of time, will cause the voltage at the center point of the capacitor divider to drift either towards the input voltage or ground. However, in an average current limit scheme, the PWM cycle is terminated through the PWM comparator, by pulling down the PWM control input. Because of its averaging nature, the PWM control voltage is essentially held at a constant dc voltage. Therefore, the on-time of successive PWM cycles are equal, thus maintaining balance of the center-point of the capacitor divider.

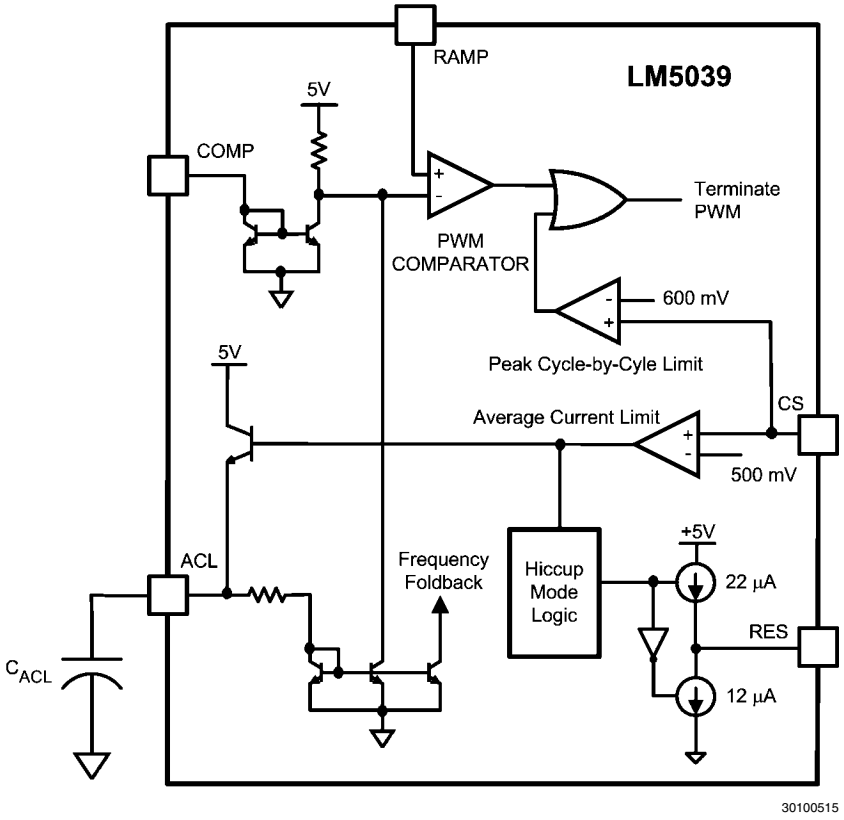


FIGURE 2. Peak Cycle-by-Cycle and Average Current Limit Circuitry

The CS pin is driven by a signal representative of the primary current. During a continuous overload event, the 500mV comparator sources pulses of current into the average current limit pin (ACL). A capacitor connected to the ACL pin smooths and averages the pulses. When the ACL capacitor is charged to approximately 2V, it starts pulling down the PWM comparator input via the current mirror shown in *Figure 2*. As the overload event persists, the ACL takes control of the duty cycle through the PWM comparator, instead of peak cycle-by-cycle control. The average current limiting can be disabled by shorting the ACL pin to GND.

A small R-C filter connect to the CS pin and located near the controller is recommended to suppress noise. An internal 36Ω MOSFET connected to the CS input discharges the external current sense filter capacitor at the conclusion of every cycle. The discharge MOSFET remains on for an additional 50 ns after the HO or LO driver switches high to blank leading edge transients in the current sensing circuit. Discharging the CS pin filter each cycle and blanking leading edge spikes reduces the filtering requirements and improves the current sense response time.

Frequency Foldback

Ideally, a power converter will have the characteristics of a constant current source while operating in current limit. In reality, the current limit level tends to increase as the output voltage decreases. In a hard-short condition, avoiding an increase of the average output current requires extremely low duty cycles. However, the minimum achievable on-time is limited due to propagation and turn-off delays. In a fixed frequency converter, the peak output inductor current creeps up during the minimum on-time and does not have enough off-time to come back down. Therefore, the average output current increases. The propagation delay of the LM5039 has been optimized to about 50ns and the turn-off time mainly depends on the total gate charge of the external power FET.

To avoid the output current tail when the power converter is in average current limit, the LM5039 oscillator frequency is proportionally decreased. In a hard-short condition, the oscillator frequency is reduced to 1/3rd the oscillator frequency set by the RT resistor. The frequency foldback is implemented only in the average current limit condition. and it does not affect the ac response of the control loop.

Overload Protection Timer

The LM5039 provides a current limit restart timer to disable the outputs and force a delayed restart (hiccup mode) if a current limit condition is repeatedly sensed. The number of current limit events required to trigger the restart is programmable by the external capacitor at the RES pin. During each PWM cycle, the LM5039 either sources or sinks current from the RES pin capacitor. If no current limit is detected during a cycle, an 12 µA discharge current sink is enabled to pull the RES pin to ground. If a current limit is detected, the 12 µA sink current is disabled and a 22µA current source causes the voltage at the RES pin to gradually increase. The LM5039 protects the converter with peak cycle-by-cycle and average current limiting while the voltage at RES pin increases. If the RES voltage reaches the 2.5V threshold, the following restart sequence occurs:

- The RES, ACL and SS capacitors are fully discharged
- The soft-start current source is reduced from 110 µA to 1.2 µA
- The SS capacitor voltage slowly increases. When the SS voltage reaches ≅1V, the PWM comparator will produce the first narrow output pulse. After the first pulse occurs, the SS source current reverts to the normal 110 µA level. The SS voltage increases at its normal rate, gradually increasing the duty cycle of the output drivers
- If the overload condition persists after restart, peak cycle-by-cycle and average current limiting will begin to increase the voltage on the RES capacitor again, repeating the hiccup mode sequence
- If the overload condition no longer exists after restart, the RES pin will be held at ground by the 12 µA current sink and normal operation resumes. Restart timer is initiated as the signal at CS pin crosses 500mV and works the same if the controller is in average current limit mode or pure peak cycle-by-cycle current limiting.

The overload timer function is very versatile and can be configured for the following modes of protection:

1. Continuous Current limit only: The hiccup mode can be completely disabled by connecting a zero to 50 kΩ resistor from the RES pin to AGND. In this configuration, the peak cycle-by-cycle/average current-limit protection will limit the output current indefinitely and no hiccup sequences will occur.

2. Hiccup only: The timer can be configured for immediate activation of a hiccup sequence upon detection of an overload by leaving the RES pin open circuit.

3. Delayed Hiccup: Connecting a capacitor to the RES pin provides a programmed interval of peak cycle-by-cycle and average current limiting before initiating a hiccup mode restart, as previously described. The dual advantages of this configuration are that a short term overload will not cause a hiccup mode restart but during extended overload conditions, the average dissipation of the power converter will be very low.

4. Externally Controlled Hiccup: The RES pin can also be used as an input. By externally driving the pin to a level greater than the 2.5V hiccup threshold, the controller will be forced into the delayed restart sequence. For example, the external trigger for a delayed restart sequence could come from an over-temperature protection circuit or an output overvoltage sensor.

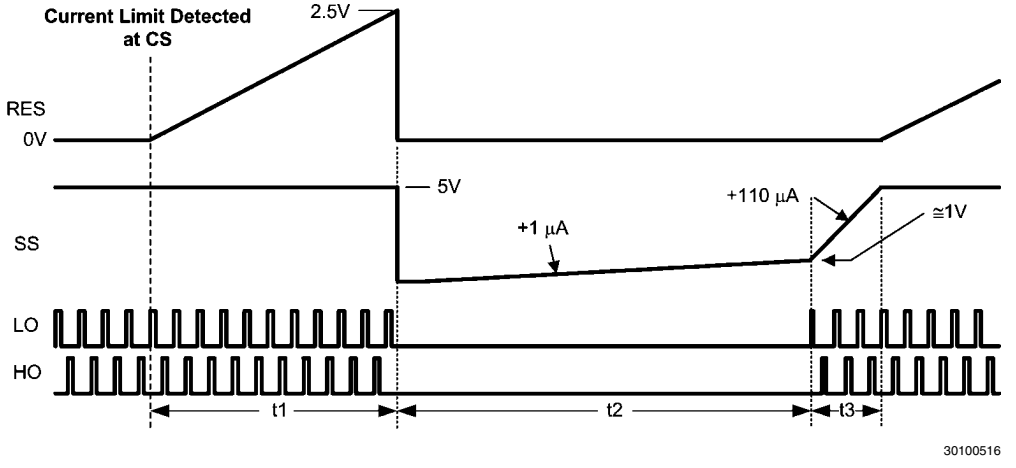


FIGURE 3. Current Limit Restart Timing

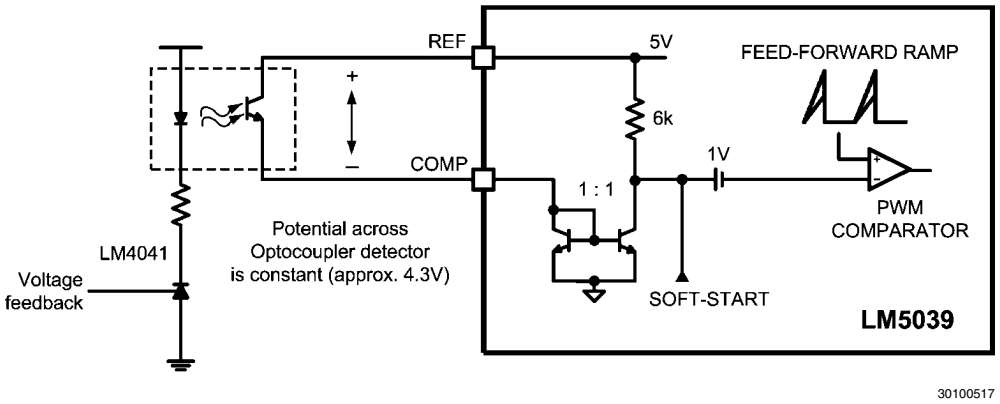


FIGURE 4. Optocoupler to COMP Interface

Soft-Start

The soft-start circuit allows the regulator to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. When bias is supplied to the LM5039, the SS pin capacitor is discharged by an internal MOSFET. When the UVLO, VCC and REF pins reach their operating thresholds, the SS capacitor is released and charged with a 110 µA current source. The PWM comparator control voltage is clamped to the SS pin voltage by an internal amplifier. When the PWM comparator input reaches 1V, output pulses commence with slowly increasing duty cycle. The voltage at the SS pin eventually increases to 5V, while the voltage at the PWM comparator increases to the value required for regulation as determined by the voltage feedback loop.

One method to shutdown the regulator is to ground the SS pin. This forces the internal PWM control signal to ground, reducing the output duty cycle quickly to zero. Releasing the SS pin begins a soft-start cycle and normal operation resumes. A second shutdown method is discussed in the UVLO section.

PWM Comparator

The pulse width modulation (PWM) comparator compares the voltage ramp signal at the RAMP pin to the loop error signal. This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The loop error signal is received from the external feedback and isolation circuit is in the form of a control current into the COMP pin. The COMP pin current is internally mirrored by a matched pair of NPN transistors which sink current through a 5 kΩ resistor connected to the 5V reference. The resulting control voltage passes through a 1V level shift before being applied to the PWM comparator.

An opto-coupler detector can be connected between the REF pin and the COMP pin. Because the COMP pin is controlled by a current input, the potential difference across the opto-coupler detector is nearly constant. The bandwidth limiting phase delay which is normally introduced by the significant capacitance of the opto-coupler is thereby greatly reduced. Higher loop bandwidths can be realized since the bandwidth-limiting pole associated with the opto-coupler is now at a much higher frequency. The PWM comparator polarity is configured such that with no current into the COMP pin, the controller produces the maximum duty cycle at the main gate driver outputs, HO and LO.

Feed-Forward Ramp and Volt • Second Clamp

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to VIN, AGND, and the RAMP pin are required to create the PWM ramp signal. The slope of the signal at RAMP will vary in proportion to the input line voltage. This varying slope provides line feed-forward information necessary to improve line transient response with voltage mode control. The RAMP signal is compared to the error signal by the pulse width modulator comparator to control the duty cycle of the HO and LO outputs. With a constant error signal, the on-time (T_{ON}) varies inversely with the input voltage (VIN) to stabilize the Volt • Second product of the transformer primary signal. The power path gain of conventional voltage-mode pulse width modulators (oscillator generated ramp) varies directly with input voltage. The use of a line generated ramp (input voltage feed-forward) nearly eliminates this gain variation. As a result, the feedback loop is only required to make very small corrections for large changes in input voltage.

In addition to the PWM comparator, a Volt • Second Clamp comparator also monitors the RAMP pin. If the ramp amplitude exceeds the 2.2V threshold of the Volt • Second Clamp comparator, the on-time is terminated. The C_{FF} ramp capacitor is discharged by an internal 32Ω discharge MOSFET controlled by the V•S Clamp comparator. If the RAMP signal does not exceed 2.2V before the end of the clock period, then the internal clock will enable the discharge MOSFET to reset capacitor C_{FF}.

By proper selection of R_{FF} and C_{FF} values, the maximum on-time of HO and LO can be set to the desired duration. The on-time set by the Volt • Second Clamp varies inversely to the line voltage because the RAMP capacitor is charged by a resistor (R_{FF}) connected to VIN while the threshold of the clamp is a fixed voltage (2.2V). An example will illustrate the use of the Volt • Second Clamp comparator to achieve a 50% duty cycle limit at 200kHz with a 48V line input. A 50% duty cycle at a 200kHz requires a 2.5µs on-time. To achieve this maximum on-time clamp level:

$$R_{FF} \times C_{FF} = \frac{T_{ON} + 10\%}{\ln\left[\left(1 - \frac{2.2V}{VIN}\right)^{-1}\right]} = \frac{2.5\ \mu s + 0.25\ \mu s}{\ln\left[\left(1 - \frac{2.2V}{48V}\right)^{-1}\right]} = 58.6\ \mu s$$

The recommended capacitor value range for C_{FF} is 100 pF to 1000 pF. 470 pF is a standard value that can be paired with

an 124 kΩ to approximate the desired 58.6µs time constant. If load transient response is slowed by the 10% margin, the R_{FF} value can be increased. The system signal-to-noise will be slightly decreased by increasing R_{FF} x C_{FF}.

Oscillator, Sync Capability

The LM5039 oscillator frequency is set by a single external resistor connected between the RT and AGND pins. To set a desired oscillator frequency, the necessary RT resistor is calculated from:

$$RT = \left(\frac{1}{F_{OSC}}\right) \times 10 \times 10^{9}$$

For example, if the desired oscillator frequency is 400kHz (HO and LO each switching at 200 kHz) a 24.9kΩ resistor would be the nearest standard one percent value.

Each output (HO, LO, SR1 and SR2) switches at half the oscillator frequency. The voltage at the RT pin is internally regulated to a nominal 2V. The RT resistor should be located as close as possible to the IC, and connected directly to the pins (RT and AGND). The tolerance of the external resistor, and the frequency tolerance indicated in the Electrical Characteristics, must be taken into account when determining the worst case frequency range.

The LM5039 can be synchronized to an external clock by applying a narrow pulse to the RT pin. The external clock must be at least 10% higher than the free-running oscillator frequency set by the RT resistor. If the external clock frequency is less than the RT resistor programmed frequency, the LM5039 will ignore the synchronizing pulses. The synchronization pulse width at the RT pin must range between 15ns to 150ns. The clock signal should be coupled into the RT pin through a 100 pF capacitor. When the synchronizing pulse transitions low-to-high (rising edge), the voltage at the RT pin must be driven to exceed 3.2V volts from its nominal 2 VDC level. During the clock signal's low time, the voltage at the RT pin will be clamped at 2 VDC by an internal regulator. The output impedance of the RT regulator is approximately 100Ω. The RT resistor is always required, whether the oscillator is free running or externally synchronized.

Gate Driver Outputs (HO & LO)

The LM5039 provides two alternating gate driver outputs, the floating high side gate driver HO and the ground referenced low side driver LO. Each driver is capable of sourcing 1.25A and sinking 2A peak. The HO and LO outputs operate in an alternating manner, at one-half the internal oscillator frequency. The LO driver is powered directly by the VCC regulator. The HO gate driver is powered from a bootstrap capacitor connected between HB and HS. An external diode connected between VCC (anode pin) and HB (cathode pin) provides the high side gate driver power by charging the bootstrap capacitor from VCC when the switch node (HS pin) is low. When the high side MOSFET is turned on, HB rises to a peak voltage equal to $V_{VCC} + V_{HS}$ where V_{HS} is the switch node voltage.

The HB and VCC capacitors should be placed close to the pins of the LM5039 to minimize voltage transients due to parasitic inductances since the peak current sourced to the MOSFET gates can exceed 1.25A. The recommended value of the HB capacitor is 0.01 µF or greater. A low ESR / ESL capacitor, such as a surface mount ceramic, should be used to prevent voltage droop during the HO transitions.

The maximum duty cycle for each output is equal to or slightly less than 50% due to a programmed sync rectifier delay. The programmed sync rectifier delay is determined by the DLY pin resistor. If the COMP pin is open circuit, the outputs will operate at maximum duty cycle. The maximum duty cycle for each output can be calculated with the following equation:

$$\text{Maximum Duty Cycle} = \frac{\frac{1}{2}T_S - T1}{T_S}$$

Where T_S is the period of one complete cycle for either the HO or LO outputs, T1 is the programmed sync rectifier delay. For example, if the oscillator frequency is 200 kHz, each output will cycle at 100 kHz (T_S = 10 µs). Using no programmed delay, the maximum duty cycle at this frequency is calculated to be 50%. Using a programmed sync rectifier delay of 100 ns, the maximum duty cycle is reduced to 49%. Because there is no fixed deadtime in LM5039, it is recommended that the delay pin resistor be not less than 10k. Internal delays, which are not guaranteed, are the only protection against cross conduction if the programmed delay is zero, or very small.

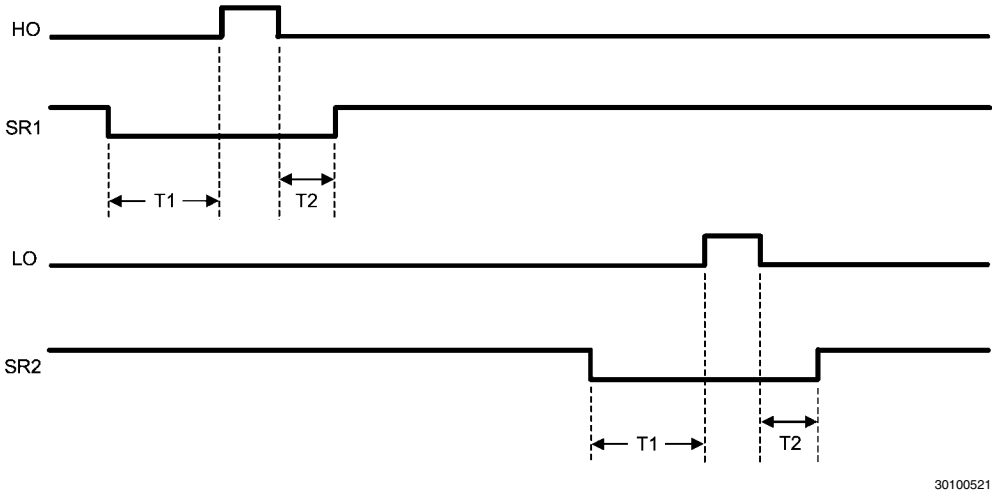


FIGURE 5. HO, LO, SR1 and SR2 Timing Diagram

Synchronous Rectifier Control Outputs (SR1 & SR2)

Synchronous rectification (SR) of the transformer secondary provides higher efficiency, especially for low output voltage converters. The reduction of rectifier forward voltage drop (0.5V - 1.5V) to 10mV - 200mV V_{DS} voltage for a MOSFET significantly reduces rectification losses. In a typical application, the transformer secondary winding is center tapped, with the output power inductor in series with the center tap. The SR MOSFETs provide the ground path for the energized secondary winding and the inductor current. *Figure 5* shows that the SR2 MOSFET is conducting while HO enables power transfer from the primary. The SR1 MOSFET must be disabled during this period since the secondary winding connected to the SR1 MOSFET drain is twice the voltage of the center tap. At the conclusion of the HO pulse, the inductor current continues to flow through the SR1 MOSFET body diode. Since the body diode causes more loss than the SR MOSFET, efficiency can be improved by minimizing the T2 period while maintaining sufficient timing margin over all conditions (component tolerances, etc.) to prevent shoot-through current. When LO enables power transfer from the primary, the SR1 MOSFET is enabled and the SR2 MOSFET is off.

During the time that neither HO nor LO is active, the inductor current is shared between both the SR1 and SR2 MOSFETs which effectively shorts the transformer secondary and cancels the inductance in the windings. The SR2 MOSFET is disabled before LO delivers power to the secondary to prevent power being shunted to ground. The SR2 MOSFET body diode continues to carry about half the inductor current until the primary power raises the SR2 MOSFET drain voltage and reverse biases the body diode. Ideally, deadtime T1 would be set to the minimum time that allows the SR MOSFET to turn off before the SR MOSFET body diode starts conducting.

The SR1 and SR2 outputs are powered directly by the VCC regulator. Each output is capable of sourcing and sinking 0.5A peak. Typically, the SR1 and SR2 signals control SR MOSFET gate drivers through a pulse transformer. The actual gate sourcing and sinking currents are provided by the secondary-side bias supply and gate drivers.

The timing of SR1 and SR2 with respect to HO and LO is shown in *Figure 5*. SR1 is configured out of phase with HO and SR2 is configured out of phase with LO. The deadtime between transitions is programmable by a resistor connected from the DLY pin to the AGND pin. Typically, R_{DLY} is set in the range of 10kΩ to 100kΩ. The deadtime periods can be calculated using the following formulae:

$$T1 = .003 \times R_{DLY} + 4.6 \text{ ns}$$

$$T2 = .0007 \times R_{DLY} + 10.01 \text{ ns}$$

When UVLO falls below 1.25V, or during hiccup current limit, both SR1 and SR2 are held low. During normal operation if soft-start is held low, both SR1 and SR2 will be high.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum rated junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state with the output drivers (HO, LO, SR1 and SR2), the bias regulators (VCC and REF) disabled. This helps to prevent catastrophic failures from accidental device overheating. During thermal shutdown, the soft-start capacitor is fully discharged and the controller follows a normal start-up sequence after the junction temperature falls to the operating level (145°C).

Applications Information

The following information is intended to provide guidelines for the power supply designer using the LM5039.

VIN

The voltage applied to the VIN pin, which may be the same as the system voltage applied to the power transformer's primary (V_{PWR}), can vary in the range of 13 to 105V. The current into VIN depends primarily on the gate charge provided to the output drivers, the switching frequency, and any external loads on the VCC and REF pins. It is recommended that the filter shown in *Figure 6* be used to suppress transients which may occur at the input supply. This is particularly important when VIN is operated close to the maximum operating rating of the LM5039.

When power is applied to VIN and the UVLO pin voltage is greater than 0.4V, the VCC regulator is enabled and supplies current into an external capacitor connected to the VCC pin. When the voltage on the VCC pin reaches the regulation point of 7.6V, the voltage reference (REF) is enabled. The reference regulation set point is 5V. The HO, LO, SR1 and SR2 outputs are enabled when the two bias regulators reach their set point and the UVLO pin potential is greater than 1.25V. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8.3V to shut off the internal start-up regulator.

After the outputs are enabled and the external VCC supply voltage has begun supplying power to the IC, the current into VIN drops below 1 mA. VIN should remain at a voltage equal to or above the VCC voltage to avoid reverse current through protection diodes.

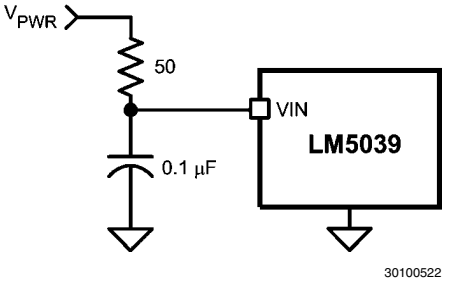


FIGURE 6. Input Transient Protection

FOR APPLICATIONS >100V

For applications where the system input voltage exceeds 100V or the IC power dissipation is of concern, the LM5039 can be powered from an external start-up regulator as shown in *Figure 7*. In this configuration, the VIN and the VCC pins should be connected together, which allows the LM5039 to be operated below 13V. The voltage at the VCC pin must be greater than 8.3V yet not exceed 15V. An auxiliary winding can be used to reduce the power dissipation in the external regulator once the power converter is active. The NPN base-emitter reverse breakdown voltage, which can be as low as 5V for some transistors, should be considered when selecting the transistor.

CURRENT SENSE

The CS pin needs to receive an input signal representative of the transformer's primary current, either from a current sense transformer or from a resistor in series with the source of the LO switch, as shown in *Figure 8* and *Figure 9*. In both cases, the sensed current creates a ramping voltage across R1, and the R_F/C_F filter suppresses noise and transients. R1, R_F and C_F should be located as close to the LM5039 as possible, and the ground connection from the current sense transformer, or R1, should be a dedicated track to the AGND pin. The current sense components must provide greater than 0.6V (typ) at the CS pin when an over-current condition exists.

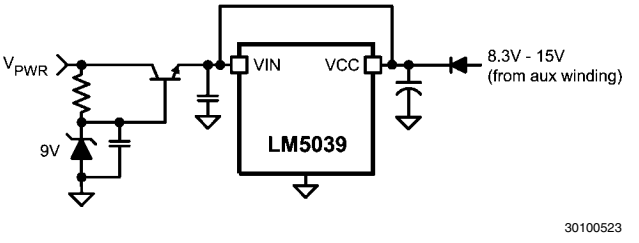


FIGURE 7. Start-up Regulator for V_{PWR} >100V

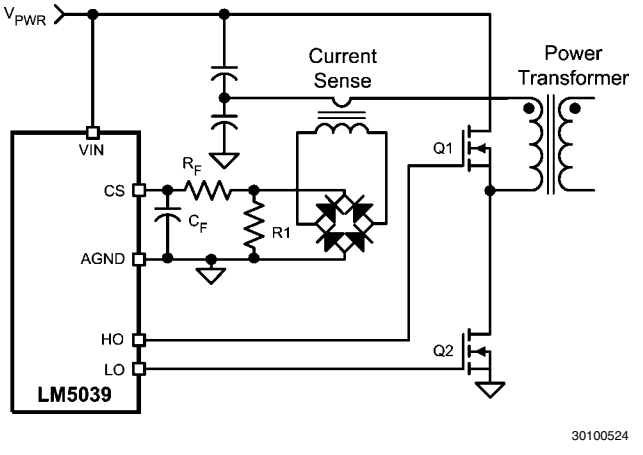


FIGURE 8. Current Sense Using Current Sense Transformer

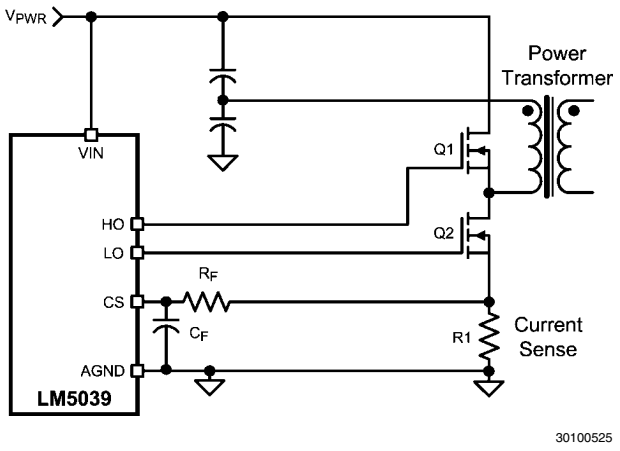


FIGURE 9. Current Sense Using Current Sense Resistor (R1)

If the current sense resistor method is used, the over-current condition will only be sensed while LO is driving the low-side MOSFET. Over-current while HO is driving the high-side MOSFET will not be detected. In this configuration, it will take 4 times as long to initiate a restart event since each over-current event during LO enables the 22µA RES pin current source for one oscillator period, and then the lack of an over-current event during HO enables the 12µA RES pin current sink for one oscillator period. The value of the RES capacitor can be reduced to decrease the time before restart cycle is initiated.

When using the resistor current sense method, an imbalance in the input capacitor voltages may develop when operating in peak cycle-by-cycle current limiting mode. If the imbalance persists for an extended period, excessive currents in the non-sensed MOSFET, and possible transformer saturation may result. This condition is inherent to the half-bridge topology operated with peak cycle-by-cycle current limiting and is compounded by only sensing in one leg of the half-bridge circuit. The imbalance is greatest at large duty cycles (low input voltages). It is recommended to activate average current limit circuitry in such a configuration. However, since only alternative cycles source current into the ACL capacitor, ACL capacitor needs to be halved. This could still lead to a slight imbalance depending upon the input/output voltage levels and the impedance mismatch between the two phases of the half-bridge due to the additional CS resistor in the bottom half.

HO, HB, HS and LO

Attention must be given to the PC board layout for the low-side driver and the floating high-side driver pins HO, HB and HS. A low ESR/ESL capacitor (such as a ceramic surface mount capacitor) should be connected close to the LM5039, between HB and HS to provide high peak currents during turn-on of the high-side MOSFET. The capacitor should be large enough to supply the MOSFET gate charge (Qg) without discharging to the point where the drop in gate voltage affects the MOSFET $R_{DS(ON)}$. A value ten to twenty times Qg is recommended.

$$C_{BOOST} = 20 \times \frac{Q_g}{VCC}$$

The diode (D_{BOOST}) that charges C_{BOOST} from VCC when the low-side MOSFET is conducting should be capable of withstanding the full converter input voltage range. When the high-side MOSFET is conducting, the reverse voltage at the diode is approximately the same as the MOSFET drain voltage because the high-side driver is boosted up to the converter input voltage by the HS pin, and the high side MOSFET gate is driven to the HS voltage plus VCC. Since the anode of D_{BOOST} is connected to VCC, the reverse potential across the diode is equal to the input voltage minus the VCC voltage. D_{BOOST} average current is less than 20mA in most applications, so a low current ultra-fast recovery diode is recommended to limit the loss due to diode junction capacitance. Schottky diodes are also a viable option, particularly for lower input voltage applications, but attention must be paid to leakage currents at high temperatures.

The internal gate drivers need a very low impedance path to the respective decoupling capacitors; the VCC cap for the LO driver and C_{BOOST} for the HO driver. These connections should be as short as possible to reduce inductance and as wide as possible to reduce resistance. The loop area, defined by the gate connection and its respective return path, should be minimized.

The high-side gate driver can also be used with HS connected to PGND for applications other than a half bridge converter (e.g. Push-Pull). The HB pin is then connected to VCC, or any supply greater than the high-side driver undervoltage lockout (approximately 6.5V). In addition, the high-side driver can be configured for high voltage offline applications where the high-side MOSFET gate is driven via a gate drive transformer.

PROGRAMMABLE DELAY (DLY)

The R_{DLY} resistor programs the delays between the SR1 and SR2 signals and the HO and LO driver outputs. *Figure 5* shows the relationship between these outputs. The DLY pin is nominally set at 2.5V and the current is sensed through R_{DLY} to ground. This current is used to adjust the amount of deadtime before the HO and LO pulse (T1) and after the HO and LO pulse (T2). Typically R_{DLY} is in the range of 10kΩ to 100kΩ. The deadtime periods can be calculated using the following formulae:

$$T1 = .003 \times R_{DLY} + 4.6 \text{ ns}$$

$$T2 = .0007 \times R_{DLY} + 10.01 \text{ ns}$$

It is recommended that the delay resistor be not less than 10K. If the programmed delay is zero, it can either short the secondary, or potentially result in cross-conduction in the primary, or both. Should an SR MOSFET remain on while the opposing primary MOSFET is supplying power through the power transformer, the secondary winding will experience a momentary short circuit, causing a significant power loss to occur.

When choosing the R_{DLY} value, worst case propagation delays and component tolerances should be considered to assure that there is never a time where both SR MOSFETs are enabled AND one of the primary side MOSFETs is enabled. The time period T1 should be set so that the SR MOSFET has turned off before the primary MOSFET is enabled. Conversely, T1 and T2 should be kept as low as tolerances allow to optimize efficiency. The SR body diode conducts during the time between the SR MOSFET turns off and the power transformer begins supplying energy. Power losses increase when this happens since the body diode voltage drop is many times higher than the MOSFET channel voltage drop. The interval of body diode conduction can be observed with an oscilloscope as a negative 0.7V to 1.5V pulse at the SR MOSFET drain.

UVLO Divider Selection

A dedicated comparator connected to the UVLO pin is used to detect under-voltage condition. When the UVLO pin voltage is below 0.4V, the controller is in a low current shutdown mode. For a UVLO pin voltage greater than 0.4V but less than 1.25V the controller is in standby mode. Once the UVLO pin voltage is greater than 1.25V, the controller is fully enabled. When the UVLO pin voltage rises above 1.25V threshold, an internal 23µA current source is activated thus providing threshold hysteresis. The 23µA current source is deactivated when the voltage at the UVLO pin falls below 1.25V. Resistance values for R1 and R2 can be determined from the following equations:

$$R_1 = \frac{V_{HYS}}{23\ \mu A}$$

$$R_2 = \frac{1.25 \times R_1}{V_{PWR} - 1.25}$$

Where V_{PWR} is the desired turn-on voltage and V_{HYS} is the desired UVLO hysteresis at VPWR.

For example, if the LM5039 is to be enabled when VPWR reaches 33V, and disabled when VPWR is decreased to 30V, R1 should be 130kΩ, and R2 should be 5.11kΩ. The voltage at the UVLO pin should not exceed 7V at any time. Be sure to check both the power and voltage rating (0603 resistors can be rated as low as 50V) for the selected R1 resistor. To maintain the threshold's accuracy, a resistor tolerance of 1% or better is recommended. Remote configuration of the controller's operational modes can be accomplished with open drain device(s) connected to the UVLO pin as shown in *Figure 10*.

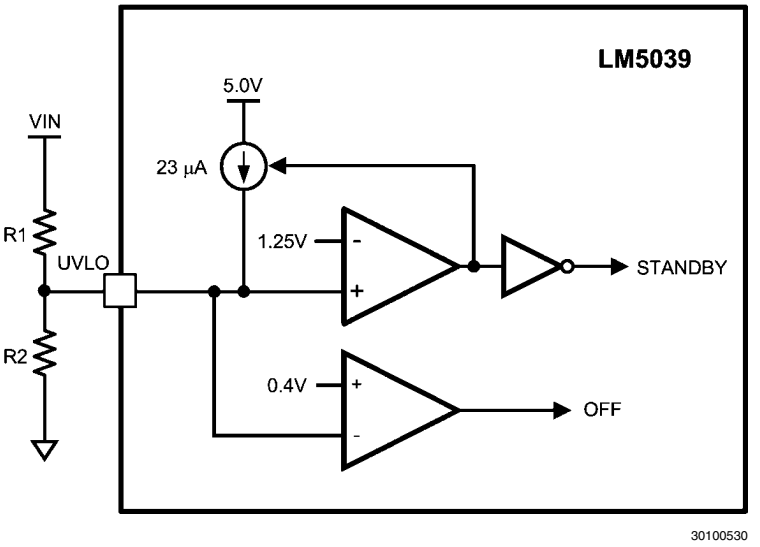


FIGURE 10. Basic UVLO Configuration

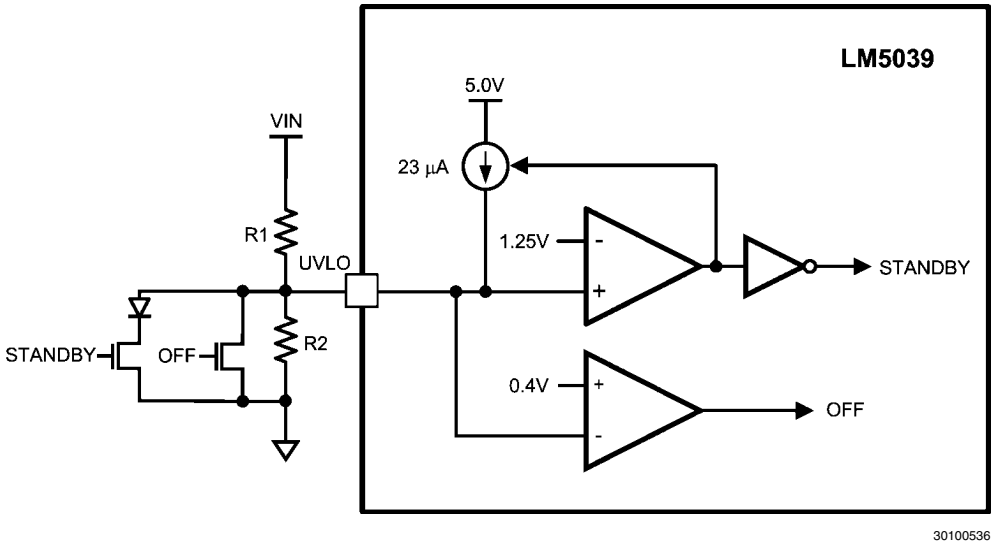


FIGURE 11. Remote Disable and Control

AVERAGE CURRENT LIMIT

The average current control circuitry is activated by connecting an appropriate capacitor from the ACL pin to AGND. In an overload condition, the current sourced by the ACL capacitor pulls down the input of the PWM comparator which is normally controlled through the COMP pin to terminate the PWM cycle. Once the ACL pin voltage reaches 1V, the PWM cycle is controlled by the average current limiter. The ACL capacitor should be selected for minimal ripple. Ripple on the ACL capacitor will result in a ripple at the center-point of the capacitor divider. It should be noted that a larger value of the ACL capacitor can slowdown the time it takes for the average current limit circuitry to take control and could possibly result in the center-point of the half-bridge capacitor divider drifting during cycle-by-cycle limiting. The magnitude of the drift of the center-point of the half-bridge capacitor once the converter hits the current limit depends upon the value of the half-bridge capacitors, the primary current, and the pulse width. For the LM5039 evaluation board, ACL capacitor values ranging from 0.047uF to 0.47uF balanced the half-bridge center point in both soft-short and hard-short conditions. When configuring the LM5039 with hiccup mode restart, the ACL and RES capacitors should be configured such that the time required for the RES pin to reach 2.5V is greater than the time required for average current limit circuitry to take control.

HICCUP MODE CURRENT LIMIT RESTART (RES)

The basic operation of the hiccup mode current limit restart is described in the functional description. The delay time to restart is programmed with the selection of the RES pin capacitor C_{RES} as illustrated in *Figure 12*.

In the case of continuous peak cycle-by-cycle average current limit detection at the CS pin, the time required for C_{RES} to reach the 2.5V hiccup mode threshold is:

$$t1 = \frac{C_{RES} \times 2.5V}{22\ \mu A} = 114\ k\Omega \times C_{RES}$$

For example, if C_{RES} = 0.01 µF the time t1 is approximately 1.14 ms.

The cool down time, t2 is set by the soft-start capacitor (C_{SS}) and the internal 1 µA SS current source, and is equal to:

$$t2 = \frac{C_{SS} \times 1V}{1\ \mu A} = 1\ M\Omega \times C_{SS}$$

If C_{SS} = 0.01 µF t2 is ≅10 ms.

The soft-start time t3 is set by the internal 110 µA current source, and is equal to:

$$t3 = \frac{C_{SS} \times 4V}{110\ \mu A} = 40\ k\Omega \times C_{SS}$$

If C_{SS} = 0.01 µF t3 is ≅363 µs.

The time t2 provides a periodic cool-down time for the power converter in the event of a sustained overload or short circuit. This off time results in lower average input current and lower power dissipation within the power components. It is recommended that the ratio of t2 / (t1 + t3) be in the range of 5 to 10 to take advantage of this feature.

If the application requires no delay from the first detection of a current limit condition to the onset of the hiccup mode (t1 = 0), the RES pin can be left open (no external capacitor). If it is desired to disable the hiccup mode entirely, the RES pin should be connected to ground (AGND).

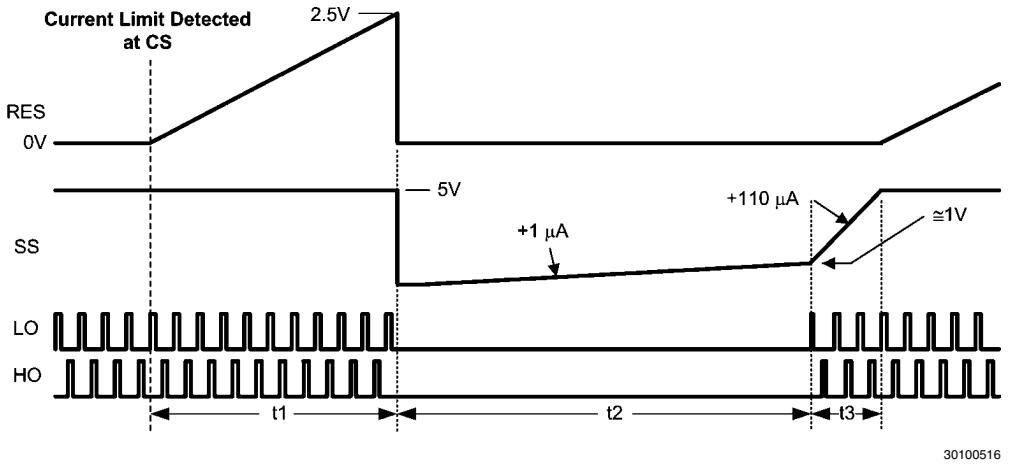


FIGURE 12. Hiccup Over-Load Restart Timing

Printed Circuit Board Layout

The LM5039 Current Sense and PWM comparators are very fast, and respond to short duration noise pulses. The components at the CS, COMP, SS, ACL, UVLO, DLY and the RT pins should be as physically close as possible to the IC, thereby minimizing noise pickup on the PC board tracks.

Layout considerations are critical for the current sense filter. If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense filter components and to the IC pins. The ground side of the transformer should be connected via a dedicated PC board track to the AGND pin, rather than through the ground plane.

If the current sense circuit employs a sense resistor in the drive transistor source, low inductance resistors should be used. In this case, all the noise sensitive, low-current ground tracks should be connected in common near the IC, and then a single connection made to the power ground (sense resistor ground point).

The gate drive outputs of the LM5039 should have short, direct paths to the power MOSFETs in order to minimize inductance in the PC board traces. The SR control outputs should also have minimum routing distance through the pulse transformers and through the secondary gate drivers to the sync FETs.

The two ground pins (AGND, PGND) must be connected together with a short, direct connection, to avoid jitter due to relative ground bounce.

If the internal dissipation of the LM5039 produces high junction temperatures during normal operation, the use of multiple vias under the IC to a ground plane can help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) will help reduce the junction temperatures. If using forced air cooling, avoid placing the LM5039 in the airflow shadow of tall components, such as input capacitors.

Application Circuit Example

The following schematic shows an example of a 100W half-bridge power converter controlled by the LM5039. The operating input voltage range (V_{PWR}) is 36V to 75V, and the output voltage is 3.3V. The output current capability is 30 Amps. Current sense transformer T2 provides information to the CS pin for current limit protection. The error amplifier and reference, U3 and U5 respectively, provide voltage feedback via opto-coupler U4. Synchronous rectifiers Q4, Q5, Q6 and Q7 minimize rectification losses in the secondary. An auxiliary winding on transformer T1 provides power to the LM5039 VCC pin when the output is in regulation. The input voltage UVLO thresholds are ≅34V for increasing V_{PWR}, and ≅32V for decreasing V_{PWR}. The circuit can be shut down by driving the ON/OFF input (J2) below 1.25V with an open-collector or open-drain circuit. An external synchronizing frequency can be applied through a 100pF capacitor to the RT input (U1 pin 5). The regulator output is current limited at ≅34A.

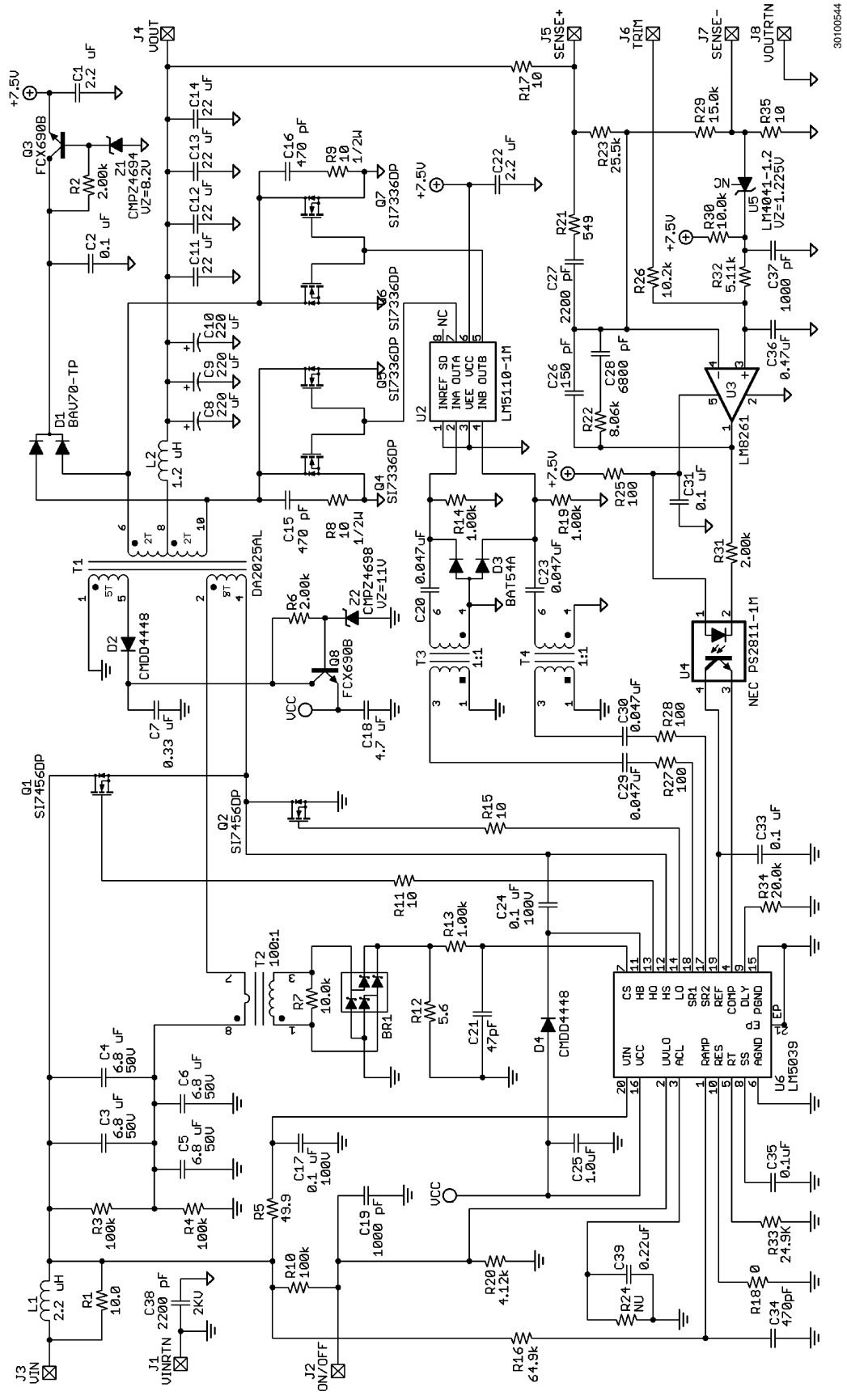
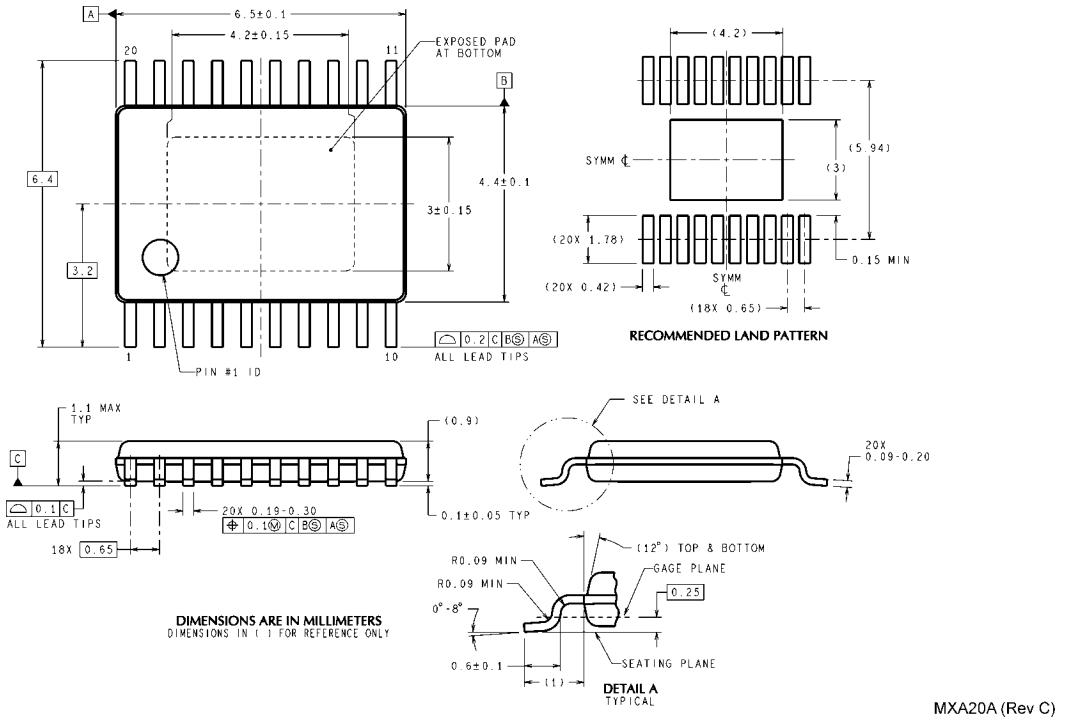


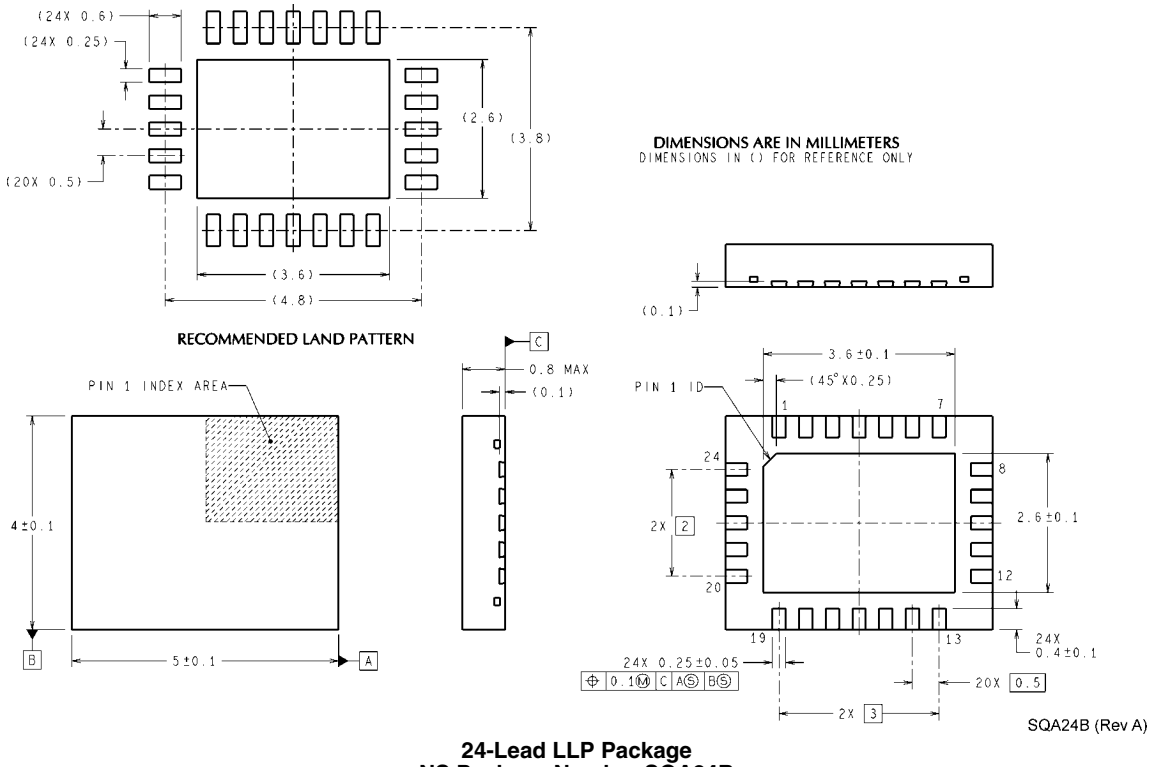
FIGURE 13. Evaluation Board Schematic

Physical Dimensions inches (millimeters) unless otherwise noted



MXA20A (Rev C)

Molded TSSOP-20
NS Package Number MXA20A



SQA24B (Rev A)

24-Lead LLP Package
NS Package Number SQA24B

Notes

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Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
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