M52957AFP

Distance Detection Signal Processing for 3V Supply Voltage

REJ03F0069-0100Z
Rev.1.0
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Description

M52957AFP is a semiconductor integrated circuit containing distance detection signal processing circuit for 3V supply voltage.

This device transforms each optical inflow current I1 and I2 from PSD SENSOR into the voltage, and integrates that output after doing calculation corresponds to I1/(I1+I2), and outputs it as the time data(pulse term).

Features

- Wide supply voltage range Vcc=2.2 to 5.5V
- Includes clamp level switching circuit
  (Switch is 16 kinds by outside control)
- Includes STANDBY function
- Includes POWER ON RESET function

Application

Auto focus control for the CAMERA

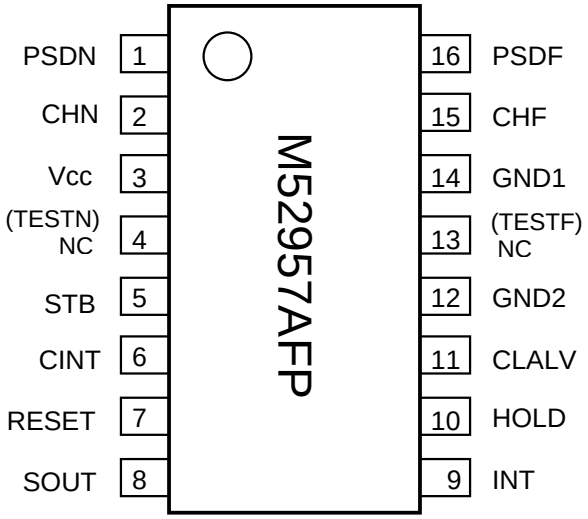
Sensor for short distance etc

Recommended Operating Condition

Rated supply voltage • • • • • • • • • • • • • • • • 3.0V

Supply voltage • • • • • • • • • • • • • • • • 2.2 to 5.5V

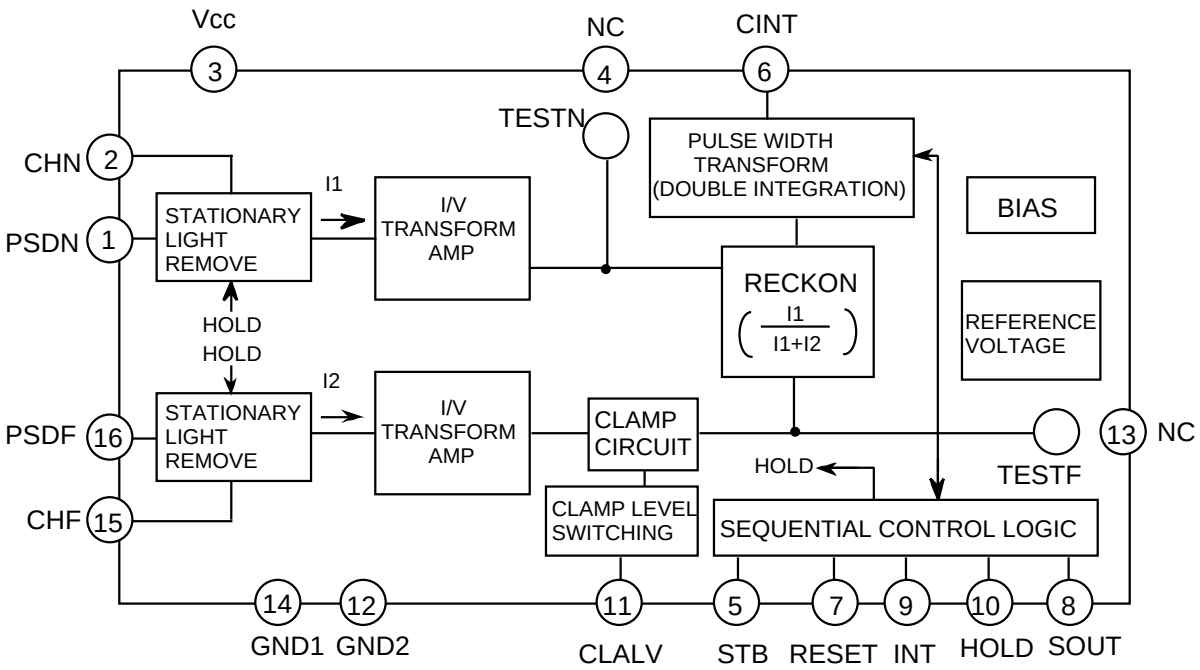
Pin Configuration



Outline 16P2E

Note: pin4,13 is connected only engineering sample

Block Diagram



Note: pin4,13 is connected only engineering sample

Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted.)

Parameter	Symbol	Ratings	Unit	Remark
Supply voltage	VCC	7.0	V	note 1
Power dissipation	Pd	320	mW	Ta=25°C
Thermal derating	Kθ	–3.2	mW/°C	Ta≥25°C
Pin supply voltage	VIF	7.0	V	Pin5, 7, 8, 9, 10, 11
Another pin supply voltage	VI/O	–0.3 to VCC + 0.3	V	note 2
Output pin inflow current	Isout	0.5	mA	NPN open collector
Operating temperature	Topr	–10 to 50	°C	
Storage temperature	Tstg	–40 to 125	°C	

Notes : 1. As a principle, do not provide a supply voltage reversely.
2. As a principle, do not provide the terminals with the voltage over supply voltage or under ground voltage.

Electrical characteristics

(Ta = 25°C, VCC = 5.0V, unless otherwise noted.)

Classification	Parameter	Symbol	Limits			Unit	Test conditions	Note
			Min.	Typ.	Max.			
	Operating supply voltage range	VCC	2.2	3.0	5.5	V		
Consuming current	Usual consuming current	ICC1	—	5.9	7.7	mA		
	While Rapid charge consuming current 1	ICC2	—	17.7	23.0	mA	While CH rapid charge consuming current	*1
	While Rapid charge consuming current 2	ICC3	—	19.0	24.7	mA	While CH and CINT rapid charge consuming current	*1
	While STAND BY consuming current	ICC4	—	—	1.0	µA		*1
HOLD pin	HOLD "H" input voltage	VHOH	1.1	—	7.0	V		
	HOLD "L" input current	VHOL	0	—	0.3	V		
	HOLD "H" input current	IHOH	—	—	1.0	µA	VIH=5.5V	
	HOLD "L" input voltage	IHOL	–100	–75	–50	µA	VIL=0V	
INT pin	INT "H" input voltage	VINH	1.1	—	7.0	V		
	INT "L" input voltage	VINL	0	—	0.3	V		
	INT "H" input current	IINH	—	—	1.0	µA	VIH=5.5V	
	INT "L" input current	IINL	–100	–75	–50	µA	VIL=0V	
CLALV pin	CLALV "H" input voltage	VCLH	1.1	—	7.0	V		
	CLALV "L" input voltage	VCLL	0	—	0.3	V		
	CLALV "H" input current	ICLH	—	—	1.0	µA	VIH=5.5V	
	CLALV "L" input current	ICLL	–100	–75	–50	µA	VIL=0V	
RESET pin	RESET "H" input voltage	VREH	1.1	—	7.0	V		
	RESET "L" input voltage	VREL	0	—	0.3	V		
	RESET "H" input current	IREH	—	—	1.0	µA	VIH=5.5V	
	RESET "L" input current	IREL	–100	–75	–50	µA	VIL=0V	
STB pin	STB "H" input voltage	VSTH	VCC–0.3	—	7.0	V		
	STB "L" input voltage	VSTL	0	—	0.3	V		
	STB "H" input current	ISTH	—	—	3.0	µA	VIH=5.5V	
	STB "L" input current	ISTL	–150	–100	–50	µA	VIL=0V	
HOLD C	CH rapid charge current	ICHQC	–2000	–1000	–500	µA	IPSD=5µA , VCH=0V	*1
	CH stationary charge current	ICHC	–30	–20	–10	µA	VCH=0V	*1
	CH stationary discharge current	ICHD	10	20	30	µA	VCH=1.5V	*1

Electrical characteristics (cont.)

(Ta = 25°C, VCC = 3.0V, unless otherwise noted.)

Classification	Parameter	Symbol	Limits			Unit	Test conditions	Note
			Min.	Typ.	Max.			
Double integration	CINT rapid charge current	ICINTC	84	120	156	µA	VCI=1V (CINT stable period)	*1
	CINT reference voltage	VCINT	1.6	1.8	2.0	V	GND criterion	*1
	The first integration current	ICI1	4.06	5.80	7.54	µA	VCINT=1.5V	*1
	The second integration current	ICI2	–3.20	–2.46	–1.27	µA	VCHF=2V , VCHN=0V	*1
	The first integration current stability percentage	ΔICI1	—	—	10	%		*2
	The second integration current stability percentage	ΔICI2	—	—	10	%		*2
	The first and second integration current ratio	ICI12	2.12	2.36	2.60		| ICI1 | / | ICI2 |	
AF input condition 1	AF output time(9:1)-1	D(9:1) - 1	11.78	13.40	15.02	msec	Near side9 : Far side1	*3
	AF output time(6:4)-1	D(6:4) - 1	7.77	8.95	10.13	msec	Near side6 : Far side4	*3
	AF output time(3:7)-1	D(3:7) - 1	3.77	4.51	5.25	msec	Near side3 : Far side7	*3
	AF slope -1	ΔAF - 1	6.57	8.89	11.21	msec		*3
	AF linearity-1	LAF - 1	0.9	1.0	1.1			*3
AF input condition 2	AF output time(9:1)-2	D(9:1) - 2	11.78	13.40	15.02	msec	Near side9 : Far side1	*3
	AF output time(6:4)-2	D(6:4) - 2	7.77	8.95	10.13	msec	Near side6 : Far side4	*3
	AF output time(3:7)-2	D(3:7) - 2	3.77	4.51	5.25	msec	Near side3 : Far side7	*3
	AF slope -2	ΔAF - 2	6.57	8.89	11.21	msec		*3
	AF linearity-2	LAF - 2	0.9	1.0	1.1			*3
AF input condition 3	AF output time(9:1)-3	D(9:1) - 3	11.78	13.40	15.02	msec	Near side9 : Far side1	*3
	AF output time(6:4)-3	D(6:4) - 3	7.77	8.95	10.13	msec	Near side6 : Far side4	*3
	AF output time(3:7)-3	D(3:7) - 3	3.77	4.51	5.25	msec	Near side3 : Far side7	*3
	AF slope -3	ΔAF - 3	6.57	8.89	11.21	msec		*3
	AF linearity-3	LAF - 3	0.9	1.0	1.1			*3
AF input condition 1 minus 2	ΔAF output time(9:1)	ΔD(9:1)	—	—	280	µsec	Near side9 : Far side1 (Condition 1-2)	
	ΔAF output time(6:4)	ΔD(6:4)	—	—	280	µsec	Near side6 : Far side4 (Condition 1-2)	
	ΔAF output time(3:7)	ΔD(3:7)	—	—	280	µsec	Near side3 : Far side7 (Condition 1-2)	
Data	SOUT leak current	ISOUTL	—	—	1.0	µA	VIN = 5.5V	
	SOUT saturation voltage	VSOUTS	—	—	0.3	V	IOUT=500µA	
Sensor	Signal light saturation current	ΔINF	3.0	—	—	µA		*4
	Stationary light remove current	IPSD	—	—	30	µA		*4
	Clamp level	ICLAM	–30	—	30	%	Change quantity for Typ. current	

- *1 : Set up the logic control terminal, correspond to the parameter.
- *2 : Change ratio between the first integration current and the second integration current at a voltage of CINT that is {CINT reference voltage(VCINT)-0.1V} and 1V.

$$\Delta I_{CI}1=\left(1-\frac{\text{The first integration current (CINT=1V)}}{\text{The first integration current (CINT=VCINT-0.1V)}}\right)\times 100\%$$

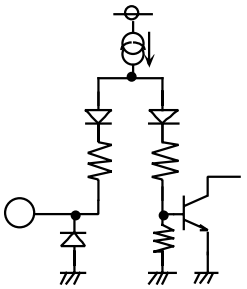
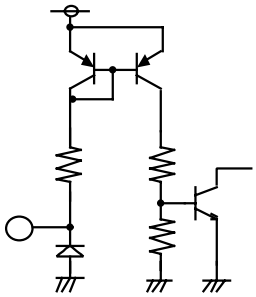
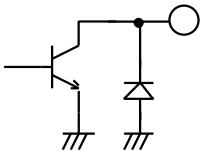
$$\Delta I_{CI}2=\left(1-\frac{\text{The second integration current (CINT=1V)}}{\text{The second integration current (CINT=VCINT-0.1V)}}\right)\times 100\%$$

- *3 : Connect the resistance of 120KΩ instead of PSD and establish current output from PHOTO COUPLER correspond to the parameter. And input the varied resistance ratio. And measure the pulse width of SOUT output at that time, obtain AFslope and AF linearity from the equations below.

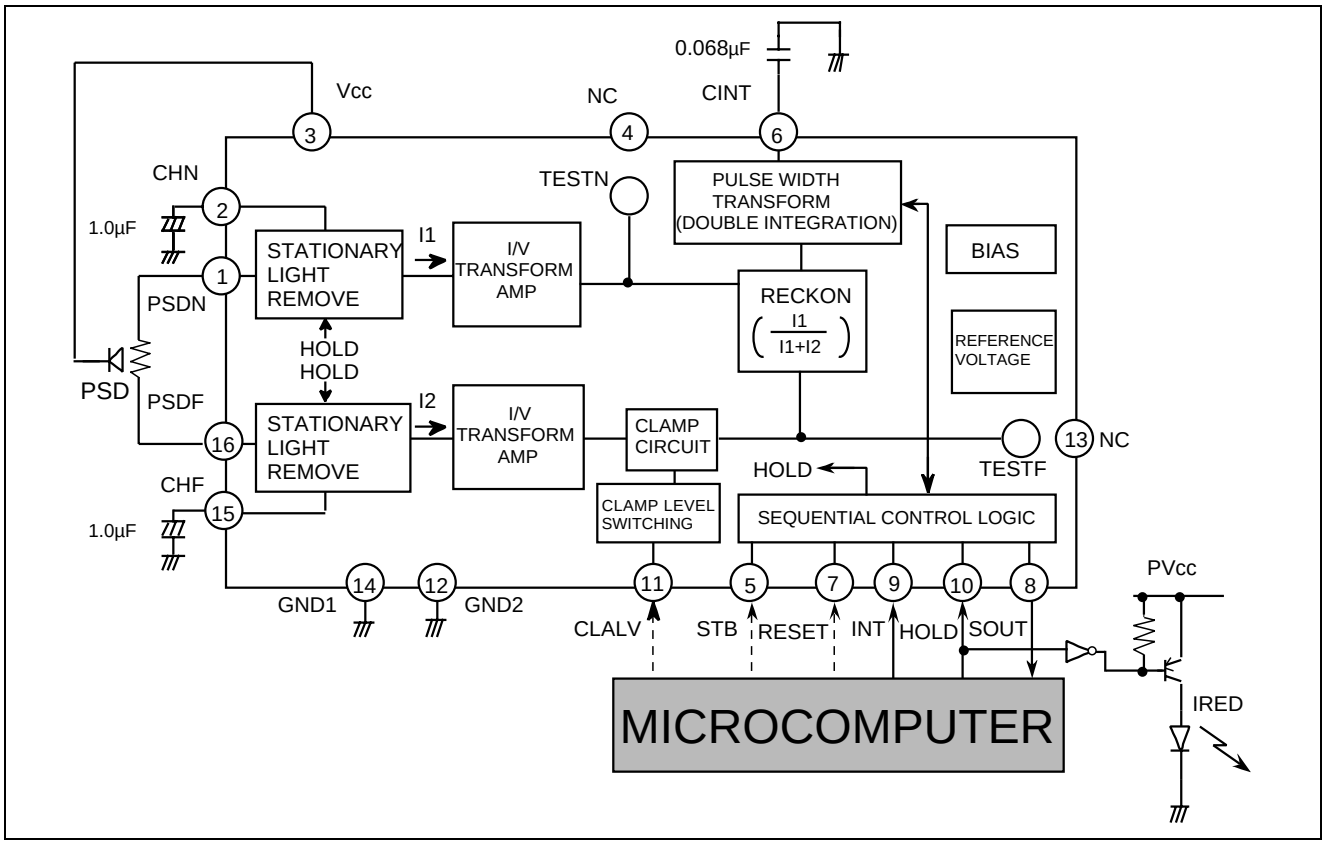
  Input condition1: I_{PSD} (Stationary light current)=0 I1+I2=100nA
  Input condition2: I_{PSD} (Stationary light current)=0 I1+I2=50nA
  Input condition3: I_{PSD} (Stationary light current)=10µA I1+I2=100nA
  D(9 : 1) • • • The pulse width of SOUT output at input with I1:I2=9:1
  D(6 : 4) • • • The pulse width of SOUT output at input with I1:I2=6:4
  D(3 : 7) • • • The pulse width of SOUT output at input with I1:I2=3:7

  AF slope : DAF = D(9 : 1) - D(7 : 3)
  AF linearity : L(AF) = (D(9 : 1) - D(6 : 4)) / (D(6 : 4) - D(7 : 3))
  PSD quite resistance : 120KΩ
- *4 : The input current of one side channel when stationary light remove circuit and I/V transform AMP is not saturated.

Description of Pin

Pin name	Circuit diagram	Parameter	Limits			Unit	Test conditions and note
			Min.	Typ.	Max.		
HOLD INT CLALV RESET		"H"input voltage	1.1	—	7.0	V	
		"L"input voltage	0	—	0.3		
		"H"input current	—	—	1.0	µA	VIH=5.5V
		"L"input current	-100	-75	-50		VIL=0V
STB		"H"input voltage	VCC -0.3	—	7.0	V	
		"L"input voltage	0	—	0.3		
		"H"input current	—	—	3.0	µA	VIH=5.5V
		"L"input current	-150	-100	-50		VIL=0V
SOUT		"L"output voltage	—	—	0.3	V	IOL=500µA
		"H"leak current	—	—	1.0	µA	VIN=5.5V

Application Example



Controls

(1) STB

This terminal enables IC to operate. IC is Standby at HIGH in this terminal. IC can operate at LOW in this terminal.

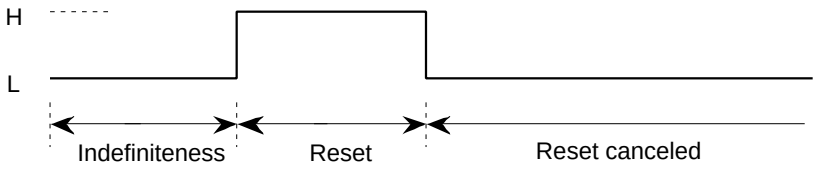
(2) RESET

This terminal resets the whole IC including a logic. This terminal resets IC at HIGH.

This terminal cancel resetting IC at the edge from HIGH to LOW.

IC includes power on reset function. The control from external is also possible.

The reset term in IC takes OR between power on reset and control signal from external.



While this terminal is HIGH,dielectric divide pole countermeasures circuit of integration condenser is active.

(3)CLALV

This terminal sets up clamp level.

As including D/A of 4bit, 16way clamp level setting is possible by inputting clock after reset is canceled(include none clamp).

Set up current value of each bit is on the right table.
The number of input clock and set up clamp level is as follows.

bit	Set up current (Typ.)
1	0.125 nA
2	0.25 nA
3	0.5 nA
4	1.0 nA

Clock value	Clamp level(Typ.)
0	None clamp
1	0.125 nA
2	0.250 nA
3	0.375 nA
4	0.500 nA
5	0.625 nA
6	0.750 nA
7	0.875 nA
8	1.000 nA
9	1.125 nA
10	1.250 nA
11	1.375 nA

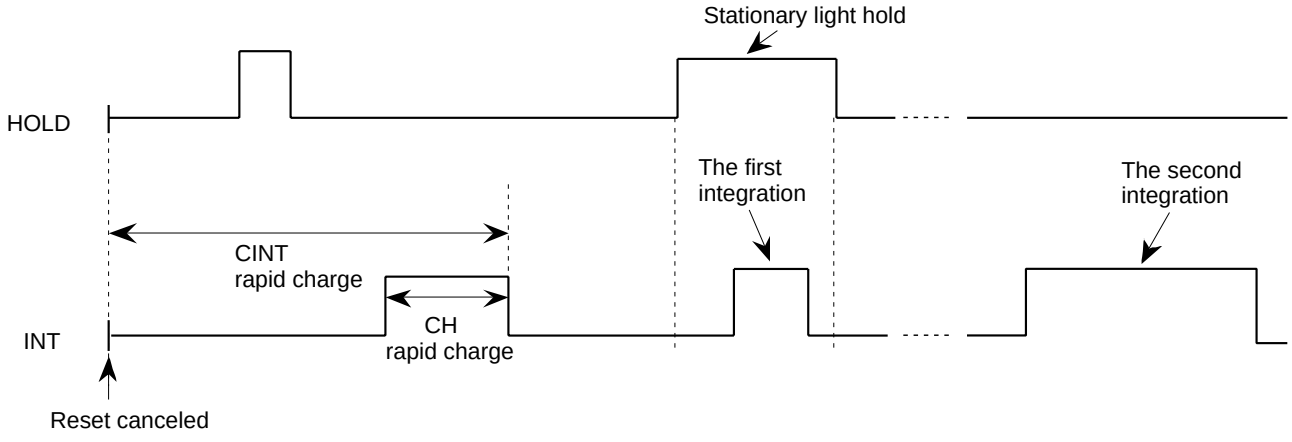
Clock value	Clamp level(Typ.)
12	1.500 nA
13	1.625 nA
14	1.750 nA
15	1.875 nA
16	None clamp
17	0.125 nA
18	0.250 nA
19	0.375 nA
20	0.500 nA
⋮	⋮
⋮	⋮
⋮	⋮

Clamp level is established with fall edge of input clock.
It repeats the same value after 16 clock.

(4) HOLD INT

These terminals implement the following controls by inputting HIGH/LOW.

a. CINT rapid charge ON , OFF
b. CHrapid charge ON , OFF
c. Stationary light hold ON , OFF
d. The first integration ON , OFF
e. The second integration ON , OFF



a. CINT rapid charge

After reset is canceled, the capacity of CINT is charged rapidly until INT terminal first falls.

b. CH rapid charge

After reset is canceled, the capacity of CH is charged rapidly until INT terminal first rises and falls.

c. Stationary light hold

After reset is canceled, holds the stationary light while HOLD terminal is HIGH.

d. The first integration

After reset is canceled, as HOLD terminal is HIGH and INT terminal is HIGH, the first integration is implemented while INT terminal is HIGH. Therefore, the first integration must be finished(INT terminal from HIGH to LOW) until stationary light hold will be completed (HOLD terminal from HIGH to LOW)

e. The second integration

After reset is canceled, the second integration is implemented as HOLD terminal is LOW and INT terminal is HIGH. And, the second integration is completed by exceeding judgment level of CINT terminal although INT terminal is HIGH.

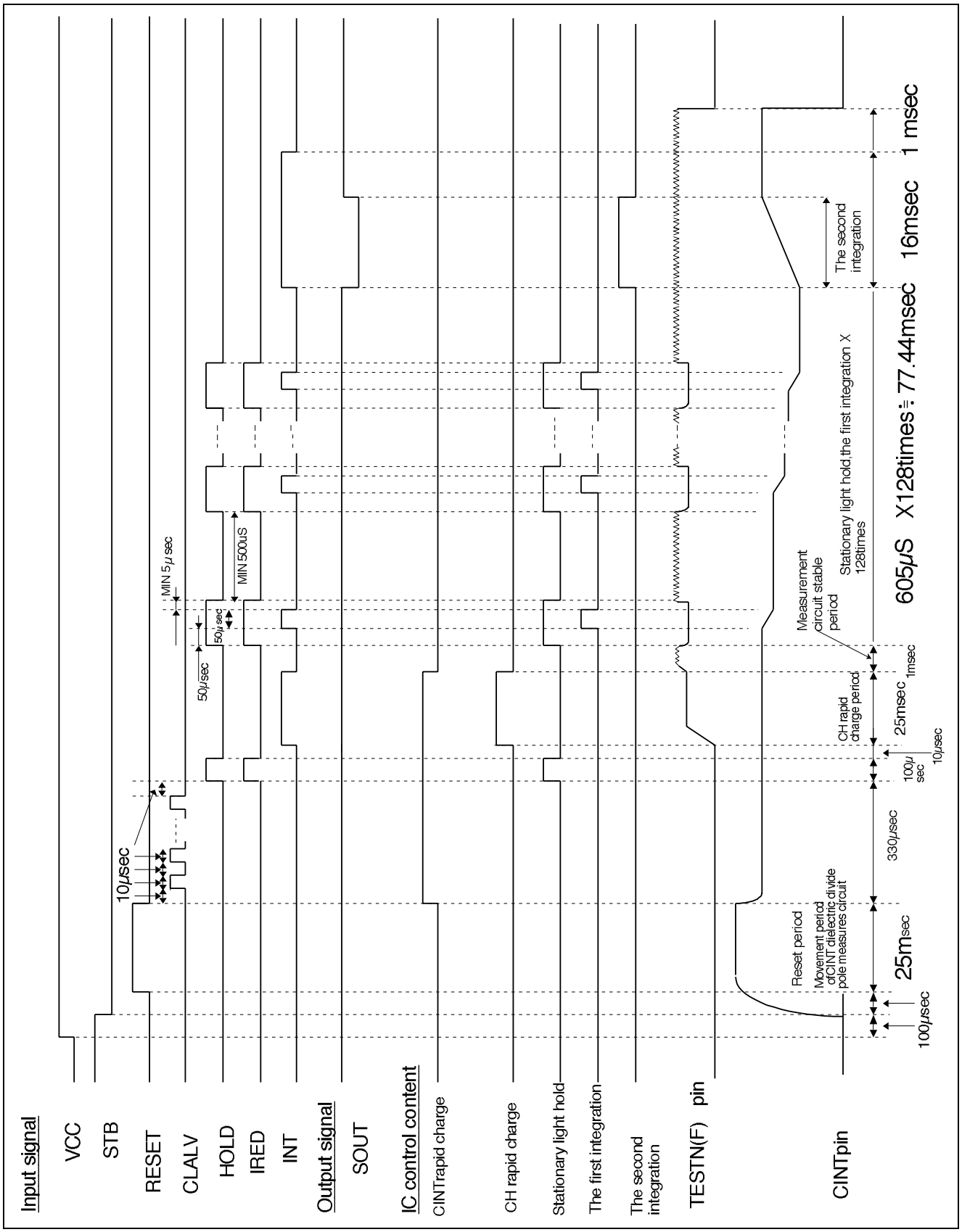
(5)SOUT

When the second integration starts, This terminal becomes from HIGH to LOW.

If CINT terminal exceeds judge level or INT terminal becomes from HIGH to LOW, this terminal becomes from LOW to HIGH.

(notice)As the signal from microcomputer, the signal that controls IRED ON/OFF is required except for above mentioned control signals. But applying the timing of HOLD is available.

Sequential Time Chart Example

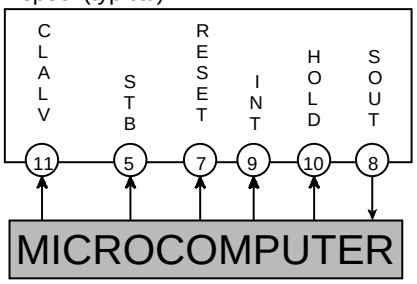


Mask Option

(1) The second integration current value can be doubled.(2.5µ ⟶ 5.0µA)

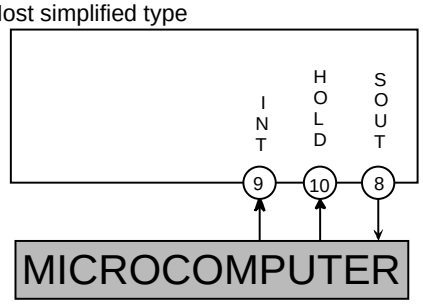
(2) Control terminal variation

① Full spec (typical)



This type uses CLALV,STB,RESET,INT,HOLD,SOUT terminal as I/F terminal to the microcomputer.
This is the typical type at M52957AFP.

② Most simplified type



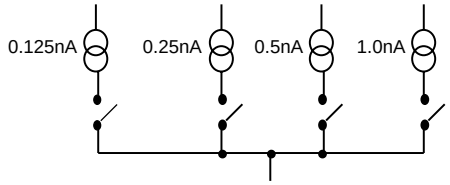
This type does not connect CLALV,STB,RESET terminals to the microcomputer.
When above mentioned terminals are not connected to the microcomputer without changing mask,connect each terminal to the ground. In this case,clamp level becomes 0 and standby function is lost. Power on reset in IC is used as reset.

③ Explanation of the terminal that can be simplified.

(a)CLALV • • • • • In the typical type,16way clamp levels can be set by the external control,but also the terminal can be simplified by mask option as follows.

(I) Clamp level fixation • • • • • Selects 1 point from 16 steps of clamp level and fixes it.

(II) Clamp level 2 step changeover • • • Selects 2 points from clamp level and switches it by changing CLALV terminal HIGH/LOW. However,as selecting 2 points,there is a following constraint.

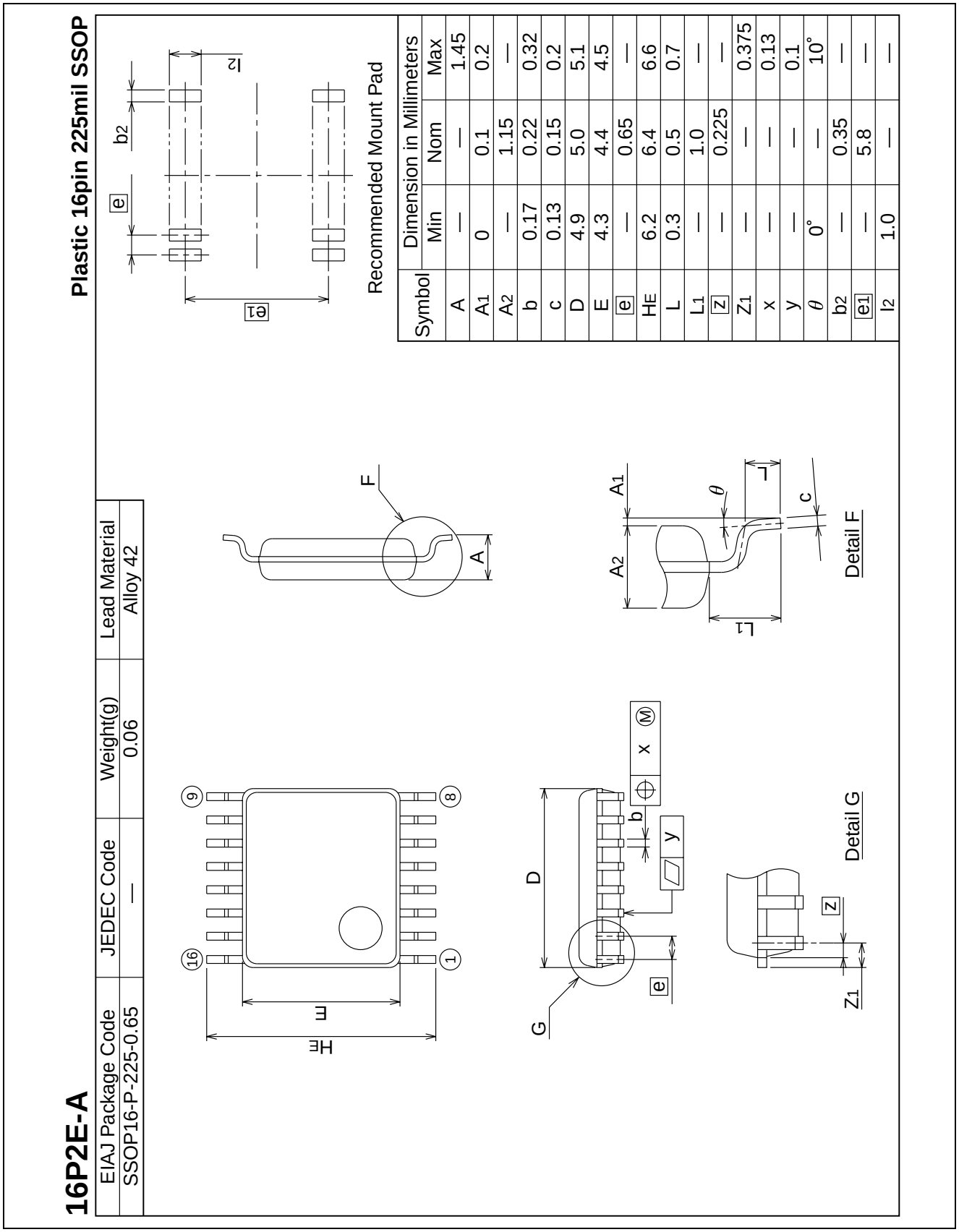


Fixes 3 parts of 4 switches correspond to each bit in figure to ON or OFF,controls another part by CLALV terminal .

(b)STB • • • • • • When no standby function required such as VCC is suitched ON/OFF, STB terminal can be eliminated.

(c)RESET • • • • • Since IC include power on reset circuit, RESET terminal can be eliminated, As merit of controlling RESET terminal from outside, distance detection time can be shortened because there is no need to switch VCC to STB terminal ON/OFF at consecutive distance detection.

Package Dimensions



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.45
A_1	0	0.1	0.2
A_2	—	1.15	—
b	0.17	0.22	0.32
c	0.13	0.15	0.2
D	4.9	5.0	5.1
E	4.3	4.4	4.5
e	—	0.65	—
H_E	6.2	6.4	6.6
L	0.3	0.5	0.7
L_1	—	1.0	—
Z	—	0.225	—
Z_1	—	—	0.375
x	—	—	0.13
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.35	—
e_1	—	5.8	—
l_2	1.0	—	—

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