YAMAHA

YDA136

D-60

STEREO 60W-100W DIGITAL AUDIO POWER AMPLIFIER CONTROLLER

■Outline

YDA136 (D-60) is a high efficient and high output digital audio power amplifier controller IC.
By combining a general purpose PowerMOSFET (hereafter called PowerMOSFET) which is connected with YDA136 and BTL, it is able to compose a high efficient audio power amplifier such as 60Wx2ch (Supplied voltage=32V, RL=6Ω) and 100Wx2ch (Supplied voltage=40V, RL=6Ω).
YDA136 has 24bit 192kHz (max) DAC and 6 to -73dB（1dB Step） of electron volumes in addition to a digital amplifier controller, and supports a digital audio signal input. Furthermore, it also supports an analog audio signal input with DAC bypasses.
YDA136 realizes a high-standing audio characteristic that is lower noise and distortion rate by performing an analog feedback from PowerMOSFET output, and by using Yamaha's unique modulation method.
YDA136 also equips a function (Over current detection function) which protects a circuit from a short of speaker output terminal (after the LC filter) and a function (Supplied voltage detection function) which prevents a malfunction by detecting a power supply falling.
Moreover, it has a function (Clock stop detection function) to protect a circuit by detecting a stop termination of PWM carrier clock and a function (High-temperature detection function) to protect a circuit by detecting the unusual high-temperature condition of it-self.
At last, by making three YDA136 to daisy-chain connection, the audio system of 6ch is easily realizable.

■Features

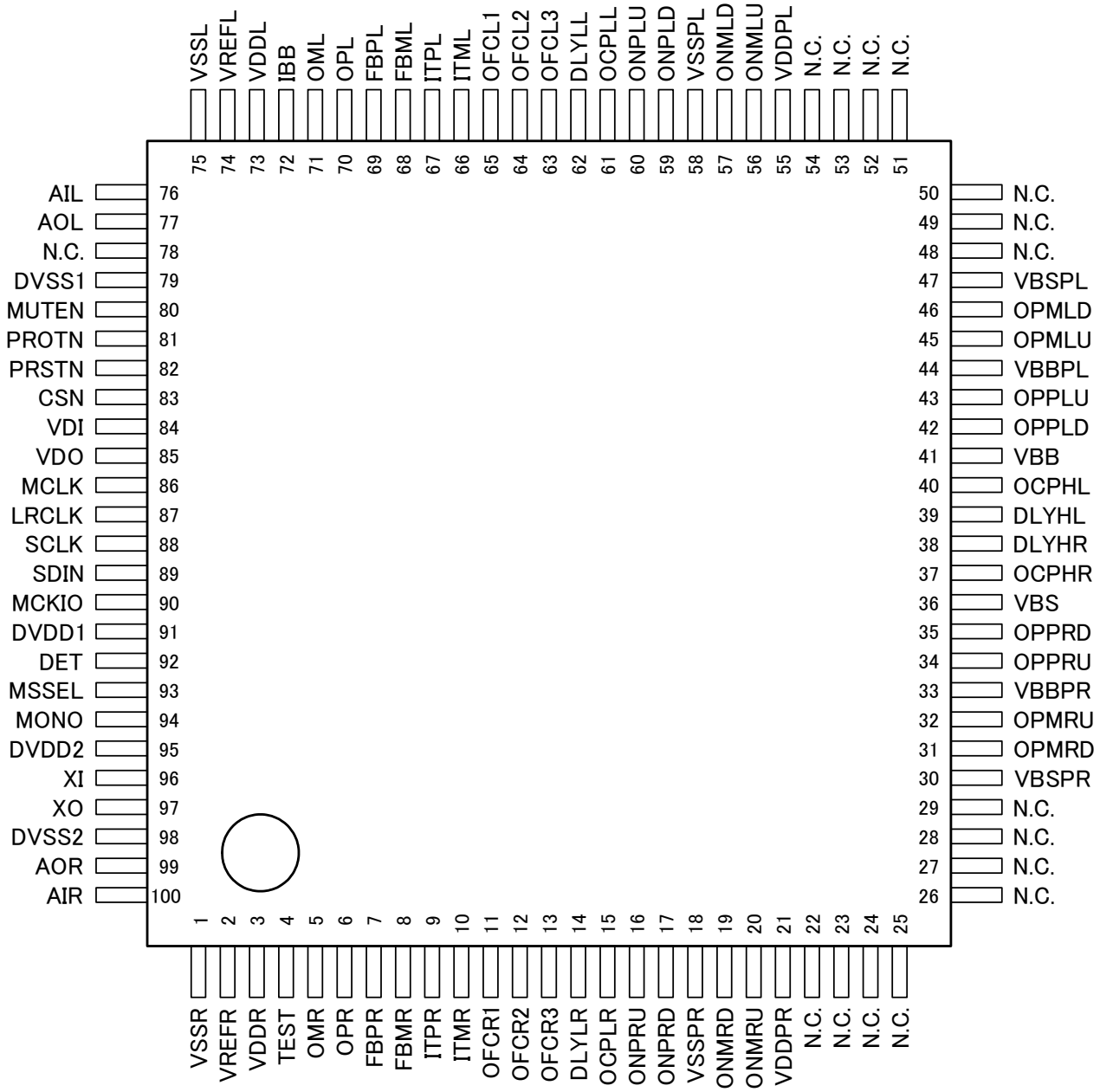
- High Output Power
  - 100W (VBB=40V, RL=6Ω)
  - 60W (VBB=32V, RL=6Ω)
- Low Distortion Rate(THD+N)
  - 0.05% (Po=50W, 1kHz, RL=6Ω, at digital input)
  - 0.03% (Po=50W, 1kHz, RL=6Ω, at analog input)
- High S/N Ratio
  - 100dB (VBB=40V, A-filter, Gain=21.7+6dB, RL=6Ω, at digital input
- Low Residual Noise
  - 100μV (VBB=40V, Gain=21.7+6dB, at digital input)
  - 70μV (VBB=40V, Gain=21.7+6dB, at analog input)
- Channel Separation
  - 80dB (1kHz, Po=50W)

- Supports 24bit Digital input and Analog input
- Built-in 6 to -73dB（1dB Step） of electron volume
- Multi-channel synchronous operation by switching Master/Slave function.
- Protect reset function
- Hard mute function
- Monophonic function
- Unusual operation detection protection function (Over current, Supplied voltage, Speaker terminal short, Clock stop, Heat）
- Pop noise rejection function at the time of power-up
- 100 pin plastic SQFP
  Pin lead plating with Pd-free (YDA136-SZ)

YAMAHA CORPORATION

YDA136 CATALOG
CATALOG No.:LSI-4DA136A20
2005.4

■Terminal Configuration



＜100pin SQFP Top View＞

■Terminal Functions

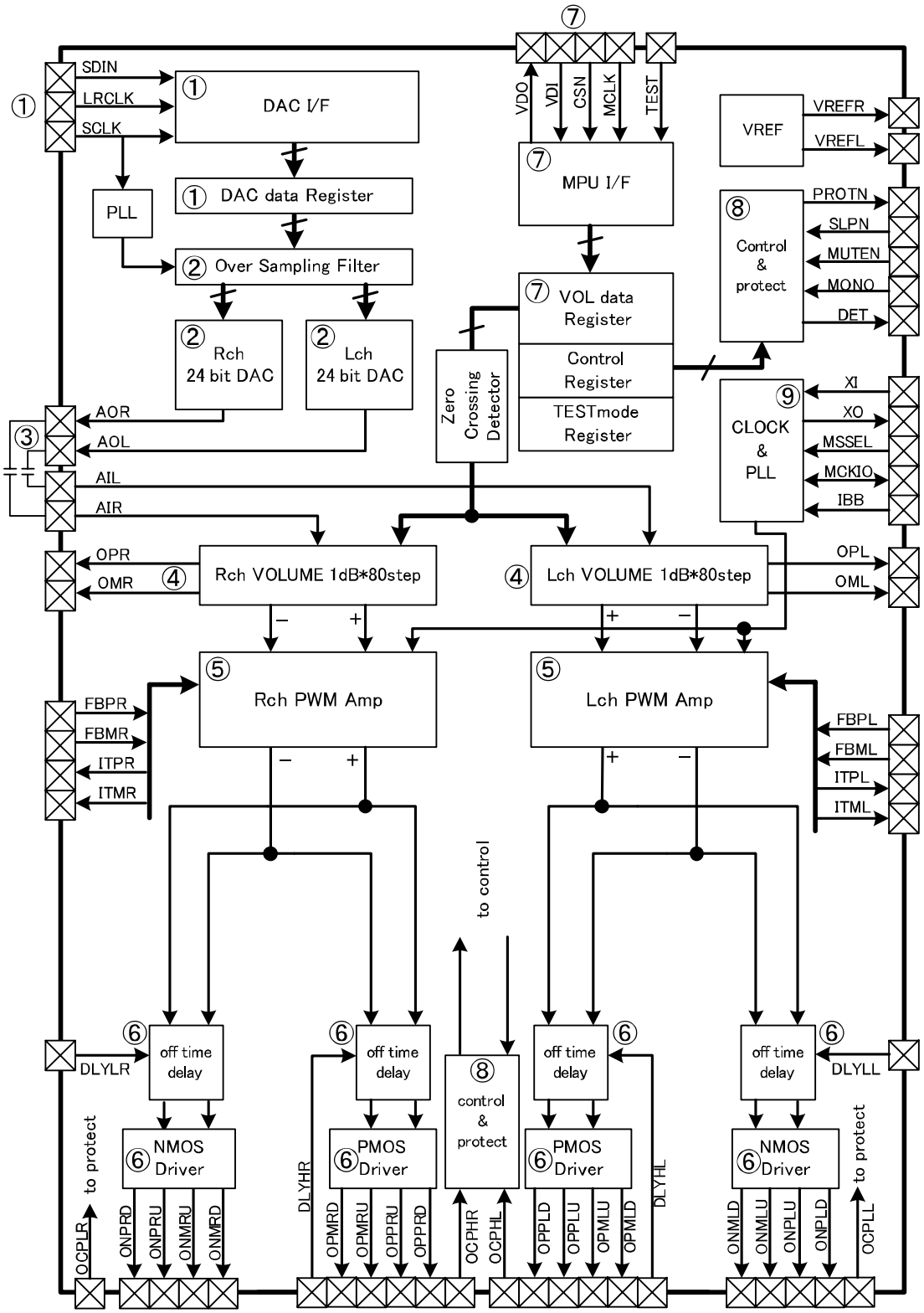
No.	Name	I/O	Function
1	VSSR	PWR	Rch Analog Ground Terminal
2	VREFR	AO	Rch Reference Voltage Output Terminal
3	VDDR	PWR	Rch Analog Power Terminal
4	TEST	DI	Test Terminal: Usually, use it by “L” fixation.
5	OMR	AO	Rch Electron Volume Output Terminal Inverted side
6	OPR	AO	Rch Electron Volume Output Terminal Noninverted side
7	FBPR	AI	Rch Digital Amplifier Input Terminal Noninverted side
8	FBMR	AI	Rch Digital Amplifier Input Terminal Inverted side
9	ITPR	AO	Rch External Filter Element Connection Terminal Noninverted side
10	ITMR	AO	Rch External Filter Element Connection Terminal Inverted side
11	OFCR1	AI	Hold to “H” level.
12	OFCR2	AI	Hold to “L” level.
13	OFCR3	AI	Hold to “L” level.
14	DLYLR	AI	Rch Low-Side Driver Off-time Setting Terminal
15	OCPLR	AI	Rch Low-Side Over Current Detection Terminal
16	ONPRU	DO	Rch Low-Side Driver Output Terminal Noninverted side (Pull-up)
17	ONPRD	DO	Rch Low-Side Driver Output Terminal Noninverted side (Pull-down)
18	VSSPR	PWR	Rch Low-Side Driver Ground Terminal
19	ONMRD	DO	Rch Low-Side Driver Output Terminal Inverted side (Pull-down)
20	ONMRU	DO	Rch Low-Side Driver Output Terminal Inverted side (Pull-up)
21	VDDPR	PWR	Rch Low-Side Driver Power Terminal
22	N.C.	—	Non connection.
23	N.C.	—	Non connection.
24	N.C.	—	Non connection.
25	N.C.	—	Non connection.
26	N.C.	—	Non connection.
27	N.C.	—	Non connection.
28	N.C.	—	Non connection.
29	N.C.	—	Non connection.
30	VBSPR	PWRH	Rch High-Side Driver Power Terminal
31	OPMRD	DOH	Rch High-Side Driver Output Terminal Inverted side (Pull-down)
32	OPMRU	DOH	Rch High-Side Driver Output Terminal Inverted side (Pull-up)
33	VBBPR	PWRH	Rch High-Side Driver Power Terminal
34	OPPRU	DOH	Rch High-Side Driver Output Terminal Noninverted side (Pull-up)
35	OPPRD	DOH	Rch High-Side Driver Output Terminal Noninverted side (Pull-down)
36	VBS	PWRH	High-Side Common Circuit Power Terminal
37	OCPHR	AIH	Rch High-Side Over Current Detection Terminal
38	DLYHR	AIH	Rch High-Side Driver Off-time Setting Terminal
39	DLYHL	AIH	Lch High-Side Driver Off-time Setting Terminal
40	OCPHL	AIH	Lch High-Side Over Current Detection Terminal
41	VBB	PWRH	High-Side Common Circuit Power Terminal
42	OPPLD	DOH	Lch High-Side Driver Output Terminal Noninverted side (Pull-down)
43	OPPLU	DOH	Lch High-Side Driver Output Terminal Noninverted side (Pull-up)
44	VBBPL	PWRH	Lch High-Side Driver Power Terminal
45	OPMLU	DOH	Lch High-Side Driver Output Terminal Inverted side (Pull-up)
46	OPMLD	DOH	Lch High-Side Driver Output Terminal Inverted side (Pull-down)
47	VBSPL	PWRH	Lch High-Side Driver Power Terminal
48	N.C.	—	Non connection.
49	N.C.	—	Non connection.
50	N.C.	—	Non connection.

Note: DI: Digital Input Terminal, DO: Digital Output Terminal, DIO: Digital I/O Terminal, DOH: High-Side Digital Output Terminal
AI: Analog Input Terminal, AO: Analog Output Terminal, AIH: High-Side Analog Input Terminal
PWR: Low-Side Power Terminal, PWRH: High-Side Power Terminal

No.	Name	I/O	Function
51	N.C.	—	Non connection.
52	N.C.	—	Non connection.
53	N.C.	—	Non connection.
54	N.C.	—	Non connection.
55	VDDPL	PWR	Lch Low-Side Driver Power Terminal
56	ONMLU	DO	Lch Low-Side Driver Output Terminal Inverted side (Pull-up)
57	ONMLD	DO	Lch Low-Side Driver Output Terminal Inverted side (Pull-down)
58	VSSPL	PWR	Lch Low-Side Driver Ground Terminal
59	ONPLD	DO	Lch Low-Side Driver Output Terminal Noninverted side (Pull-down)
60	ONPLU	DO	Lch Low-Side Driver Output Terminal Noninverted side (Pull-up)
61	OCPLL	DO	Lch Low-Side Over Current Detection Terminal
62	DLYLL	AI	Lch Low-Side Driver Off-time Setting Terminal
63	OFCL3	AI	Hold to “L” level.
64	OFCL2	AI	Hold to “L” level.
65	OFCL1	AI	Hold to “H” level.
66	ITML	AO	Lch External Filter Elements Connection Terminal Inverted side
67	ITPL	AO	Lch External Filter Elements Connection Terminal Noninverted side
68	FBML	AI	Lch Digital Amplifier Input Terminal Inverted side
69	FBPL	AI	Lch Digital Amplifier Input Terminal Noninverted side
70	OPL	AO	Lch Electron Volume Output Terminal Noninverted side
71	OML	AO	Lch Electron Volume Output Terminal Inverted side
72	IBB	AI	VBB Power-voltage Detection Terminal (Supplied-voltage feedback Terminal)
73	VDDL	PWR	Lch Analog Power Terminal
74	VREFL	AO	Lch Reference Power-voltage Output Terminal
75	VSSL	PWR	Lch Analog Ground Terminal
76	AIL	AI	Lch Electron Volume Input Terminal (Analog Signal Input Terminal)
77	AOL	AO	Lch DAC Output Terminal
78	N.C.	—	Non connection.
79	DVSS1	PWR	Digital Ground Terminal
80	MUTEN	DI	Mute Control Terminal
81	PROTN	DO	Unusual Detection Output Terminal (Open-drain)
82	PRSTN	DI	Protect Reset Control Terminal
83	CSN	DI	MPU Interface Chip-select Input Terminal
84	VDI	DI	MPU Interface Serial Data Input Terminal
85	VDO	DO	MPU Interface Serial Data Output Terminal
86	MCLK	DI	MPU Interface Serial Clock Input Terminal
87	LRCLK	DI	DAC Interface Serial Word Clock Input Terminal
88	SCLK	DI	DAC Interface Serial Clock Input Terminal
89	SDIN	DI	DAC Interface Serial Data Input Terminal
90	MCKIO	DIO	Clock Input/Output Terminal
91	DVDD1	PWR	Digital Power Terminal
92	DET	DO	Startup Standby Time Setting Terminal
93	MSSEL	DI	Slave mode/Master mode Change Terminal
94	MONO	DI	Monophonic Control Terminal
95	DVDD2	PWR	CERALOCK Power Terminal
96	XI	DI	CERALOCK Connection Terminal
97	XO	DO	CERALOCK Connection Terminal
98	DVSS2	PWR	CERALOCK Ground Terminal
99	AOR	AO	Rch DAC Output Terminal
100	AIR	AI	Rch Electron Volume Input Terminal (Analog Signal Input Terminal)

Note: DI: Digital Input Terminal, DO: Digital Output Terminal, DIO: Digital I/O Terminal, DOH: High-Side Digital Output Terminal
AI: Analog Input Terminal, AO: Analog Output Terminal, AIH: High-Side Analog Input Terminal
PWR: Low-Side Power Terminal, PWRH: High-Side Power Terminal
“CERALOCK” is the trademark of Murata Manufacturing Co., Ltd.

■Block Diagram

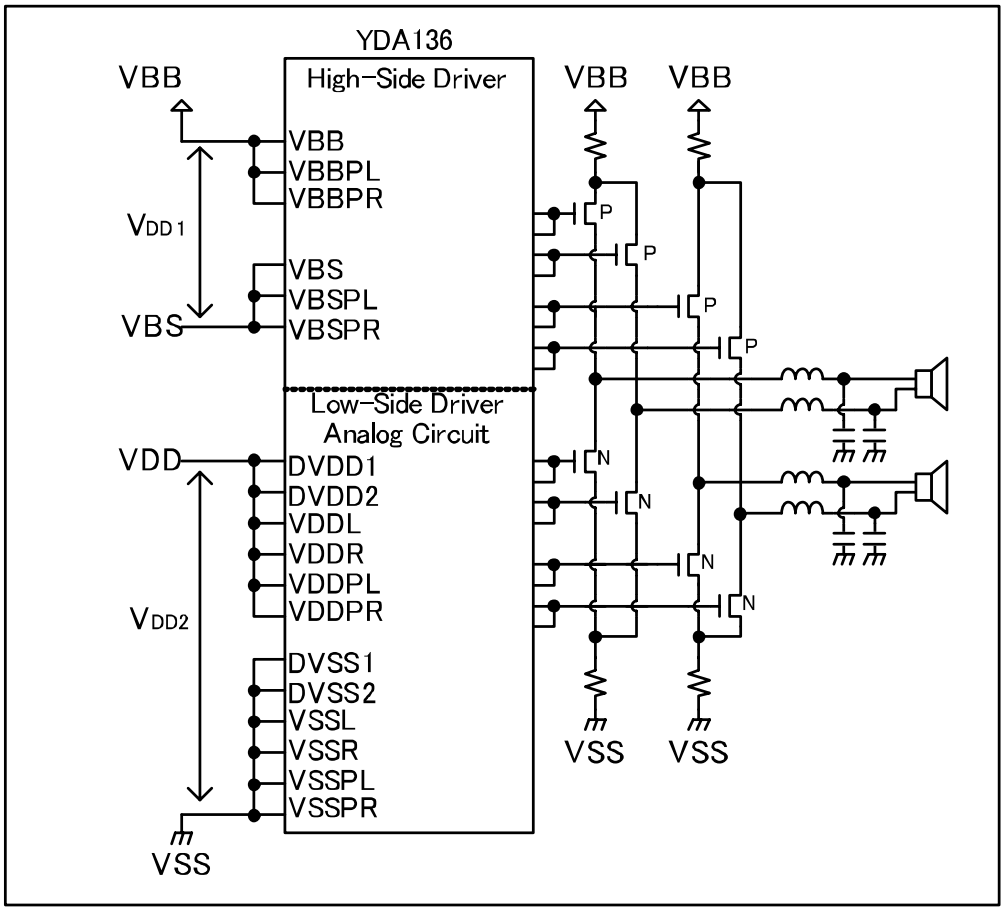


■Description of Block Functions

① Stores the digital audio signal into DAC data register through a DAC interface.
② Inputs into DAC through an over-sampling filter, and converts into an analog signal.
③ Performs a DC cut to DAC output data with the exterior capacitor of IC.
④ Performs a volume control and Differential signal conversion.
⑤ Performs a pulse width modulation
Negative feedbacks from the output of an external PowerMOSFET buffer.
⑥ Performs an Off-time delay control, and drives an external PowerMOSFET(Pch, Nch).
High current digital pulse signal is output from external PowerMOSFET (Pch, Nch)
The digital pulse signal is converted into audio signals by external LC filter and transmitted to speaker.
⑦ Stores the 7-bit volume data and control data into volume register and control register respectively through a MPU interface.
⑧ Operation control circuit and protect circuit
⑨ Master clock generation circuit and carrier clock generation circuit

■Supply of Power

YDA136 needs to be supplied the following two kinds of power supplies, the object for Low-Side drivers (Analog Circuit), and the object for High-Side drivers, in addition to a power stage power supply (VBB, VSS).
Be sure to use VDD power for Low-Side driver and VBS for High-Side driver.



■Description of Terminals Functions

●Power Supply Terminal

Lo-Side Power Supply Terminal (VDD Power Supply)

DVDD1	Digital Power
DVDD2	CERALOCK Power
VDDL	Lch Analog Power
VDDR	Rch Analog Power
VDDPL	Lch Low-Side Driver Power
VDDPR	Rch Low-Side Driver Power

Lo-Side Ground Terminal (VSS Ground)

DVSS1	Digital Ground
DVSS2	CERALOCK Ground
VSSL	Lch Analog Ground
VSSR	Rch Analog Ground
VSSPL	Lch Low-Side Driver Ground
VSSPR	Rch Low-Side Driver Ground

High-Side Power Supply Terminal (VBB Power Supply)

VBB	High-Side Power
VBBPL	Lch High-Side Driver Power
VBBPR	Rch High-Side Driver Power

High-Side Power Supply Terminal (VBS Power Supply)

VBS	High-Side Power
VBSPL	Lch High-Side Driver Power
VBSPR	Rch High-Side Driver Power

●Control Terminal

MUTEN	Hard Mute Control Terminal L: Hard mute mode H: Normal mode
PRSTN	Protect Reset Control Terminal L: Protect reset mode H: Normal mode
PROTN	Unusual Detection Output Terminal L: Protect mode Hi-Z: Normal mode Since it is an OpenDrain output, be sure to pull-up by resistance.
MONO	Monophonic Control Terminal L: Stereo mode H: Monophonic mode
DET	Start up Standby Time Setting Terminal Sets up a Start up Standby Time (T_{WAIT}) by connecting a capacitor into this terminal.
TEST	Test Terminal Hold to “L” level.

●Clock Terminal

XI	CERALOCK Connection Terminal Master mode: Connects a CERALOCK for 4.19MHz oscillation. Slave mode: Fixes to “L.”
XO	CERALOCK Connection Terminal Master mode: Connects a CERALOCK for 4.19MHz oscillation. Slave mode: Makes to “OPEN”.
MSSEL	Slave mode/ Master mode Selection Terminal L: Master mode H: Slave mode
MCKIO	4. 19MHz Clock I/O Terminal Master mode: Clock Output Slave mode: Clock Input

●Digital Interface Terminal

MPU Interface

CSN	MPU	Interface Chip-select Input
MCLK	MPU	Interface Serial Clock Input
VDI	MPU	Interface Serial Data Input
VDO	MPU	Interface Serial Data Output

DAC Interface

LRCLK	DAC	Interface Serial Word Clock Input
SCLK	DAC	Interface Serial Clock Input
SDIN	DAC	Interface Serial Data Input

●Analog I/O Terminal

DAC Output Terminal

AOL	Lch	DAC Output
AOR	Rch	DAC Output

Be sure to make AOR to an OPEN state or to connect to VSS in Monophonic mode.

Electron Volume Input

AIL	Lch	Volume Input Signal
AIR	Rch	Volume Input Signal

Be sure to make AIR to an OPEN state or to connect to GND in Monophonic mode.

Electron Volume Output

OPL	Lch	Electron Volume Output Terminal Noninverted side
OML	Lch	Electron Volume Output Terminal Inverted side
OPR	Rch	Electron Volume Output Terminal Noninverted side
OMR	Rch	Electron Volume Output Terminal Inverted side

Be sure to make both OPR and OMR to a OPEN state or to connect to VSS in Monophonic mode.

●Terminals for PWM modulation Circuits

FBPL	Lch	Digital Amplifier Input	Noninverted side
FBML	Lch	Digital Amplifier Input	Inverted side
ITPL	Lch	for External Filter Element Connection	Noninverted side
ITML	Lch	for External Filter Element Connection	Inverted side
DLYLL	Lch	Low-Side Driver Off-time Setting	
DLYHL	Lch	High-Side Driver Off-time Setting	
FBPR	Rch	Digital Amplifier Input	Noninverted side
FBMR	Rch	Digital Amplifier Input	Inverted side
ITPR	Rch	for External Filter Element Connection	Noninverted side
ITMR	Rch	for External Filter Element Connection	Inverted side
DLYLR	Rch	Low-Side Driver Off-time Setting	
DLYHR	Rch	High-Side Driver Off-time Setting	

Be sure to make each terminal of Rch to an OPEN state or to connect to VSS in Monophonic mode. In addition, as for a High-side terminal, be sure to make it to an OPEN state and to connect to VBS.

●PowerMOSFET Drive Terminal

OPPLU	Lch High-Side Driver Output	Noninverted side	Pull-up
OPPLD	Lch High-Side Driver Output	Noninverted side	Pull-down
ONPLU	Lch Low-Side Driver Output	Noninverted side	Pull-up
ONPLD	Lch Low-Side Driver Output	Noninverted side	Pull-down
OPMLU	Lch High-Side Driver Output	Inverted side	Pull-up
OPMLD	Lch High-Side Driver Output	Reversal side	Pull-down
ONMLU	Lch Low-Side Driver Output	Inverted side	Pull-up
ONMLD	Lch Low-Side Driver Output	Inverted side	Pull-down
OPPRU	Rch High-Side Driver Output	Noninverted side	Pull-up
OPPRD	Rch High-Side Driver Output	Noninverted side	Pull-down
ONPRU	Rch Low-Side Driver Output	Noninverted side	Pull-up
ONPRD	Rch Low-Side Driver Output	Noninverted side	Pull-down
OPMRU	Rch High-Side Driver Output	Noninverted side	Pull-up
OPMRD	Rch High-Side Driver Output	Noninverted side	Pull-down
ONMRU	Rch Low-Side Driver Output	Noninverted side	Pull-up
ONMRD	Rch Low-Side Driver Output	Noninverted side	Pull-down

Low-Side Driver means the PowerMOSFET (Nch). High-Side Driver means the PowerMOSFET(Pch).
The through rate control of PowerMOSFET is performed by connecting a resistor between the pull-up side output of a Low-Side driver and PowerMOSFET (Nch) and between the pull-down side of a High-Side driver and PowerMOSFET (Pch).

●Terminal for Protect Function

OCPHL	Lch High-Side Over Current Detection Terminal
OCPLL	Lch Low-Side Over Current Detection Terminal
OCPHR	Rch High-Side Over Current Detection Terminal
OCPLR	Rch Low-Side Over Current Detection Terminal

IBB VBB Supplied Voltage Detection Terminal
This terminal operates also as a supplied voltage feedback terminal.
Be sure to input a specific voltage divided by a resistor VBB and VSS.

●VREF Terminal

VREFL Lch Reference Voltage Output Terminal
Be sure to connect a stabilization capacity.

VREFR Rch Reference Voltage Output Terminal
Be sure to connect a stabilization capacity.

●Test Terminal etc.

TEST	Hold to “L” level.
OFCL1	Hold to “H” level.
OFCR1	Hold to “H” level.
OFCL2	Hold to “L” level.
OFCR2	Hold to “L” level.
OFCL3	Hold to “L” level.
OFCR3	Hold to “L” level.

■Terminal Condition in each Mode

●Operation Mode

YDA136 becomes an operation mode as the following table by the state in each input terminal.

	PRSTN Terminal Level	MUTEN Terminal Level	MONO Terminal Level	Over Current Detection		Power Detection			Carrier Clock Frequency	Junction Temperature	PROTN Terminal Level	Lch High-Side Driver Output	Lch Low-Side Driver Output	Rch High-Side Driver Output	Rch Low-Side Driver Output
				VBB - V(OCPHL) VBB - V(OCPHR)	V(OCPLL) - VSS V(OCPLR) - VSS	V(IBB)	V_{DD1} = VBB - VBS	V_{DD2} = VDD - VSS							
Low Voltage Detection Mode	-	-	-	-	-	< V_{IB}	-	-	-	-	Hi-z	H	L	H	L
	-	-	-	-	-	-	< V_{VB}	-	-	-	Hi-z	H	L	H	L
	-	-	-	-	-	-	-	< V_{VD}	-	-	Hi-z	H	L	H	L
Protect Reset Mode	L	-	-	-	-	> V_{IB}	> V_{VB}	> V_{VD}	-	-	Hi-z	H	L	H	L
High temperature Detection Mode	H	-	-	-	-	↑	↑	↑	-	> Tmax	L	H	L	H	L
Hardware Mute Mode	H	L	-	-	-	↑	↑	↑	-	< Tmax	Hi-z	H	L	H	L
Over Current Detection Mode	H	H	-	> V_{OC1}	-	↑	↑	↑	-	-	L	H	L	H	L
	H	H	-	-	< V_{OC2}	↑	↑	↑	-	-	L	H	L	H	L
Clock Stop Detection Mode	H	H	-	< V_{OC1}	< V_{OC1} > V_{OC2}	↑	↑	↑	< F_{C1}	< Tmax	Hi-z	H	L	H	L
	H	H	-	↑	↑	↑	↑	↑	> F_{C2}	↑	Hi-z	H	L	H	L
Stereo Mode	H	H	L	↑	↑	↑	↑	↑	> F_{C1} < F_{C2}	↑	Hi-z	P	P	P	P
Monaural Mode	H	H	H	↑	↑	↑	↑	↑	↑	↑	Hi-z	P	P	*1	L

Note:

1) "-" means all input conditions.
2) "H" means "H" level, and "L" means "L" level. In addition, "P" means "Pulse oscillation condition".
3) "*1" means indefinite state.
4) Rch over current detection terminal "OCPLR and OCPHR" can not be operated in Monophonic mode.
5) In the over current detection mode, the mode is continued even if it goes out of the over current condition. The over current detection mode is canceled by protect reset mode.
6) All registers are initialized when V_{DD2} voltage (VDD-VSS) becomes below V_{VD} in the low voltage detection modes.
7) When YDA136 it-self heats higher than the unusual temperature (Tmax), it will become a high temperature detection mode.

●Digital Audio Signal Input Mode / Analog Audio Signal Input Mode

YDA136 can input both Digital Audio Signal and Analog Audio Signal.
In case of input for the digital audio signal, be sure to connect DAC output terminal (AOL, AOR) and electron volume input terminal (AIL, AIR) through capacitor for DC cut.
In addition, in case of input for the analog audio signal; be sure to connect an analog audio signal to electron volume input terminal (AIL,AIR) through a capacitor for DC cut.
At this time, the output of DAC can be made into High-Z by setting the DAC input format of a control register as MODE8.

■Functional Explanation of Operations

●Description of Registers

The volume register and the control register are allocated to address “0” and “1” in the register, respectively. Each 14-bit register is mapped as follows.

Register Map

	Address	Bit													
		D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Volume Register	0	R6	R5	R4	R3	R2	R1	R0	L6	L5	L4	L3	L2	L1	L0
Control Register	1	ZERO	CF	OSFN	MOD2	MOD1	MOD0	FS1	FS0	T5	T4	T3	T2	T1	T0

R6…R0 : Rch Volume Register
L6…L0 : Lch Volume Register
ZERO : Volume Zero-cross Function Selection Register
CF : Carrier Clock Frequency Selection Register
OSFN : Over Sampling Filter Function Selection Register
MOD2…0 : DAC Input Format Selection Register
FS1…0 : Over Sampling Mode Selection Register
T5…T0 : (Reserved) Be held at “0.”

●Volume Register

Volume Register	L6 R6	L5 R5	L4 R4	L3 R3	L2 R2	L1 R1	L0 R0
vol=Mute	1	1	1	1	1	1	1
vol= 6dB	1	1	1	1	1	1	0
vol= 5dB	1	1	1	1	1	0	1
vol= 4dB	1	1	1	1	1	0	0
vol= 3dB	1	1	1	1	0	1	1
vol= 2dB	1	1	1	1	0	1	0
vol= 1dB	1	1	1	1	0	0	1
vol= 0dB	1	1	1	1	0	0	0
vol= -1dB	1	1	1	0	1	1	1
vol= -2dB	1	1	1	0	1	1	0
vol= -3dB	1	1	1	0	1	0	1
vol= -4dB	1	1	1	0	1	0	0
vol= -5dB	1	1	1	0	0	1	1
vol= -6dB	1	1	1	0	0	1	0
vol= -7dB	1	1	1	0	0	0	1
vol= -8dB	1	1	1	0	0	0	0
vol= -9dB	1	1	0	1	1	1	1
vol= -10dB	1	1	0	1	1	1	0
vol= -11dB	1	1	0	1	1	0	1
vol= -12dB	1	1	0	1	1	0	0
vol= -13dB	1	1	0	1	0	1	1
vol= -14dB	1	1	0	1	0	1	0
vol= -15dB	1	1	0	1	0	0	1
vol= -16dB	1	1	0	1	0	0	0
vol= -17dB	1	1	0	0	1	1	1
vol= -18dB	1	1	0	0	1	1	0
vol= -19dB	1	1	0	0	1	0	1
vol= -20dB	1	1	0	0	1	0	0
vol= -21dB	1	1	0	0	0	1	1
vol= -22dB	1	1	0	0	0	1	0
vol= -23dB	1	1	0	0	0	0	1
vol= -24dB	1	1	0	0	0	0	0
vol= -25dB	1	0	1	1	1	1	1
vol= -26dB	1	0	1	1	1	1	0
vol= -27dB	1	0	1	1	1	0	1
vol= -28dB	1	0	1	1	1	0	0
vol= -29dB	1	0	1	1	0	1	1
vol= -30dB	1	0	1	1	0	1	0
vol= -31dB	1	0	1	1	0	0	1
vol= -32dB	1	0	1	1	0	0	0
vol= -33dB	1	0	1	0	1	1	1
vol= -34dB	1	0	1	0	1	1	0
vol= -35dB	1	0	1	0	1	0	1
vol= -36dB	1	0	1	0	1	0	0
vol= -37dB	1	0	1	0	0	1	1
vol= -38dB	1	0	1	0	0	1	0
vol= -39dB	1	0	1	0	0	0	1
vol= -40dB	1	0	1	0	0	0	0
vol= -41dB	1	0	0	1	1	1	1
vol= -42dB	1	0	0	1	1	1	0
vol= -43dB	1	0	0	1	1	0	1
vol= -44dB	1	0	0	1	1	0	0
vol= -45dB	1	0	0	1	0	1	1
vol= -46dB	1	0	0	1	0	1	0
vol= -47dB	1	0	0	1	0	0	1
vol= -48dB	1	0	0	1	0	0	0
vol= -49dB	1	0	0	0	1	1	1
vol= -50dB	1	0	0	0	1	1	0
vol= -51dB	1	0	0	0	1	0	1
vol= -52dB	1	0	0	0	1	0	0
vol= -53dB	1	0	0	0	0	1	1
vol= -54dB	1	0	0	0	0	1	0
vol= -55dB	1	0	0	0	0	0	1
vol= -56dB	1	0	0	0	0	0	0

Volume Register	L6 R6	L5 R5	L4 R4	L3 R3	L2 R2	L1 R1	L0 R0
vol= -57dB	0	1	1	1	1	1	1
vol= -58dB	0	1	1	1	1	1	0
vol= -59dB	0	1	1	1	1	0	1
vol= -60dB	0	1	1	1	1	0	0
vol= -61dB	0	1	1	1	0	1	1
vol= -62dB	0	1	1	1	0	1	0
vol= -63dB	0	1	1	1	0	0	1
vol= -64dB	0	1	1	1	0	0	0
vol= -65dB	0	1	1	0	1	1	1
vol= -66dB	0	1	1	0	1	1	0
vol= -67dB	0	1	1	0	1	0	1
vol= -68dB	0	1	1	0	1	0	0
vol= -69dB	0	1	1	0	0	1	1
vol= -70dB	0	1	1	0	0	1	0
vol= -71dB	0	1	1	0	0	0	1
vol= -72dB	0	1	1	0	0	0	0
vol= -73dB	0	1	0	1	1	1	1
	0	1	0	1	1	1	0
	0	1	0	1	1	0	1
	0	1	0	1	1	0	0
	0	1	0	1	0	1	1
	0	1	0	1	0	1	0
	0	1	0	1	0	0	1
	0	1	0	1	0	0	0
	0	1	0	0	1	1	1
	0	1	0	0	1	1	0
	0	1	0	0	1	0	1
	0	1	0	0	1	0	0
	0	1	0	0	0	1	1
	0	1	0	0	0	1	0
	0	1	0	0	0	0	1
	0	1	0	0	0	0	0
	0	0	1	1	1	1	1
	0	0	1	1	1	1	0
	0	0	1	1	1	0	1
	0	0	1	1	1	0	0
	0	0	1	1	0	1	1
	0	0	1	1	0	1	0
	0	0	1	1	0	0	1
	0	0	1	1	0	0	0
vol=Mute	0	0	1	0	1	1	1
	0	0	1	0	1	1	0
	0	0	1	0	1	0	1
	0	0	1	0	1	0	0
	0	0	1	0	0	1	1
	0	0	1	0	0	1	0
	0	0	1	0	0	0	1
	0	0	1	0	0	0	0
	0	0	0	1	1	1	1
	0	0	0	1	1	1	0
	0	0	0	1	1	0	1
	0	0	0	1	1	0	0
	0	0	0	1	0	1	1
	0	0	0	1	0	1	0
	0	0	0	1	0	0	1
	0	0	0	1	0	0	0
	0	0	0	0	1	1	1
	0	0	0	0	1	1	0
	0	0	0	0	1	0	1
	0	0	0	0	1	0	0
	0	0	0	0	0	1	1
	0	0	0	0	0	1	0
	0	0	0	0	0	0	1
	0	0	0	0	0	0	0

●Volume Zero-cross Function Selection

Control Register	ZERO	CF	OSFN	MOD2	MOD1	MOD0	FS1	FS0	T5	T4	T3	T2	T1	T0
Zero-cross Function Termination	0	*	*	*	*	*	*	*	*	*	*	*	*	*
Zero-cross Function Operation	1	*	*	*	*	*	*	*	*	*	*	*	*	*

After a rewrite of register, be sure to cancel mute after waiting for $T_{ZERO.}$

●Carrier Clock Frequency Selection

Control Register	ZERO	CF	OSFN	MOD2	MOD1	MOD0	FS1	FS0	T5	T4	T3	T2	T1	T0
Carrier Frequency＝524kHz	*	0	*	*	*	*	*	*	*	*	*	*	*	*
Carrier Frequency＝466kHz	*	1	*	*	*	*	*	*	*	*	*	*	*	*

After rewrite of register, be sure to cancel mute after waiting for T_{CF}.

●Over Sampling Filter Function Selection

Control Register	ZERO	CF	OSFN	MOD2	MOD1	MOD0	FS1	FS0	T5	T4	T3	T2	T1	T0
Over Sampling Filter Operation	*	*	0	*	*	*	*	*	*	*	*	*	*	*
Over Sampling Filter Termination	*	*	1	*	*	*	*	*	*	*	*	*	*	*

After a rewrite of register, be sure to cancel mute after waiting for T_{OSFN}.

●DAC Input Format Selection

Control Register	ZERO	CF	OSFN	MOD2	MOD1	MOD0	FS1	FS0	T5	T4	T3	T2	T1	T0
MODE1	*	*	*	0	0	0	*	*	*	*	*	*	*	*
MODE2	*	*	*	0	0	1	*	*	*	*	*	*	*	*
MODE3	*	*	*	0	1	0	*	*	*	*	*	*	*	*
MODE4	*	*	*	0	1	1	*	*	*	*	*	*	*	*
MODE5	*	*	*	1	0	0	*	*	*	*	*	*	*	*
MODE6	*	*	*	1	0	1	*	*	*	*	*	*	*	*
MODE7	*	*	*	1	1	0	*	*	*	*	*	*	*	*
MODE8	*	*	*	1	1	1	*	*	*	*	*	*	*	*

After a rewrite of register, be sure to cancel mute after waiting for $T_{MOD.}$

●Over Sampling Mode Selection

Control Register	ZERO	CF	OSFN	MOD2	MOD1	MOD0	FS1	FS0	T5	T4	T3	T2	T1	T0
4x Mode	*	*	*	*	*	*	0	0	*	*	*	*	*	*
2x Mode	*	*	*	*	*	*	0	1	*	*	*	*	*	*
1x Mode	*	*	*	*	*	*	1	0	*	*	*	*	*	*
Auto Mode	*	*	*	*	*	*	1	1	*	*	*	*	*	*

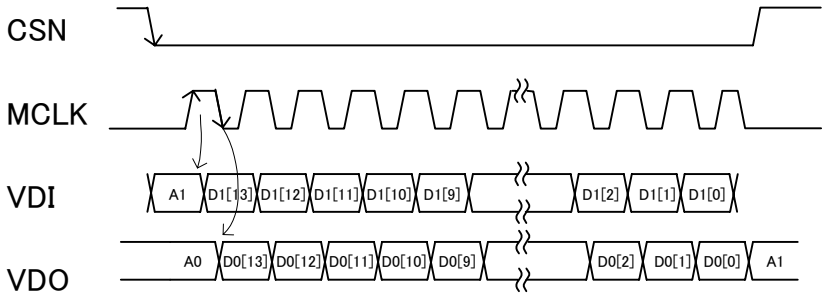
After a rewrite of register, be sure to cancel mute after waiting for T_{FS}.

■MPU Interface Function

By using the following three terminals “CSN, MCLK, and VDI”, data is written into Volume register and Control register.
In case of writing data in the Control register, be sure to set mute to Volume register in advance. After a write of Control register or after the given time (T_{ZERO}, T_{CF}, T_{OSFN}, T_{MOD}, and T_{FS}), be sure to cancel mute condition.

●Input Format

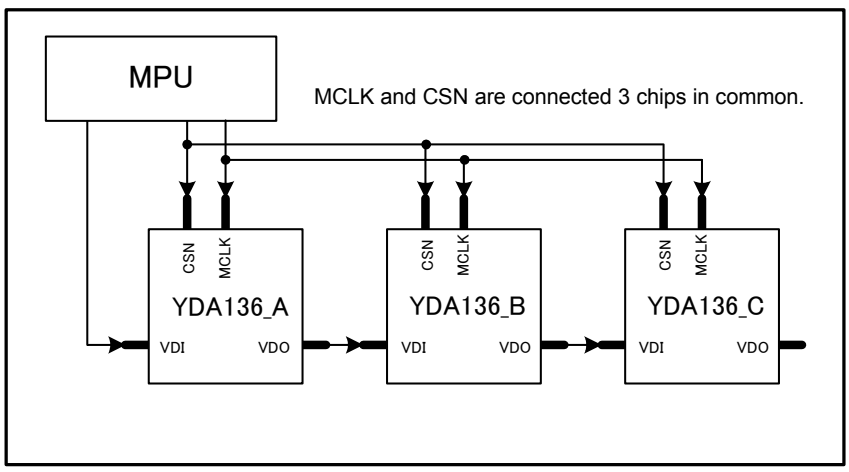
Please input the data of each 14-bit register into a VDI terminal in MSB first following address bits. The data input from VDI terminal is taken into internal shift register at the rising edge of MCLK terminal when CSN terminal is “L.” The data input into shift register is written into the register of the appointed address at the rising edge of CSN terminal.
All the values of registers after a power up are set to “0.”
After a power supply starting, the MPU interface works after passing over a serial access prohibition time (T_{PUP}).
Be sure to perform a power supply staring first, and then perform a write of the data to a register after a serial access prohibition time (T_{PUP}).



Here, A1 and D1 [13:0] indicates a register to update and data. In addition, A0 and D0 [13:0] indicates a data input into VDI terminal before 16-clock.

●Daisy-chain

Multiple Daisy-chain connections for multi-channel system are available in YDA136. For example, 6ch system can be realized by connecting three YDA136 with Daisy-chain connection.
By connecting a VDO terminal of first YDA136 to VDI terminal of the second YDA136; and then, connecting a VDO output of second YDA136 to a VDI terminal of the third YDA136, it becomes available to control those three YDA136 simultaneously without a complex addressing.
The data in which it overflowed from the internal 15-bit shift register among the data inputted into each VDI terminal of YDA136 is output from a VDO terminal synchronizing with falling edge of a MCLK terminal.
By setting CSN terminal to “L” during the number of YDA136×15-clock which daisy-chain connection was made, an input data is taken into each shift register of YDA136.
Then, writing is simultaneously performed to a volume register (control register) from the shift register of all YDA136 connected to the daisy-chain by setting the CSN terminal of YDA136 to “H.”



■DAC Function

YDA136 has a 24-bit×2ch of DAC.
The DAC supports the following eight kinds of sampling frequencies (Fs), and it has an over sampling filter corresponding to each sampling frequencies.

32kHz、44.1kHz、48kHz、64kHz、88.4kHz、96kHz、176.4kHz、192kHz

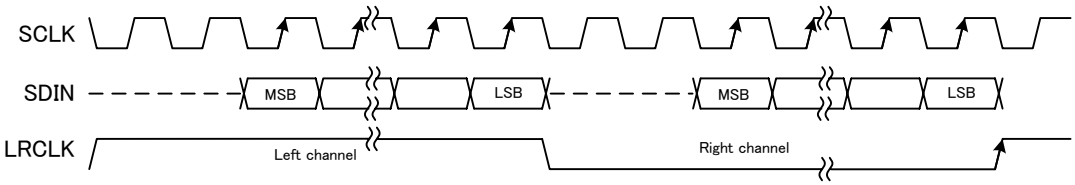
The output full-scale of this DAC is 1Vrms.

●DAC Interface

Be sure to input a digital audio signal from the following three terminals, SDIN, LRCLK, and SCLK.
DAC interface of YDA136 supports the seven DAC input formats.
Be sure to set up control registers, MOD2, MOD1, and MOD0, and then select a DAC input format to use.
When using the YDA136 as Digital Audio Signal mode, be sure not to stop a SCLK signal except when electronic volume is mute, protection reset mode, or hard mute mode.

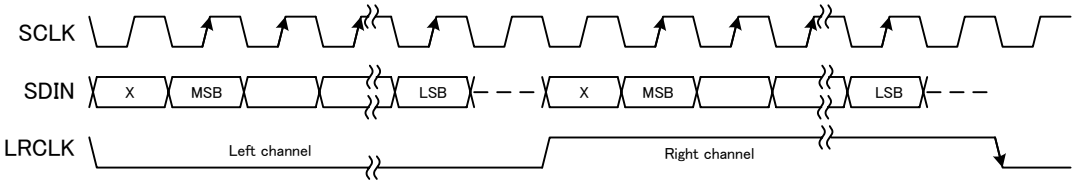
DAC Input Format

MODE1(16bit) MODE2(20bit) MODE3(24bit)



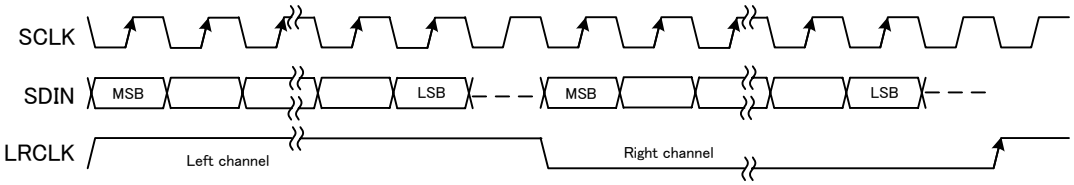
A SDIN bit is sampled by the rising edge of SCLK.
When LRCLK is "H", be sure to input data for Left channel by right justified.
When LRCLK is "L", be sure to input data for Right channel by right justified.
SDIN data is written into a DAC data register by the rising edge of LRCLK.
64-clock for one-word.

MODE4(16bit) MODE5(20bit) MODE6(24bit)



A SDIN bit is sampled by the rising edge of SCLK.
When LRCLK is "L", be sure to input data for Left channel in left justified with a vacant bit.
When LRCLK is "H", be sure to input data for Right channel in left justified with a vacant bit.
SDIN data is written into a DAC data register by the falling edge of LRCLK.
64-clock for one-word.

MODE7



A SDIN bit is sampled by the rising edge of SCLK.
When LRCLK is "H", be sure to input data for Left channel by right justified.
When LRCLK is "L", be sure to input data for Right channel by right justified.
SDIN data is written into a DAC data register by the rising edge of LRCLK.
64-clock for one-word.

MODE8

Analog Audio Signal Input Mode

●Over Sampling Filter

Be sure to set up the Over Sampling mode according to a sampling frequency (Fs) of audio signals to input.
Over sampling filter mode can be set up by FS1 and FS0 in the control register.
In addition, an over sampling filter can be bypassed by the setting of control register OSF.

When Fs is 32kHz, 44.1kHz or 48kHz	: Sets up to the 4x mode.
When Fs is 64kHz, 88.2kHz, or 96kHz	: Sets up to the 2x mode.
When Fs is 176.4kHz or 192kHz	: Sets up to the 1x mode.

When it is set as Auto mode, the above mentioned over sampling modes are set up by detecting a sampling frequency (Fs) of audio signal which was input.

■Volume Function

YDA136 has the electronic volume which can be set up in the range from +6dB to -73dB by 1dB step.
By inputting an analog signal from AIL (AIR) terminal, and attenuating with the set up volume value, this electronic volume outputs a differential analog signal from an OPL (OPR) terminal and OML (OMR) terminal.
Non-inverted signal from OPL (OPR) terminal and inverted signal from OML (OMR) terminal is output.
The maximum input level is 1Vrms and the maximum output level is 1Vrms.
Be sure to set a volume value to a volume register through a MPU serial data interface.
Moreover, in order to suppress the noise at the time of volume value change, a mode (Zero-cross mode) which changes a volume value when an output signal carries out a zero-cross, is provided as an option.

●Volume Register

D [13:7] of a volume register shows the volume value of R channels, and D [6:0] shows the volume value of L channels.
"1111111" and from "0101110" to "0000000" becomes mute among each volume value.
At this time, a DAC output signal turns into a non-signal irrespective of an input.

●Zero-cross Mode

This is the volume change mode, which reduces the noise generated at the time of change of the volume value of electronic volume.
When this mode is selected, the volume value is changed under the following conditions.

- At the time of an audio signal carries out a Zero-cross
- After the volume change is set up
- After the volume value setting time ($T_{ZEROWAIT}$)

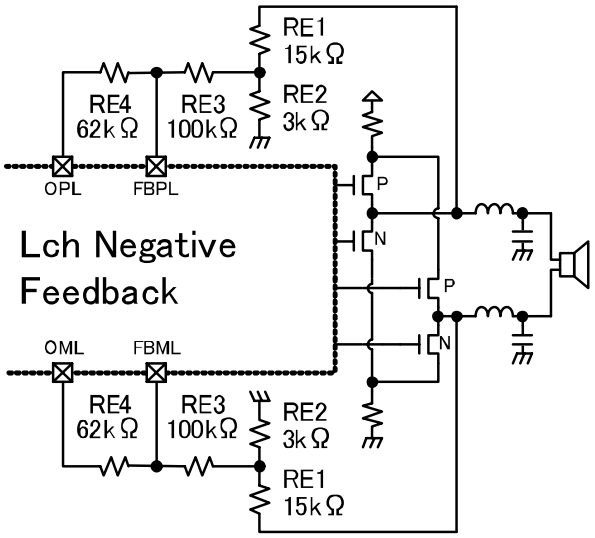
When not selected, the volume is changed regardless of the input after the volume setting.
By ZERO of a control register, Zero-cross mode can be set.

■Digital Amplifier Function

YDA136 has a 2-channel differential analog signal input digital amplifier controller.
This digital amplifier controller consists of High-Side and Low-Side PowerMOSFET drivers and a PWM circuit.
By combining the two sets of Pch/Nch PowerMOSFET in each channel, a digital amplifier (60W to 100W) can be configured.
To each PowerMOSFET driver, it is possible to set up an off-time individually, and it can be set as the optimal driver according to PowerMOSFET to be used.
AM intermodulation can be performed with AM reception interference reduction function.
Moreover, it can be optimized to the digital amplifier which has a lower distortion by adding a filter element to a PWM circuit.

●Gain Setup Method

The gain of digital amplifier can be set up by external resistance (RE1 to RE4).



The gain of digital amplifier can be calculated with the following formula.

$$Av(dB) = 20 \cdot \log\left(\frac{RE1 \cdot RE2 + RE2 \cdot RE3 + RE1 \cdot RE3}{RE2 \cdot (RE4 + 400\Omega)}\right)$$

However, be sure to set RE4 as more than 10kΩ according to the capability of a built-in operational amplifier.

●Characteristic Improvement by External Filter Element Connection

Although it is possible to realize high performance digital amplifier by the PWM circuit, by adding resistor and a capacitor between DBPL(FBPR) and ITPL (ITPR), and between FBML (FBMR) and ITML (ITMR), it is possible to optimize a circuit further and to improve distortion rate.

●Clock Input

YDA136 operates synchronizing with 4.19MHz clock.
Be sure to connect a 4.16MHz CERALOCK or to supply a clock to YDA136 from the outside.
Be sure to always supply a clock except protection reset mode and hard mute mode.
When using a CERALOCK, be sure to set MSSEL terminal to “L” and to set YDA136 to a master mode.
In case of supplying a clock from the outside, be sure to set MSSL terminal to “H” and to set YDA136 to a slave mode.

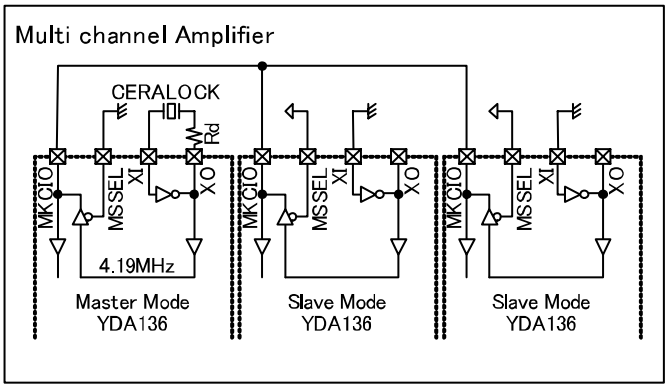
Master mode

Be sure to set MSSEL terminal to “L.”
Connects CELALOCK to XI and XO terminal.
Be sure to set the oscillation frequency to 4.19MHz.
At this time, a master clock (4.19MHz) is output from a MCKIO terminal.

Slave mode

Be sure to set MSSEL terminal to “H.”
Be sure to input a master clock (4.19MHz) into a MCKIO terminal.
At this time, be sure to set XI terminal to “L” and set XO terminal to open state.

When making a multi channel amplifier by using multiple YDA136, a system with little interference between channels can be constituted by using one YDA136 in master mode, and using the remainder in slave mode as shown in the following figure.

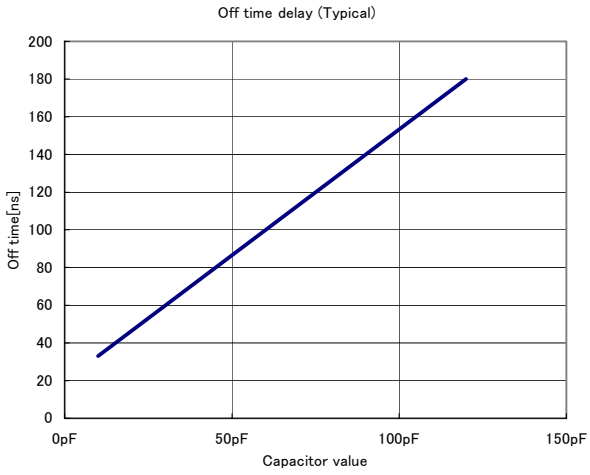


●AM Reception Interference Reduction Function

YDA136 outputs the pulse made by modulating the career clock, which is made by dividing the input master clock.
In order to reduce cross talk caused by the coincidence between harmonics of the output pulse and AM radio frequency, YDA136 has the changing (frequency hopping) function of two carrier clock frequencies.
A carrier clock frequency can be chosen by the control register CF.

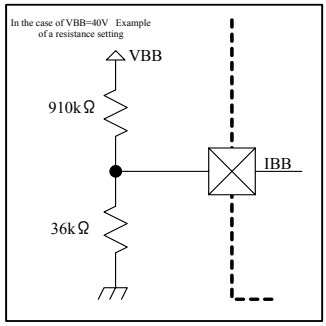
●Off-time Setup Function

A setup of an off-time is individually possible for YDA136 to the High-Side driver and Low-Side driver of Lch and each Rch.
Off-time adjustment of the Low-Side driver of Lch and each Rch is possible by the capacitor that is connected to a DLYLL terminal and a DLYLR terminal.
Moreover, off-time adjustment of the High-Side driver of Lch and each Rch is possible by the capacitor connected to a DLYHL terminal and a DLYHR terminal.
Relation between capacitance value of the capacitor and the relation of an off-time is shown in the figure.
(Under characteristic adjustment)



●IBB Terminal Setting

In the PWM circuit, the IBB terminal is used and VBB power supply voltage is feedbacked. Simultaneously, under voltage detection of VBB power supply voltage is performed by monitoring the voltage of the terminal.
After making 1.5V by dividing VBB voltage with resistors, an then be sure to input it into IBB terminal.
Set for the voltage of the IBB terminal not to become 1.6V or more even if the VBB voltage moves.

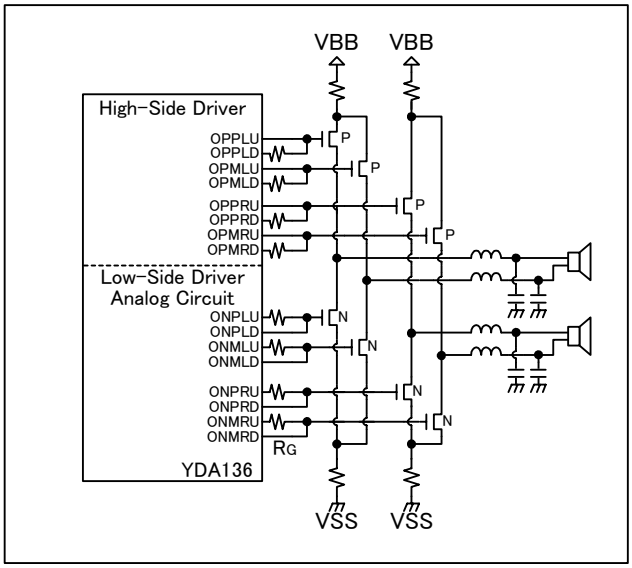


●PowerMOSFET Drive Function

Since it is BTL connection digital amplifier, external connection of two sets per channel of Pch and Nch PowerMOSFET is made.
A High-Side driver output is connected to Pch PowerMOSFET, and a Low-Side driver output is connected to Nch PowerMOSFET as shown below.

Non-inverted side Pch PowerMOSFET : Be sure to connect to OPPLU and OPPLD (OPPRU,OPPRD). (High-Side Driver Output)
Non-inverted side Nch PowerMOSFET : Be sure to connect to ONPLU and ONPLD (ONPRU,ONPRD). (Low-Side Driver Output)
Inverted side Pch PowerMOSFET : Be sure to connect to OPMLU and OPMLD (OPMRU,OPMRD). (High-Side Driver Output)
Inverted side Nch PowerMOSFET : Be sure to connect to ONMLU and ONMLD (ONMRU,ONMRD) (Low-Side Driver Output)

There are two output terminals to one PowerMOSFET, and they mean the pull-up output and the pull-down output, respectively.
By connecting gate resistor (R_G) between each driver output and PowerMOSFET, slew-rate of both pull-up and pull-down side separately.
In the example of peripheral circuit connection, resistor (R_G) of 20Ω is connected with the pull-down side output of Pch PowerMOSFET and the pull-up side output of Nch PowerMOSFET.



In addition, total amount of electric charges (Qg) of gates in PowerMOSFET, which is used by connecting to YDA136, should be 20nC or less (Vgs=5V).

■Protect Function

●Over Current Detection Function

YDA136 has a function to perform an over current protection by detecting a voltage drop of the current detection resistor connected to the source side of PowerMOSFET.
When the voltage of an over-current detection terminal fulfills the following conditions, it judges that it is in an over-current condition, and becomes over-current detection mode, and then a circuit is protected.

Voltage to be monitored	Over-current detection mode threshold
Low-Side over-current detection terminal (OCPLL, OCPLR) Voltage	$< V_{OC2}$
High-Side over-current detection terminal (OCPHL, OCPHR) Voltage and VBB Potential difference	$> V_{OC1}$

In the example of peripheral circuit connection, the following four over-current conditions are detected, and then it becomes an over-current detection mode.

- A condition in which signals after LC filter and VSS power supply is shorted.
- A condition in which signals after LC filter of non-inverted side and signals after LC filter of inverted side is shorted.
- A condition in which one side of a speaker was connected to LC filter, and another side of a speaker is shorted to the VSS power supply.

In over-current detection mode, PROTN terminal is set to "L", simultaneously it turns off all PowerMOSFET (hard mute) and protects a circuit.
After it is made to over-current detection mode, even if an over-current condition is canceled, it is not canceled but is held as it is.
Over-current detection mode can be canceled by intercepting a power supply or setting a PRSTN terminal to "L" at once.

●Power Detection Function

YDA136 monitors the following three kinds voltage.
When which voltage is less than regular voltage, it becomes low voltage detection mode.

Voltage to be monitored	Constant Voltage Detection Mode Threshold
IBB Terminal Voltage(It is proportional to the voltage between V_{BB} and V_{SS})	V_{IB2}
V_{DD1} (Voltage between V_{BB} and V_{BS})	V_{VB2}
V_{DD2} (Voltage between V_{DD} and V_{SS})	V_{VD2}

Here, since the IBB terminal has input the signal which divided VBB voltage, the IBB terminal will act as the monitor of the VBB voltage.
Hard mute is operated in low voltage detection mode.
Among these, all registers are reset when V_{DD2} voltage is less than threshold voltage (V_{VD2}).
Then, when three kinds of power supply voltage rises and a low voltage detection mode threshold is exceeded altogether, the low voltage detection mode is canceled and a hard mute is also canceled after starting standby time (T_{WAIT}).

●Starting Standby Time Setup

Starting standby time (T_{WAIT}) can be set up by connecting a capacitor to the DET terminal of YDA136.
Be sure to set up to usually be set to T_{WAIT}>=600msec for internal initialization of YDA136.
The value of starting standby time (T_{WAIT}) and capacity (C_{DET}) of and the capacitor linked to a DET terminal serves as the following relations.

$$T_{WAIT} = 60(k\Omega) \times C_{DET}(F)$$

In the case of the capacity value (10 μ F) of the capacitor in the example of peripheral circuit connection, T_{WAIT} is set to 600msec.

●Clock Stop Detection Function

YDA136 becomes clock stop detection mode, when a career clock frequency exceeds a maximum (F_{C1}) of operation or it is less than a minimum (F_{C1}).
Hard mute is carried out in clock stop detection mode.
If a career clock frequency enters within normal limits, clock stop detection mode will be canceled and hard mute will be canceled.

●High Temperature Detection Function

YDA136 is acting as the internal monitor of the temperature of YDA136 self, and when it becomes an unusual temperature exceeding Tjmax, it serves as high temperature detection mode.
In high temperature detection mode, a PROTN terminal is set to "L" at the same time it carries out hard mute.
Then, a PROTN terminal is set to "H" at the same time it cancels high temperature detection mode and cancels hard mute, when temperature falls and it becomes a normal range.

●Self-recovery function

By connecting a PROTN terminal and a PRSTN terminal, when a PROTN terminal is set to "L" by over-current detection and high temperature detection, it can be set as fixed time protection reset mode, and hard mute release (automatic return) can be carried out after starting standby time (T_{WAIT}).

■Control Function

●Hard Mute Function

YDA136 serves as hard mute mode, when a MUTEN terminal is "L."
In hard mute mode, they are all PowerMOSFETs. It turns off (hard mute).
Hard mute will be canceled if a MUTEN terminal is set to "H."
Rewriting of all registers is possible for during a hard mute mode period.

●Protect Reset Function

YDA136 serves as protection reset mode, when a PRSTN terminal is "L."
A PROTN terminal is set to "H" in protection reset mode.
Hard mute is carried out simultaneously, the circuit which operates inside IC is minimized, and consumption current is reduced.
After canceling protection reset mode, using a PRSTN terminal as "H", after starting standby time (T_{WAIT}), hard mute is canceled and a start of operation is carried out.
Rewriting of all registers is possible for during a hard mute mode period.
Moreover, a register is by protection reset mode. is not carried out.

●Monophonic Function

YDA136 serves as monophonic mode, when a MONO terminal is “H.”
In monophonic mode, only Lch outputs an audio signal, and all the circuits related to Rch is stopped.
Moreover, it becomes stereo mode when a MONO terminal is “L.”
In monophonic mode, the over-current detection function by the OCPLR terminal and the PCPHR terminal does not operate.
Please perform the change in monophonic mode and stereo mode at the time of interception of a power supply.
The change in the monophonic mode by the MONO terminal at the time of power supply impression and stereo mode is forbidden.

■Typical Voltage

Since a VREFL terminal and a VREFR terminal output $1/2*V_{DD2}$ voltage respectively, be sure to connect and stabilize a capacitor.

■Initialization / Power-down

●System Initialization

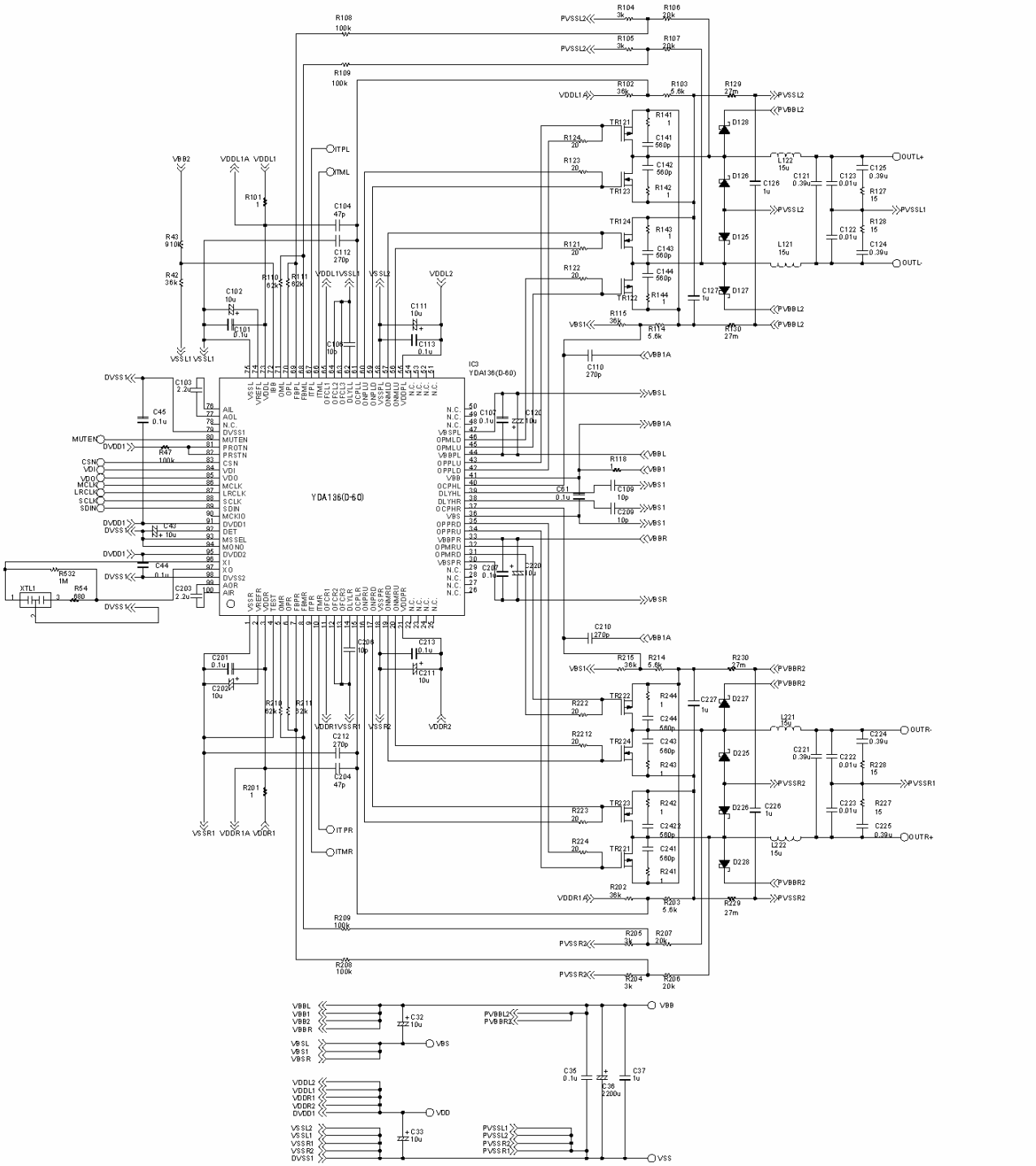
All registers are initialized when V_{DD2} voltage (VDD-VSS) becomes less than V_{VD} in low voltage detection modes.
The initial value of each register is “0.”

●Power-down

At the time of power interception, be sure to intercept a power after set it as a hard mute mode.

■Example of System Composition

●Example of peripheral circuit connection



■Electrical Characteristics

●Absolute Maximum Rating

Item	Symbol	Min	Max	Unit
VBB Power Supply Voltage	V_{BB}	−0.3	50	V
VBS Power Supply Voltage	V_{BS}	V_{BB}−7.0	V_{BB}+0.3	V
VDD Power Supply Voltage	V_{DD}	−0.3	7.0	V
High-Side Input Terminal Voltage Range*1)	V_{IN1}	V_{BS}−0.3	V_{BB}+0.3	V
Low-Side Input Terminal Voltage Range	V_{IN2}	−0.3	V_{DD}+0.3	V
Welding Temperature	Tjmax		125	ºC
Storage Temperature Range	T_{STG}	−50	125	ºC

*1) The voltage range to DLYHL, DLYHR, OCPHL, and OCPHR are indicated.

●Recommended Operation Condition

Item	Symbol	Min	Typ	Max	Unit
VBB Power Supply Voltage	V_{BB}	20		50	V
VBS Power Supply Voltage	V_{BS}	V_{BB}−4.75	V_{BB}−5.0	V_{BB}−5.25	V
VDD Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Speaker Impedance	R_L	4	6		Ω
Operation Ambient Temperature	Ta	−40	25	85	ºC

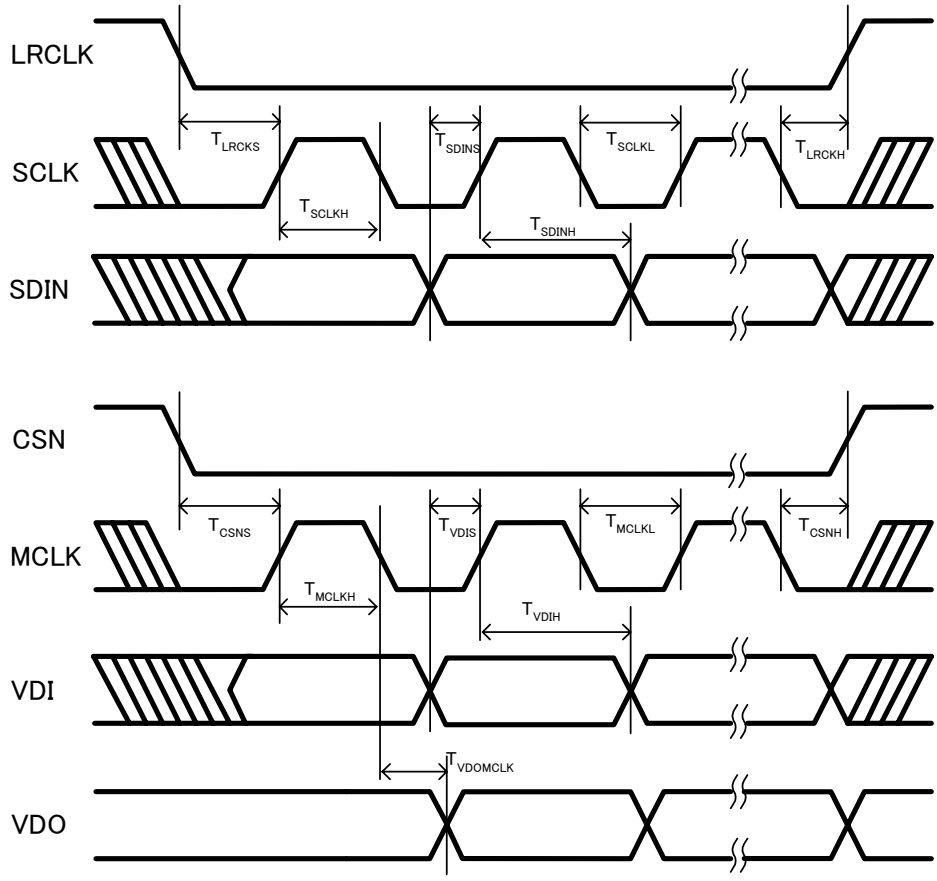
●DC Characteristics（Adjust Condition：V_{DD}＝5.0V, V_{BB}=40V, Ta=−40 to 85℃）

Item	Symbol	Min	Typ	Max	Unit
High-Side Driver H Level Output Voltage (I_{OH}=−100mA)	V_{OHPD}	V_{BB}−0.4			V
High-Side Driver L Level Output Voltage (I_{OL}=+100mA)	V_{OLPD}			V_{BS}+0.4	V
Low-Side Driver H Level Output Voltage (I_{OH}=−100mA)	V_{OHND}	V_{DD}−0.4			V
Low-Side Driver L Level Output Voltage (I_{OL}=+100mA)	V_{OLND}			0.4	V
XO Terminal H Level Output Voltage (I_{OH}=−80μA)	V_{OHXO}	V_{DD}−0.4			V
XO Terminal L Level Output Voltage (I_{OL}=+1.6mA)	V_{OLXO}			0.4	V
MCKIO Terminal H Level Output Voltage (I_{OH}=−80μA)	V_{OHMC}	V_{DD}−0.4			V
MCKIO Terminal L Level Output Voltage (I_{OL}=+1.6mA)	V_{OLMC}			0.4	V
PROTN Terminal L Level Output Voltage (I_{OL}=+1.6mA)	V_{OLPR}			0.4	V
Digital Terminal H Level Input Voltage	V_{IH}	2.2			V
Digital Terminal L Level Input Voltage	V_{IL}			0.8	V
MCKIO, MSSEL Terminal H Level Input Voltage	V_{IHMC}	0.7×V_{DD}			V
MCKIO, MSSELTerminal H Level Input Voltage	V_{ILMC}			0.3×V_{DD}	V
IBB Terminal Power Detection Threshold Voltage (Start)	V_{IB1}		0.75		V
High-Side Driver power Power Detection Threshold Voltage (Start)	V_{VB1}		4.0		V
High-Side Driver power Power Detection Threshold Voltage (CO)	V_{VB2}		3.8		V
Low-Side Driver power Power Detection Threshold Voltage (Start)	V_{VD1}		4.0		V
Low-Side Driver power Power Detection Threshold Voltage (CO)	V_{VD2}		3.8		V
High-Side Over-current Detection Thrshol Voltage	V_{OC1}		1.25		V
Low-Side Over-current Detection Thrshol Voltage	V_{OC1}		1.25		V
Low-Side Over-current Detection Thrshol Voltage	V_{OC2}		0.6		V
VREFL, VREFR Terminal Output Voltage	V_{REF}		2.5		V
Stereo Mode VBB Power Consumption (No-Signal)	I_{BB}		3		mA
Stereo Mode High-Side Power Consumption (No-Signal)	I_{D1}		35		mA
Stereo Mode Low-Side Power Consumption (No-Signal)	I_{D2}		50		mA
Mute Mode VBB Power Consumption	I_{BBM}		3		mA
Mute Mode High-Side Power Consumption	I_{D1M}		6		mA
Mute Mode Low-Side Power Consumption	I_{D2M}		28		mA
Protection Reset Mode VBB Power Consumption	I_{BBP}		3		mA
Protection Reset Mode High-Side Power Consumption	I_{D1P}		6		mA
Protection Reset Low-Side Power Consumption	I_{D2P}		10		mA

●AC Characteristic（Adjust Condition：V_{DD}＝5.0V, V_{DDH}=5.0V, V_{BB}=40V, Ta=－40 to 85℃）

Item	Symbol	Min	Typ	Max	Unit
SCLK Frequency	$1/T_{SCLK}$		*1)		MHz
SCLK High Time	T_{SCLKH}	40			ns
SCLK Low Time	T_{SCLKL}	40			ns
SDIN Input Setup Time	T_{SDINS}	20			ns
SDIN Input Hold Time	T_{SDINH}	20			ns
LRCK Setup Time	T_{LRCKS}	30			ns
LRCK Hold Time	T_{LRCKH}	30			ns
MCLK Frequency	F_{MCLK}			6.25	MHz
MCLK High Time	T_{MCLKH}	80			ns
MCLK Low Time	T_{MCLKL}	80			ns
VDI Input Setup Time	T_{VDIS}	20			ns
VDI Input Hold Time	T_{VDIH}	20			ns
CSN Setup Time	T_{CSNS}	30			ns
CSN Hold Time	T_{CSNH}	30			ns
VDO Output Delay (to MCLK Edge) （C_L=20pF）	$T_{VDOMCLK}$			60	ns

*1) $1/T_{SCLK}$=64Fs(Fs=32 to 192kHz)



●Audio Characteristic

(Measurement Condition: V_{DD}＝5.0V, V_{DDH}=5.0V, V_{BB}=40V, Ta=25℃, Fs=48kHz, Volume=0dB、100W Specifications (Gain=22.6dB+6dB), filter is as example of peripheral circuit connection, Speaker Impedance＝6Ω)

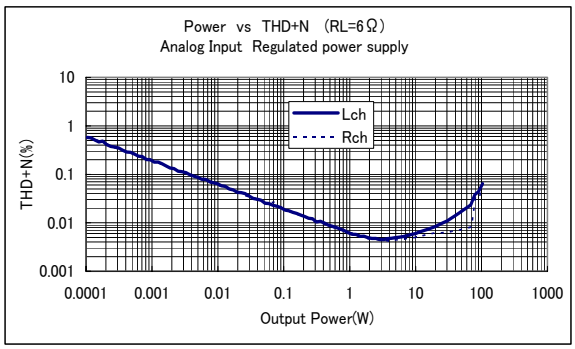
Item	Symbol	Min	Typ	Max	Unit
Distortion（Input=1kHz, Output=50W, at Digital Input）	THD+N		0.05		dB
Distortion（Input=1kHz, Output=50W、at Analog Input）	THD+N		0.03		dB
Residual Noise（Gain=22.6+6dB）	Vn		100		μV
Signal-Noise Ratio（A-filter, Gain=22.6+6dB）	SNR		100		dB
Channel Separation（Input=1kHz, Output=50W）	CS		80		dB

Note) All the values of audio characteristics were obtained by using our evaluation circumstance.
The characteristics may vary according to the Power MOSFET, coils, capacitors and pattern layout that are used in the system.

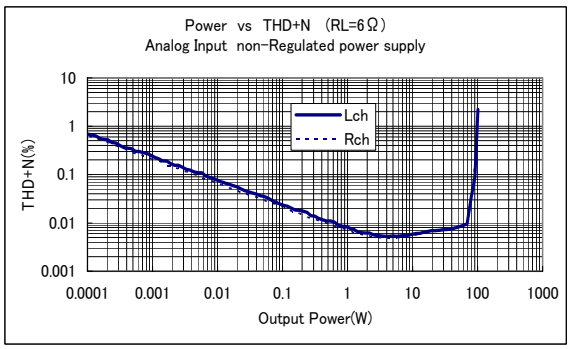
●Timing Rules and Regulations

Item	Symbol	Min	Typ	Max	Unit
Operation Standby Time (C_{DET}=10μF)	T_{WAIT}		0.6		s
Standby Time after a write of ZERO register	T_{ZERO}			10	ms
Standby Time after a write of CF register	T_{CF}			10	ms
Standby Time after a write of OSFN register	T_{OSFN}			10	ms
Standby Time after a write of MOD register	T_{MOD}			10	ms
Standby Time after a write of FS register	T_{FS}			10	ms

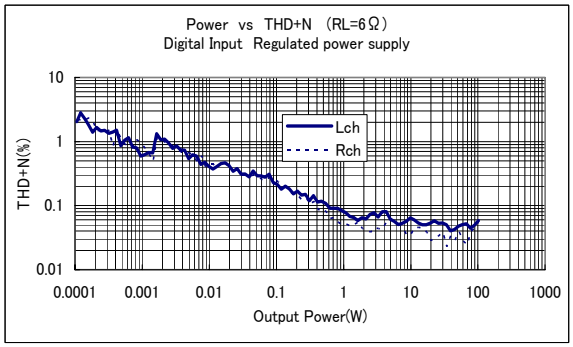
■Typical characteristics examples



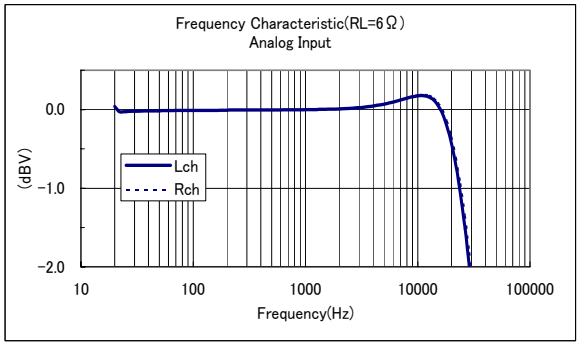
RL = 6Ω VBB = 40V VBS = 35V VDD = 5V
Freq = 1kHz Filter : <20kHz
PowerMOSFET : 2SJ545, 2SK2933(RENESAS)



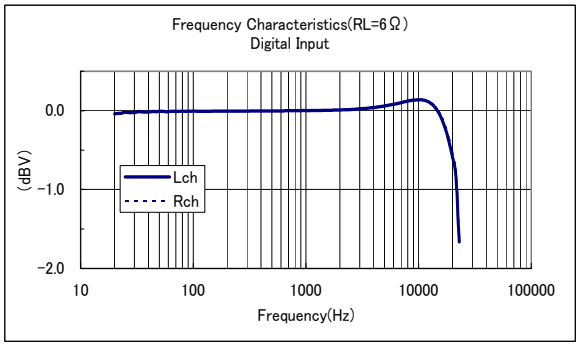
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PowerMOSFET : 2SJ545, 2SK2933(RENESAS)



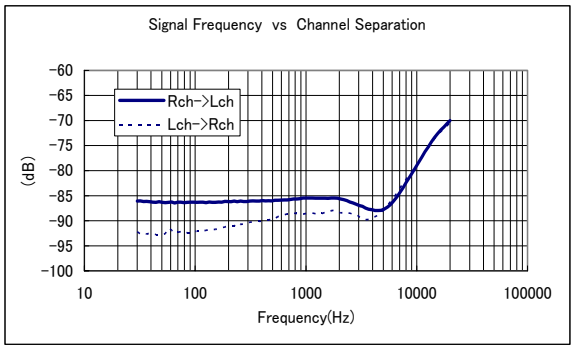
RL = 6Ω VBB = 40V VBS = 35V VDD = 5V
Freq = 1kHz(Fs = 48kHz 16bit ×4) Filter : <20kHz
PowerMOSFET : 2SJ545, 2SK2933(RENESAS)



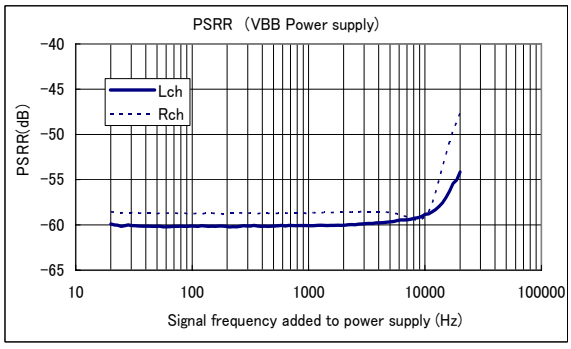
VBB = 40V VBS = 35V VDD = 5V Half Power
Lo = 15uH Co = 0.39uF RL = 6Ω
PowerMOSFET : 2SJ545, 2SK2933(RENESAS)



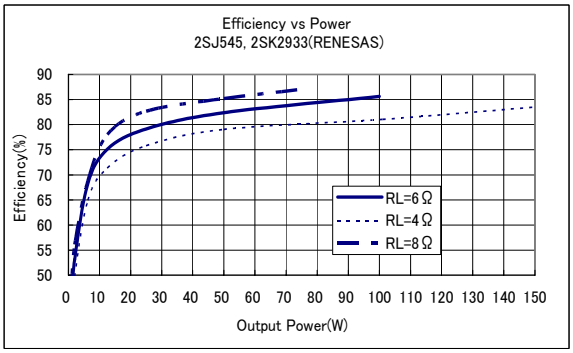
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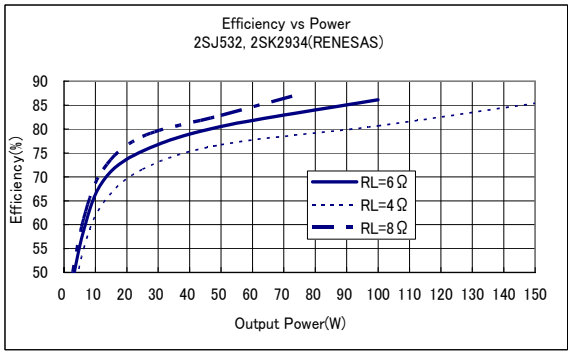
RL = 6Ω VBB = 40V VBS = 35V VDD = 5V Half Power
Analog Input Freq = 1kHz
PowerMOSFET : 2SJ545, 2SK2933(RENESAS)



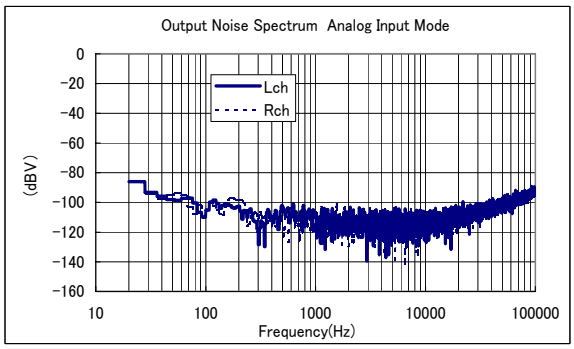
VBB = 40V±100mVrms VBS = 35V VDD = 5V RL = 6Ω
Analog Input Freq = 1kHz
PowerMOSFET : 2SJ545, 2SK2933(RENESAS)



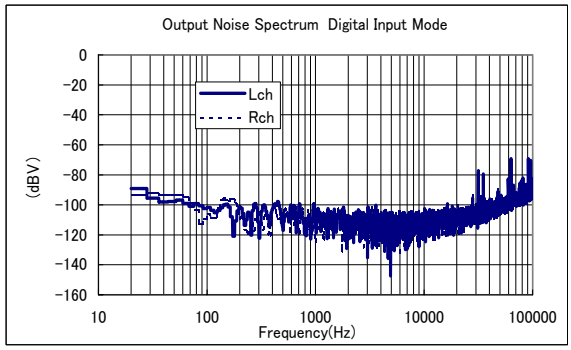
VBB = 40V VBS = 35V VDD = 5V
Freq = 1kHz(Fs = 48kHz 16bit ×4)
PowerMOSFET : 2SJ545, 2SK2933(RENESAS)



VBB = 40V VBS = 35V VDD = 5V
Freq = 1kHz(Fs = 48kHz 16bit ×4)
PowerMOSFET : 2SJ532, 2SK2934(RENESAS)



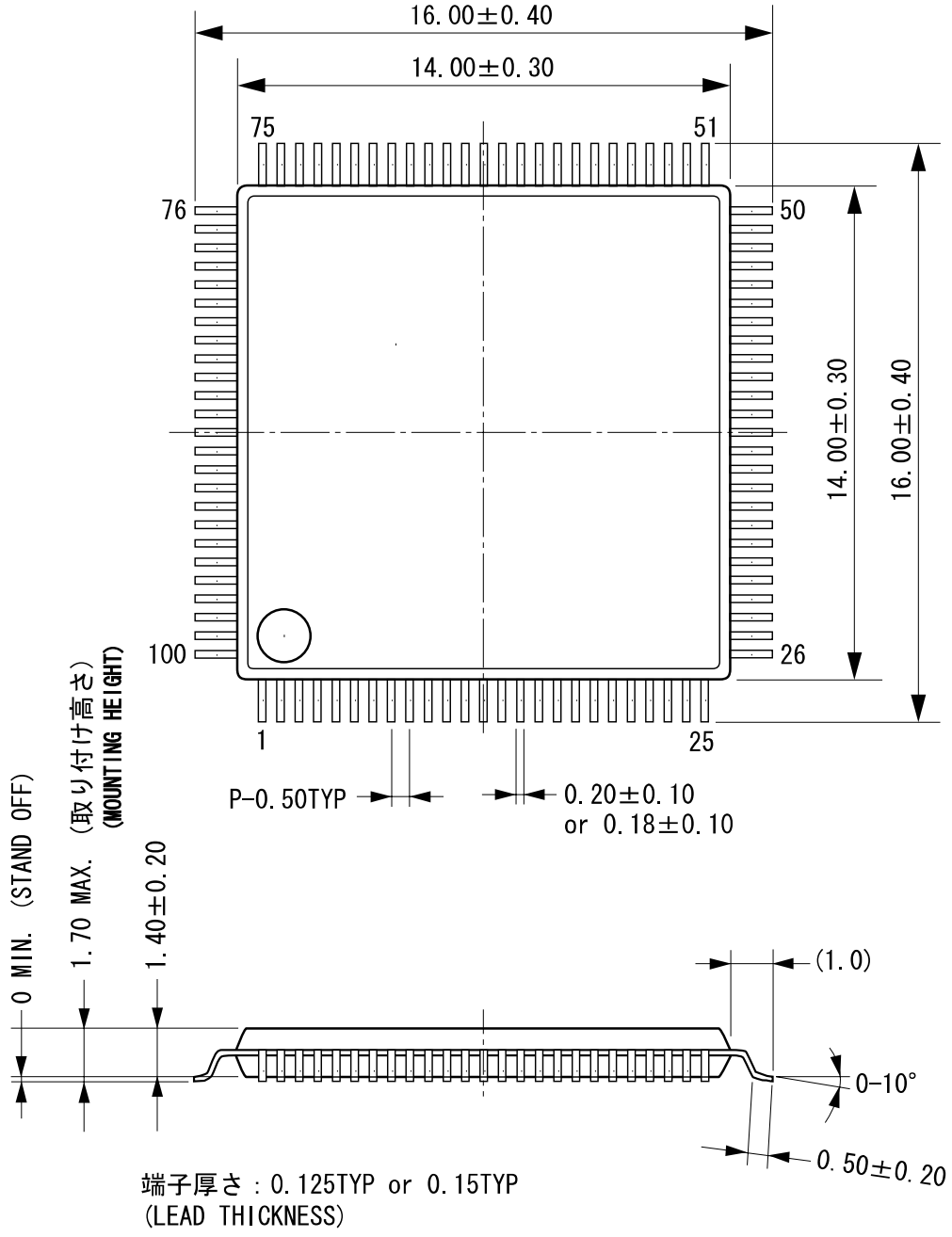
RL = 6Ω VBB = 40V VBS = 35V VDD = 5V
MOSFET : 2SJ545, 2SK2933(RENESAS)
PowerMOSFET : 2SJ545, 2SK2933(RENESAS)



RL = 6Ω VBB = 40V VBS = 35V VDD = 5V
MOSFET : 2SJ545, 2SK2933(RENESAS)
PowerMOSFET : 2SJ545, 2SK2933(RENESAS)

■Package Outline

C-PK100SP-1



モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位：mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

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