DS125DF111 Multi-Protocol 2-Channel 9.8 - 12.5 Gb/s Retimer

1 Features

- Pin Compatible Retimer Family
  - DS110DF111 with DFE: 8.5 - 11.3 Gbps
  - DS125DF111 with DFE: 9.8 - 12.5 Gbps
- Adaptive CTLE: 33 dB Max Boost at 6.25 GHz
- Self Tuning 5-Tap DFE
- Raw Equalized and Retimed Data Loopback
- Adjustable Transmit V_{OD}: 600 to 1300 mVp-p
- Settable Tx De-Emphasis Driver 0 to –12dB
- Low Power Consumption: 220 mW/Channel
- Locks to Half/Quarter/Eighth Data Rates for Legacy Support
- On-Chip Eye Monitor (EOM), PRBS Generator
- Input Signal Detection, CDR Lock Detection/Indicator
- Single 3.3-V or 2.5-V Power Supply
- SMBus, EEPROM, or Pin Based Configuration
- 4-mm x 4-mm, 24-Pin WQFN Package
- Operating Temp Range: –40°C to 85°C

2 Applications

- Front Port Optical Interconnects
- SFF-8431
- 10G/1G Ethernet
- CPRI

3 Description

The DS125DF111 is a dual channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS125DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR) and transmit driver on each channel.

The DS125DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < $1x10^{-15}$. For less demanding applications/interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible.

Each channel of the DS125DF111 independently locks to specific serial data at data rates from 9.8 to 12.5 Gbps or to any supported sub-rate of these data rates. This simplifies system design and lowers overall cost.

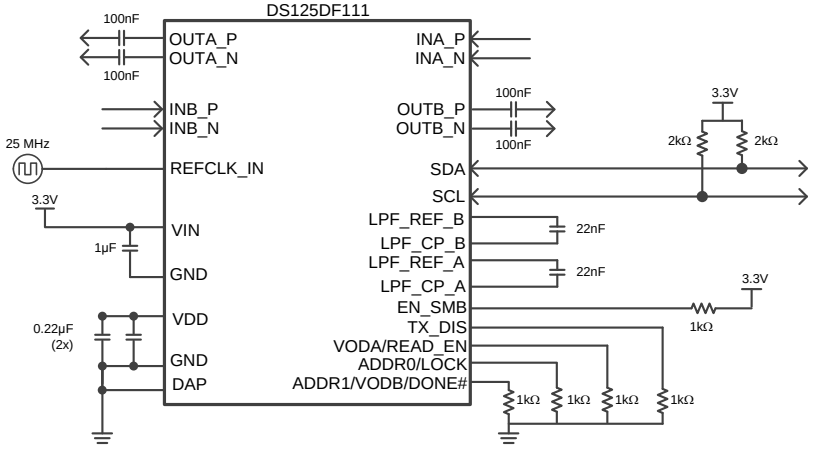
Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high speed serial data.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS125DF111	WQFN (24)	4.0 mm × 4.0 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

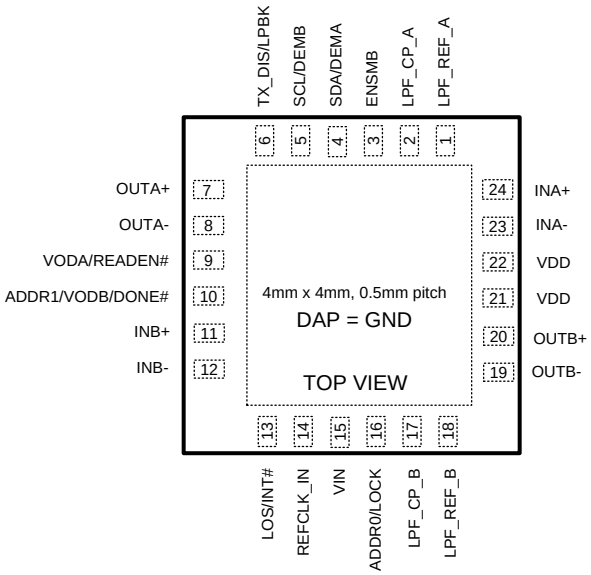
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2014) to Revision A	Page
• Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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5 Pin Configuration And Functions

RTW Package
24-Pin WQFN
Top View



Pin Functions

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
HIGH SPEED DIFFERENTIAL I/OS			
OUTA±	7, 8	O, CML	Inverting and non-inverting CML-compatible differential outputs. Outputs require AC coupling
OUTB±	20, 19	O, CML	Inverting and non-inverting CML-compatible differential outputs. Outputs require AC coupling
INA±	24, 23	I, CML	Inverting and non-inverting CML-compatible differential inputs. An on-chip 100 Ω terminating resistor connects INA+ to INA- Inputs require AC coupling. TI recommends 100 nF capacitors. Note that for SFP+ applications, AC coupling is included as part of the SFP+ module.
INB±	11, 12	I, CML	Inverting and non-inverting CML-compatible differential inputs. An on-chip 100 Ω terminating resistor connects INB+ to INB- Inputs require AC coupling. TI recommends 100 nF capacitors. Note that for SFP+ applications, AC coupling is included as part of the SFP+ module.
LOOP FILTER CONNECTION PIN			
LPF_CP_A, LPF_REF_A	2, 1	I/O, analog	Loop filter connection, place a 22 nF ± 10% capacitor in series between LPF_CP_A and LPF_REF_A
LPF_CP_B, LPF_REF_B	17, 18	I/O, analog	Loop filter connection, place a 22 nF ± 10% capacitor in series between LPF_CP_B and LPF_REF_B
REFERENCE CLOCK I/O			
REFCLK_IN	14	I, LVCMOS	25 MHz ± 100 ppm clock from external Oscillator

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Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
INDICATOR PINS			
LOCK	16	O, LVCMOS	LOCK VOH is referenced to V_{IN} voltage level. Note that this pin is shared with strap input functions read at startup. The Address value loaded into pin 16 (ADDR0) at startup changes the definition of the LOCK pin output. See the Shared Register Definition in Table 7 for more details.
LOS/INT#	13	O, Open Drain	Output is driven LOW when a valid signal is present on INA. Output is released when signal on INA is lost (LOS). This output can be redefined as an INT# signal which will be driven LOW for any of the following conditions.(1) 1. The EOM check returns a value below the HEO/VEO interrupt threshold. 2. CDR check returns lock/loss status. 3. Signal Detector returns detect/loss status.
SMBus MODE PINS			
ENSMB	3	I, 4-Level	System Management Bus (SMBus) enable pin HIGH = Register Access, SMBus Slave mode FLOAT = SMBus Master read from External EEPROM 20 K to GND = Reserved LOW = External Pin Control Mode. See section on *Pin Mode Limitation*
SDA	4	I, SMBus O, Open Drain	Data Input / Open Drain Output External pull-up resistor is required. Pin is 3.3 V LVCMOS tolerant(1)
SCL	5	I, SMBus O, Open Drain	Clock input in SMBus slave mode. Can also be an open drain output in SMBus master mode Pin is 3.3 V LVCMOS Tolerant(1)
TX_DIS	6	I, 4-Level	Disable the OUTB transmitter HIGH = OUTA Enabled/OUTB Disabled FLOAT = Reserved 20 K to GND = Reserved LOW = OUTA/OUTB Enabled (normal operation)
ADDR0	16	I, LVCMOS	This pin sets the SMBus address for the retimer. This pin is a strap input. The state is read on power-up to set the SMBus address in SMBus control mode. The latched value of ADDR0 read at startup will change the LOCK output definition. See the Shared Register Definition in Table 7 for more details.(2)
ADDR1/DONE#	10	IO, LVCMOS	This pin sets the SMBus address for the retimer in SMBus Slave Mode. DONE#. VOH is referenced to V_{IN} voltage level. DONE# goes low to indicate that the SMBus master EEPROM read has been completed in SMBus Master Mode(2)
READEN#	9	I, LVCMOS	Initiates SMBus master EEPROM read. When multiple DS125DF111 are connected to a single EEPROM, the READEN# input can be daisy chained to the DONE# output. In SMBus Slave Mode this pin should be tied to Logic 0. (3)
PIN CONTROL (ENSMB = LOW) (4)			
DEMA	4	I, 4-Level	Set CHA output de-emphasis level in pin control mode (3)
DEMB	5	I, 4-Level	Set CHB output de-emphasis level in pin control mode (3)
LPBK	6	I, 4-Level	HIGH = INA goes to OUTA, INB goes to OUTB FLOAT = INB goes to OUTA and OUTB 20 K to GND = INA goes to OUTA and OUTB LOW = INA goes to OUTB, INB goes to OUTA(3)
VODA	9	I, 4-Level	Set CHA output launch amplitude in pin control mode (3).
VODB	10	I, 4-Level	Set CHB output launch amplitude in pin control mode(3)

(1) The LOS/INT# pin is an open drain output which requires external pull-up resistor (typically connected to 2.5 V or 3.3 V for system logic compatibility) to achieve a HIGH level.
(2) This pin is shared with other functions.
(3) This pin is shared with other functions.
(4) When in pin control mode, the DS125DF111 device operates at 12.288, 9.8304, 6.144, 4.9152, 3.072, 2.4576, 1.536, or 1.2288 Gbps and has limited VOD and De-Emphasis control. See Table 9.

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Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
POWER			
V_{DD}	21, 22	Power	V_{DD} = 2.5 V ± 5%. See Figure 12. 3.3-V supply mode: V_{DD} = 2.5 V is supplied the internal output regulator. Pins only require de-coupling caps; no external supply is needed. 2.5-V supply mode: V_{DD} input = 2.5 V ± 5%.
V_{IN}	15	Power	Regulator Input (3)with Integrated Supply Mode Control. See Figure 12. 3.3-V supply mode: V_{IN} input = 3.3 V ± 10%. 2.5-V Mode Operation: V_{IN} Supply Input = 2.5 V ± 5%. Connect directly to V_{DD} supply pins.
DAP	PAD	Power	GND reference The exposed pad at the center of the package must be connected to ground plane of the board with at least 4 vias to lower the ground impedance and improve the thermal performance of the package

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

	MIN	MAX	UNIT
Supply Voltage (V_{DD})	–0.5	2.75	V
Supply Voltage (V_{IN})	–0.5	4	V
LVCMOS Input/Output Voltage	–0.5	4	V
4-Level Input Voltage (2.5-V mode)	–0.5	2.75	V
4-Level Input Voltage (3.3-V mode)	–0.5	4	V
SMBus Input/Output Voltage	–0.5	4	V
CML Input Voltage	–0.5	V_{DD} + 0.5	V
CML Input Current	–30	30	mA
Storage temperature, T_{stg}	–40	125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*.
(2) Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. For soldering specifications, see product folder at SNOA549.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM(1)	MAX	UNIT
Supply Voltage	2.5 V Mode	2.375	2.5	2.625	V
	3.3 V Mode	3	3.3	3.6	
Ambient Temperature		–40	25	+85	°C
SMBus (SDA, SCL) Pull-up Supply Voltage		2.7	3.3	3.6	V

(1) Typical values represent the most likely parametric norm as determined at the time of design and characterization. Actual typical values may vary over time and will also depend on the application and configuration.

6.4 Thermal Information

THERMAL METRIC(1)		DS125DF111 RTW (WQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
R_Baud	Input baud rate (primary VCO range)	Full Rate: DS125DF111	9.8		12.5	Gbps
R_Baud2	Divide by 2	Half Rate: DS125DF111	4.9		6.25	Gbps
R_Baud4	Divide by 4	Quarter Rate: DS125DF111	2.45		3.125	Gbps
R_Baud8	Divide by 8	Eighth Rate: DS125DF111	1.225		1.5625	Gbps
F_{SDC}	SMBus Clock Rate	Slave Mode Clock Rate	100		400	kHz
		Master Mode Clock Rate	280	400	520	
REFCLK	Reference Clock Rate	± 100 ppm		25		MHz
DC_{REFCLK}	Reference Clock Duty Cycle		40%	50%	60%	
POWER SUPPLY CURRENT						
I_{DD}	DS125DF111 Current Consumption (Whole Device)	Average Supply Current, Default Settings, CHA and CHB Locked DFE Enabled		175		mA
		Average Supply Current, CHA and CHB Locked Default Settings except DFE Disabled		155		mA
		Maximum Transient Supply Current Default Settings: CHA and CHB valid input signal detected CHA and CHB acquiring LOCK(2)		294	333	mA
NTps	Supply Noise Tolerance	50 Hz to 100 Hz		100		mVp-p
		100 Hz to 10 MHz		40		mVp-p
		10 MHz to 3.0 GHz		10		mVp-p
LVCMOS (ADDR[1:0], READEN#, REFCLK_IN, DONE#, LOCK)						
V_{IH}	High level input voltage	2.5 V or 3.3 V Supply Mode	1.7		V_{IN}	V
V_{IL}	Low level input voltage	2.5 V or 3.3 V Supply Mode			0.7	
V_{OH1}	High level output voltage	I_{OH} = -3 mA	2		V_{IN}	V
V_{OH2}	High level output voltage	I_{OH} = –100 µA		V_{IN} - 0.1		
V_{OL}	Low level output voltage	I_{OL} = 3 mA			0.4	
I_{IN}	Input leakage current	V_{INPUT} = GND or V_{IN}	–15		15	µA
4-LEVEL INPUTS (ENSMB, DEMA, DEMB, LPBK, TX_DIS, VODA, VODB)						
I_{IH-R}	Input leakage current High	V_{INPUT} = V_{IN}			80	µA
I_{IL-R}	Input leakage current Low	V_{INPUT} = GND	–160			µA
OPEN DRAIN (LOS/INT#)						
V_{OL}	Low level output voltage	I_{OL} = 3 mA			0.4	V
SIGNAL DETECT						
SDH	Signal Detect: ON Threshold Level	Default level to assert Signal Detect, 12.5 Gbps, PRBS31		18		mVp-p
SDL	Signal Detect: OFF Threshold Level	Default level to de-assert Signal Detect, 12.5 Gbps, PRBS31		14		mVp-p
CML RX INPUTS						
R_Rd	DC Input differential Resistance		80	100	120	Ω
RL_{RX-IN}	Input Return-Loss	SDD11 10 MHz		–19		dB
		SDD11 2.0 GHz		–13		
		SDD11 6.0 - 11.1 GHz		-8		
$V_{RX-LAUNCH}$	Source Transmit Signal Level	Tx Launch amplitude of driver connected to DS125DF111 inputs(3)			1600	mVp-p

(1) Typical values represent the most likely parametric norm as determined at the time of design and characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(2) Peak current only occurs during lock acquisition, limit is for power supply design not needed for thermal calculations.
(3) DS125DF111 equalizer is optimized to adapt to Tx Launch amplitudes between 600 - 1200 mV. Amplitudes above or below this range will reduce the overall equalizer performance.

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Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
TRANSMIT JITTER SPECS (4)						
T_{TJ}	Total Jitter (@ BER = 1E-12)	PRBS7, 9.8304 Gbps		7.5		ps
T_{RJ}	Random Jitter	PRBS7, 9.8304 Gbps		0.33		ps (RMS)
T_{DJ}	Deterministic Jitter	PRBS7, 9.8304 Gbps		3.6		ps
CLOCK AND DATA RECOVERY						
$BW_{P\ LL}$	PLL Bandwidth -3 dB	Measured at 12.5 Gbps, 0.4 UI Sj Injection		3.9		MHz
J_{TOL}	Total jitter tolerance	Jitter per SFF-8431 Appendix D.11 Combination of Dj, Pj, and Rj		> 0.7		UI
T_{LOCK1}	CDR Lock Time	Best Lock Time 9.8304 Gbps Adapt Mode 0 (Register 0x31[6:5]) CTLE Set - no Auto adapt Disable HEO/VEO Lock Monitor - (Register 0x3E[7]) HEO/VEO thresholds set to 0 - (Register 0x6A[7:0]) Rate/Subrate limited to single divide ratio. See Table 9 CDR Reset and Release - (Register 0x0A[3:2]) Signal Detect Preset and Release - Before input signal is present (Register 0x14[7:6])		1.3		ms
T_{LOCK2}	CDR Lock Time	Standards Based, 9.8304 Gbps, Default settings(5)		35		ms
$TEMP_{LOCK}$	CDR Lock	Lock Temperature Range –40°C to 85°C operating range		125		°C

(4) Rj and Dj Jitter decomposition as reported by TEK DSA8200 Sampling scope using a 80E09 Electrical sampling module, 80A06 Pattern trigger, and 82A04 Phase Reference Module.
(5) The typical LOCK time can vary based on data-rate, input channel, and specific DS125DF111 settings.

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6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
CML TX OUTPUTS						
T_V_{DIFF0}	Output differential voltage	Default setting, 8T pattern	400	550	675	mVp-p
T_V_{DIFF7}	Output differential voltage	Maximum setting, 8T pattern Requires SMBus Control	1000	1200		mVp-p
V_{OD_DE}	De-emphasis Level	Maximum setting, VOD and DE Requires SMBus Control Input: 9.8304 Gbps, 16T pattern		–12		dB
T_Rd	DC Output Differential Resistance			100		Ω
T_R/T_F	Output Rise/Fall Time	Full Slew Rate (Channel Reg 0x18[2] = 0), minimum VOD 20% - 80%, See Figure 1. Input: 9.8304 Gbps, 8T Pattern		36		ps
T_{RS}/T_{FS}	Output Rise/Fall Time	Limited Slew Rate (Channel Reg 0x18[2] = 1), minimum VOD 20% - 80%, See Figure 1. Input: 9.8304 Gbps, 8T Pattern		50		ps
T_{SDD22}	Output differential mode return loss	SDD22 10 MHz - 2.0 GHz		–18		dB
SDD22 5.5 GHz		–11				
SDD22 6 - 11.1 GHz		–9				
T_{PD}	Propagation Delay	Retimed Data: 9.8304 Gbps, See Figure 2.		1.5UI + 200ps		ps
T_{PD-RAW}	Propagation Delay	Raw Data: 9.8304 Gbps, See Figure 2.		200		ps
SERIAL BUS INTERFACE CHARACTERISTICS(1) See Figure 3.						
V_{IL}	Data, Clock Input Low Voltage (SDA / SCL)				0.8	V
V_{IH}	Data, Clock Input High Voltage (SDA / SCL)		2.1		3.6	V
V_{OL}	Output Low Voltage	SDA or SCL, IOL = 1.25 mA	0		0.36	V
T_R	SDA Rise Time, Read Operation	SDA, RPU = 4.7 K, Cb < 50 pF		140		ns
T_F	SDA Fall Time, Read Operation	SDA, RPU = 4.7 K, Cb < 50 pF		60		ns
$T_{SU;DAT}$	Setup Time, Read Operation			560		ns
$T_{HD;DAT}$	Hold Time, Read Operation			615		ns
C_{IN}	Input Capacitance	SDA or SCL		< 5		pF
T_R	SCL and SDA, Rise Time				300	ns
T_F	SCL and SDA, Rise Time				1000	ns

(1) EEPROM interface requires 520 kHz capable EEPROM device.

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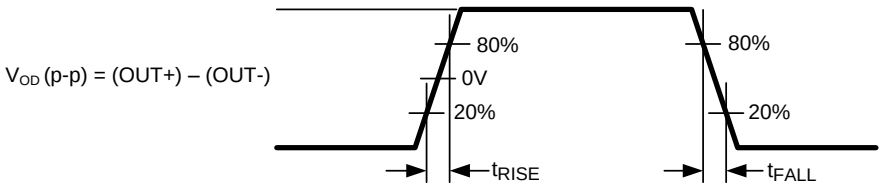


Figure 1. Differential Output Edge Rate

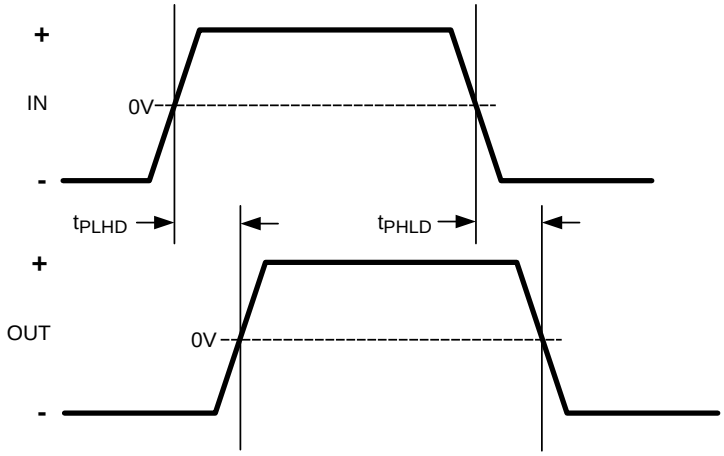


Figure 2. Differential Propagation Delay

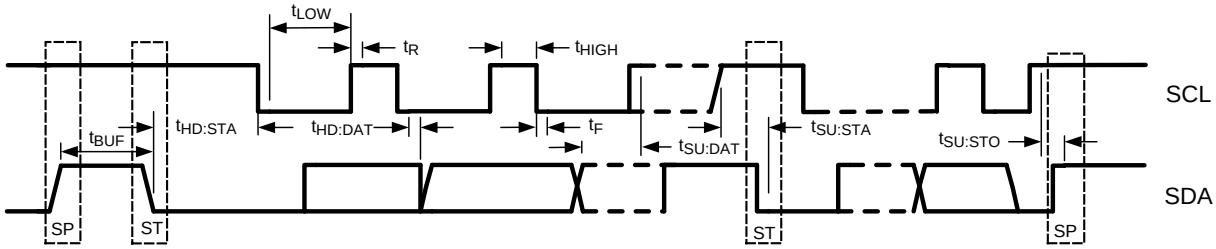
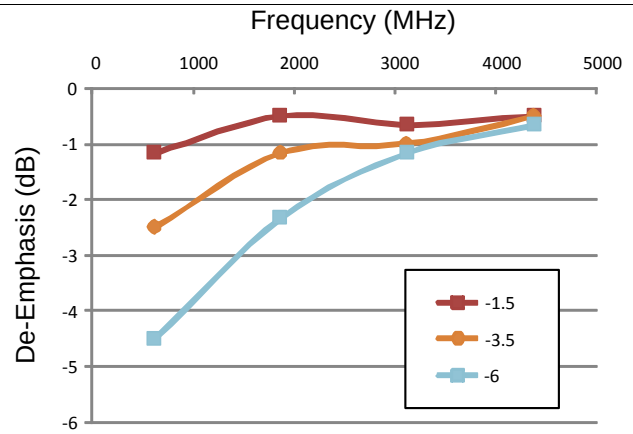


Figure 3. SMBus Timing Diagram

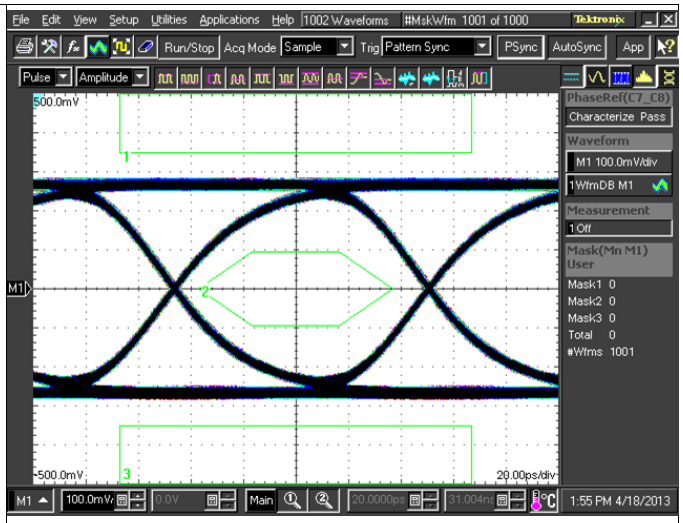
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6.7 Typical Characteristics



Test Conditions
Datarate: 10.3125 Gbps with a PRBS7 pattern
VOD Setting: 1000mV
Temperature: 25°C and VDD = 2.5V

Figure 4. De-Emphasis Gain vs. Frequency



Jitter Measurements

Rj (RMS): 315 fs Dj: 3.74 ps Tj (1E-12): 7.33 ps

Figure 5. Output Eye Diagram 10.3125 Gbps

7 Detailed Description

7.1 Overview

The DS125DF111 is a low-power, multi-rate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the DS125DF111's input. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS125DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS125DF111.

7.2 Functional Block Diagram

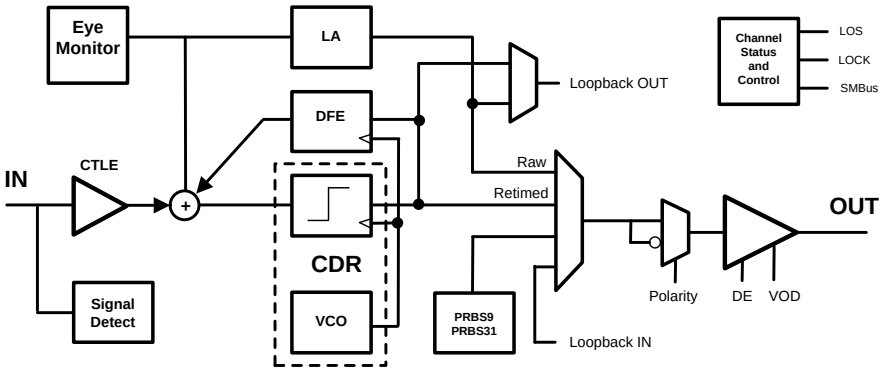


Figure 6. 1 of 2 Channels, DS125DF111 Data Path Block Diagram

7.3 Feature Description

7.3.1 Device Data Path Operation

The data path operation of the DS125DF111 is shown in the data path block diagram of Figure 6. The functional sections are as follows.

- Input Channel Equalization
- Clock and Data Recovery
- PRBS Pattern Generator
- Datapath Multiplexer and Output Driver
- Reference Clock
- Control Pins
- Eye Opening Monitor

7.3.1.1 Input Channel Equalization

Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium.

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Feature Description (continued)

To make configuration of these settings easier, the DS125DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS125DF111, immediately after the DS125DF111 acquires phase lock.

The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS125DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS125DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. See Table 23 for additional information on CTLE settings and gain levels.

The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS125DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments.

7.3.1.2 Clock and Data Recovery

The DS125DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system.

7.3.1.3 PRBS Pattern Generator

Each channel in the DS125DF111 can be configured to generate and output its own pseudo random bit sequence (PRBS). The DS125DF111 pattern generators support the following PRBS sequences:

- PRBS-9, $2^9 - 1$
- PRBS-31, $2^{31} - 1$

7.3.1.4 Datapath Multiplexer and Output Driver

The DS125DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath.

The DS125DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features

- Amplitude
- De-Emphasis
- Edge Rate
- Polarity

The DS125DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS125DF111. The CTLE compensates for lossy transmission media at the input to the DS125DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS125DF111.

When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS125DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

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Feature Description (continued)

An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.

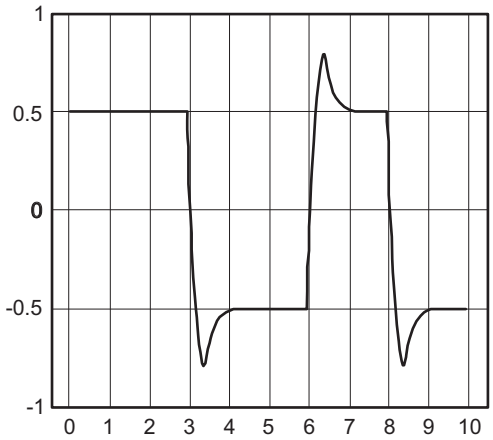


Figure 7. Idealized De-Emphasis Waveform

The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently.

7.3.1.5 Reference Clock

A 25 MHz ±100 ppm reference clock is required for proper device operation. The DS125DF111 uses the reference clock to determine when its VCO is properly phase-locked to the incoming data-rate. The DS125DF111 does not include a crystal driver, so a stand-alone external oscillator is required.

The DS125DF111 is set to phase lock to a constrained set of data-rates, the digital circuitry in the device pre-configures the VCO frequency. This enables the DS125DF111 to detect very quickly that a loss of lock has occurred.

The phase noise of the reference clock is not critical. Any commercially-available 25 MHz oscillator (±100ppm maximum) can provide an acceptable reference clock. The 25 MHz clock high level input voltage must match the V_{IN} level utilized on the DS125DF111.

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Feature Description (continued)

7.3.1.6 Control Pins

The 4-level input pins utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings when ENSMB=0. There is an internal 30K pull-up and a 60K pull-down connected to the package pin. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Using the 1K pull-up, 1K pull-down, no connect, and 20K pull-down provide the optimal voltage levels for each of the four input states.

Table 1. 4-Level Inputs

LEVEL	SETTING	VOLTAGE
0	1 K to GND	0.1 V
R	20 K to GND	0.33 * V_{IN}
Float	No connection	0.67 * V_{IN}
1	1 K to V_{IN}	V_{IN} - 0.05V

In order to minimize the startup current associated with the integrated 2.5-V regulator the 1 K pull-up / pull-down resistors are recommended. If several 4 level inputs require the same setting, it is possible to combine two or more 1 K resistors into a single lower value resistor. As an example; combining two inputs with a single 500 Ω resistor is a good way to save board space.

7.3.1.6.1 Pin Mode Limitation

Using the control pins directly does limit the ability of the DS125DF111 CTLE to correctly adapt to high frequency datarates in high loss input channel scenarios. For input channels with more than 15 dB of loss the CTLE Adaption table and or adaption algorithm needs to be modified in the SMBus channel register so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at the lowest settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. See Table 23 for additional information on CTLE settings and gain levels.

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7.3.1.7 Eye Opening Monitor

The DS125DF111's Eye Opening Monitor (EOM) measures the internal data eye at the input of the CDR and can be used for 2 functions:

1. Horizontal Eye Opening (HEO) and Vertical Eye Opening (VEO) measurement
2. Full Eye Diagram Capture

The HEO measurement is made at the 0V crossing and is read in channel register 0x27. The VEO measurement is made at the 0.5 UI mark and is read in channel register 0x28. The HEO and VEO registers can be read from channel registers 0x27 and 0x28 at any time while the CDR is locked. The following equations are used to convert the contents of channel registers 0x27 and 0x28 into their appropriate units:

- HEO [UI] = ch reg 0x27 ÷ 64
- VEO [mV] = ch reg 0x28 x 3.125

A full eye diagram capture can be performed when the CDR is locked. The eye diagram is constructed within a 64 x 64 array, where each cell in the matrix consists of an 16-bit word. Users can manually adjust the vertical scaling of the EOM or allow the state machine to control the scaling which is the default option. The horizontal scaling controlled by the state machine and is always directly proportional to the data rate.

When a full eye diagram plot is captured, the retimer will shift out 4 16-bit words of junk data that should be discarded followed by 4096 16-bit words that make up the 64 x 64 eye plot. The first actual word of the eye plot from the retimer is for (X, Y) position (0,0). Each time the eye plot data is read out the voltage position is incremented. Once the voltage position has incremented to position 63, the next read will cause the voltage position to reset to 0 and the phase position to increment. This process will continue until the entire 64 x 64 matrix is read out. Figure 8 shows the EOM read out sequence overlaid on top of a simple eye opening plot. In this plot any hits are shown in green. This type of plot is helpful for quickly visualizing the HEO and VEO. Users can apply different algorithms to the output data to plot density or color gradients to the output data.

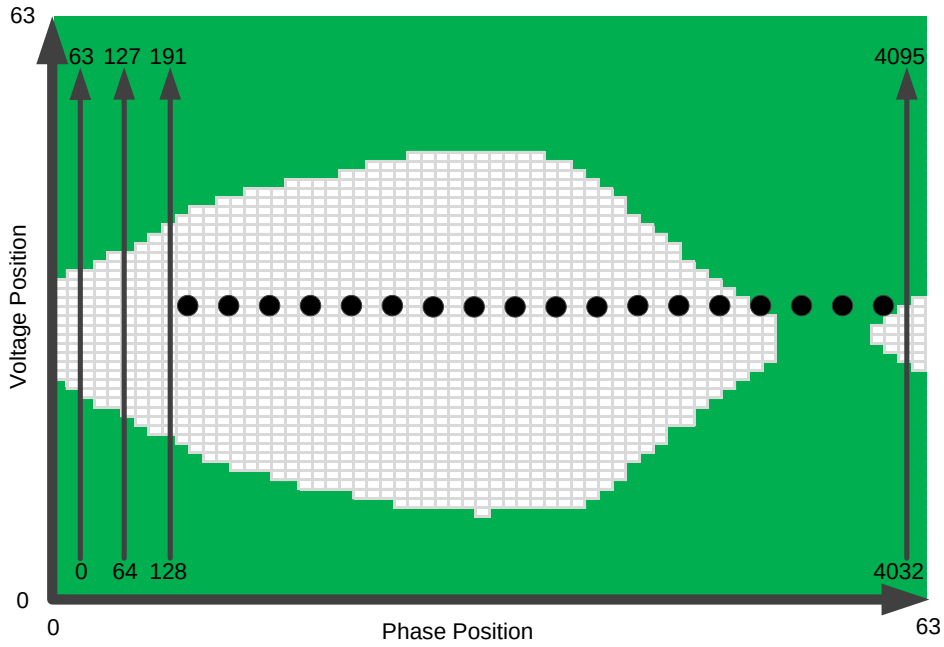


Figure 8. EOM Full Eye Capture Readout

To manually control the EOM vertical range, remove scaling control from the state machine then select the desired range:

1. Channel Reg 0x2C[6] → 0
2. See Table 2

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Table 2. Eye Opening Monitor Vertical Range Settings

CHANNEL REG 0x11[7:6] VALUE	EOM VERTICAL RANGE [mV]
2'b00	±100
2'b01	±200
2'b10	±300
2'b11	±400

The EOM operates as an under-sampled circuit. This allows the EOM to be useful in identifying over equalization, ringing and other gross signal conditioning issues. However, the EOM cannot be correlated to a bit error rate.

The EOM can be accessed in two ways to read out the entire eye plot:

- Multi-byte reads can be used such that data is repeatedly latched out from channel register 0x25.
- Or single byte reads. With single byte reads, the MSB are located in register 0x25 and the LSB are located in register 0x26. In this mode, the device must be addressed each time a new byte is read.

To perform a full eye capture with the EOM, follow these steps within the desired channel register set:

Table 3. Eye Opening Monitor Full Eye Capture Instructions

STEP	REGISTER [bits]	VALUE	DESCRIPTION
1	0x3E[7]	0	Disable lock EOM lock monitoring
2	0x2C[6] 0x11[7:6]	0 2'b--	Set the desired EOM vertical range
3	0x11[5]	0	Power on the EOM
4	0x24[7]	1	Enable fast EOM
5	0x24[0] 0x25 0x26	1	Begin read out of the 64 x 64 array, discard first 4 words Ch reg 0x24[0] is self clearing. 0x25 is the MSB of the 16-bit word 0x26 is the LSB of the 16-bit word
6	0x25 0x26		Continue reading information until the 64 x 64 array is complete.
7	0x3E[7] 0x2C[6] 0x11[5] 0x24[7,1]	1 1 1 0	Return the EOM to its original state. Undo steps 1-4

7.4 Device Functional Modes

To select different programming device, the ENSMB pin selects the control modes. The DS125DF111device can be programmed using external pin control, a SMBus controller, or through an EEPROM configuration load.

Table 4. ENSMB Control Description

ENSMB PIN	DESCRIPTION	READEN# terminal
High	SMBus Slave Mode	Pull Low to initiate reading configuration data from the EEPROM
Float	SMBus Master Mode	Tie Low to enable proper address strapping on power up
R	N/A	
Low	Pin Mode Control	Shared with VODA terminal control function

7.4.1 Control Pin Mode

The 4-level input pins utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings when ENSMB=0. There is an internal 30K pull-up and a 60K pull-down connected to the package pin. These resistors, together with the external resistor connection combine to achieve the desired voltage level. Using the 1K pull-up, 1K pull-down, no connect, and 20K pull-down provide the optimal voltage levels for each of the four input states.

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Table 5. 4-Level Inputs

LEVEL	SETTING	VOLTAGE
0	1K to GND	0.1 V
R	20K to GND	0.33 * VIN
Float	No connection	0.67 * VIN
1	1K to VIN	VIN - 0.05V

Note: V_{IN} = 2.5V in 2.5V Mode and V_{IN} = 3.3V in 3.3V Mode

In order to minimize the startup current associated with the integrated 2.5-V regulator the 1K pull-up / pull-down resistors are recommended. If several 4 level inputs require the same setting, it is possible to combine two or more 1K resistors into a single lower value resistor. As an example; combining two inputs with a single 500 Ohm resistor is a good way to save board space.

7.4.2 SMBus Master Mode and SMBus Slave Mode

In SMBus master mode the DS125DF111 reads its initial configuration from an external EEPROM upon powerup. The serial EEPROM must support a minimum frequency of 520 KHz. Once the DS125DF111 has finished reading its initial configuration from the external EEPROM in SMBus master mode it reverts to SMBus slave mode and can be further configured by an external controller over the SMBus. Two device pins initiate reading the configuration from the external EEPROM and indicate when the configuration read is complete.

- DONE#
- READEN#

These pins are meant to work together. When the DS125DF111 is powered up in SMBus master mode, it reads its configuration from the external EEPROM. This is triggered when the READEN# pin goes low. When the DS125DF111 is finished reading its configuration from the external EEPROM, it drives its DONE# pin low. In this mode, as the name suggests, the DS125DF111 acts as an SMBus master during the time it is reading its configuration from the external EEPROM. After the DS125DF111 has finished reading its configuration from the EEPROM, it releases control of the SMBus and becomes a SMBus slave. In applications where there is more than one DS125DF111 on the same SMBus, bus contention can result if more than one DS125DF111 tries to take command of the SMBus as the SMBus master at the same time. The READEN# and DONE# pins prevent this bus contention.

In a system where the DS125DF111s are meant to operate in SMBus master mode, the READEN# pin of one retimer should be wired to the DONE# pin of the next. The system should be designed so that the READEN# pin of one (and only one) of the DS125DF111s in the system is driven low on power-up. This DS125DF111 will take command of the SMBus on power-up and will read its initial configuration from the external EEPROM. When it is finished reading its configuration, it will set its DONE# pin low. This pin should be connected to the READEN# pin of another DS125DF111. When this DS125DF111 senses its READEN# pin driven low, it will take command of the SMBus and read its initial configuration from the external EEPROM, after which it will set its DONE# pin low. By connecting the DONE# pin of each DS125DF111 to the READEN# pin of the next DS125DF111, each DS125DF111 can read its initial configuration from the EEPROM without causing bus contention.

7.5 Programming

7.5.1 SMBus Interface

7.5.1.1 Address Lines

In either SMBus Master or Slave mode the DS125DF111 must be assigned a SMBus address. A unique address should be assigned to each device on the SMBus.

The SMBus address is latched into the DS125DF111 approximately 25 ms after power-up. The address is read in from the state of the ADR[1:0] lines upon power-up. A floating address line input will be interpreted as a logic 0.

The DS125DF111 can be configured with any of 4 SMBus addresses. The SMBus addressing scheme uses the least significant bit of the SMBus address as the Write/Read_N address bit. When an SMBus device is addressed for writing, this bit is set to 0; for reading, to 1. Table 6 shows the write address setting for the DS125DF111 versus the values latched in on the address line at power-up.

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Programming (continued)

7.5.1.2 Device Configuration in SMBus Slave Mode

The configurable settings of the DS125DF111 may be set independently for each channel at any time after power up using the SMBus. A register write is accomplished when the controller sends a START condition on the SMBus followed by the Write address of the DS125DF111 to be configured. See Table 6 for the mapping of the address lines to the SMBus Write addresses. After sending the Write address of the DS125DF111, the controller sends the register address byte followed by the register data byte. The DS125DF111 acknowledges each byte written to the controller according to the data link protocol of the SMBus Version 2.0 Specification. See this specification for additional information on the operation of the SMBus.

There are two types of device registers in the DS125DF111. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF111. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers.

The channel registers are used to set all the configuration settings of the DS125DF111. They provide independent control for each channel of the DS125DF111 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF111 on a channel-by-channel basis.

7.5.1.3 Bit Fields in the Register Set

Many of the registers in the DS125DF111 are divided into bit fields. This allows a single register to serve multiple purposes, which may be unrelated. Often configuring the DS125DF111 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged.

7.5.1.4 Writing To and Reading from the Control/Shared Registers

Any write operation targeting register 0xff writes to the control/shared register 0xff. This is the only register in the DS125DF111 with an address of 0xff. Bit 2 of register 0xff is used to select either the control/shared register set or a channel register set. If bit 2 of register 0xff is cleared (written with a 0), then all subsequent read and write operations over the SMBus are directed to the control/shared register set. This situation persists until bit 2 of register 0xff is set (written with a 1). There is a register with address 0x00 in the control/shared register set, and there is also a register with address 0x00 in each channel register set. If you read the value in register 0x00 when bit 2 of register 0xff is cleared to 0, then the value returned by the DS125DF111 is the value in register 0x00 of the control/shared register set. If you read the value in register 0x00 when bit 2 of register 0xff is set to 1, then the value returned by the DS125DF111 is the value in register 0x00 of the selected channel register set. The channel register set is selected by bits 1:0 of register 0xff. If bit 3 of register 0xff is set to 1 and bit 2 of register 0xff is also set to 1, then any write operation to any register address will write all the channel register sets in the DS125DF111 simultaneously. This situation will persist until either bit 3 of register 0xff or bit 2 of register 0xff is cleared.

Note that when you write to register 0xff, independent of the current settings in register 0xff, the write operation ALWAYS targets the control/shared register 0xff. This channel select register, register 0xff, is unique in this regard. Table 7 shows the control/shared register set.

Table 6. SMBus Write Address Assignment(1)

ADDR1	ADDR0	SMBus WRITE ADDRESS	SMBus READ ADDRESS
0	0	0x30	0x31
0	1	0x32	0x33
1	0	0x34	0x35
1	1	0x36	0x37

(1) A floating ADDR[1:0] pin at power-up will be interpreted as a logic 0.

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Table 7. Control and Shared Register Space

ADDRESS (HEX)	DEFAULT REGISTER VALUE (HEX)	BITS	DEFAULT BIT VALUE (BINARY)	MODE	DESCRIPTION
0x00	00	7:4	0000	R	SMBus Address Strap Observation <3:0>
0x01	61	7:5	011	R	Device Revision
		4:0	0 0001	R	Device ID
0x04	01	6	0	R/W/SC	Self-Clearing Reset for Control/Shared Registers
		5	0	R/W	Reset for SMBus Master Mode
		4	0	R/W	Force EEPROM Configuration
0x05	00	4	0	R	Indicates EEPROM read complete
		3	0	R	Indicates Channel A has interrupted
		2	0	R	Indicates Channel B has interrupted
0x06	00	3:0	0000	R/W	Write to 0xA'h to observe SMBus Address strap in Reg 0x00[7:4]
0x07	04	1	0	R/W	Loopback: Loopback Input of Channel B to output of Channel A
		0	0	R/W	Loopback: Loopback Input of Channel A to output of Channel B
0xff	00	7:6	00	R/W	Controls LOCK pin output **(ADDR0 = 0 or Float)** 00: Logical OR of Lock Status from CH A and CH B 01: Lock Status from Channel A 10: Lock Status from Channel B 11: Logical AND of Lock Status from CH A and CH B Controls LOCK pin output **(ADDR0 = 1)** 00: Logical NOR of Lock Status from CH A and CH B 01: NOT Lock Status from Channel A 10: NOT Lock Status from Channel B 11: Logical NAND of Lock Status from CH A and CH B
		5	0	R/W	Loss of Signal / Interrupt (LOS/INT) pin output 0: LOS 1: Interrupt
		3	0	R/W	Selects Both Channels for Register Write. Register read from one channel based on the selected channel in register 0xff bits 1:0. See Table 8
		2	0	R/W	0 = reads/writes directed to shared registers 1 = reads/writes directed to channel registers based on target channel defined by register 0xff bits 1:0. See Table 8
		1:0	0	R/W	Selects Target Channel for Register Reads and Writes. See Table 8

7.5.1.5 SMBus Strap Observation

Register 0x00, bits 7:4

In order to communicate with the DS125DF111 over the SMBus, it is necessary for the SMBus controller to know the address of the DS125DF111. The address strap observation bits in control/shared register 0x00 are primarily useful as a test of SMBus operation. In order to use the address strap observation bits of control/shared register 0x00, it is necessary first to set the diagnostic test control bits of control/shared register 0x06. This four bit field should be written with a value of 0xa. When this value is written to bits 3:0 of control/shared register 0x06, then the value of the SMBus address straps can be read in register 0x00, bits 7:4. The value read will be the same as the value present on the ADDR line when the DS125DF111 powers up. For example, if a value of 0x0 is read from control/shared register 0x00, bits 7:4, then at power-up the ADDR line was set to 0. The DS125DF111 is set to a SMBus Write address of 0x30.

7.5.1.6 Interrupt Channel Flag Bits

Register 0x05, bits 3:2

The operation of these bits is described in the section on interrupt handling later in this data sheet.

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7.5.1.7 Control/Shared Register Reset

Register 0x04, bit 6

Register 0x04, bit 6, clears all the control/shared registers back to their factory defaults. This bit is self clearing, so it is cleared after it is written and the control/shared registers are reset to their factory default values.

7.5.1.8 Device Revision and Device ID

Register 0x01

Control/shared register 0x01 contains the device revision and device ID. The device ID will be different for the different devices in the retimer family. This register is useful because it can be interrogated by software to determine the device variant and revision installed in a particular system. The software might then configure the device with appropriate settings depending upon the device variant and revision.

Table 8. Channel Select Register Values Mapped to Register Set Target

REGISTER 0xFF VALUE (HEX)	SHARED/CHANNEL REGISTER SELECTION	BROADCAST CHANNEL REGISTER SELECTION	TARGETED CHANNEL REGISTER SELECTION	COMMENTS
0x00	Shared	N/A	N/A	All reads and writes target shared register set
0x04	Channel	No	A	All reads and writes target channel register set
0x05	Channel	No	B	All reads and writes target channel register set
0x0c	Channel	Yes	A	All writes target all channel register sets, all reads target Channel A register set
0x0d	Channel	Yes	B	All writes target all channel register sets, all reads target Channel B register set

7.5.1.9 Channel Select Register

Register 0xff, bits 3:0

Register 0xff, as described above, selects the channel or channels for channel register reads and writes. It is worth describing the operation of this register again for clarity. If bit 3 of register 0xff is set, then any channel register write applies to all channels. Channel register read operations always target only the channel specified in bits 1:0 of register 0xff regardless of the state of bit 3 of register 0xff. Read and write operations target the channel register sets only when bit 2 of register 0xff is set.

Bit 2 of register 0xff is the universal channel register enable. This bit must be set in order for any channel register reads and writes to occur. If this bit is set, then read operations from or write operations to register 0x00, for example, target channel register 0x00 for the selected channel rather than the control/shared register 0x00. In order to access the control/shared registers again, bit 2 of register 0xff should be cleared. Then the control/shared registers can again be accessed using the SMBus. Write operations to register 0xff always target the register with address 0xff in the control/shared register set. There is no other register, and specifically, no channel register, with address 0xff.

All eight bits of this register should always be set to the desired values whenever this register is written. The register set target selected by each valid value written to the channel select register is shown in Table 8.

7.5.1.10 Resetting Individual Channels of the Retimer

Register 0x00, bit 2, and register 0x0a, bits 3:2

Bit 2 of channel register 0x00 is used to reset all the registers for the corresponding channel to their factory default settings. This bit is self-clearing. Writing this bit will clear any register changes you have made in the DS125DF111 since it was powered-up.

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To reset just the CDR state machine without resetting the register values, which will re-initiate the lock and adaptation sequence for a particular channel, use channel register 0x0a. Set bits 2 and 3 of this register to enable the reset override and force the CDR state machine into reset. These bits can be set in the same operation. When both bits are subsequently cleared, the CDR state machine will resume normal operation. If a signal is present at the input to the selected channel, the DS125DF111 will attempt to lock to it and will adapt its CTLE and its DFE according to the currently configured adapt mode for the selected channel. The adapt mode is configured by channel register 0x31, bits 6:5.

7.5.1.11 Rate and Subrate Setting

Each channel of the DS125DF111 will, by default operate at the primary datarates of 12.288 Gbps and 9.8304 Gbps. In addition to the primary rates, the DS125DF111 will operate at divide by 2/4/8 datarates using the default settings. The device can be configured to operate with limited VCO divide ratios by selecting a RATE/SUBRATE combination other than the default value of 0110'b. For example, selecting a RATE (Reg: 0x2F bits [7:6]) and SUBRATE (Reg: 0x2F bits [5:4]) of 0000'b will limit the DS125DF111 to 1.2288 Gbps (Group 0 = 9.8304 / 8) and 12.288 Gbps (Group 1 = 12.288 / 1).

Table 9. Rate/Subrate VCO and Data-Rate Information

RATE	SUBRATE	GROUP 0 DIVIDE RATIOS(1)	GROUP 1 DIVIDE RATIOS(1)
00	00	8	1
00	01	1, 2, 4	1
00	10	1, 2, 4	1, 2, 4
00	11	1, 2, 4	1, 2, 4
01	00	2, 4	2, 4
01	01	1, 4	1, 4
01 (default)	10 (default)	1, 2, 4, 8	1, 2, 4, 8
01	11	1	1
10	00	1	1
10	01	1	1
10	10	2	2
10	11	2, 4	2, 4
11	00	1	1
11	01	1	1
11	10	1	1
11	11	8	1

(1) The default datarates are Group 0 = 9.8304, 4.9152, 2.4576, 1.2288 Gbps and Group 1 =12.288, 6.144, 3.072, 1.536 Gbps.

The DS125DF111 is designed to lock to signals conforming to several different data transmission standards. These standards may define a single data rate or multiple data rates. The rate and subrate settings of the DS125DF111 are used to select which VCO divide ratios to enable. The DS125DF111 searches specific datarates within these enabled VCO divide ratios starting with divide by 8 and working up to divide by 1.

To select datarates based on frequencies other than the VCO defaults a group of PPM Counter registers (0x60 - 0x64) need to be reprogrammed.

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Table 10. Group 0 VCO Frequency Programming Registers

GROUP 0 VCO (GHZ)	REGISTER 0x60[7:0]	REGISTER 0x61[7]	REGISTER 0x61[6:0]	REGISTER 0x64[7:4]
Frequency	Group 0 PPM Count [7:0]	Override Group 0 PPM	Group 0 PPM Count [14:8]	Group 0 PPM Delta[3:0]

Table 11. Group 1 VCO Frequency Programming Registers

GROUP 1 VCO (GHZ)	REGISTER 0x62[7:0]	REGISTER 0x63[7]	REGISTER 0x63[6:0]	REGISTER 0x64[3:0]
Frequency	Group 1 PPM Count [7:0]	Override Group 1 PPM	Group 1 PPM Count [14:8]	Group 1 PPM Delta[3:0]

Table 12. Programming Values for Common Data Rates

VCO GROUP 0 (GHz)	VCO GROUP 1 (GHz)	REGISTER 0x60	REGISTER 0x61	REGISTER 0x62	REGISTER 0x63	REGISTER 0x64
9.8304	12.288	0x26	0xB1	0x70	0xBD	0xFF
9.95328	9.95328	0xC4	0xB1	0xC4	0xB1	0xCC
10.0	10.3125	0x00	0xB2	0x90	0xB3	0xCD
10.51875	10.51875	0x98	0xB4	0x98	0xB4	0xDD
10.70957	11.0957	0x8C	0xB5	0x7A	0xB7	0xDE

To set the VCO Registers for other datarates within the VCO range, the formulas shown can be used to populate the Group 0/1 VCO programming registers.

Table 13. Group 0 VCO Programming Equations

PARAMETER	VALUE or EQUATION	COMMENT
Reference Clock	F0 = 25e6	Internally the reference clock always operates at 25 MHz
Desired Group 0 VCO Frequency	F1	F1 is the frequency of the VCO which is equal to the desired data rate. If the desired data rate uses dividers, be sure to multiply the data rate by the divide setting to get the correct VCO frequency
Number of Reference Clocks	N = 1024	
VCO Freq ÷ 32	F2 = F1 ÷ 32	
Counts of VCO Freq ÷ 32 required	F3 = F2 x N ÷ F0	
Counts of VCO Freq ÷ 32 required rounded	F4	Integer value only. Convert this value to binary. Program the upper 7 bits to channel register 0x61[6:0] and the lower 8 bits to ch register 0x60[7:0]. Be sure to set channel register 0x61[7] to 1 to enable the override function for manual programming.
PPM error due to rounding	Err = 1e6 x (F4 – F3) ÷ F3	
VCO Freq ÷ 32 (1000 PPM tolerance)	F5 = F4 ÷ 1000	Group 0 PPM Delta (Register 0x64[7:4]) Integer Value only, maximum value = 15. Convert to Hex for register.

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Table 14. Group 1 VCO Programming Equations

PARAMETER	VALUE or EQUATION	COMMENT
Reference Clock	F0 = 25e6	Internally the reference clock always operates at 25 MHz
Desired Group 1 VCO Frequency	F1	F1 is the frequency of the VCO which is equal to the desired data rate. If the desired data rate uses dividers, be sure to multiply the data rate by the divide setting to get the correct VCO frequency
Number of Reference Clocks	N = 1024	
VCO Freq ÷ 32	F2 = F1 ÷ 32	
Counts of VCO Freq ÷ 32 required	F3 = F2 x N ÷ F0	
Counts of VCO Freq ÷ 32 required rounded	F4	Integer value only. Convert this value to binary. Program the upper 7 bits to ch register 0x63[6:0] and the lower 8 bits to ch register 0x62[7:0]. Be sure to set channel register 0x63[7] to 1 to enable the override function for manual programming.
PPM error due to rounding	Err = 1e6 x (F4 – F3) ÷ F3	
VCO Freq ÷ 32 (1000 PPM tolerance)	F5 = F4 ÷ 1000	Group 1 PPM Delta (Register 0x64[3:0]) Integer Value only, maximum value = 15. Convert to Hex for register.

7.5.1.12 Overriding the CTLE Boost Setting

Register 0x03, Register 0x2D, bit 3, and Register 0x3a

To override the adaptive CTLE boost settings, channel register 0x03 is used in conjunction with override register bit for the CTLE (0x2D[3]). If the override bit is set in 0x2D[3], CDR LOCK re-acquisition will fail in CTLE adapt modes 1-3.

The current CTLE setting applied to the high-speed analog input can always be read back from register 0x52. This readback register value is valid for adaptive CTLE settings or when the override mechanism is enabled and the CTLE value from register 0x03 is being used.

When in divide by 4 or 8 VCO settings, CTLE channel register 0x3A comes into play. Divide by 4 and divide by 8 data-rates do not automatically adapt the CTLE setting, they use the value in register 0x3A as a settable CTLE level.

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7.5.1.13 Overriding the Output Multiplexer

Register 0x09, bit 5 and Register 0x1e, bits 7:5

By default, the DS125DF111 output for each channel will be as shown in Table 15 and Table 16.

Table 15. Default Output Status Description

INPUT SIGNAL STATUS	CHANNEL STATUS	OUTPUT STATUS
Absent	No Signal Detected	Mute
Present	Not Locked	Set by 0x1e[7:5]
Present	Locked	Raw or Retimed, Set by 0x1e[7:5], 0x09[5]

Table 16. Output Multiplexer Override Settings, Register 0x1e Bit 7:5

REGISTER 0x1E[7:5]	OUTPUT MULTIPLEXER	COMMENTS
111	Mute	
100	PRBS Generator	See *Using the PRBS Generator* for additional information on PRBS generator usage.
001	Retimed Data	Default when the retimer is locked
000	Raw Data	Output of the CTLE + DFE, before retiming

This default behavior can be modified by register writes. Register 0x1e, bits 7:5, contain the output multiplexer override value. The values of this three-bit field and the corresponding meanings of each are shown in Table 16.

When no signal is present at the input to the selected channel of the DS125DF111 the signal detect circuitry will power down the channel. This includes the output driver which is therefore muted when no signal is present at the input.

7.5.1.14 Overriding the VCO Divider Selection

Register 0x09, bit 2, and Register 0x18, bits 6:4

In normal operation, the DS125DF111 sets its VCO divider to the correct divide ratio, either 1, 2, 4, or 8 depending upon the bit rate of the signal at the channel input and the selected rate/subrate code. It is possible to override the divider selection. This might be desired if the VCO is set to free run, for example, to output a PRBS signal at a sub-harmonic of the actual VCO frequency.

In order to override the VCO divider settings, first set bit 2 of register 0x09. This is the VCO divider override enable. Once this bit is set, the VCO divider setting is controlled by the value in register 0x18, bits 6:4. The valid values for this three-bit field are 0x0 to 0x3. The mapping of the bit field values to the divider ratio is shown in Table 17.

Table 17. Divider Ratio Map

BIT FIELD VALUE REG 18 [6:4]	DIVIDER RATIO
0	1
1	2
2	4
3	8

In order for the DS125DF111 to acquire LOCK, the override divider selection must be included in the Group 0 VCO list for the current Rate/Subrate setting.

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7.5.1.15 Using the Internal Eye Opening Monitor

Register 0x11, bits 7:6 and bit 5, Register 0x22, bit 7, Register 0x24, bit 7 and bit 0, Register 0x25, Register 0x26, Register 0x27, Register 0x28, Register 0x2a and Register 0x3e, bit 7

The DS125DF111 includes an internal eye opening monitor. The eye opening monitor is used by the retimer to compute a figure of merit for automatic adaptation of the CTLE and the DFE. It can also be controlled and queried through the SMBus by a system controller. Note that eye monitor is not equivalent to a pattern checker, it is possible under very stressful input conditions that the adapted CTLE/DFE settings will incorrectly determine the proper value of the incoming data pattern.

The eye opening monitor produces error hit counts for settable phase and voltage offsets of the comparator in the retimer. This is similar to the way many Bit Error Rate Test Sets measure eye opening. At each phase and amplitude offset setting, the eye opening monitor determines the nominal bit value (“0” or “1”) using its primary comparator. This is the bit value that is resynchronized to the recovered clock and presented at the output of the DS125DF111. The eye opening monitor also determines the bit value detected by the offset comparator. This information yields an eye contour. Here's how this works.

If the offset comparator is offset in voltage by an amount larger than the vertical eye opening, for example, then the offset comparator will always decide that the current bit has a bit value of “0”. When the bit is really a “1”, as determined by the primary comparator, this is considered a bit error. The number of bit errors is counted for a settable interval at each setting of the offset phase and voltage of the offset comparator. These error counts can be read from registers 0x25 and 0x26 for sequential phase and voltage offsets. These error counts for all phase and voltage offsets form a 64 X 64 point array. A surface or contour plot of the error hit count versus phase and voltage offset produces an eye diagram, which can be plotted by external software.

The eye opening monitor works in two modes. In the first, only the horizontal and vertical eye openings are measured. The eye opening monitor first sweeps its variable-phase clock through one unit interval with the comparison voltage set to the mid-point of the signal. This determines the mid-point of the horizontal eye opening. The eye opening monitor then sets its variable phase clock to the mid-point of the horizontal eye opening and sweeps its comparison voltage. These two measurements determine the horizontal and vertical eye openings. The horizontal eye opening value is read from register 0x27 and the vertical eye opening from register 0x28. Both values are single byte values.

The measurement of horizontal and vertical eye opening is very fast. The speed of this measurement makes it useful for determining the adaptation figure of merit. In normal operation, the HEO and VEO are automatically measured periodically to determine whether the DS125DF111 is still in lock. Reading registers 0x27 and 0x28 will yield the most-recently measured HEO and VEO values.

In normal operation, the eye monitor circuitry is powered down most of the time to save power. When the eye is to be measured under external control, it must first be enabled by writing a 0 to bit 5 of register 0x11. The default value of this bit is 1, which powers down the eye monitor except when it is powered-up periodically by the CDR state machine and used to test CDR lock. The eye monitor must be powered up to measure the eye under external SMBus control.

Bits 7:6 of register 0x11 are also used during eye monitor operation to set the EOM voltage range. This is described below. A single write to register 0x11 can set both bit 5 and bits 7:6 in one operation.

Register 0x3e, bit 7, enables horizontal and vertical eye opening measurements as part of the lock validation sequence. When this bit is set, the CDR state machine periodically uses the eye monitor circuitry to measure the horizontal and vertical eye opening. If the eye openings are too small, according to the pre-determined thresholds in register 0x6a, then the CDR state machine declares lock loss and begins the lock acquisition process again. For SMBus acquisition of the internal eye, this lock monitoring function must be disabled. Prior to overriding the EOM by writing a 1 to bit 0 of register 0x24, disable the lock monitoring function by writing a 0 to bit 7 of register 0x3e.

Once the eye has been acquired, you can reinstate HEO and VEO lock monitoring by once again writing a 1 to bit 7 of register 0x3e. Under external SMBus control, the eye opening monitor can be programmed to sweep through all its 64 states of phase and voltage offset autonomously. This mode is initiated by setting register 0x24, bit 7, the fast_eom mode bit.

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Register 0x22, bit 7, the eom_ov bit, should be cleared in this mode. When the fast_eom bit is set, the eye opening monitor operation is initiated by setting bit 0 of register 0x24, which is self-clearing. As soon as this bit is set, the eye opening monitor begins to acquire eye data. The results of the eye opening monitor error counter are stored in register 0x25 and 0x26. In this mode the eye opening monitor results can be obtained by repeated multi-byte reads from register 0x25. It is not necessary to read from register 0x26 for a multi-byte read. As soon as the eight most significant bits are read from register 0x25, the eight least significant bits for the current setting are loaded into register 0x25 and they can be read immediately. As soon as the read of the eight most significant bits has been initiated, the DS125DF111 sets its phase and voltage offsets to the next setting and starts its error counter again. The result of this is that the data from the eye opening monitor is available as quickly as it can be read over the SMBus with no further register writes required. The external controller just reads the data from the DS125DF111 over the SMBus as fast as it can. When all the data has been read, the DS125DF111 clears the eom_start bit.

If multi-byte reads are not used, meaning that the device is addressed each time a byte is read from it, then it is necessary to read register 0x25 to get the MSB (the eight most significant bits) and register 0x26 to get the LSB (the eight least significant bits) of the current eye monitor measurement. Again, as soon as the read of the MSB has been initiated, the DS125DF111 sets its phase and voltage offsets to the next setting and starts its error counter again. In this mode both registers 0x25 and 0x26 must be read in order to get the eye monitor data. The eye monitor data for the next set of phase and voltage offsets will not be loaded into registers 0x25 and 0x26 until both registers have been read for the current set of phase and voltage offsets. In all eye opening monitor modes, the amount of time during which the eye opening monitor accumulates eye opening data can be set by the value of register 0x2a. In general, the greater this value the longer the accumulation time. When this value is set to its maximum possible value of 0xff, the maximum number of samples acquired at each phase and amplitude offset is approximately 218. Even with this setting, the eye opening monitor values can be read from the SMBus with no delay. The eye opening monitor operation is sufficiently fast that the SMBus read operation cannot outrun it.

The eye opening is measured at the input to the data comparator. At this point in the data path, a significant amount of gain has been applied to the signal by the CTLE. In many cases, the vertical eye opening as measured by the EOM will be on the order of 400 to 500 mV peak-to-peak. The secondary comparator, which is used to measure the eye opening, has an adjustable voltage range from ±100 mV to ±400 mV. The EOM voltage range is normally set by the CDR state machine during lock and adaptation, but the range can be overridden by writing a two-bit code to bits 7:6 of register 0x11. The values of this code and the corresponding EOM voltage ranges are shown in Table 18.

Table 18. EOM Voltage Range vs Reg 0x11 [7:6]

VALUE IN BITS 7:6 OF REGISTER 0x11	EOM VOLTAGE RESOLUTION (mv)	EOM VOLTAGE RANGE (± mV)
0x0	3.125	±100
0x1	6.250	±200
0x2	9.375	±300
0x3	12.500	±400

Note that the voltage ranges shown in Table 18 are the post CTLE voltage ranges of the signal at the input to the data path comparator. These values are not directly equivalent to any observable voltage measurements at the input to the DS125DF111. Note also that if the EOM voltage range is set too small the voltage sweep of the secondary comparator may not be sufficient to capture the vertical eye opening. When this happens the eye boundaries will be outside the vertical voltage range of the eye measurement.

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To summarize, the procedure for reading the eye monitor data from the DS125DF111is shown below.

1. Select the DS125DF111 channel to be used for the eye monitor measurement by writing the channel select register, register 0xff, with the appropriate value as shown in Table 8. If the correct channel register set is already selected, this step may be skipped.
2. Select the eye monitor voltage range by setting bits 7:6 of register 0x11 according to the values in Table 18. The CDR state machine will have set this range during lock acquisition, but it may be necessary to change it to capture the entire vertical eye extent.
3. Power up the eye monitor circuitry by clearing bit 5 of register 0x11. Normally the eye monitor circuitry is powered up periodically by the CDR state machine. Clearing bit 5 of register 0x11 enables the eye monitor circuitry unconditionally. This bit should be set again once the eye acquisition is complete. Clearing bit 5 and setting bits 7:6 of register 0x11 as desired can be combined into a single register write if desired.
4. Clear bit 7 of register 0x22. This is the eye monitor override bit. It is cleared by default, so you may not need to change it.
5. Set bit 7 of register 0x24. This is the fast eye monitor enable bit.
6. Set bit 1 of register 0x24. This initiates the automatic fast eye monitor measurement. This bit can be set at the same time a bit 7 of register 0x24 if desired.
7. Read the data array from the DS125DF111. This can be accomplished in two ways.
   - If you are using multi-byte reads, address the DS125DF111 to read from register 0x25. Continue to read from this register without addressing the device again until you have read all the data desired. The read operation can be interrupted by addressing the device again and then resumed by reading once again from register 0x25.
   - If you are not using multi-byte reads, then read the MSB for each phase and amplitude offset setting from register 0x25 and the LSB for each setting from register 0x26. In this mode, you address the device each time you want to read a new byte.
8. In either mode, the first four bytes do not contain valid data. These should be discarded.
9. Continue reading eye monitor data until you have read the entire 64X64 array.
10. Clear bit 7 of register 0x24. This disables fast eye monitor mode.
11. Set bit 5 of register 0x11. This will return control of the eye monitor circuitry to the CDR state machine.
12. Set bit 7 of register 0x3e. This re-enables the HEO and VEO lock monitoring.

7.5.1.16 Overriding the DFE Tap Weights and Polarities

Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x24, bit 2, Register 0x2f, bit 0, and Registers 0x71–0x75

For the DS125DF111 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired.

Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, which powers down the DFE, should be cleared. This bit is cleared by default. It is not necessary to change the default settings of these registers, but verify that they are set as described.

It is necessary to set bit 7 of register 0x15 to manually set the DFE tap weights. This bit is cleared by default.

Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting.

The polarity of the tap weight for tap 1 is set using bit 7 of the same register, register 0x12. The polarity is set to 0 by default, which corresponds to a negative algebraic sign for the tap.

The other four taps are set using four-bit fields in registers 0x20 and 0x21. The polarities of these taps are set by bits 3:0 in register 0x11. These tap polarities are all set to 0 by default.

As is the case for the CTLE settings, if changing the DFE tap weights or polarities causes the DS125DF111 to lose lock, it may readapt its CTLE in order to reacquire lock. If this occurs, the CTLE settings may appear to change spontaneously when the DFE tap weights are changed. The mechanism is the same as that described above for the CTLE boost settings.

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When the DS125DF111 is set to adapt mode 2 or 3 using bits 6:5 of register 0x31, it will automatically adapt its DFE whenever its CDR state machine is reset. This occurs when the user manually resets the CDR state machine using bits 3:2 of register 0x0a, or when a signal is first presented at the input to the channel when the channel is in an unlocked state.

Regardless of the adapt mode, DFE adaptation can be initiated under SMBus control. Because the DFE tap weight registers are used by the DFE state machine during adaptation, they may be reset prior to adaptation, which can cause the adaptation to fail. The DFE tap observation registers can be used to prevent this.

Prior to initiating DFE adaptation under SMBus control, write the starting values of the DFE tap settings into the DFE tap weight registers, registers 0x11, 0x12, 0x20, and 0x21. The values can be read from the observation registers, registers 0x71 through 0x75. For each DFE tap, read the current value in the observation register. Both the polarities and the tap weights are contained in the observation registers. For each DFE tap, write the current tap polarity and tap weight into the DFE tap register. Once all these values have been written, DFE adaptation can be initiated and it will proceed normally. If the DS125DF111 fails to find a set of DFE tap weights producing a better adaptation figure of merit than the starting tap weights, the starting tap weights will be retained and used.

CTLE adaptation can also be initiated manually. Setting and then clearing bit 0 of register 0x2f will initiate adaptation of the CTLE. As with the DFE, if the DS125DF111 fails to find a set of CTLE settings that produce a better adaptation figure of merit than the starting CTLE values, the starting CTLE values will be retained and used.

7.5.1.17 Enabling Slow Rise/Fall Time on the Output Driver

Register 0x18, bit 2

Normally the rise and fall times of the output driver of the DS125DF111 are set by the slew rate of the output transistors. By default, the output transistors are biased to provide the maximum possible slew rate, and hence the minimum possible rise and fall times. In some applications, slower rise and fall times may be desired. For example, slower rise and fall times may reduce the amplitude of electromagnetic interference (EMI) produced by a system.

Setting bit 2 of register 0x18 will adjust the output driver circuitry to increase the rise and fall times of the signal. Setting this bit will approximately double the nominal rise and fall times of the DS125DF111 output driver. This bit is cleared by default.

7.5.1.18 Using the PRBS Generator

Register 0x1e, bits 7 and 4, Register 0x30, and Register 0x0d

Table 19. Programming Sequence 1: (Requires Valid and Locked Input Data Pattern)

STEP	REGISTER ADDRESS	REGISTER DATA	REGISTER MASK	COMMENTS
1	0xFF	0x0C	0xFF (write bits[7:0])	Enable Broadcast
2	0x09	0x20	0x20 (only write bit[5])	Override Loopthru Select
3	0x1E	0x80	0xE0 (only write bits[7:5])	Output MUX Select PRBS Generator
4	0x1E	0x10	0x10	Power-up PRBS Generator
5	0x30	0x08	0x08	Power-up PRBS Clock
6	0x30	0x00	0x03	Select PRBS9 pattern (511 bits)
7	0x0D	0x20	0x20	Enable PRBS Clock

Notes:

1. To select PRBS31 instead of PRBS9, change Register Data 0x30 = 0x02 with mask of 0x03 in Step 6.
2. To only select Channel A, change Register Data 0xFF = 0x04 in Step 1.
3. To only select Channel B, change Register Data 0xFF = 0x05 in Step 1.
4. It has been noted in product testing that some pattern analyzers use an alternate PRBS9 polarity.

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Table 20. Programming Sequence 2: (Free-Running VCO @ ~10.3 Gbps, No Input Data Required)

STEP	REGISTER ADDRESS	REGISTER DATA	REGISTER MASK	COMMENTS
1	0xFF	0x0C	0xFF (write bits[7:0])	Enable Broadcast
2	0x00	0x04	0x04 (only write bit[2])	Reset Channel Registers
3	0x14	0x80	0x80 (only write bit[7])	Preset Signal Detect
4	0x09	0x04	0x04	Override divider select
5	0x09	0x80	0x80	Override VCO cap count
6	0x08	0x12	0x1F	Set VCO cap count to 12'h
7	0x18	0x00	0x70	Select divider select to 000'b
8	0x09	0x08	0x08	Override charge pump power downs
9	0x1B	0x00	0x03	Disable both charge pumps
10	0x09	0x40	0x40	Override Loop-filter DAC
11	0x1F	0x12	0x1F	Set Loop-filter DAC override value
12	0x1E	0x10	0x10	Enable PRBS Generator
13	0x30	0x08	0x0F	Enable Digital Clock - set pattern to PRBS9
14	0x09	0x20	0x20	Override Loopthru Select
15	0x1E	0x80	0xE0	Output MUX Select PRBS Generator
16	0x0D	0x20	0x20	PRBS Seed Load

Notes:

1. To select PRBS31 instead of PRBS9, change Register Data 0x30 = 0x0A in Step 13.
2. To achieve a data-rate of approximately 12.2 Gbps change Register Data 0x08 = 0x05 in Step 6.
3. To achieve a data-rate of approximately 9.8 Gbps change Register Data 0x08 = 0x16 in Step 6.
4. To only select Channel A, change Register Data 0xFF = 0x04 in Step 1.
5. To only select Channel B, change Register Data 0xFF = 0x05 in Step 1.
6. With a free running VCO the actual output frequency will change with temperature and voltage. BERT is not recommended in this mode.

7.5.1.19 Inverting the Output Polarity

Register 0x1f, bit 7

In some systems, the polarity of the data does not matter. In systems where it does matter, it is sometimes necessary, for the purposes of trace routing, for example, to invert the normal polarities of the data signals. The DS125DF111 can invert the polarity of the data signals by means of a register write. Writing a 1 to bit 7 of register 0x1f inverts the polarity of the output signal for the selected channel. This can provide additional flexibility in system design and board layout.

7.5.1.20 Figure of Merit Adaption

Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6

The default figure of merit for both the CTLE and DFE adaptation is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both large and approximately equal in magnitude. This usually provides optimum bit error rate performance for most transmission channels.

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Table 21. DS125DF111 Adaption Algorithm Settings, Register 0x31 Bits 6:5

REGISTER 0X31, BIT 6 adapt_mode [1]	REGISTER 0x31, BIT 5 adapt_mode [0]	ADAPT MODE SETTING <1:0>	ADAPTION ALGORITHM
0	0	00	No Adaption
0	1	01	Adapt CTLE Until Optimum
1	0	10	Adapt CTLE Until Optimum the DFE, then CTLE Again (Default)
1	1	11	Adapt CTLE Until Lock, the DFE, the CTLE Again

In the DS125DF111 the CTLE figure of merit type is selected using the two-bit field in register 0x31, bits 6:5.

Table 22. DFE Figure of Merit Type Settings

VALUE IN BITS 5:4 OF REGISTER 0x2C	FIGURE OF MERIT TYPE
0x0	Both HEO and VEO used
0x1	Only HEO used
0x2	Only VEO used
0x3 (Default)	Both HEO and VEO used

The DS125DF111 capability of adapting based on the following Figure Of Merit.

FOM = Minimum [HEO, VEO]

where

- HEO = Horizontal Eye Opening
- VEO = Vertical Eye Opening
- FOM = Figure of Merit

7.5.1.21 Setting the Rate and Subrate for Lock Acquisition

Register 0x2f, bits 7:6 and bits 5:4

The rate and subrate settings, which constrain the data rate search can be set using channel register 0x2f. Bits 7:6 are RATE<1:0>, and bits 5:4 are SUBRATE<1:0>.

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7.5.1.22 Setting the Adaption/Lock Mode

Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a

There are four adaptation modes available in the DS125DF111.

- Mode 0: The user is responsible for setting the CTLE and DFE (for the DS125DF111) values. This mode is used if the transmission channel response is fixed.
- Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled , but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces.
- Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0.
- Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels.

Bits 6:5 of register 0x31 determine the adaptation mode to be used. The mapping of these register bits to the adaptation algorithm is shown in.

By default the DS125DF111 requires that the equalized internal eye exhibit horizontal and vertical eye openings greater than a pre-set minimum in order to declare a successful lock. The minimum values are set in register 0x6a.

The DS125DF111 continuously monitors the horizontal and vertical eye openings while it is in lock. If the eye opening falls below the threshold set in register 0x6a, the DS125DF111 will declare a loss of lock.

The continuous monitoring of the horizontal and vertical eye openings may be disabled by clearing bit 7 of register 0x3e.

7.5.1.23 Initiating Adaption

Register 0x24, bit 2, and Register 0x2f, bit 0

When the DS125DF111 becomes unlocked, it will automatically try to acquire lock. If an adaptation mode is selected using bits 6:5 in register 0x31, the DS125DF111 will also try to adapt its CTLE and DFE.

Adaptation can also be initiated by the user. CTLE adaptation can be initiated by setting and then clearing register 0x2f, bit 0. In the DS125DF111, DFE adaptation can be initiated by setting and then clearing bit 2 of register 0x24. The Adaption for CTLE and DFE is also initiated by cycling the CDR reset bits in register 0x0a [3:2].

7.5.1.24 Overriding the CTLE Settings Used for CTLE Adaption

Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x40-0x4f

The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF111 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF111 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF111 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF111 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF111 still continues to try additional CTLE settings for a pre-determined trial count called the “look-beyond” count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The “look-beyond” count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default.

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The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x4F. The default values for these settings are shown in Table 23. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF111.

Table 23. CTLE Settings for Adaption, Register 0x40-0x4F

REGISTER (HEX)	BITS 7:6 (STAGE 0)	BITS 5:4 (STAGE 1)	BITS 3:2 (STAGE 2)	BITS 1:0 (STAGE 3)	CTLE BOOST STRING	HEX VALUE	GAIN (dB) @ 6.25 GHz	ADAPTATION INDEX
40	0	0	0	0	0000	00	3	0
41	1	0	0	0	1000	40	8	1
42	2	0	0	0	2000	80	11	2
43	1	1	0	0	1100	50	13	3
44	3	0	0	0	3000	C0	14	4
45	2	1	0	0	2100	90	15	5
46	1	1	1	0	1110	54	17	6
47	2	2	0	0	2200	A0	18	7
48	2	3	0	0	2300	B0	20	8
49	2	1	1	1	2111	95	24	9
4A	1	2	2	1	1221	69	26	10
4B	3	1	1	1	3111	D5	27	11
4C	2	1	2	1	2121	99	28	12
4D	2	2	1	1	2211	A5	29	13
4E	3	2	1	2	3212	E6	31	14
4F	3	3	2	1	3321	F9	33	15

As an alternative to, or in conjunction with, writing the CTLE boost setting registers 0x40 through 0x4f, it is possible to set the starting CTLE boost setting index. To override the default setting, which is 0, set bit 3 of register 0x2f. When this bit is set, the starting index for adaptation comes from register 0x39, bits 4:0. This is the index into the CTLE settings table in registers 0x40 through 0x4f. When this starting index is 0, which is the default, CTLE adaptation starts at the first setting in the table, the one in register 0x40, and continues until the optimum Figure of Merit (FOM) is reached.

Adjusting the starting index helps the DS125DF111 CTLE to correctly adapt to 8b/10b encoded high frequency datarates in high loss input channel scenarios. For input channels with more than 15 dB of loss the CTLE Adaption table and or adaption algorithm needs to be modified in the SMBus channel register so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at the lowest settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption FOM temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER.

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Table 24. VOD Settings

VODA/B (Pin 9 / Pin 10)	BIT 2, sel_vod[2]	BIT 1, sel_vod[1]	BIT 0, sel_vod[0]	OUTPUT VOD (mVppd)
0	0	0	0	600
R	0	0	1	700
	0	1	0	800
	0	1	1	900
F	1	0	0	1000
1	1	0	1	1100
	1	1	0	1200
	1	1	1	1300

7.5.1.25 Setting the Output Differential Voltage

Register 0x2d, bits 2:0

There are eight levels of output differential voltage available in the DS125DF111 SMBus register settings, from 0.6 V to 1.3 V in 0.1 V increments. The values in bits 2:0 of register 0x2d set the output VOD. The available VOD settings and the corresponding values of this bit field are shown in Table 24. Not all VOD levels are available using the VODA/B control pins when ENSMB = 0.

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

DEMA/B (Pin 4 / Pin 5)	REG 0X15 BIT [2], drv_dem[2]	REG 0X15 BIT [1], drv_dem[1]	REG 0X15 BIT [0], drv_dem[0]	REG 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

7.5.1.27 CTLE Setting for Divide by 4 and Divide by 8 VCO Ranges

Register 0x3a, bits 7:0

In the DS125DF111 the default CTLE setting for lower speed signals is taken directly from register 0x3a and is not automatically adapted. For long, high loss input channels this value may need to be increased from the default (minimum) CTLE setting.

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7.6 Register Maps

7.6.1 Reading To and Writing from the Channel Registers

Each channel has a complete set of channel registers associated with it. The channel registers or the control/ shared registers are selected by channel select register 0xff. The settings in this register control the target for subsequent register reads and writes until the contents of register 0xff are explicitly changed by a register write to register 0xff. As noted, there is only one register with an address of 0xff, the channel select register.

Table 26. Channel Register Definition

ADDRESS (HEX)	DEFAULT VALUE (HEX)	BITS	DEFAULT VALUE (BINARY)	EEPROM	MODE	DESCRIPTION
0x00	00	2	0	N	R/W/SC	Reset Channel Registers to Defaults (Self-clearing)
0x01	00	4	0	N	R	CDR Lock Loss Interrupt
		0	0			Signal Detect Loss Interrupt
0x02	00	7:0	00'h	N	R	CDR Status [7:0] Bit[7] = Reserved Bit[6] = Reserved Bit[5] = Fail Lock Check Bit[4] = Lock Bit[3] = CDR Lock Bit[2] = Reserved Bit[1] = Reserved Bit[0] = Reserved
0x03	00	7:6	00	Y	R/W	Used for setting CTLE value when Channel Register 0x2D[3] is high. Read-back value going to analog in Channel Register 0x52. CTLE Boost Stage [0] <1:0> Bits [7:6] CTLE Boost Stage [1] <1:0> Bits [5:4] CTLE Boost Stage [2] <1:0> Bits [3:2] CTLE Boost Stage [3] <1:0> Bits [1:0]
		5:4	00	Y	R/W	
		3:2	00	Y	R/W	
		1:0	00	Y	R/W	
0x08	00	7:5	000	N	R/W	Reserved
		4:0	00000	Y	R/W	CDR Cap_DAC Start Group 0
0x09	00	7	0	Y	R/W	Reserved
		6	0	Y	R/W	Reserved
		5	0	Y	R/W	Enable Override Output Mux (Register 0x1E[7:5])
		4:3	00	Y		Reserved
		2	0	Y		Enable Override Divider Select (Register 0x18[6:4])
		1:0	00	Y		Reserved
0x0A	10	7:5	000	Y	R/W	Reserved
		4	1	Y		Reserved
		3	0	Y		Enable CDR Reset Override (Register 0x0A[2])
		2	0	Y		CDR Reset Override Bit
		1:0	00	Y		Reserved
0x0B	0F	7:5	000	N	R/W	Reserved
		4:0	1111	Y	R/W	CDR Cap_DAC Start Group 1
0x0C	08	7:4	0000		R/W	Status Control[3:0]
		3	1	N	R/W	Single Bit Transition Detector – Lock Qualification 1: Enables SBT 0: Disables SBT
		2	0	Y		Reserved
		1:0	00	N		Reserved

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Register Maps (continued)

Table 26. Channel Register Definition (continued)

ADDRESS (HEX)	DEFAULT VALUE (HEX)	BITS	DEFAULT VALUE (BINARY)	EEPROM	MODE	DESCRIPTION
0x0D	00	7:6	00	N	R/W	Reserved
		5	0	Y		PRBS pattern shift Enable. Use in conjunction with 0x1E[4] and 0x30[3] to start PRBS. Note: This bit must be set high last.
		4:0	00000	N		Reserved
0x0E	93	7:0	1001 0011	Y	R/W	Reserved
0x0F	69	7:0	0110 1001	Y	R/W	Reserved
0x10	3A	7:5	001	Y	R/W	Reserved
		4:0	11010			
0x11	20	7:6	00	Y	R/W	Eye Opening Monitor Voltage Range <1:0> 00: 3.125 mV 01: 6.250 mV 10: 9.375 mV 11: 12.500 mV
		5	1	Y		Eye Opening Monitor Power Down
		4	0	N	R/W	Reserved
		3	0	Y	R/W	DFE Tap 2 Polarity (Use w/manual DFE override, 0x15[7])
		2	0	Y		DFE Tap 3 Polarity (Use w/manual DFE override, 0x15[7])
		1	0	Y		DFE Tap 4 Polarity (Use w/manual DFE override, 0x15[7])
		0	0	Y		DFE Tap 5 Polarity (Use w/manual DFE override, 0x15[7])
0x12	A0	7	1	Y	R/W	DFE Tap 1 Polarity (Use w/manual DFE override, 0x15[7])
		6	0	N	R/W	Reserved
		5	1	Y	R/W	DFE Select negative gm
		4:0	00000	Y		DFE Tap 1 Weight <4:0>
0x13	90	7	1	N	R/W	Reserved
		6	0	Y		
		5	0	N	R/W	
		4	1	Y	R/W	Enable DC offset control
		3	0	Y	R/W	Reserved
		2	0	Y	R/W	CTLE Boost Stage 3, Bit 2 (Limiting Bit)
		1	0	Y	R/W	Enable DWDM Mode
		0	0	Y	R/W	Reserved
0x14	00	7	0	Y	R/W	Force Signal Detect On
		6	0	Y	R/W	Force Signal Detect Off
		5:4	00	Y	R/W	Signal Detect – Assert Reference Levels
		3:2	00	Y	R/W	Signal Detect – De-assert Reference Levels
		1:0	00	N		Reserved

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Register Maps (continued)

Table 26. Channel Register Definition (continued)

ADDRESS (HEX)	DEFAULT VALUE (HEX)	BITS	DEFAULT VALUE (BINARY)	EEPROM	MODE	DESCRIPTION
0x15	10	7	0	Y	R/W	Enables manual DFE tap settings Use with 0x11[3:0], 0x12[7], 0x12[4:0], 0x20[7:0], 0x21[7:0]
		6	0	Y	R/W	Compress the range of de-emphasis to 0-6 dB
		5	0			Reserved
		4	1			Reserved
		3	0	Y	R/W	Driver Power-Down
		2:0	000	Y	R/W	Driver De-emphasis Setting<2:0>; 0dB - 12dB; See Table 25
0x16	7A	7:4	0111	Y	R/W	Reserved
		3:0	1010	Y		
0x17	25	7:4	0010	Y	R/W	Reserved
		3:0	0101	Y		
0x18	40	7	0	N	R/W	Reserved
		6:4	100	Y		VCO Divider Ratio <2:0> (Enable from Register 0x09, Bit 2) 000: Full-Rate 001: Divide by 2 010: Divide by 4 011: Divide by 8 100: Default value at power up
		3	0	N		
		2	0	N		Enable slow rise/fall time edge rate
		1:0	00	N		Reserved
0x19	37	7:6	00	N	R/W	Reserved
		5:0	110111	Y		
0x1A	00	7:4	0000	Y	R/W	Reserved
		3:0	0000	N		
0x1B	03	7:2	000000	N	R/W	Reserved
		1:0	11	Y		
0x1C	24	7:5	001	Y	R/W	Reserved
		4:2	001			
		1:0	00			
0x1D	00	7	0	Y	R/W	Reserved
		6:0	000000	N		
0x1E	E1	7:5	111	Y	R/W	Selects PFD MUX for Loopback 000: Raw Data 001: Re-timed Data 100: PRBS Generator 111: Mute
		4	0	N	R/W	Enable the PRBS serializer, used with 0x1E[7:5], 0x30[3:0], 0x0D[5]
		3	0	Y	R/W	Disable the DFE function (Disable = 1)
		2:1	00			Reserved
		0	1			Reserved
0x1F	55	7	0	Y	R/W	Invert the polarity of the driver
		6	1			Reserved
		5:0	010101	N		Reserved

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Register Maps (continued)

Table 26. Channel Register Definition (continued)

ADDRESS (HEX)	DEFAULT VALUE (HEX)	BITS	DEFAULT VALUE (BINARY)	EEPROM	MODE	DESCRIPTION
0x20	00	7:4	0000	Y	R/W	DFE Tap 5 Weight <3:0> (Use w/manual DFE override, 0x15[7])
		3:0	0000	Y		DFE Tap 4 Weight <3:0> (Use w/manual DFE override, 0x15[7])
0x21	00	7:4	0000	Y	R/W	DFE Tap 3 Weight <3:0> (Use w/manual DFE override, 0x15[7])
		3:0	0000	Y		DFE Tap 2 Weight <3:0> (Use w/manual DFE override, 0x15[7])
0x22	00	7	0	Y	R/W	Eye Monitor override
		6	0	Y		Reserved
		5:0	00000	N		Reserved
0x23	40	7	0	Y	R/W	Eye Monitor Get HEO VEO override
		6	1	Y	R/W	DFE Override
		5:0	000000	N	R/W	Eye Monitor VDAC
0x24	00	7	0	N	R/W	Enable Fast Eye Opening Monitor Mode
		6	0	N	R	DFE Error - No Lock
		5	0	N	R	Get HEO VEO Error - No hits at crossing
		4	0	N	R	Get HEO VEO Error - Vertical Eye not visible
		3	0	N	R/W	Reserved
		2	0	N	R/W/SC	Start DFE Adaptation (Self- Clearing)
		1	0	N	R/W/SC	Start Get HEO VEO Measurement (Self-Clearing)
		0	0	N	R/W/SC	Start Eye Opening Monitor Counter (Self-Clearing)
0x25	00	7:0	00'h	N	R	Eye Opening Monitor Count <15:8>
0x26	00	7:0	00'h	N	R	Eye Opening Monitor Count <7:0>
0x27	00	7:0	00'h	N	R	HEO Value <7:0> (Measured in 0-63 phase settings)
0x28	00	7:0	00'h	N	R	VEO Value <7:0>
0x29	00	7	0	N	R/W	Reserved
		6:5	00		R	Eye Opening Monitor Voltage Range Setting <1:0> See 0x11[7:6]
		4:0	00000		R/W	Reserved
0x2A	30	7:0	30'h	Y	R/W	Eye Opening Monitor Timer Threshold <7:0>
0x2B	00	7:6	00	N	R/W	Reserved
		5:4	00	Y		Reserved
		3:0	0000	Y		Minimum hits for HEO-VEO hit counter
0x2C	72	7	0	N	R/W	Reserved
		6	1	Y		Scale VEO based on Eye Monitor Vrange
		5:4	11	Y		DFE Adaptation Figure of Merit Type <1:0> 00: Not Valid 01: State Machine uses only HEO 10: State Machine uses only VEO 11: State Machine uses both HEO and VEO
		3:0	0010	Y		Determines number of DFE settings to look-beyond current best Figure of Merit (FOM)

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Register Maps (continued)

Table 26. Channel Register Definition (continued)

ADDRESS (HEX)	DEFAULT VALUE (HEX)	BITS	DEFAULT VALUE (BINARY)	EEPROM	MODE	DESCRIPTION
0x2D	80	7	1	Y	R/W	Enable Driver Short Circuit protection
		6	0			Enable FAST signal detect
		5	0			Increase the Assert and De-assert reference thresholds
		4	0			Set high (1) to decrease the signal detect gain
		3	0			Set high (1) to override the EQ setting going to the analog from 0x03[7:0]
		2:0	000			Output Driver VOD [2:0] 000: 600 mV 001: 700 mV 010: 800 mV 011: 900 mV 100: 1000 mV 101: 1100 mV 110: 1200 mV 111: 1300 mV
0x2E	00	7:6	00	N	R/W	Reserved
		5	0	Y		
		4:3	00	N		
		2	0	Y		
		1:0	00	N		
0x2F	66	7:6	01	Y	R/W	RATE <1:0>
		5:4	10			SUBRATE <1:0>
		3	0			CTLE Adaptation Index Override 0: CTLE adaption will start at Reg_0x40 + Reg_0x39[3:0]. So this may be used to preclude lower CTLE settings. 1: CTLE will not adapt and will use the CTLE setting of Reg_0x40 + Reg_0x39[3:0] for scalar divide ratios of 1 or 2. Divide ratios of 4 & 8 will take CTLE settings from 0x3A unless 0x55[0] is high, which will revert to the setting in Reg_0x40 + Reg_0x39[3:0].
		2	1			Enable PPM Check - for Lock qualifier
		1	1			Enable FLD Check - for Lock qualifier
		0	0	N	R	Start CTLE Adaptation
0x30	00	7:6	00	N	R/W	
		5	0		R	
		4	0		R	Goes High if Interrupt from CDR Goes High
		3	0	Y	R/W	Enable PRBS digital CLK
		2	0	N		Reserved
		1:0	00	Y		PRBS Pattern[1:0]

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Register Maps (continued)

Table 26. Channel Register Definition (continued)

ADDRESS (HEX)	DEFAULT VALUE (HEX)	BITS	DEFAULT VALUE (BINARY)	EEPROM	MODE	DESCRIPTION
0x31	40	7	0			Reserved
		6:5	10	Y	R/W	Adaptation Mode <1:0> 00: No adaption 01: Adapt only CTLE till optimal 10: Adapt CTLE till optimal, then DFE, then CTLE again 11: Adapt CTLE till LOCK, then DFE, then CTLE till optimal
		4:3	00	Y	R/W	CTLE Adaptation Figure of Merit Type <1:0> 00: SM uses both HEO and VEO 01: SM uses only HEO 10: SM uses only VEO 11: SM uses both HEO and VEO
		2:0	000	N		Reserved
0x32	11	7:4	0001	Y	R/W	HEO Interrupt Threshold <3:0> Compares HEO value, Reg_0x27[7:0] vs. threshold of Reg_0x32[7:4]*4
		3:0	0001	Y	R/W	VEO Interrupt Threshold <3:0> Compares VEO value, Reg_0x28[7:0] vs. threshold of Reg_0x32[3:0]*4
0x33	88	7:4	1000	Y	R/W	HEO Threshold for CTLE Adaptation Handoff to DFE Adaptation Compares HEO value, Reg_0x27[7:0] vs. threshold of Reg_0x33[7:4]*2
		3:0	1000	Y	R/W	VEO Threshold for CTLE Adaptation Handoff to DFE Adaptation Compares HEO value, Reg_0x27[7:0] vs. threshold of Reg_0x33[3:0]*2
0x34	3F	7	0	N	R	PPM Error Ready
		6	0	Y	R/W	Low power disable
		4:5	11			Lock Counter
		3:0	1111			Maximum DFE Tap Absolute Value for Taps 2–5 <3:0>
0x35	1F	7:6	00	Y	R/W	
		5	0			Get PPM Error from PPM count - clears when done
		4:0	1 1111			Maximum DFE Tap Absolute Value for Tap 1 <4:0>
0x36	31	7	0	Y	R/W	Reserved
		6	0			Enable HEO/VEO Interrupt
		5:4	11	Y		Reserved
		3	0	N		Reserved
		2	0	Y		Cap DAC range override enable
		1:0	01	Y		Cap DAC range[1:0]
0x37	00	7:0	00'h	N	R	CTLE Status
0x38	00	7:0	00'h	N	R	DFE Status

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Register Maps (continued)

Table 26. Channel Register Definition (continued)

ADDRESS (HEX)	DEFAULT VALUE (HEX)	BITS	DEFAULT VALUE (BINARY)	EEPROM	MODE	DESCRIPTION
0x39	00	7	0	N	R/W	Reserved
		6:5	00	Y		Reserved
		4:0	0 0000			Start Index for CTLE Adaptation <4:0> (Enable from Register 0x2f, Bit 3)
0x3A	00	7:6	00	Y	R/W	Fixed CTLE Stage 0 Boost Setting for Divide Ratios 4 and 8 <1:0>
		5:4	00		R/W	Fixed CTLE Stage 1 Boost Setting for Divide Ratios 4 and 8 <1:0>
		3:2	00		R/W	Fixed CTLE Stage 2 Boost Setting for Divide Ratios 4 and 8 <1:0>
		1:0	00		R/W	Fixed CTLE Stage 3 Boost Setting for Divide Ratios 4 and 8 <1:0>
0x3B	00	7:0	00'h	N	R	PPM Count MSB
0x3C	00	7:0	00'h	N	R	PPM Count LSB
0x3D	00	7	0	Y	R/W	Reserved
		6:0	000000	N		
0x3E	80	7	1	Y	R/W	Enable HEO/VEO lock monitoring once SBT/FLD declare lock. Once the lock and adaptation processes are complete, HEO/VEO monitoring is performed once per the interval determined by Reg_0x69[3:0].
		6:0	0000000	N		Reserved
0x3F	00	7	0	Y	R/W	Reserved
		6:0	0000000	N		
0x40 - 0x4F				Y	R/W	CTLE Settings for Adaptation Table 20
0x50	00	7	0	N	R/W	Reserved
		6	0	Y		Reserved
		5	0	N		Reserved
		4	0	Y		Slicer Sign Bit
		3:0	0000	Y		Slicer adjustment in 5mV steps. Maximum adjustment value is 50mV or 0x50[3:0] = A'h
0x51	00	7:0	00'h	Y	R/W	Reserved
0x52	00	7:0	00'h	N	R	CTLE Boost setting readback register.
0x53	00	7:0	00'h	N	R/W	Reserved
0x54	00	7	0	N	R	Signal Detect observation bit.
		6	0			EQ Limiting (CTLE Stage 3[2]) observation bit.
		5:2	0000			Reserved
		1	0			CDR Lock Interrupt
		0	0			Signal Detect Interrupt
0x55	00	7	0	N	R/W	Reserved
		6:5	00	Y		Reserved
		4	0	N		Allows observation of the alternate HEO/VEO Figure of Merit In Reg_0x27 and Reg_0x28
		3:1	0	Y		Reserved
		0	0	Y		Enables Adaption in the lower divide ratios

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Register Maps (continued)

Table 26. Channel Register Definition (continued)

ADDRESS (HEX)	DEFAULT VALUE (HEX)	BITS	DEFAULT VALUE (BINARY)	EEPROM	MODE	DESCRIPTION
0x56	00	7:4	0000	N	R/W	Reserved
		3	0	Y		CDR Lock Interrupt Enable Bit. [1]: Enable CDR LOCK Interrupt (Register 0x54[1]) [0]: Default
		2	0	Y		Signal Detect Interrupt Enable Bit. [1]: Enable Signal Detect Interrupt (Register 0x54[0]) [0]: Default
		1	0	Y		CDR Loss of Lock Interrupt Enable Bit. [1]: Enable CDR LOSS of LOCK Interrupt (Register 0x01[4]) [0]: Default
		0	0	Y		Signal Loss Interrupt Enable Bit. [1]: Enable Signal Loss Interrupt (Register 0x01[0]) [0]: Default
0x60	26	7:0	26'h	Y	R/W	Group 0 (Rate/Subrate defined) PPM counter <7:0> LSBs
0x61	B1	7	1	Y	R/W	Override standard Group 0 tie cells for PPM count and tolerance with Channel Registers 0x60, 0x61, and 0x64
		6:0	011 0001			Group 0 (Rate/Subrate defined) PPM counter <14:8> MSBs
0x62	70	7:0	70'h	Y	R/W	Group 1 (Rate/Subrate defined) PPM counter <7:0> LSBs
0x63	BD	7	1	Y	R/W	Override standard Group 1 tie cells for PPM count and tolerance with Channel Registers 0x62, 0x63, and 0x64
		6:0	011 1101			Group 1 (Rate/Subrate defined) PPM counter <14:8> MSBs
0x64	FF	7:4	1111	Y	R/W	Group 0 PPM Delta
		3:0	1111			Group 1 PPM Delta
0x65	00	7:0	00'h	N	R/W	Reserved
0x66	00	7:0	00'h	N	R/W	Reserved
0x67	00	7:6	00	N	R/W	Reserved
		5	0	Y		Reserved
		4:0	00000	N		Reserved
0x68	00	7:0	00'h	N	R/W	Reserved
0x69	0A	7:4	0000	N	R/W	Reserved
		3:0	1010	Y		HEO/VEO interval while monitoring lock. Monitoring will take place 1 out of the indicated count intervals (default h'A). Interval time is determined 0x2B[5:4], which is 6.5ms by default.
0x6A	44	7:4	0100	N	R/W	Vertical Eye Opening Lock Threshold <3:0>
		3:0	0100			Horizontal Eye Opening Lock Threshold <3:0>
0x6B	40	7:0	40'h	Y	R/W	Adaptation Figure of Merit Term A<7:0> FoM = Min [(HEO - B)*A, (VEO - C)*(1-A)] FoM = Min [(HEO - 0x6C) * (0x6B)/127, (VEO - 0x6D) * (128 - 0x6B)/127]

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Register Maps (continued)

Table 26. Channel Register Definition (continued)

ADDRESS (HEX)	DEFAULT VALUE (HEX)	BITS	DEFAULT VALUE (BINARY)	EEPROM	MODE	DESCRIPTION
0x6C	00	7:0	0x0	Y	R/W	Adaptation Figure of Merit Term B<7:0> FoM = Min [(HEO - B)*A, (VEO - C)*(1-A)] FoM = Min [(HEO - 0x6C) * (0x6B)/127, (VEO - 0x6D) * (128 - 0x6B)/127]
0x6D	00	7:0	0x0	Y	R/W	Adaptation Figure of Merit Term C<7:0> FoM = Min [(HEO - B)*A, (VEO - C)*(1-A)] FoM = Min [(HEO - 0x6C) * (0x6B)/127, (VEO - 0x6D) * (128 - 0x6B)/127]
0x6E	00	7	0	Y	R/W	Enable Alternate Figure of Merit for CTLE Adaptation
		6	0	Y		Enable Alternate Figure of Merit for DFE Adaptation
		5:0	000000	N		Reserved
0x6F	00	7:0	00'h	N	R/W	Reserved
0x70	03	7:3	00000	N	R/W	Reserved
		2:0	011			CTLE Adaptation Look-Beyond Count <2:0>
0x71	00	7:6	00	N	R/W	Reserved
		5	0		R	DFE Tap 1 Polarity (Read Only)
		4:0	0 0000		R	DFE Tap 1 Weight (Read Only) <4:0>
0x72	00	7:5	000	N	R/W	Reserved
		4	0		R	DFE Tap 2 Polarity (Read Only)
		3:0	0000		R	DFE Tap 2 Weight (Read Only) <3:0>
0x73	00	7:5	000	N	R/W	Reserved
		4	0		R	DFE Tap 3 Polarity (Read Only)
		3:0	0000		R	DFE Tap 3 Weight (Read Only) <3:0>
0x74	00	7:5	000	N	R/W	Reserved
		4	0		R	DFE Tap 4 Polarity (Read Only)
		3:0	0000		R	DFE Tap 4 Weight (Read Only) <3:0>
0x75	00	7:5	000	N	R/W	Reserved
		4	0		R	DFE Tap 5 Polarity (Read Only)
		3:0	0000		R	DFE Tap 5 Weight (Read Only) <3:0>

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS125DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS125DF111 in a back plane application. The DS125DF111 can also be used for front port applications. The DS125DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates.

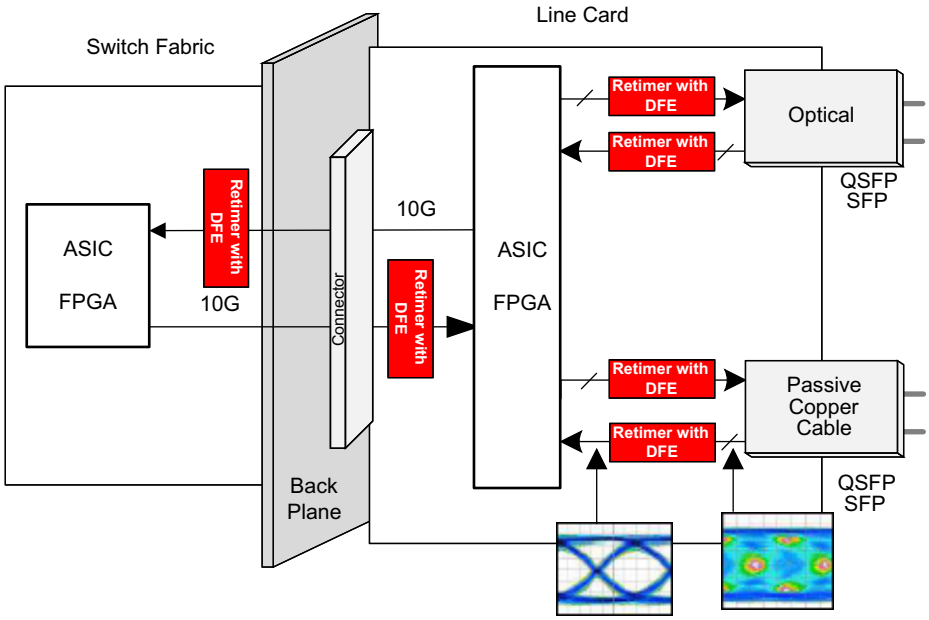


Figure 9. Typical Application

8.2.1 Design Requirements

This section lists some critical areas for high speed printed circuit board design consideration and study.

- Utilize 100-Ω differential impedance traces.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.
- Place AC-Coupling capacitors for the transmitter links near the receiver for that channel.
- The maximum body size for AC-coupling capacitors is 0402.

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Typical Application (continued)

8.2.2 Detailed Design Procedure

To begin the design process determine the following:

- Select a reference clock frequency and routing scheme.
- Plan out channel connectivity. Be sure to note any desired polarity inversion routing in the board schematics.
- Ensure that each device has a unique SMBus address if the control bus is shared with other devices or components.
- Use the IBIS-AMI model for simple channel simulations before PCB layout is complete.

Initialization Sequence: Channel Register Configurations repeated for all desired channels:

- CDR reset
- Adapt Mode Configuration
- Data rate selection
- Output driver VOD and De-Emphasis Optional Interrupt enable
- Optional Reference clock loop through enable
- CDR reset release

8.2.3 Application Curves

8.2.3.1 SFF-8431 Testing

Testing for Receiver Jitter Tolerance based on SFF-8431 section D11.

- Datarate: 10.3125 Gbps
- PRBS15 Pattern
- Output Amplitude: 700 mV
- Periodic Jitter: 70 mUI at 20 MHz
- ISI Jitter: 10" 4-mil FR4 differential microstrip + Limiting Amplifier
- Random Jitter noise source: Agilent 346B

The SFF-8431 specification combines deterministic, random, and periodic jitter components. The combination of these jitter components has been measured and calibrated to ensure adequate levels of individual jitter components and total jitter.

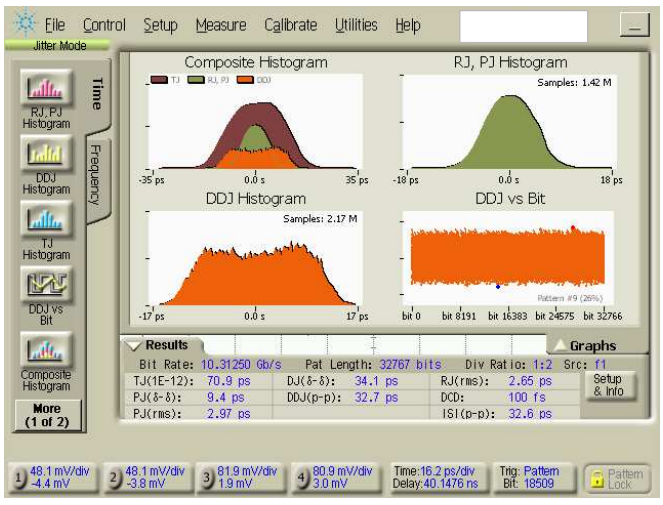


Figure 10. SFF-8431 Rx Input Jitter Profile

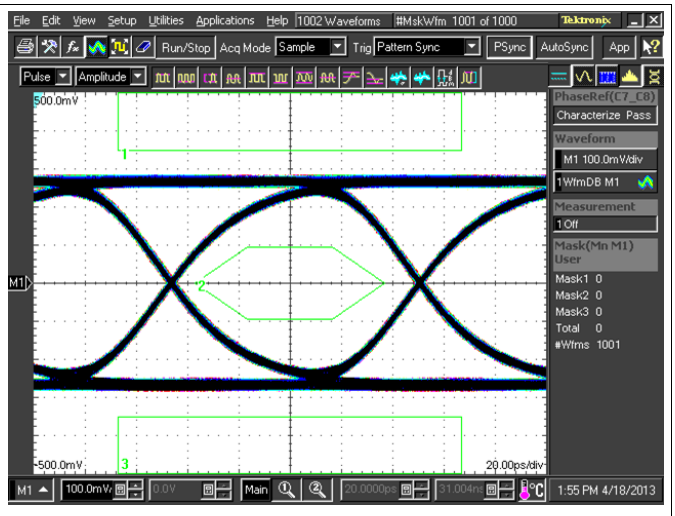


Figure 11. SFF-8431 Output Jitter Eye Mask

The SFF-8431 specification defines a transmit eye mask to ensure robust signal reception across the host - module interface.

9 Power Supply Recommendations

The DS125DF111 has an optional internal voltage regulator to provide the 2.5-V supply. In 3.3-V mode operation, the V_{IN} pin = 3.3 V is used as the power supply input to the device. The internal regulator provides 2.5 V to the V_{DD} pins of the device. A 0.22-uF cap is needed at each of the 2 V_{DD} pins for power supply de-coupling (total capacitance should be ≤ 0.5 µF). These local decoupling capacitors should be the only connection to the DS125DF111 V_{DD} net as the internal regulator is not designed to supply power to additional devices. In 2.5-V mode operation, the V_{IN} pin should be connected to directly to the 2.5-V supply, a voltage less than 2.9 V will disable the internal regulator allowing an external supply to power the DS125DF111.

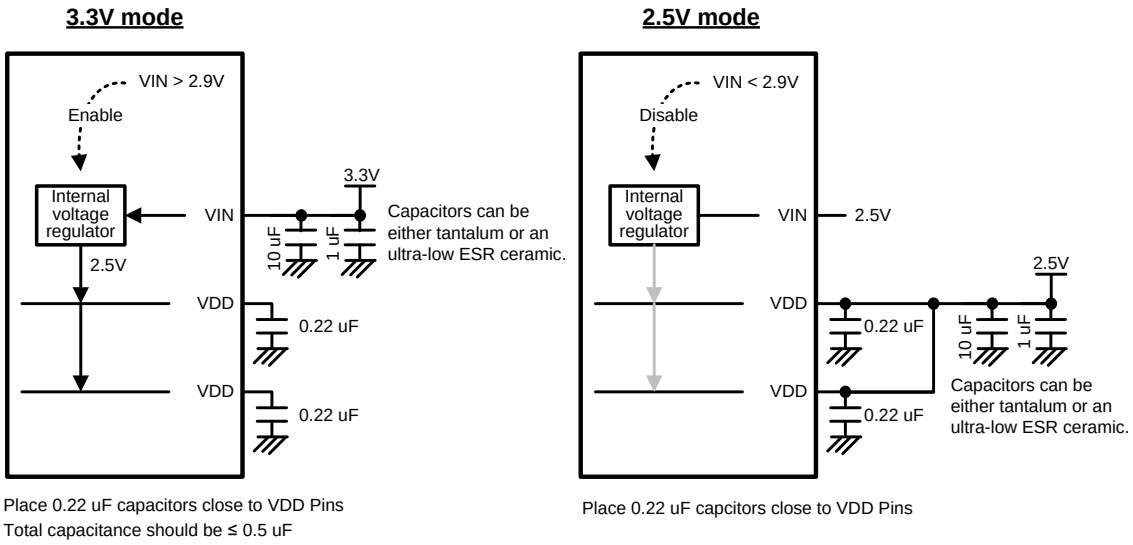


Figure 12. DS125DF111 Power Supply and Regulator Connections

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10 Layout

10.1 Layout Guidelines

The high speed inputs and outputs have been optimized to work with interconnects using a controlled differential impedance of 100Ω. Vias should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board.

Figure 13 highlights good high-speed layout techniques.

1. Maintain differential pair symmetry to minimize any signal conversion to common mode.
2. Isolate Tx - Rx differential pairs with a minimum of 5x inter-pair to intra-pair spacing ratio.
3. Decoupling should be placed as close as possible to the DS125DF111
4. Use differential vias which incorporate reference plane current returns and relief to minimize impedance disruption.
5. Use a back-drill technique to minimize via stubs.
6. Keep Loop Filter capacitors as close as possible to the DS125DF111.

10.2 Layout Example

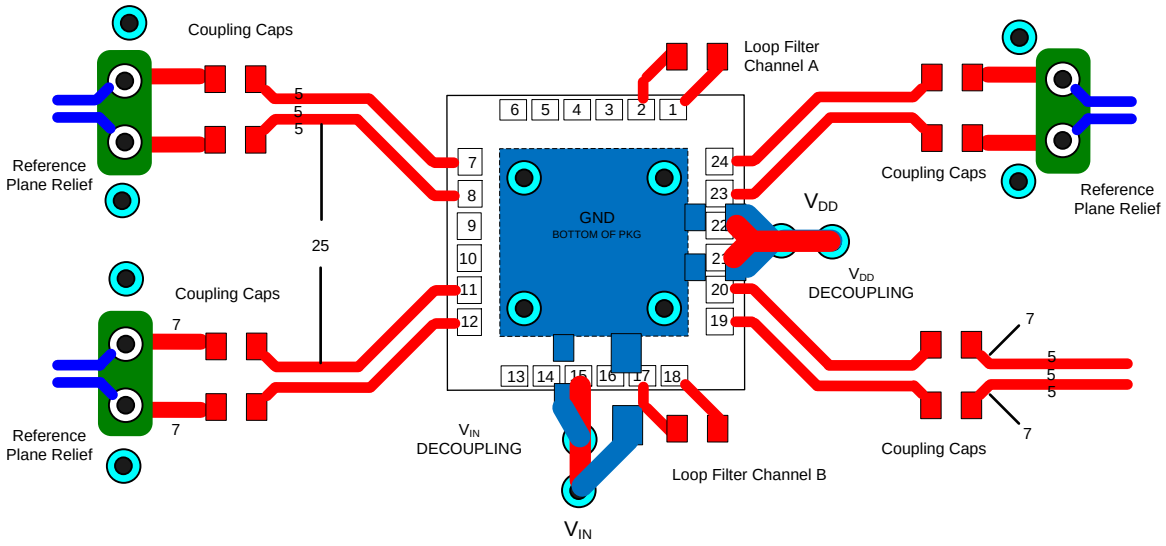


Figure 13. DS125DF111 Typical Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

Absolute Maximum Ratings for Soldering, SNOA549

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS125DF111SQ	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	2D111B2	Samples
DS125DF111SQE	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	2D111B2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

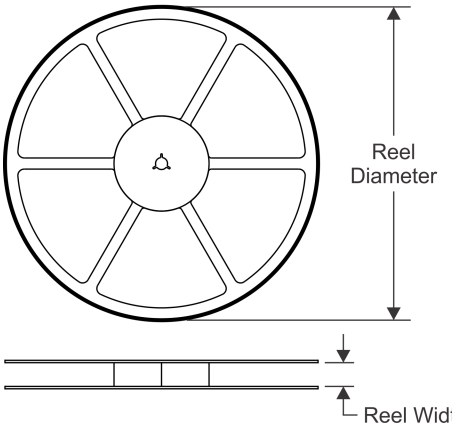
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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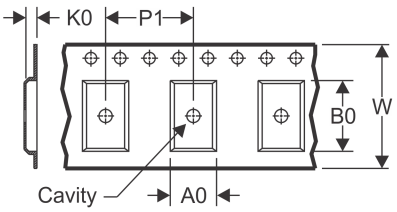
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TAPE AND REEL INFORMATION

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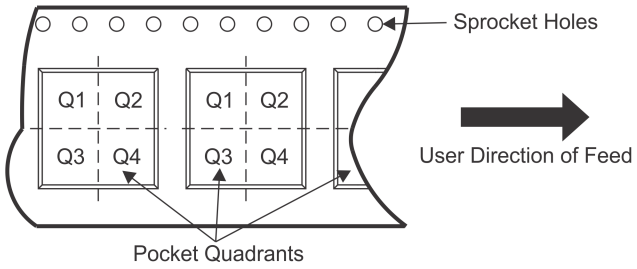


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

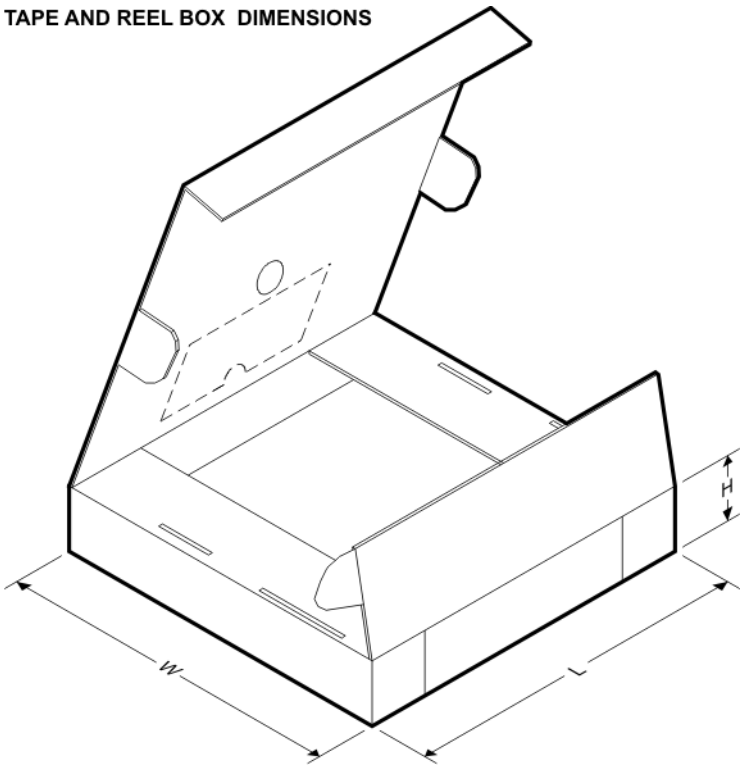
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS125DF111SQ	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
DS125DF111SQE	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

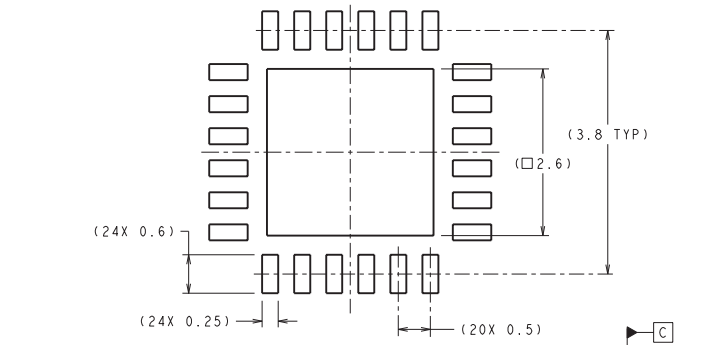
TAPE AND REEL BOX DIMENSIONS



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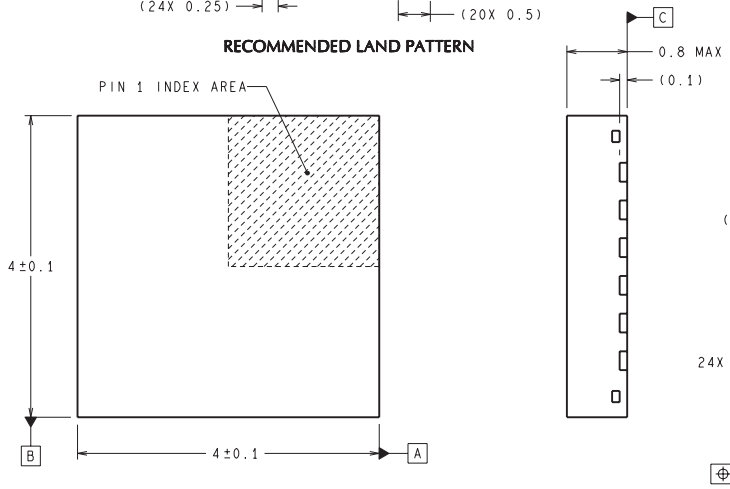
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS125DF111SQ	WQFN	RTW	24	1000	213.0	191.0	55.0
DS125DF111SQE	WQFN	RTW	24	250	213.0	191.0	55.0

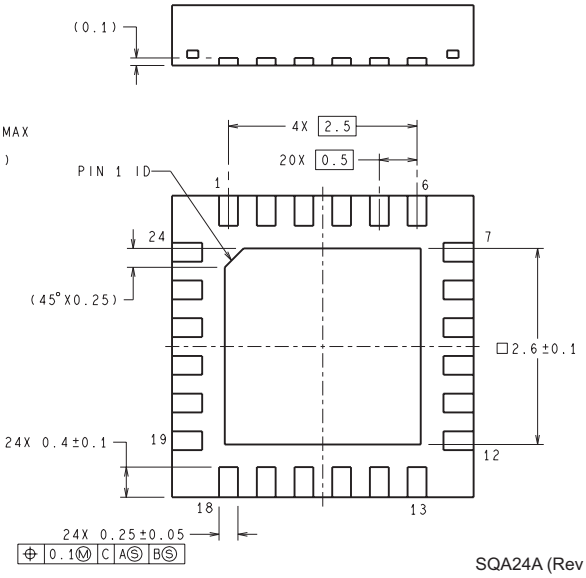
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