SONY

CXD2300Q

8-bit 18MSPS Video A/D Converter with 3.3V Power Supply Operation Function

Description

The CXD2300Q is an 8-bit CMOS A/D converter for video with synchronizing clamp function and can operate on 3.3 V power supply. The adoption of 2 step-parallel method achieves ultra-low power consumption and a maximum conversion speed of 18MSPS.

Features

- Resolution: 8-bit ± 1/2LSB (DL)
- Maximum sampling frequency: 18MSPS
- Low power consumption: 18 mW (at 18MSPS typ.) (reference current excluded)
- Synchronizing clamp function
- Clamp ON/OFF function
- Reference voltage self-bias circuit
- Input CMOS compatible
- 3-state TTL compatible output
- Single 3.3 V power supply
- Low input capacitance: 8 pF
- Reference impedance: 330 Ω (typ.)

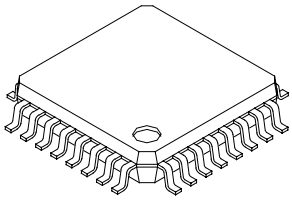
Applications

Wide range of applications that require high-speed A/D conversion such as TV and VCR.

Structure

Silicon gate CMOS IC

32 pin QFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{DD}	7	V
• Reference voltage	V_{RT}, V_{RB}	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Input voltage (Analog)	V_{IN}	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Input voltage (Digital)	V_I	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Output voltage (Digital)	V_O	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Storage temperature	Tstg	–55 to +150	°C

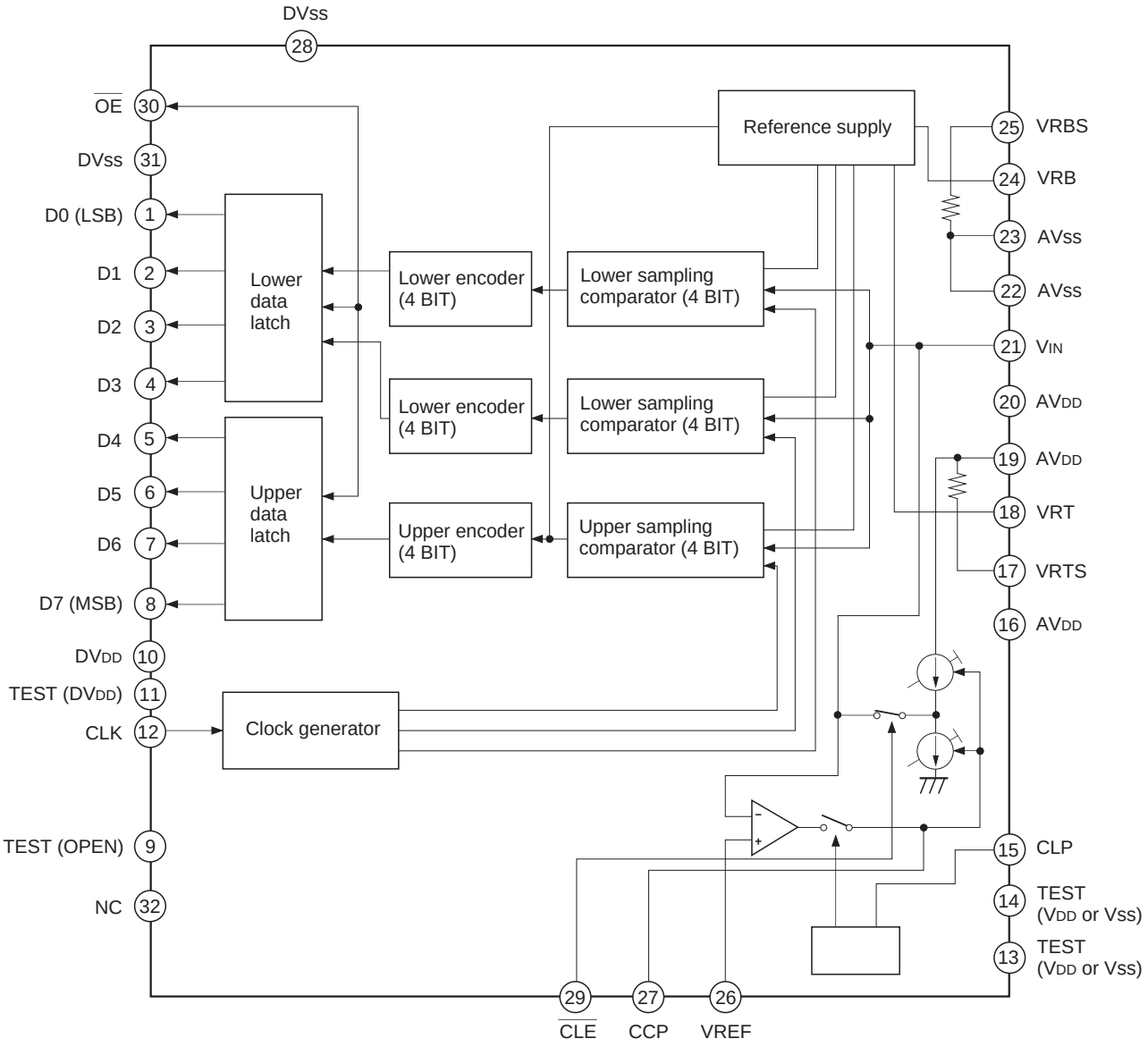
Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	3.14 to 4.0	V
	DV_{DD}, DV_{SS}		
	| DGND – AGND |	0 to 100	mV
• Reference input voltage			
	V_{RB}	0 to	V
	V_{RT}	to V_{DD}	V
• Analog input	V_{IN}	1.3 Vp-p above	
• Clock pulse width			
	Tpw_1, Tpw_0	25 ns (min) to 1.1 µs (max)	
• Operating ambient temperature			
	Topr	–40 to +85	°C

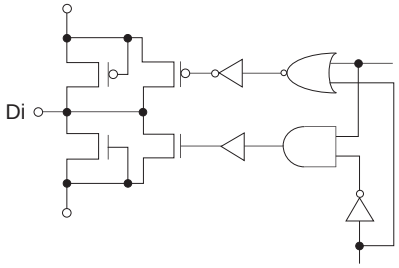
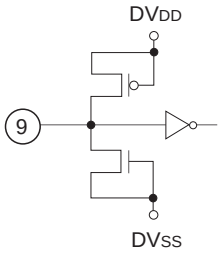
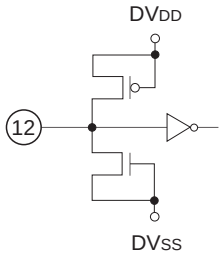
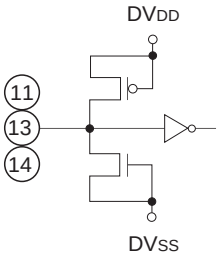
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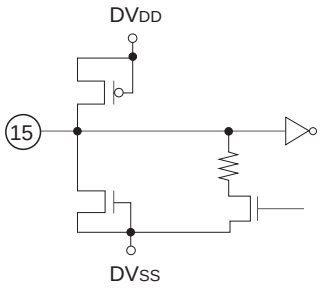
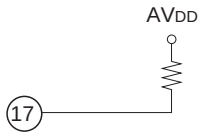
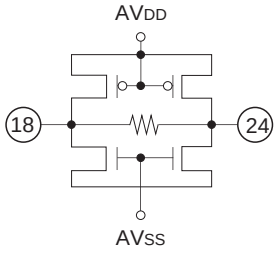
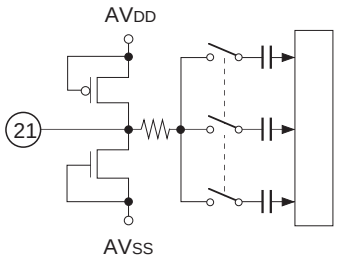
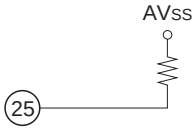
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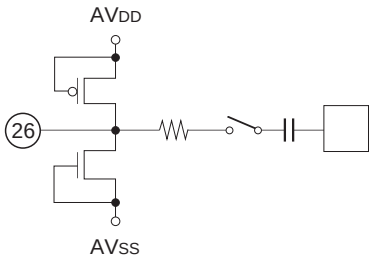
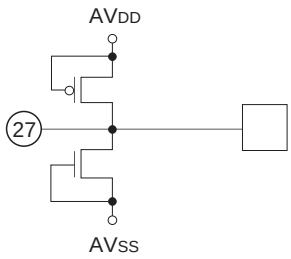
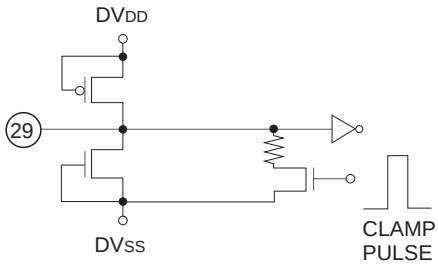
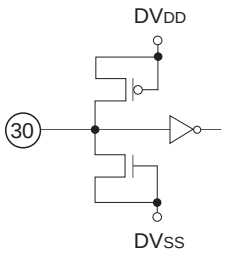
Block Diagram



Pin Description

Pin No.	Symbol	Equivalent circuit	Description
1 to 8	D0 to D7		D0 (LSB) to D7 (MSB) output
9	TEST		Leave open during normal usage.
10	DV_{DD}		Digital + 3.3 V
12	CLK		Clock input
11, 13, 14	TEST		Fix Pin 11 to V_{DD}, Pins 13 and 14 to V_{DD} or V_{SS} during normal usage.

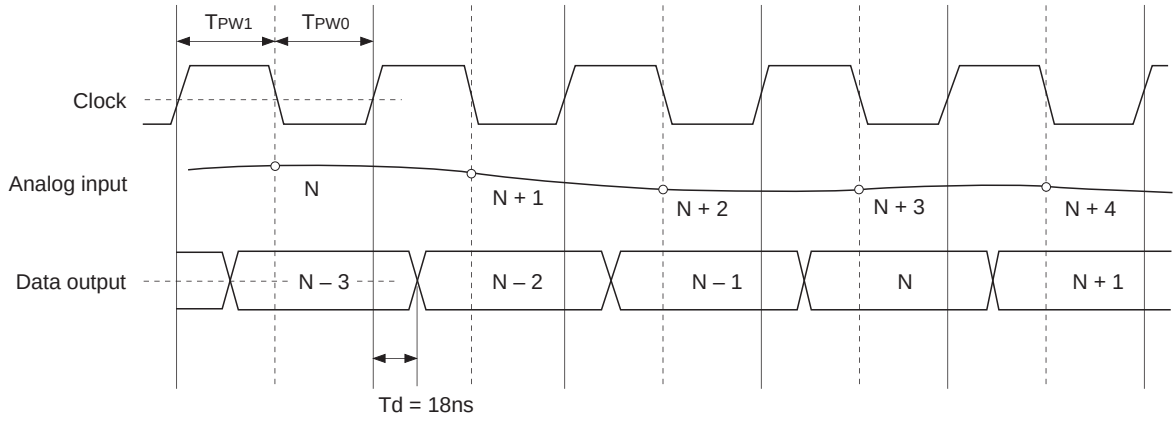
Pin No.	Symbol	Equivalent circuit	Description
15	CLP		Inputs clamp pulse to Pin 15 (CLP). Clamps the signal voltage during Low interval.
16, 19, 20	AVDD		Analog + 3.3 V
17	VRTS		Generates about +1.8 V when shorted with VRT.
18	VRT		Reference voltage (top)
24	VRB		Reference voltage (bottom)
21	VIN		Analog input
22, 23	AVSS		Analog ground
25	VRBS		Generates about +0.4 V when shorted with VRB.

Pin No.	Symbol	Equivalent circuit	Description
26	VREF		Clamp reference voltage input. Clamps so that the reference voltage and the input signal during clamp interval are equal.
27	CCP		Integrates the clamp control voltage. The relationship between the changes in CCP voltage and in V_{IN} voltage is positive phase.
28, 31	DVSS		Digital ground
29	$\overline{CLE}$		The clamp function is enabled when $\overline{CLE}$ = Low. The clamp function is set to off and the converter functions as a normal A/D converter when $\overline{CLE}$ = High. The clamp pulse can be measured by connecting $\overline{CLE}$ to DV_{DD} through a several hundred Ω resistor.
30	$\overline{OE}$		Data is output when $\overline{OE}$ = Low. Pins D0 to D7 are at high impedance when $\overline{OE}$ = High.
32	NC		NC pin

Digital Output

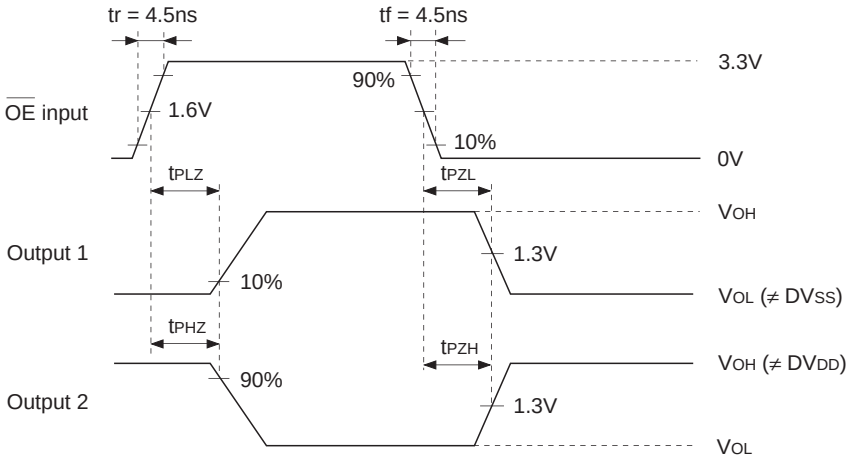
The following table shows the relationship between analog input voltage and digital output code.

Input signal voltage	Step	Digital output code MSB LSB
V_{RT}	0	1 1 1 1 1 1 1 1
:	:	:
:	127	1 0 0 0 0 0 0 0
:	128	0 1 1 1 1 1 1 1
:	:	:
V_{RB}	255	0 0 0 0 0 0 0 0



○ : Analog signal sampling point

Timing Chart I.



Timing Chart II.

Electrical Characteristics

Analog characteristics (Fc = 18MSPS, V_{DD} = 3.3 V, V_{RB} = 0 V, V_{RT} = 1.5 V, Ta = 25 °C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Conversion speed	Fc	V_{DD} = 3.14 to 4.0 V Ta = –40 to +85 °C V_{IN} = 0 to 1.5 V f_{IN} = 1 kHz ramp		0.5		18	MSPS
Analog input band width	BW	V_{IN} = 1.4 Vp-p, 17.9 MHz			–0.9		dB
Offset voltage*1	E_{OT}	Potential difference to V_{RT}		–45	–25	–5	mV
	E_{OB}	Potential difference to V_{RB}		40	60	80	
Integral non-linearity error	E_L	End point			+0.5	±1.3	LSB
Differential non-linearity error	E_D				±0.3	±0.5	
Aperture jitter	taj				30		ps
Sampling delay	tsd				4		ns
Clamp offset voltage*2	Eoc	V_{IN} = DC, PWS = 3 µs	V_{REF} = 0.5 V	–20	0	+20	mV
			V_{REF} = 1.5 V	–30	–10	+10	
Clamp pulse delay	tcpd				25		ns

*1 The offset voltage EOB is a potential difference between VRB and a point of position where the voltage drops equivalent to 1/2 LSB of the voltage when the output data changes from “00000000” to “00000001”. EOT is a potential difference between VRT and a potential of point where the voltage rises equivalent to 1/2LSB of the voltage when the output data changes from “11111111” to “11111110”.

*2 Clamp offset voltage varies individually. When using with R, G, B 3 channels, color sliding may be generated.

DC characteristics (Fc = 18MSPS, V_{DD} = 3.3 V, V_{RB} = 0 V, V_{RT} = 1.5 V, Ta = 25 °C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply current	I_{DD}	Fc = 18MSPS NTSC ramp wave input			5.5	10	mA
Reference pin current	I_{REF}			3.3	4.6	6.6	mA
Analog input capacitance	C_{IN}	V_{IN} = 0.75 V + 0.07 Vrms			8		pF
Reference resistance (V_{RT} to V_{RB})	R_{REF}			230	330	440	Ω
Self-bias	V_{RB1}	Shorts VRB and VRBS Shorts VRT and VRTS		0.33	0.36	0.39	V
	$V_{RT1} – V_{RB1}$			1.30	1.39	1.48	
Digital input voltage	V_{IH}	V_{DD} = 3.14 to 3.6 V Ta = –40 to +85 °C		2.5			V
	V_{IL}					0.5	
Digital input current	I_{IH}	V_{DD} = max	$V_{IH} = V_{DD}$			5	µA
	I_{IL}		V_{IL} = 0 V			5	
Digital output current	I_{OH}	$\overline{OE} = V_{SS}$ V_{DD} = min	$V_{OH} = V_{DD} – 0.5$ V	–1.0			mA
	I_{OL}		V_{OL} = 0.4 V	3.3			
	I_{OZH}	$\overline{OE} = V_{DD}$ V_{DD} = max	$V_{OH} = V_{DD}$			16	µA
	I_{OZL}		V_{OL} = 0 V			16	

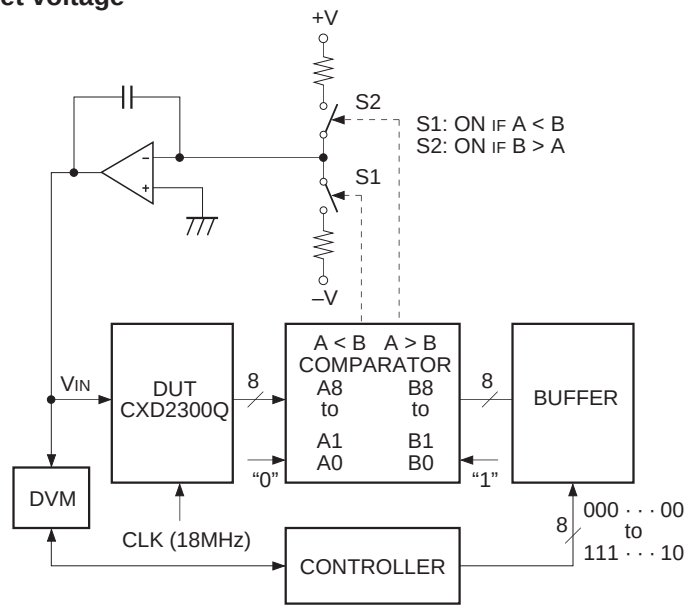
Timing (Fc = 18MSPS, V_{DD} = 3. 3V, V_{RB} = 0 V, V_{RT} = 1.5 V, Ta = 25 °C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output data delay	T_{DL}	With TTL 1 gate and 10pF load V_{DD} = 3.14 to 3.6 V Ta = –40 to +85 °C	8	18	30	ns
Tri-state output enable time	t_{PZH} t_{PZL}	R_L = 1 kΩ, C_L = 20 pF $\overline{OE}$ = 3 V → 0 V V_{DD} = 3.14 to 3.6 V Ta = –40 to +85°C	6	12	25	ns
Tri-state output disable time	t_{PHZ} t_{PLZ}	R_L = 1 kΩ, C_L = 20 pF $\overline{OE}$ = 0 V → 3 V V_{DD} = 3.14 to 3.6 V Ta = –40 to +85 °C	4	7.5	16	ns
Clamp pulse width*1	tcpw	Fc = 14.3MSPS, C_{IN} = 10 µF for NTSC wave	1.75	2.75	3.75	µs

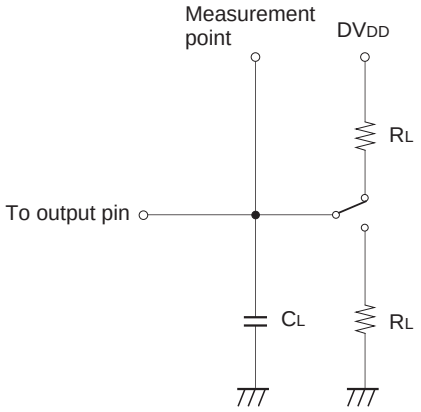
*1 The clamp pulse width is for NTSC as an example. Adjust the rate to the clamp pulse cycle (1/15.75 kHz for NTSC) for other processing systems to equal the values for NTSC.

Electrical Characteristics Measurement Circuit

Integral non-linearity error
Differential non-linearity error } **measurement circuit**
Offset voltage

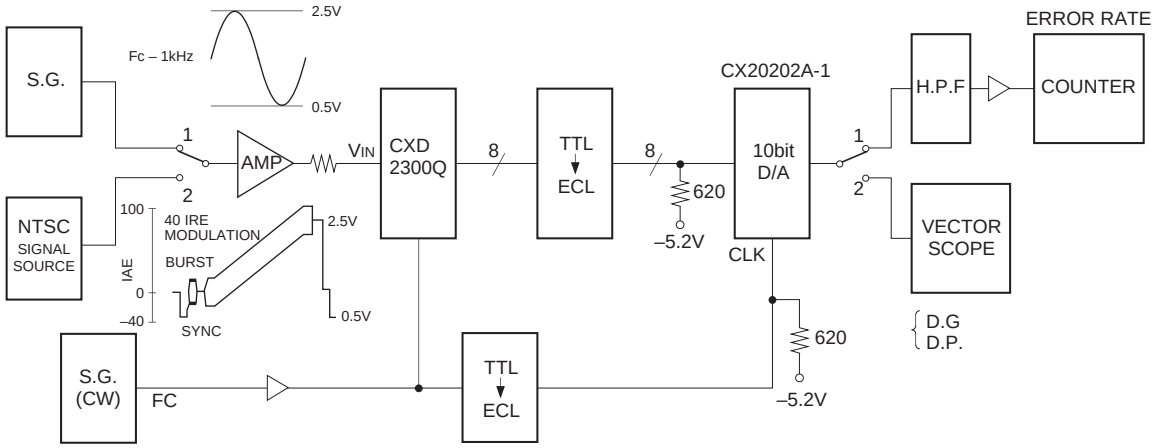


Tri-state output measurement circuit

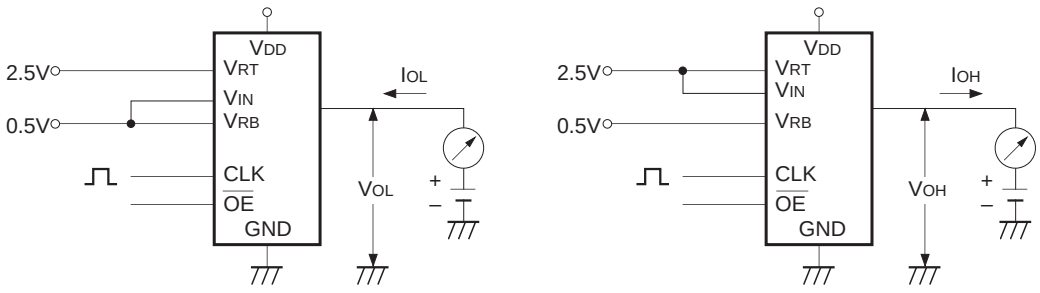


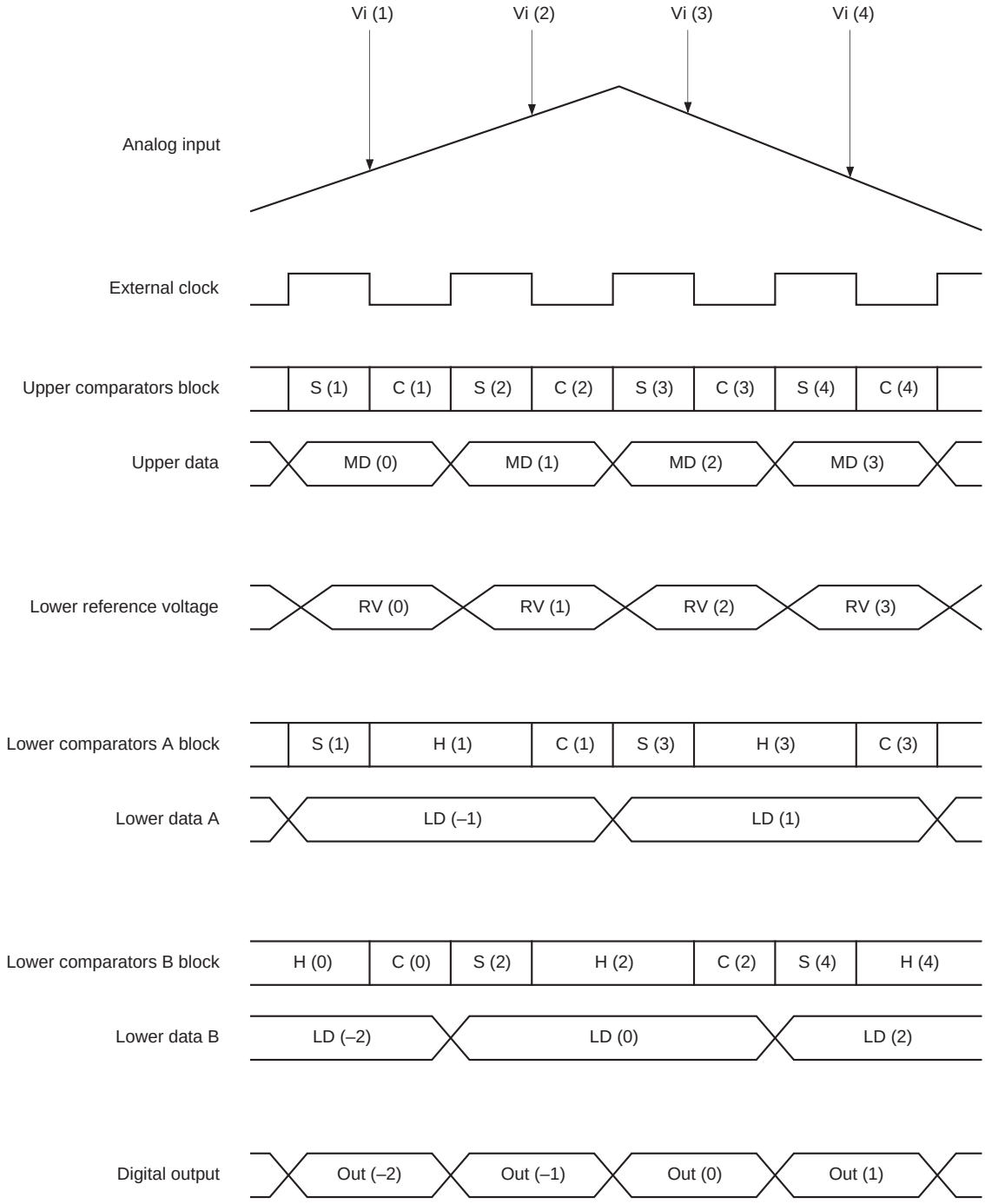
Note) CL includes capacitance of the probe and others.

Maximum operational speed
Differential gain error } **measurement circuit**
Differential phase error



Digital output current measurement circuit





Timing Chart 3

Operation (See Block Diagram and Timing Chart 3)

1. The CXD2300Q is a 2-step parallel system A/D converter featuring a 4-bit upper comparators group and 2 lower comparators groups of 4-bit each. The reference voltage that is equal to the voltage between V_{RT} – V_{RB}/16 is constantly applied to the upper 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data. VRTS and VRBS pins serve for the self generation of V_{RT} (Reference voltage top) and V_{RB} (Reference voltage bottom).

2. This IC uses an offset cancel type comparator and the comparator operates synchronously with an external clock. These modes are respectively indicated on the timing chart with S, H, C symbols. That is, the comparator performs input sampling (auto zero) mode, input hold mode and comparison mode using the external clock.

3. The operation of respective parts is as indicated in the chart. For instance input voltage Vi (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.
   The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Operation Notes

1. Power supply and ground
   To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog power supply pins, use a ceramic capacitor of about 0.1 µF set as close as possible to the pin to bypass to the respective grounds.

2. Analog input
   Compared with the flash type A/D converter, the input capacitance of the analog input is rather small.
   However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability.
   When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100 Ω in series between the amplifier output and A/D input.

3. Clock input
   The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.

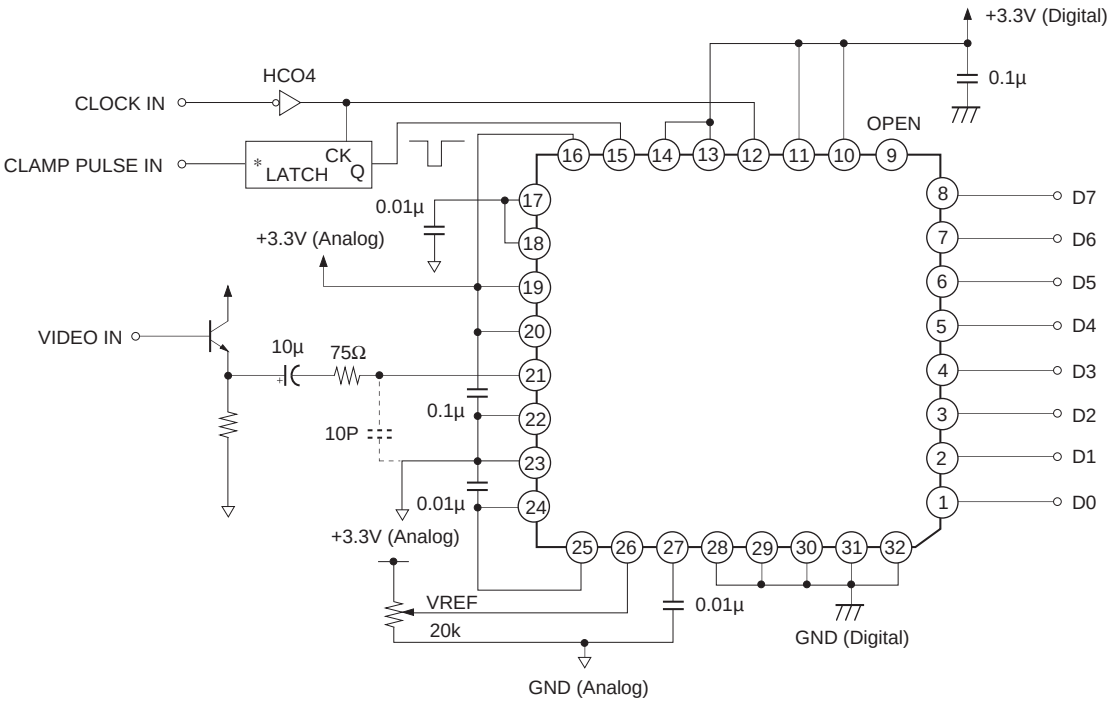
4. Reference input
   Voltage between V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. Bypassing VRT and VRB pins to analog ground, by means of a capacitor about 0.1 µF, the stable characteristics of the reference voltage are obtained. By shorting VRT and VRTS, VRB and VRBS, the self-bias function that generates V_{RT} = about 1.8 V and V_{RB} = about 0.4 V, is activated.

5. Timing
   Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18 ns.

6. $\overline{OE}$ pin
   By connecting $\overline{OE}$ to DV_{SS} output mode is obtained. By connecting $\overline{OE}$ to DV_{DD} high impedance is obtained.

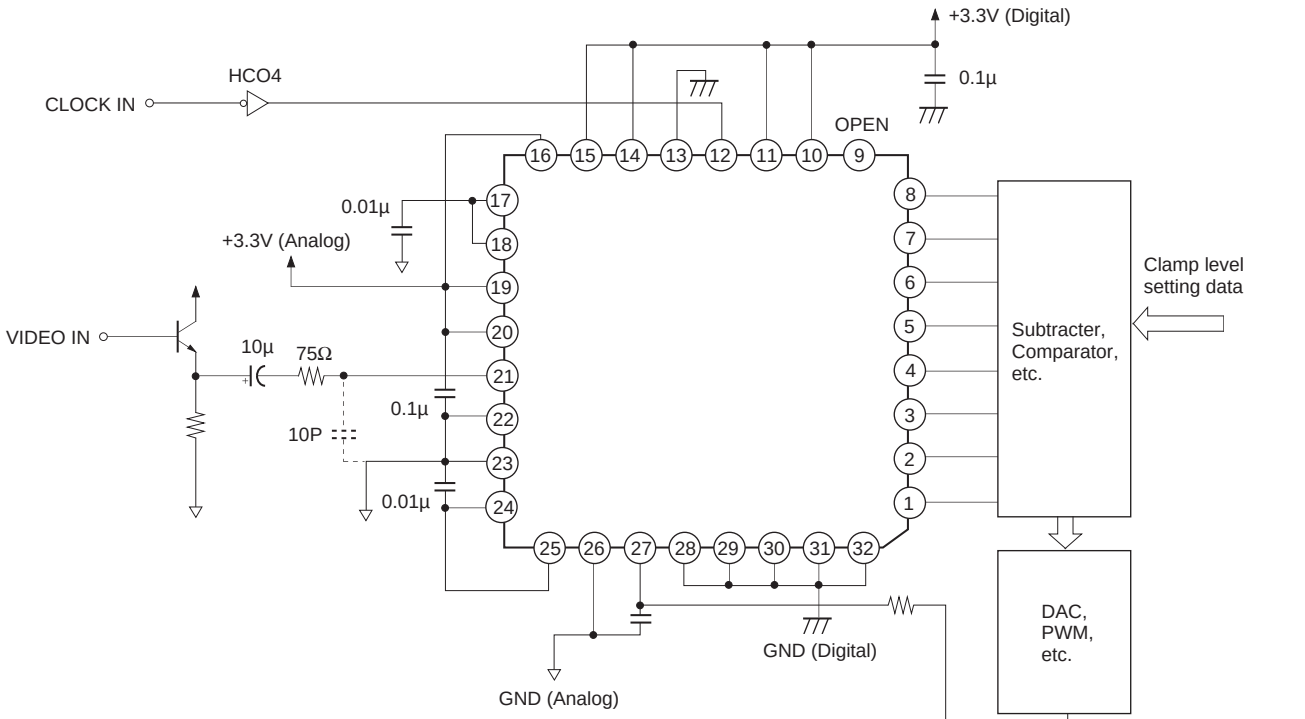
Application Circuit

(1) When clamp is used (self-bias used)



* The clamp pulse is latched by the sampling clock of ADC, but that is not necessary for basic clamp operation. However, slight small beat may be generated as vertical sag according to the relationship between the sampling frequency and the clamp pulse frequency. At such time, the latch circuit is effective in this case.

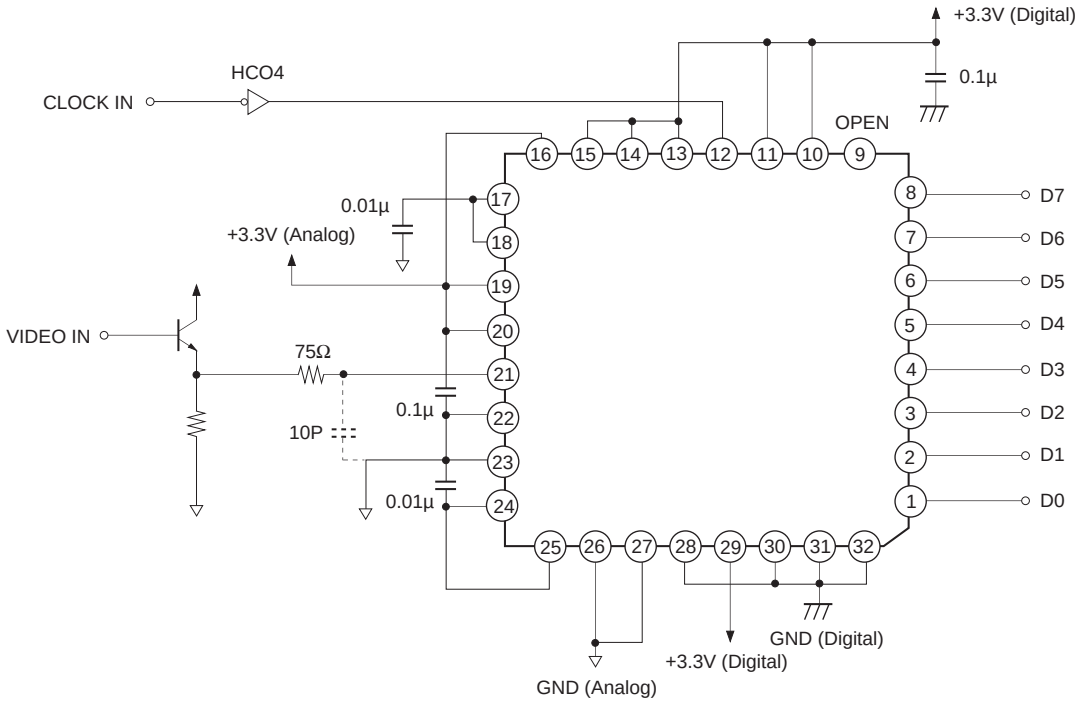
(2) Digital clamp (self-bias used)



* The relationship between the changes in CCP voltage (Pin 27) and in V_{IN} voltage is positive phase.

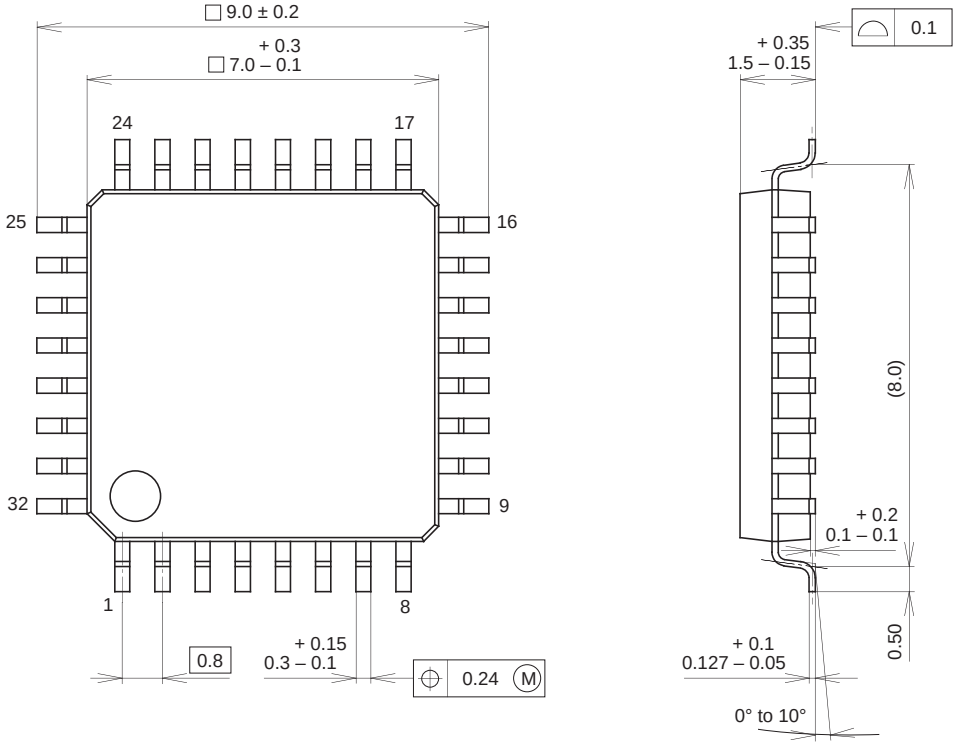
* $\Delta V_{IN}/\Delta Vccp = 3.0$ (fs = 20MSPS)

(3) When clamp is not used (self-bias used)



Package Outline Unit : mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g