ZiLOG

PRODUCT SPECIFICATION

Z84013/015
Z84C13/Z84C15
IPC INTELLIGENT PERIPHERAL CONTROLLER

FEATURES

- Z84C00 Z80 CPU with Z84C30 CTC, Z84C4X SIO, CGC, Watch Dog Timer(WDT). In addition, Z84C15 and Z84015 have Z84C20 PIO.
- High speed operation 6, 10 MHz
- 16 MHz operation for Z84C15 only.
- Low power consumption in four operation modes:
  41 mA Typ. (Run mode)
  6 mA Typ. (Idle1 mode)
  60 µA Typ. (Idle2 mode)
  0.5 µA Typ. (Stop mode)
- Wide operational voltage range (5V ± 10%).
- TTL/CMOS compatible.
- Z84013 features:
  - Z84C00 Z80 CPU
  - On-chip two channel SIO (Z80 SIO).
  - On-chip four channel Counter Timer Controller (Z80 CTC).
  - Built-in Clock Generator Controller (CGC).
  - Built-in Watch Dog Timer (WDT).
  - Noise filter to CLK/TRG inputs of the CTC.
  - 84-pin PLCC package.

  Z84015 features:
- All Z84013 features, plus on-chip two 8-bit ports (Z80 PIO) and 100-pin QFP package.

  Z84C13/Z84C15 enhancements to Z84013/Z84015:
- Power-on reset.
  - Addition of two chip select pins.
  - 32-bit CRC for Channel A of SIO.
  - Wait state generator.
  - Simplified EV mode selection.
  - Schmitt-trigger inputs to transmit and receive clocks of the SIO.
  - Crystal divide-by-one mode.
  - 100-pin VQFP (Z84C15 only)

GENERAL DESCRIPTION

The Intelligent Peripheral Controller (IPC) is a series of highly superintegrated devices with four versions. The Z84C13 and the Z84C15 are upward compatible versions of the Z84013 and the Z84015. The Z84015 is a CMOS 8-bit microprocessor integrated with the CTC, SIO, CGC, WDT and the PIO into a single 100-pin Quad Flat Pack(QFP) package. The Z84013 is the Z84015 without PIO, and is housed in a 84-pin PLCC package. The Z84C13 is the Z84013 with enhancements and the Z84C15 is the Z84015 with enhancements. These high-end superintegrated intelligent peripheral controllers are targeted for a broad range of applications ranging from error correcting modems to enhancement/cost reductions of existing hardware using Z80-based discrete peripherals. Figures 1 and 2 show the difference between the Z84013/015 and the Z84C13/Z84C15.

Hereinafter, use the word IPC on the description covering all versions (Z84C13/Z84C15 and Z84013/Z84015). Use Z84C13/C15 on the description that applies only to the Z84C13 and Z84C15, and use Z84013/015 on the description that applies only to the Z84013 and Z84015.

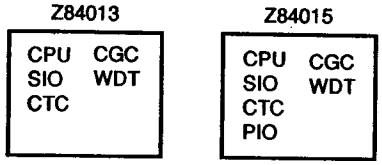


Figure 1. Z84013/015 Version

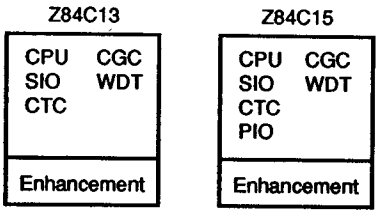


Figure 2. Z84C13/C15 Version

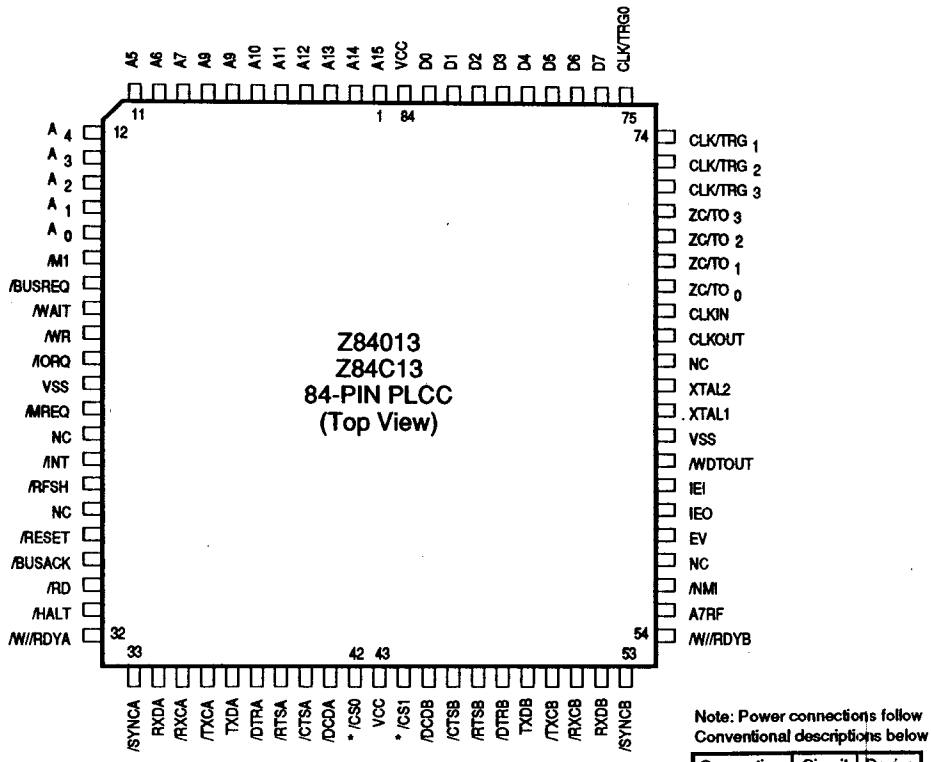
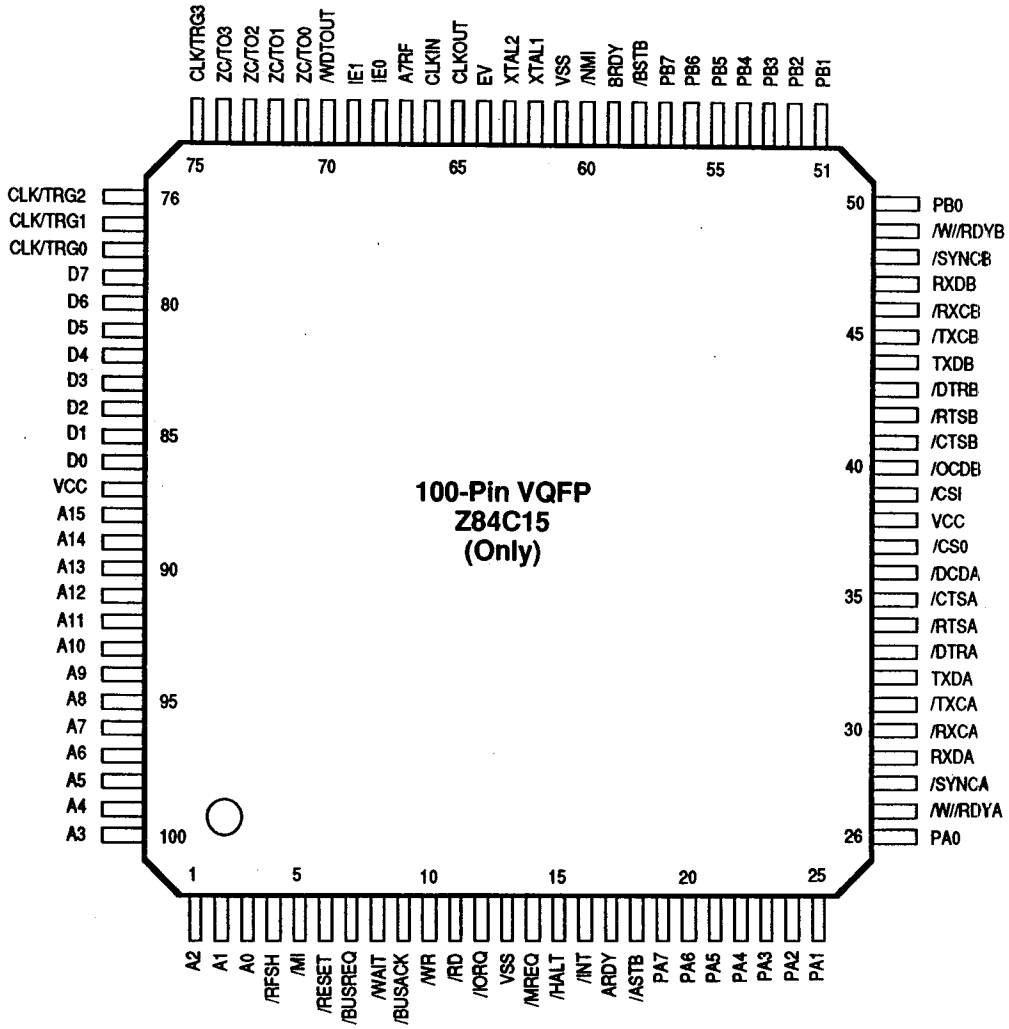


Figure 3. Z84013/Z84C13 Pin-out Assignments



Z84C15 Pin-out Assignments

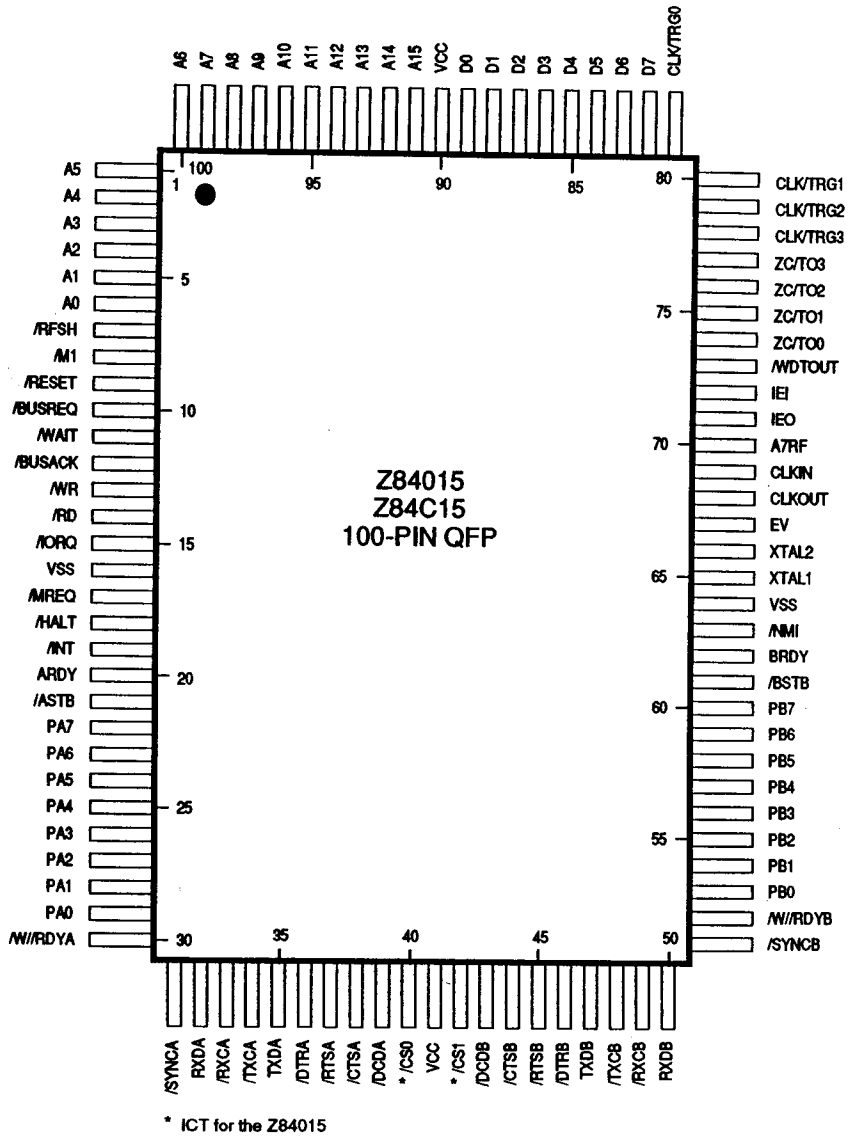


Figure 4. Z84015/Z84C15 Pin-out Assignments

PIN DEFINITIONS

The pin assignment for each device is shown in Figures 3 and 4. Following is the description on each pin. For the description and the pin number, if stated as "x13" or "x15", that applies to both Z84C13/Z84013 or Z84C15/Z84015. Otherwise, C13 for Z84C13, C15 for Z84C15, 013 for Z84013 and 015 for Z84015.

CPU SIGNALS

Pin Name	Pin Number	Input/Output, 3-State	Function
A0-A15	16-1(x13), 6-1, 100-91(x15)	I/O	16-bit address bus. Specifies I/O and memory addresses to be accessed. During the refresh period, addresses for refreshing are output. The bus is an input when the external master is accessing the on-chip peripherals.
D0-D7	83-76(x13), 89-82(x15)	I/O	8-bit bidirectional data bus. When the on-chip CPU is accessing on-chip peripherals, these lines are set to output and hold the data to/from on-chip peripherals.
/RD	30(x13), 14(x15)	I/O	Read signal. CPU read signal for accepting data from memory or I/O devices. When an external master is accessing the on-chip peripherals, it is an input signal.
/WR	20(x13), 13(x15)	I/O	Write Signal. This signal is output when data, to be stored in a specified memory or peripheral LSI, is on the MPU data bus. When an external master is accessing the on-chip peripherals, it is an input signal.
/MREQ	23(x13), 17(x15)	I/O, 3-State	Memory request signal. When an effective address for memory access is on the address bus, "0" is output. When an external master is accessing the on-chip peripherals, it is an tri-state signal.
/IORQ	21(x13), 15(x15)	I/O	I/O request signal. When addresses for I/O are on the lower 8 bits (A7-A0) of the address bus in the I/O operation, "0" is output. In addition, the /IORQ signal is output with the /M1 signal at the time of interrupt acknowledge cycle to inform peripheral LSI of the state of the interrupt response vector is when put on the data bus. When an external master is accessing the on-chip peripherals, it is an input signal.
/M1	17(x13), 8(x15)	I/O	Machine cycle "1". /MREQ and "0" are output together in the operation code fetch cycle. /M1 is output for every opcode fetch when a two byte opcode is executed. In the maskable interrupt acknowledge cycle, this signal is output together with /IORQ. It is 3-stated in EV mode.

CPU SIGNALS (Continued)

Pin Name	Pin Number	Input/Output, 3-State	Function
/RFSH	26(x13), 7(x15)	Out, 3-State	The refresh signal. When the dynamic memory refresh address is on the low order byte of the address bus, /RFSH is active along with /MREQ signal. This pin is 3-stated in EV mode.
/INT	25(x13), 19(x15)	Open drain	Maskable interrupt request signal. Interrupt is generated by peripheral LSI. This signal is accepted if the interrupt enable Flip-Flop (IFF) is set to "1". The /INT signal of on-chip peripherals is internally wired - OR without pull-up resistors and requires external pull-up. Also, interrupts from on-chip peripherals go out from this pin.
/NMI	56(x13), 63(x15)	In	Non-maskable interrupt request signal. This interrupt request has a higher priority than the maskable interrupt request and does not rely upon the state of the interrupt enable Flip-Flop (IFF).
/HALT	31(x13), 81(x15)	Out, 3-State	Halt signal. Indicates that the CPU has executed a HALT instruction. This signal is 3-stated in EV mode.
/BUSREQ	18(x13), 10(x15)	In	BUS request signal. /BUSREQ requests placement of the address bus, data bus, /MREQ, /IORQ, /RD and /WR signals into the high impedance state. /BUSREQ is normally wired-OR and a pull-up resistor is externally connected.
/BUSACK	29(x13), 12(x15)	Out (013/015), Out/3-State (C13/C15)	Bus Acknowledge signal. In response to /BUSREQ signal, /BUSACK informs a peripheral LSI that the address bus, data bus, /MREQ, /IORQ, /RD and /WR signals have been placed in the high impedance state.

Note: For the Z84013/015 the /BUSACK signal will not be 3-stated during EV mode. For the Z84C13/C15 the /BUSACK will be 3-stated during EV mode.

/WAIT	19(x13), 11(x15)	In(013/015), I/O(C13/C15)	Wait signal. /WAIT informs the CPU that specified memory or peripheral is not ready for data transfer. As long as /WAIT signal is active, MPU is continuously kept in the wait state.

Note: For the Z84C13/C15, the /WAIT pin becomes an output to bring out on-chip wait state generator during the EV mode.

CPU SIGNALS (Continued)

Pin Name	Pin Number	Input/Output, 3-State	Function
A7RF	55(x13), 70(x15)	Out	1-bit auxiliary address bus. Output is the same as bit-7 (A7) of the address bus. However, during a refresh cycle, this pin outputs the address which is the most significant bit of the 8-bit refresh address signal linked to the low order 7 bits of the address bus.

CTC SIGNALS

Pin Name	Pin Number	Input/Output, 3-State	Function
CLK/TRG0 - CLK/TRG3	75-72(x13), 81-78(x15)	In	External clock/trigger input. These four CLK/TRG pins correspond to four Counter/Timer Channels. In the counter mode, each active edge will cause the downcounter to decrement by one. In timer mode, an active edge will start the timer. It is program selectable whether the active edge is rising or falling.
ZC/TO0 - ZC/TO3	68-71(x13), 74-77(x15)	Out	Zero count/timer out signal. In either timer or counter mode, pulses are output when the down-counter has reached zero.

SIO SIGNALS

Pin Name	Pin Number	Input/Output, 3-State	Function
/W//RDYA, /W//RDYB	32,54(x13), 30,52(x15)	Out	Wait/Ready signal A and Wait/Ready signal B. Used as /WAIT or /READY depending upon SIO programming. When programmed as /WAIT they go active at "0", alerting the CPU that addressed memory or I/O devices are not ready by requesting the CPU to wait. When programmed as /READY, they are active at "0" which determines when a peripheral device associated with a DMA port is for read/write data.
/SYNCA, /SYNCB	33,53(x13), 31,51(x15)	I/O	Synchronous signals.In asynchronous receive mode, they act as /CTS and /CDC. In external sync mode, these signals act as inputs. In internal sync mode, they act as outputs.
RxDA, RxDB	34,52(x13), 32,50(x15)	In	Serial receive data signal.

SIO SIGNALS (Continued)

Pin Name	Pin Number	Input/Output, 3-State	Function
/RxCA, /RxCB	35,51(x13), 33,49(x15)	In	Receive clock signal. In the asynchronous mode, the receive clocks can be 1, 16, 32, or 64 times the data transfer rate.
/TxCA, /TxCB	36,50(x13), 34,48(x15)	In	Transmitter clock signal. In the asynchronous mode, the transmitter clocks can be 1, 16, 32, or 64 times the data transfer rate.
TxDA, TxDB	37,49(x13), 35,47(x15)	Out	Serial transmit data signal.
/DTRA, /DTRB	38,48(x13), 36,46(x15)	Out	Data terminal ready signal. When ready, these signals go active to enable the terminal transmitter. When not ready they go inactive to disable the transfer from the terminal.
/RTSA, /RTSB	39,47(x13), 37,45(x15)	Out	Request to send signal. "0" when transmitting serial data. They are active when enabling their receivers to transmit data.
/CTSA, /CTSB	40,46(x13), 38,44(x15)	In	Clear to send signal. When "0", after transmitting these signals the modem is ready to receive serial data. When ready, these signals go active to enable terminal transmitter. When not ready, these signals go inactive to disable transfer from the terminal.
/DCDA, /DCDB	41,45(x13), 39,43(x15)	In	Data carrier detect signal. When "0", serial data can be received. These signals are active to enable receivers to transmit.

SYSTEM CONTROL SIGNALS

Pin Name	Pin Number	Input/Output, 3-State	Function
IEI	60(x13), 72(x15)	In	Interrupt enable input signal. IEI is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.
IEO	59(x13), 71(x15)	Out	The interrupt enable output signal. In the daisy chain interrupt control, IEO controls the interrupt of external peripherals. IEO is active when IEI is "1" and the CPU is not servicing an interrupt from the on-chip peripherals.
/CS0 (C13/C15 only)	42(C13), 40(C15)	Out	Chip Select 0. Used to access external memory or I/O devices. This pin has been assigned to "ICT" pin on Z84013/015. This signal is decoded only from A15-A12 without control signals. Refer to "Functional Description" on-chip select signals for further explanation.

SYSTEM CONTROL SIGNALS (Continued)

Pin Name	Pin Number	Input/Output, 3-State	Function
/CS1 (C13/C15 only)	40(x13), 42(x15)	Out	Chip Select 1. Used to access external memory or I/O devices. This pin has been assigned to "ICT" pin on Z84013/015. This signal is decoded only from A15-A12 without control signals. Refer to "Functional Description" on-chip select signals for further explanation.
/WDTOUT	61(x13), 73(x15)	Out(013/015), Open Drain(C13/C15)	Watch Dog Timer Output signal. Output pulse width depends on the externally connected pin.
/RESET	28(x13), 9(x15)	Input(013/015), I/O (Open Drain) (C13/C15)	Reset signal. /RESET signal is used for initializing MPU and other devices in the system. Also used to return from the steady state in the STOP or IDLE modes.

Note: For the Z84013/Z84015 the /RESET must be kept in active state for a period of at least three system clock cycles.

Note: For the Z84C13/Z84C15, during the power-up sequence, the /RESET becomes an Open drain output and the Z84C13/C15 will drive this pin to "0" for 25 to 75 msec after the power supply passes through approx. 2.2V and then reverts to input. If it receives the /RESET signal after power-on sequence, it will drive /RESET pin for 16-processor clock cycles depending on the status of Reset Output Disable bit in Misc Control Register. If this Reset output is disabled, it must be kept in active state for a period of at least three system clock cycles. Note, that if using Z84C13/C15 in a Z84013/015 socket, modification may be required on the reset circuit since this pin is "pure input pin" on the Z84013/015. Also, the /RESET pin doesn't have internal pull-up resistors and therefore requires external pull-ups. For more details on the device, please refer to "Functional Description."

XTAL1	63(x13), 65(x15)	In	Crystal oscillator connecting terminal. A parallel resonant crystal is recommended. If external clock source is used as an input to the CGC unit, supply clock goes into this terminal. If external clock is supply to CLKIN pin (without CGC unit), this terminal must be connected to "0" or "1".
XTAL2	63(x13), 66(x15)	Out	Crystal oscillator connecting terminal.
CLKIN	67(x13), 69(x15)	In	Single-phase System Clock Input.
CLKOUT	66(x13), 68(x15)	Out	Single-phase clock output from on-chip Clock Generator/Controller.
EV	58(x13), 67(x15)	In	Evaluator signal. When "1" is applied to this pin, IPC is put in Evaluation mode.

Note: For the Z84013/015, together with /BUSREQ, the EV signal puts the IPC into the evaluation mode. When this signal becomes active, the status of /M1, /HALT and /RFSH change to input. When using Z84013/015 as an evaluator chip, the CPU is electrically disconnected after one machine cycle is executed with the EV signal "1" and the /BUSREQ signal "0". It follows the instructions from the other CPU (of ICE). Upon receiving /BUSREQ; A15-A0, /MREQ, /IORQ, /RD and /WR are changed to input and D7-D0 changes its direction. /BUSACK is NOT 3-stated so it should be disconnected by an externally connected circuit. For details, please refer to "Functional Description" on EV mode.

SYSTEM CONTROL SIGNALS (Continued)

Note: For the Z84C13/C15, to access on-chip resources from the CPU (e.g., ICE CPU), the CPU is electrically disconnected; A15-A0, /MREQ, /IORQ, /RD and /WR are changed to input; D7-D0 changes its direction; /M1, /HALT and /RFSH are put into the high impedance state when the EV pin is set to "1". Also, /BUSACK is 3-stated. For details, please refer to "Functional Description" on EV mode.

Pin Name	Pin Number	Input/Output, 3-State	Function
ICT	42,44(013), 40,42(015), Not with C13/C15	Out	Test pins. Used in the open state.
NC	24,27,57,65(x13), Not with x15		Not connected.
VCC	43,84(x13), 41,90(x15)	Power Supply	+5 Volts
VSS	22, 62(x13), 16,64(x15)	Power Supply	0 Volts

PIO SIGNALS (for the Z84x15 only)

Pin Name	Pin Number	Input/Output, 3-State	Function
/ASTB	21(x15)	In	Port A strobe pulse from a peripheral device. The signal is used as the handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see "PIO Basic Timing").
/BSTB	61(x15)	In	Port B strobe pulse from a peripheral device. This signal is used as the handshake between Port B and external circuits. The meaning of this signal is the same as /ASTB, except when Port A is in mode 2 (see "PIO Basic Timing").
ARDY	20(x15)	Out	Register A ready signal. Used as the handshake between Port A and external circuits. The meaning of this signal depends on the mode of operation selected for Port A (see "PIO Basic Timing").
BRDY	62(x15)	Out	Register B ready signal. Used as the handshake between Port B and external circuits. The meaning of this signal is the same as ARDY except when Port A is in mode 2 (see "PIO Basic Timing").
PA7-PA0	22-29(x15)	I/O, 3-State	Port A data signals. Used for data transfer between Port A and external circuits.
PB7-PB0	53-60(x15)	I/O, 3-State	Port B data signals. Used for transfer between Port B and external circuits.

The following pins have different functions between 013/015 and C13/C15

Pin Name	Pin # X13	Pin # X15	Function
/RESET	28	9	Functionality is different.
/WAIT	19	15	Functionality is different.
EV	58	67	Functionality is different.
/WDTOUT	61	73	Push-pull output on Z84013/015, Open drain on Z84 C13/C15
ICT	40, 42	42, 40	(Test pin) on Z84013/015; /CS0 and /CS1 on Z84C13/15.
TxCA, TxCB, RxCA and RxCB	35, 36, 50, 51	33, 34, 48, 49	On Z84C13/15; these signals have Schmitt-triggered inputs.
/BUSACK	29	12	In EV mode, 3-stated on Z84C13/15; remains active on Z84013/015.

FUNCTIONAL DESCRIPTION

Figure 5(a) shows the functional block diagram of the Z84013/015 and Figure 5(b) shows the functional block diagram of the Z84C13/C15. As described earlier, the only difference between the Z84x13 and the Z84x15 is the PIO not being available on the Z84x13.

Functionally, the on-chip SIO, PIO (not available on Z84x13), CTC, and the Z80 CPU are the same as the discrete devices. Therefore, for detailed description of each individual unit, refer to the Product Specification/Technical Manual of each discrete product.

The following subsections describe each individual functional unit of the IPC.

Z84C00/01 Logic Unit
The CPU provides all the capabilities and pins of the Zilog Z80 CPU. This allows 100% software compatibility with existing Z80 software. In addition, it has the pin called "A7RF" to extend DRAM refresh address to 8-bits. Refer to "Z84C01 Z80 CPU with CGC" Product Specification.

Z84C20 Parallel Input/Output Logic Unit (Z84x15 Only)
This logic unit provides both TTL- and CMOS- compatible interfaces between peripheral devices and a CPU through the use of two 8-bit parallel ports (Figure 6). The CPU configures the logic to interface to a wide range of peripheral devices with no external logic. Typical devices that are compatible with this interface are keyboards, printers, and EPROM/PAL programmers.

The parallel ports (designated Port A and Port B) are byte wide and completely compatible with the Z84C20 PIO. These two ports have several modes of operation; input, output, bi-directional, or bit control mode. Each port has two handshake signals (RDY and /STB) which are used to control data transfers. The RDY (ready) indicates that the port is ready for data transfer while /STB (strobe) is an input to the port that indicates when data transfer has occurred. Each of the ports can be programmed to interrupt the CPU upon the occurrence of specified status conditions, and generate unique interrupt vectors when the CPU responds (for more information on the operation of this portion of the logic, please refer to the Z84C20 PIO Product Specification and Technical Manual).

Z84C30 Counter/Timer Logic Unit
This logic unit provides the user with four individual 8-bit Counter/Timer Channels that are compatible with the Z84C30 CTC (Figure 7). The Counter/Timers can be programmed by the CPU for a broad range of counting and timing applications. Typical applications include event counting, interrupt and interval counting, and serial baud rate clock generation.

Each of the Counter/Timer Channels, designated Channels 0-3, have an 8-bit prescaler (when used in timer mode) and its own 8-bit counter to provide a wide range of count resolution. Each of the channels have their own Clock/Trigger input to quantify the counting process and an output to indicate zero crossing/timeout conditions. With only one interrupt vector programmed into the logic unit, each channel can generate a unique interrupt vector in response to the interrupt acknowledge cycle.

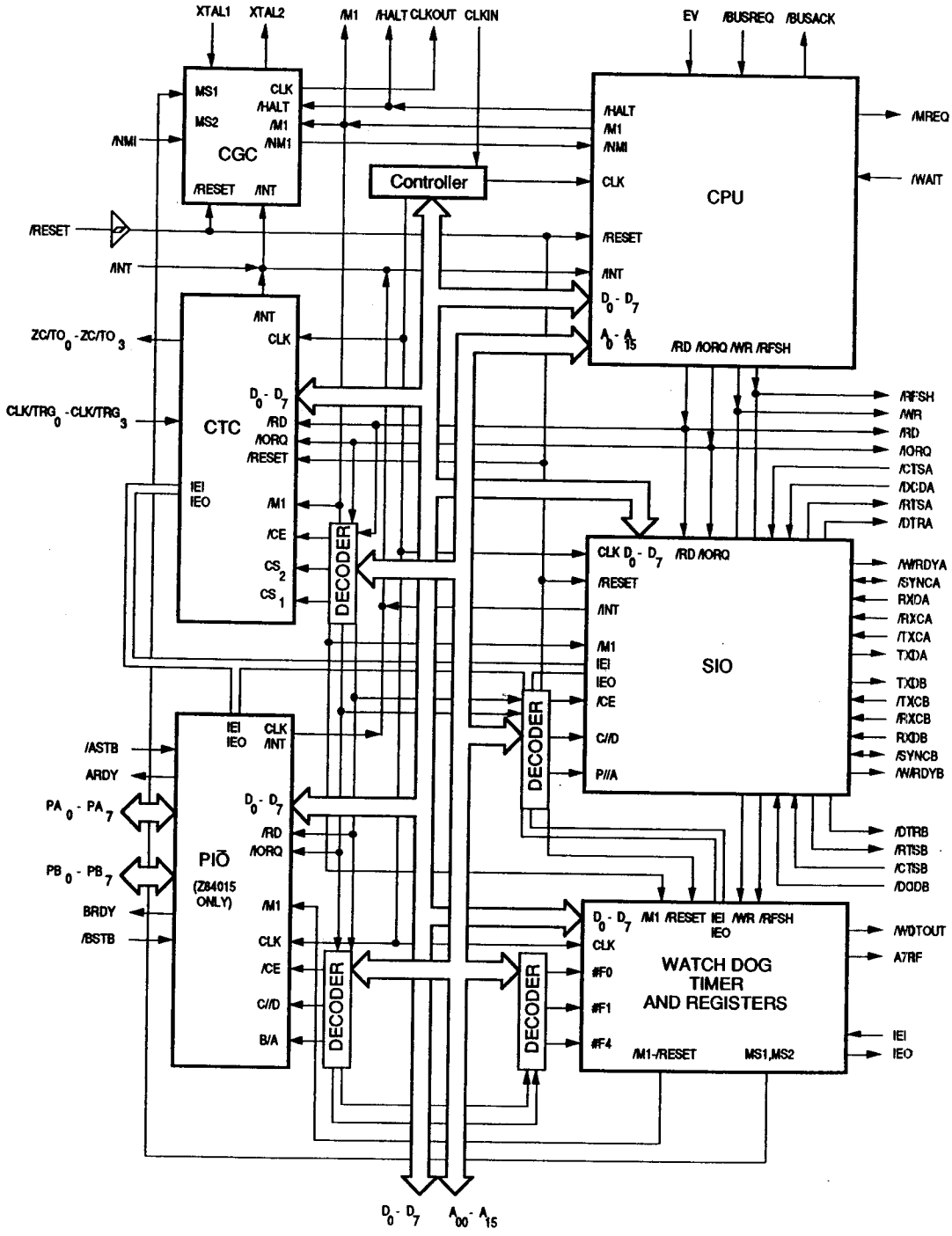


Figure 5(a). Block Diagram for 84013/015 IPC

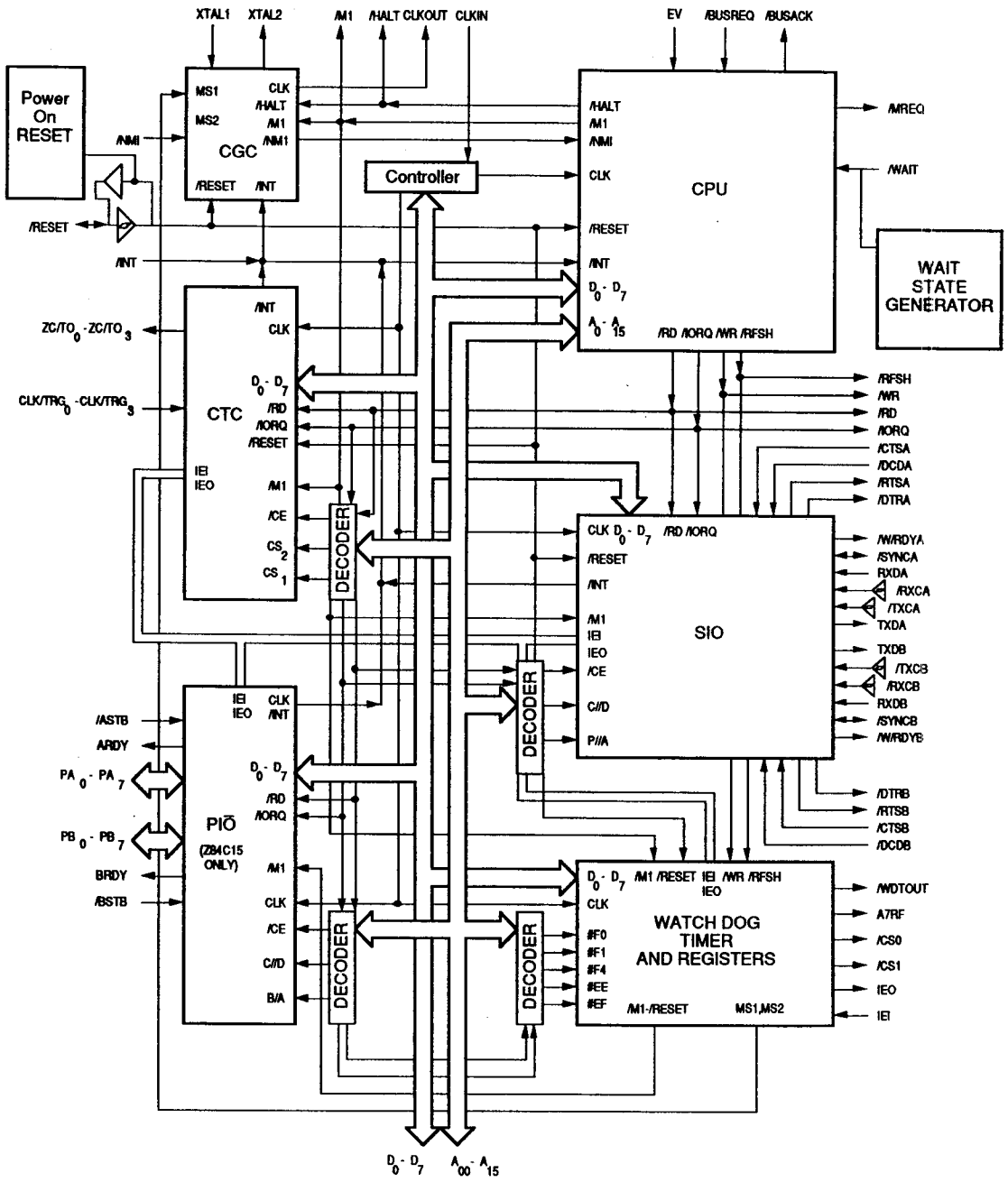


Figure 5(b). Block Diagram for 84C13/C15 IPC

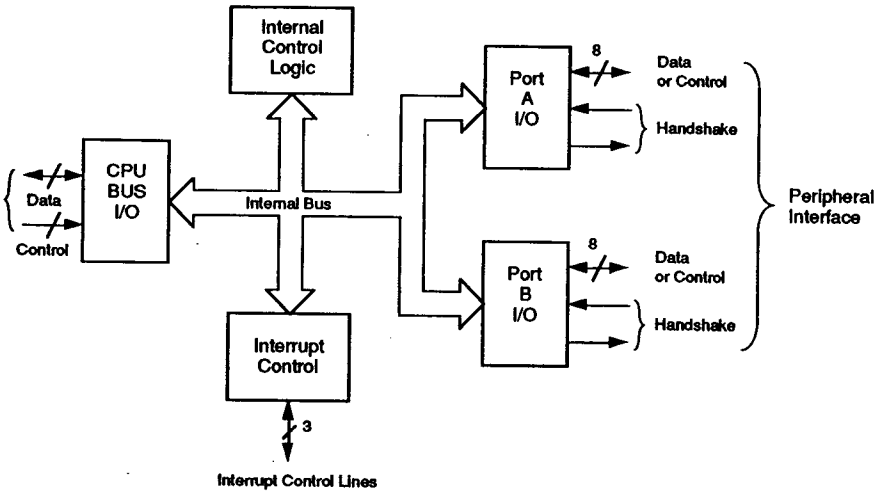


Figure 6. PIO Block Diagram

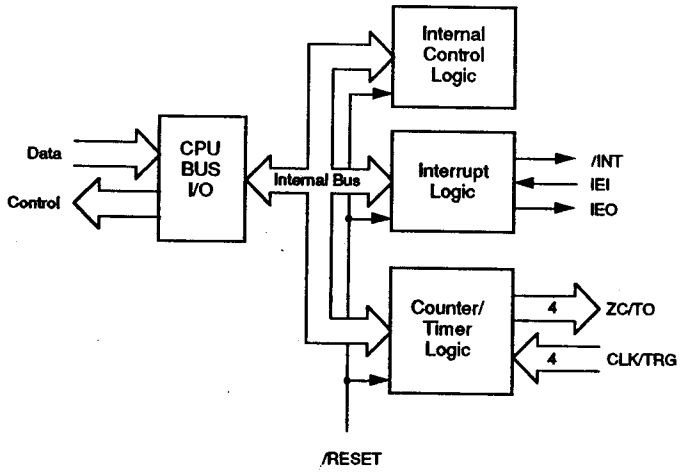


Figure 7. CTC Block Diagram

Z84C4x Serial I/O Logic Unit

This logic unit provides the user with two separate multiprotocol serial I/O channels that are completely compatible with the Z84C4x SIO. Their basic functions as serial-to-parallel and parallel-to-serial converters can be programmed by a CPU for a broad range of serial communications applications. Each channel, designated Channel A and Channel B, is capable of supporting all common asynchronous and synchronous protocols (Monosync, Bisync, and SDLC/HDLC, byte or bit oriented - Figure 8).

Z84C13/C15 Only. As an enhancement to the Z84013/015, the Z84C13/C15 can handle a 32-bit CRC on Channel A and Schmitt-trigger inputs on the /TxC and /RxC pins of both channels.

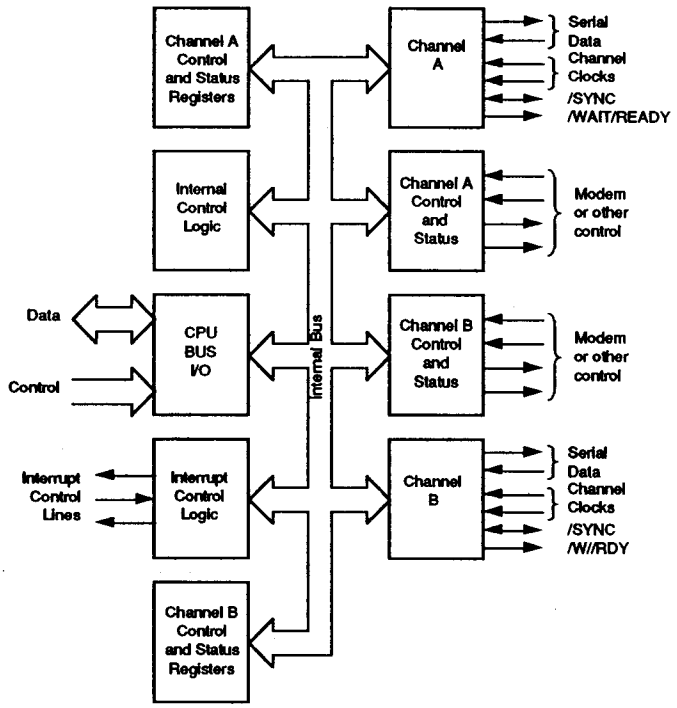


Figure 8. SIO Block Diagram

Watch Dog Timer (WDT) Logic Unit
This logic unit has been superintegrated into the IPC. It detects an operation error, caused by the program runaway, and returns to normal operation. Figure 9, shows the block diagram of the WDT. Upon Power-On Reset, this unit is enabled. If WDT is not required, but /WDTOUT is connected to /RESET or any other circuit, it has to be disabled. During the power-down mode of operation (either IDLE1/2 or Stop), the Watch Dog Timer is halted.

WDT Output (/WDTOUT pin). When the WDT is used, the "0" level signal is output from the /WDTOUT pin after a duration of time specified in the WDTP or in the WDTMR. The output pulse width is one of the following, depending on the /WDTOUT pin connection.

- The /WDTOUT is connected to the /RESET pin: The "0" level is pulsed for 5TcC (System clock cycles).
- The /WDTOUT is connected to a pin other than the /RESET pin: The "0" level is kept until the Watch Dog timer is cleared by software, or reset by /RESET pin.

CGC Logic Unit. The IPC has CGC (Clock Generator/Controller) unit. This unit is identical to the one with the Z84C01 and the Z84C50, and supports power-down modes of operation. The output from this unit is on the pin called CLKOUT, and is not connected to the system clock internally. The CLKIN pin is the system clock input. The user can connect CLKOUT to CLKIN to utilize this CGC unit, or supply external clock from CLKIN pin.

The CGC unit allows crystal input (XTAL1, XTAL2) or External Clock input on the XTAL1 pin. It has clock divide-by-two circuits and generates a half-speed clock to the input.

Z84C13/C15. The power-down modes of the IPC vary depending upon whether the system clock is fed from the CGC unit (tie CLKOUT to CLKIN) or the external clock source on the CLKIN pin. They also have divide-by-one Mode. If the clock is supplied by this CGC unit, all of the modes in "halt" state are available. When external clock is provided on the CLKIN pin, XTAL1 is not left open (tied to "0" or "1") to avoid meta-stable conditions to minimize power consumption.

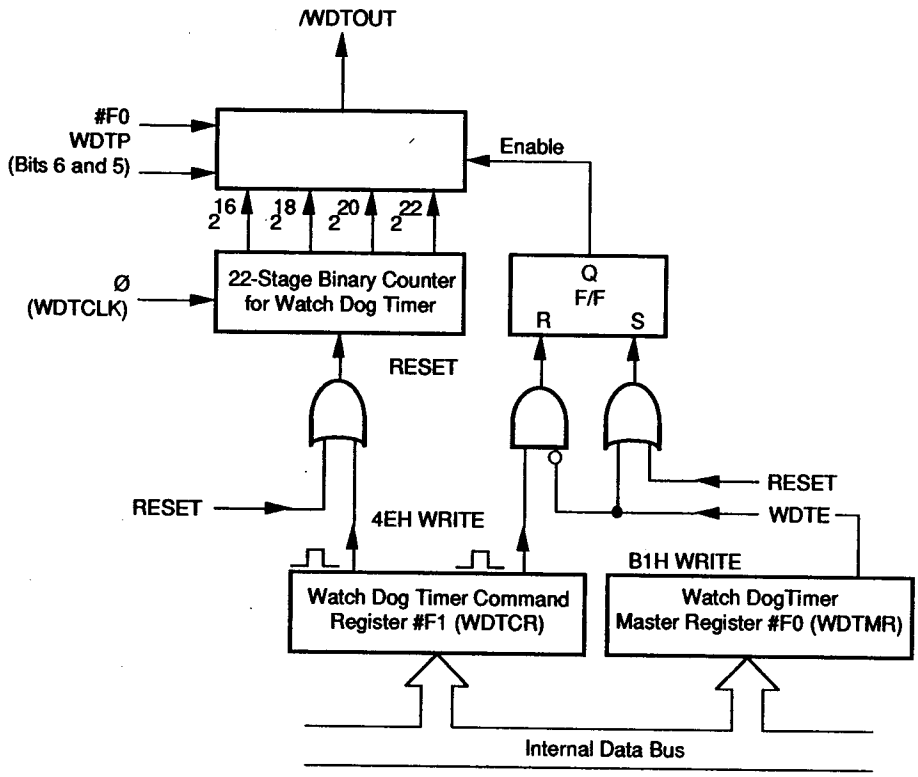


Figure 9. Block Diagram of Watch Dog Timer

Z84013/015 Only. If the system clock is provided on the CLKIN pin, none of the power-down mode (except RUN mode) is supported.

Z84C13/C15 Only. If the system clock is provided on the CLKIN pin, only the IDLE2 mode is applicable. In this mode, if the HALT instruction is executed, internal clock to the CTC is kept on "Continue", but the clock to the other components (CPU, PIO, SIO and Watch Dog Timer) are stopped. The divide-by-two circuit of the CGC unit can be skipped by programming bit D4 of the WDTMR (see "Programming" section). Upon Power-on Reset, it comes up in divide by two mode.

System Clock Generation

The IPC has a built-in oscillator circuit and the required clock can be easily generated by connecting a crystal to the external terminals (XTAL1, XTAL2). Clock output is the same frequency as half the speed of the crystal frequency. Example of oscillator connections are shown in Figure 10.

Z84C13/C15. Clock output is the same, or half, of the external frequency.

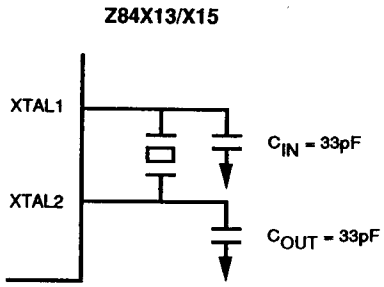


Figure 10. Circuit Configuration For Crystal

Recommended characteristics of the crystal and the values for the capacitor are as follows (the values will change with crystal frequency).

- Type of crystal: Fundamental, parallel type crystal (AT cut is recommended).
- Frequency tolerance: Application dependent.
- CL, Load capacitance: Approximately 22pf (acceptable range is 20-30pf).
- Rs, equivalent-series resistance: ≤ 150 ohms.
- Drive level: 10mW (for ≤ 10MHz crystal); 5mW (for ≥ 10MHz crystal).
- $C_{IN} = C_{OUT} = 33pF$.

Power-On Reset Logic Unit (Z84C13/C15 Only)
The Z84C13/C15 has the enhanced feature of a Power-on Reset Circuit. During the power-up sequence, the open-drain gate of the on-chip power-on Reset circuit drives /RESET pin to "0" for 25 to 75 msec after the power supply passes through approx. 2.2V. After the termination of the "Power-on Reset" cycle, the open-drain gate of the on-chip Power-on Reset circuit stops to drive the /RESET pin. It is required to have external pull-up register on the /RESET pin.

If it receives /RESET input from outside after the power-on sequence and while the Reset Output Disable bit in Misc Control Register is cleared to "0", it will drive the /RESET pin for 16-processor clock cycles from the falling edge of the external /RESET input. Otherwise, the /RESET pin must be kept in the active state for a period of at least 3 system clock cycles.

If there are power-on reset circuits outside of this device, drive this pin with OPEN-DRAIN type gates with pull-up resisters because /RESET signal is driven low for the period mentioned above during the Power-on sequence. If the external Power-on Reset circuit has push-pull type drivers and they drive the /RESET pin to "1" during that period, it may cause damage. In particular, when using Z84C13/C15 in the Z84013/015 socket, modification may be required on the external reset circuit.

Wait State Generator Unit (Z84C13/C15 Only)
The Z84C13/C15 has the enhanced feature of a Wait State Generator circuit. It is capable of generating /WAIT signals to the CPU internally. The status of the External /WAIT input line is sampled after the insertion of software wait states, except for the wait state's insertion of Interrupt Daisy Chain Wait (for this cycle, insertion of a wait state is not simple).

The Wait State Control Register can be programmed to generate multiple Wait states during different CPU cycles listed as follows.

Memory Wait and Opcode wait. The Wait State Generator can put 0 to 3 wait states in memory accesses. Additionally, one added wait state can be inserted during an /M1 (Opcode fetch) cycle, because /M1 cycle's timing requirement is tighter than memory Read/Write cycles. It generates wait states to the Memory Access in a specified address range, which is programmed in the Memory Wait Boundary Register.

I/O Wait. The Wait State generator can put 0, 2, 4 or 6 wait states in I/O accesses. Regardless of the programming of this field, no I/O wait states are inserted for accesses to on-chip peripherals.

Interrupt Vector Wait. During Interrupt acknowledge cycle, the Wait State Generator can insert one wait state after /IORQ goes active, to extend the time between /IORQ fall to vector fetch by CPU. It allows a slow vector response device.

Interrupt Daisy Chain Wait and RETI sequence extension. During Interrupt acknowledge cycle, the Wait State Generator can insert 0, 2, 4 or 6 wait states between /M1 falling to /IORQ falling edge, to extend the time required to settle daisy chain. This allows a longer daisy chain. Also, this field controls the number of wait states inserted during RETI (Return From Interrupt) cycle. If specified to insert 4 or 6 wait states during Interrupt Acknowledge cycle, Wait State Generator also inserts wait states during RETI fetch sequence. This sequence is generated with two op-code fetch cycles (Op-code is EDh followed by 4Dh). It inserts 2 or 4 wait states, respectively, if op-code followed by EDh is 4Dh. One wait state if the following op-code is not 4Dh.

Chip Select Signals (Z84C13/C15 Only)
The Z84C13/C15 has an enhanced feature of adding two chip select (/CS0, /CS1) pins. Both signals are originally IC test pins (ICT) on the Z84013/015. The boundary value for each Chip Select Signal is 4 bits wide, and compare with A15-A12 of the address. Each Chip Select Signal goes active when:

/CS0: (D3-D0 of CSBR) ≥ A15-A12 ≥ 0
/CS1: (D7-D4 of CSBR) ≥ A15-A12 > (D3-D0 of CSBR)

(Where CSBR is the contents of Chip Select Boundary Register.)

There is also a separate /CS enable bit. /CS0 is enabled on power-up with a boundary value of "F" causing /CS0 to go active for all memory accesses. /CS1 is disabled on

power-up, and boundary address is undefined. These features are controlled via the I/O control registers located at I/O address EEh and EFh. **Note that a glitch may be observed on these pins because address decode logic is decoding only A15-A12, without any control signals.** For more detail, please refer to the "Programming section."

Other functional features (Z84C13/C15 Only)
For more system design flexibility, the Z84C13/C15 has the following unique features. These features are controlled by MCR (Misc. Control Register) which is indirectly accessed via the System Control Register Pointer (SCRP, I/O address EEh), and System Control Data Port (SCDP, I/O address EFh). For more details, please refer to the "Programming" section.

- Clock Divide-by-one option
- Reset Output Disable
- 32-bit CRC Generation/Checking

Clock Divide-by-One Option. This feature is programmed through Bit D4 of MCR. Upon Power-On reset, the Clock from on-chip CGC is passed through a divide-by-two circuit. By setting this bit to one, the divide-by-two circuit is bypassed so the clock on the CLKOUT pin is equal to X'tal input. If the clock is applied to the CLKIN pin from external clock source, the status of this bit is ignored. Upon Power-on Reset, it is cleared to 0. For details, please refer to "Programming" section.

Reset Output Disable. This feature is programmed by Bit D3 of MCR. If this bit is cleared to "0", The /RESET pin becomes "Open-drain output" and is driven to "0" for 16-clock cycles from the falling edge of /RESET input. This feature is for the cases where /RESET is used to get out from the "HALT" state. If this bit is set to one, the on-chip reset circuit will not drive /RESET pin.

32-bit CRC Generation/Checking. This feature is programmed by Bit D2 of MCR. By setting this bit to one, Channel A of SIO is set to use the 32-bit CRC generator/checker instead of the original 16-bit CRC generator/checker in synchronous communication modes. The polynomial to be used in this mode is the one for the protocols such as V.42, and is (X32 + X26 + X23+ X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 + X2 + X + 1). Upon Power-on Reset, this bit is cleared to 0.

Evaluation Mode
The IPC has a built evaluation (or development) mode feature which allows the users to utilize standard Z80 development systems conveniently. This mode virtually replaces the on-chip Z80 CPU with the external CPU. In this mode, the on-chip CPU is electrically disconnected from internal bus and all 3-state signals (A15-0, D7-0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1 and /RFSH; for C13/C15, /BUSREQ as well) are tri-stated, or changed to input. This allows the development system CPU to take over and use the internal I/O registers of the IPC exactly as if the CPU was on-chip.

Z84013/015 Only. When this signal is active,the /M1, /HALT and /RFSH pins are put in the high-impedance state. In using the Z84013/015 as an evaluator chip, the CPU is electrically disconnected (put in high-impedance state) after one machine cycle is executed with the EV signal being "1" and the /BUSREQ signal being "0". Then, on-chip resources can be accessed from the outside. /BUSACK is disconnected by an externally connected circuit.

Z84C13/C15 Only. If the EV pin is tied to Vcc on Power-up, the Z84C13/C15 enters into an evaluation mode. In this mode, the internal CPU is immediately disconnected from the internal bus and all 3-state signals mentioned above are tri-stated, or changed to input. Note that the /WAIT pin became the OUTPUT pin in EV mode, and the Wait State Generator generates wait states only as programmed. If the target application board has a separate wait state generator, modification of the target may be required. /BUSACK is 3-stated in this mode.

The Z84C13/C15 behaves similarly to the situation where in regular operation, the /BUSREQ signal is asserted by an external master causing all 3-state signals to be tri-stated by the Z84C13/C15 during T1 of the following machine cycle. The /BUSREQ approach was not used for the evaluation mode to avoid significant external circuitry to work around the time period before the external CPU uses the bus for Z84C13/C15 accesses.

PROGRAMMING

I/O address assignment
The IPC 's on-chip peripherals' I/O addresses are listed in Table 1. They are fully decoded from A7-A0 and have no image.The registers with Z84C13/C15 located at I/O Address EEh and EFh are the registers to control enhanced features to Z84013/015, and not assigned on Z84C013/015.

Table 1. I/O Control Register Address

Address	Device	Channel	Register
10h	CTC	Ch 0	Control Register
11h	CTC	Ch 1	Control Register
12h	CTC	Ch 2	Control Register
13h	CTC	Ch 3	Control Register
18h	SIO	Ch. A	Data Register
19h	SIO	Ch. A	Control Register
1Ah	SIO	Ch. B	Data Register
1Bh	SIO	Ch. B	Control Register
1Ch	PIO	Port A	Data Register (Not with Z84x13)
1Dh	PIO	Port A	Command Register (Not with Z84x13)
1Eh	PIO	Port B	Data Register (Not with Z84x13)
1Fh	PIO	Port B	Command Register (Not with Z84x13)
F0h	Watch-Dog Timer		Master Register (WDTMR)
F1h	Watch-Dog Timer		Control Register (WDTCR)
F4h	Interrupt Priority Register		
EEh			System Control Register Pointer (SCRP) (Not with Z84013/015)
EFh			System Control Data Port (SCDP) (Not with Z84013/015)
	Through SCRP and SCDP		Control Register 00 - Wait State Control register (WCR) Control Register 01 - Memory Wait state Boundary Register (MWBR)
			Control Register 02 - Chip Select Boundary Register (CSBR) Control Register 03 - Misc. Control Register (MCR)

PIO REGISTERS

For more detailed information, please refer to the PIO Technical Manual. These registers are not in the Z84x13.

Interrupt Vector Word
The PIO logic unit is designed to work with the Z80 CPU in interrupt Mode 2. The interrupt word must be programmed if interrupts are used. Bit D0 must be a zero (Figure 11).

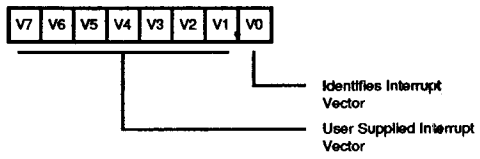


Figure 11. PIO Interrupt Vector Word

Mode Control Word

Selects the port operating mode. This word is required and is written at any time (Figure 12).

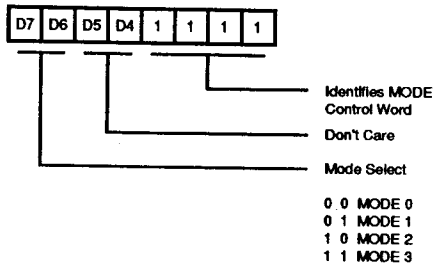


Figure 12. PIO Mode Control Word

I/O Register Control Word

When Mode 3 is selected, the Mode Control Word is followed by the I/O Register Control Word. This word configures the I/O register, which defines which port lines are inputs or outputs. A "1" indicates input while a "0" indicates output. This word is required when in Mode 3 (Figure 13).

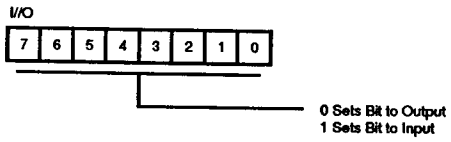
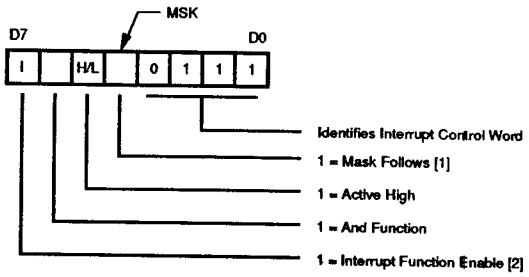


Figure 13. I/O Register Control Word

Interrupt Control Word

In Mode 3 operation, handshake signals are not used. Interrupts are generated as a logic function of the input signal levels. The Interrupt Control Word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: AND (if all input bits change to the active level, an interrupt is triggered), OR (if any one of the input bits change to the active logic level, an interrupt is triggered). The user can program which input bits are to be considered as part of this logic function. Bit D6 sets the logic function, bit D5 sets the logic level, and bit D4 specifies a mask control word to follow (Figure 14).



Note:
[1] Regardless of the operating mode, setting Bit D4 = 1 causes any pending interrupts to be cleared.
[2] The port interrupt is not enabled until the interrupt function enable is followed by an active /M1.

Figure 14. Interrupt Control Word

Mask Control Word

This word sets the mask control register, thus allowing any unused bits to be masked off. If any bits are to be masked, then bit D4 of the interrupt Control Word is set. When bit D4 of the interrupt Control Word is set, then the next word programmed is the Mask Control Word. To mask an input bit, the corresponding Mask Control Word bit is a "1" (Figure 15).

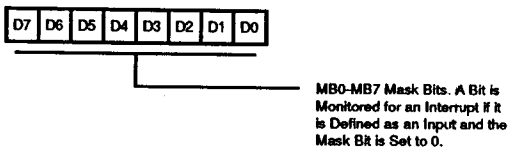


Figure 15. Mask Control Word

Interrupt Disable Word

This word can be used to enable or disable a port's interrupts without changing the rest of the port's interrupt conditions (Figure 16).

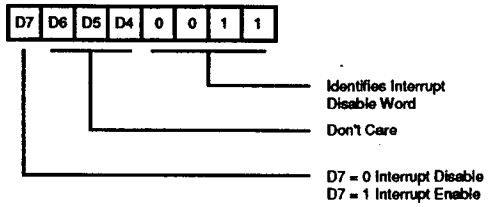


Figure 16. Interrupt Disable Word

CTC CONTROL REGISTERS

For more detailed information, refer to the CTC Technical Manual.

Channel Control Word

This word sets the operating modes and parameters as described below. Bit D0 is a "1" to indicate that this is a Control Word (Figure 17).

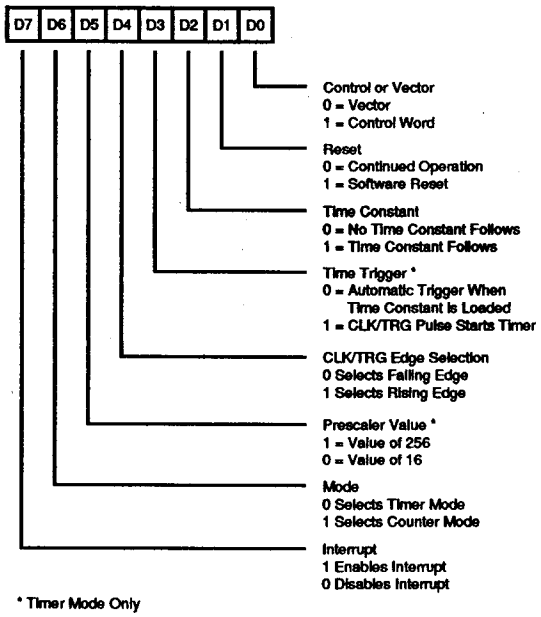


Figure 17. CTC Channel Control Word

Bit D7. *Interrupt Enable.* This bit enables the interrupt logic so that an internal INT can be generated at zero count. Interrupts are programmed in either mode and may be enabled or disabled at any time.

Bit D6. *Mode Bit.* This bit selects either Timer Mode or Counter Mode.

Bit D5. *Prescalor Factor.* This bit selects the prescalor factor for use in the timer mode. Either divide-by-16 or divide-by-256 is available.

Bit D4. *Clock/Trigger Edge Selector.* This bit selects the active edge of the CLK/TRG input pulses.

Bit D3. *Timer Trigger.* This bit selects the trigger mode for timer operation. Either automatic or external trigger may be selected.

Bit D2. *Time Constant.* This bit indicates that the next word programmed is time constant data for the downcounter.

Bit D1. *Software Reset.* Writing 1 to this bit indicates a software reset operation, which stops counting activities until another time constant word is written.

Time Constant Word

Before a channel starts counting, it must receive a time constant word. The time constant value is anywhere between 1 and 256, with "0" being accepted as a count of 256 (Figure 18).

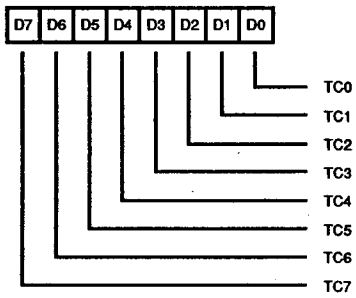


Figure 18. CTC Time Constant Word

Interrupt Vector Word

If one or more of the CTC channels have interrupt enabled, then the Interrupt Vector Word must be programmed. Only the five most significant bits of this word are programmed, and bit D0 must be "0". Bits D2-D1 are automatically modified by the CTC channels when it responds with an interrupt vector (Figure 19).

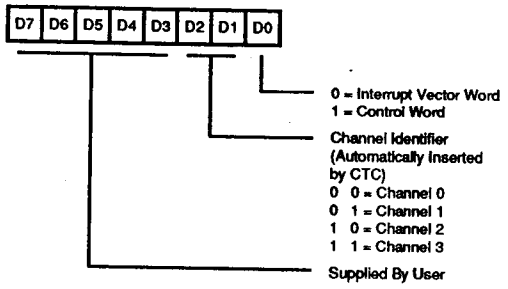


Figure 19. CTC Interrupt Vector Word

SIO REGISTERS

For more detailed information, refer to the SIO Technical Manual.

Read Registers. The SIO channel B contains three read registers while channel A contains only two that are read to obtain status information. To read the contents of a register (rather than RR0), the program must first write a pointer to WR0 in exactly the same manner as a write operation. The next I/O read cycle will place the contents of the selected read registers onto the data bus (Figure 20a, b, c).

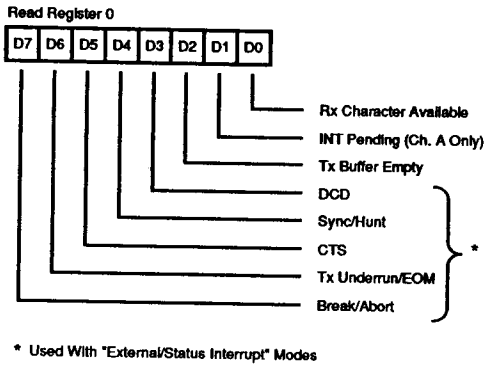


Figure 20a. SIO Read Register 0

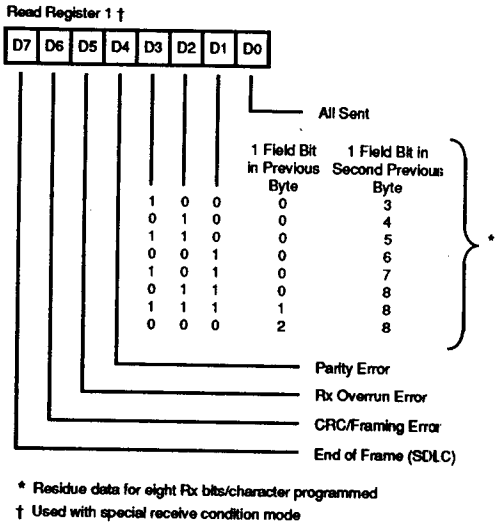


Figure 20b. SIO Read Register 1

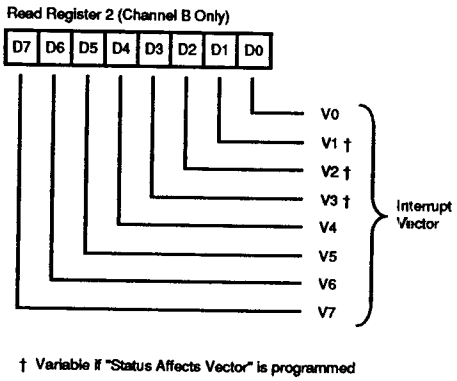


Figure 20c. SIO Read Register 2

Write Registers. The SIO Channel B contains eight write registers while Channel A contains only seven that are programmed to configure the operating mode characteristics of each channel. With the exception of WR0, programming the write registers is a two step operation. The first operation is a pointer written to WR0 which points to the selected register. The second operation is the actual control word that is written into the register to configure the SIO channel (Figure 21).

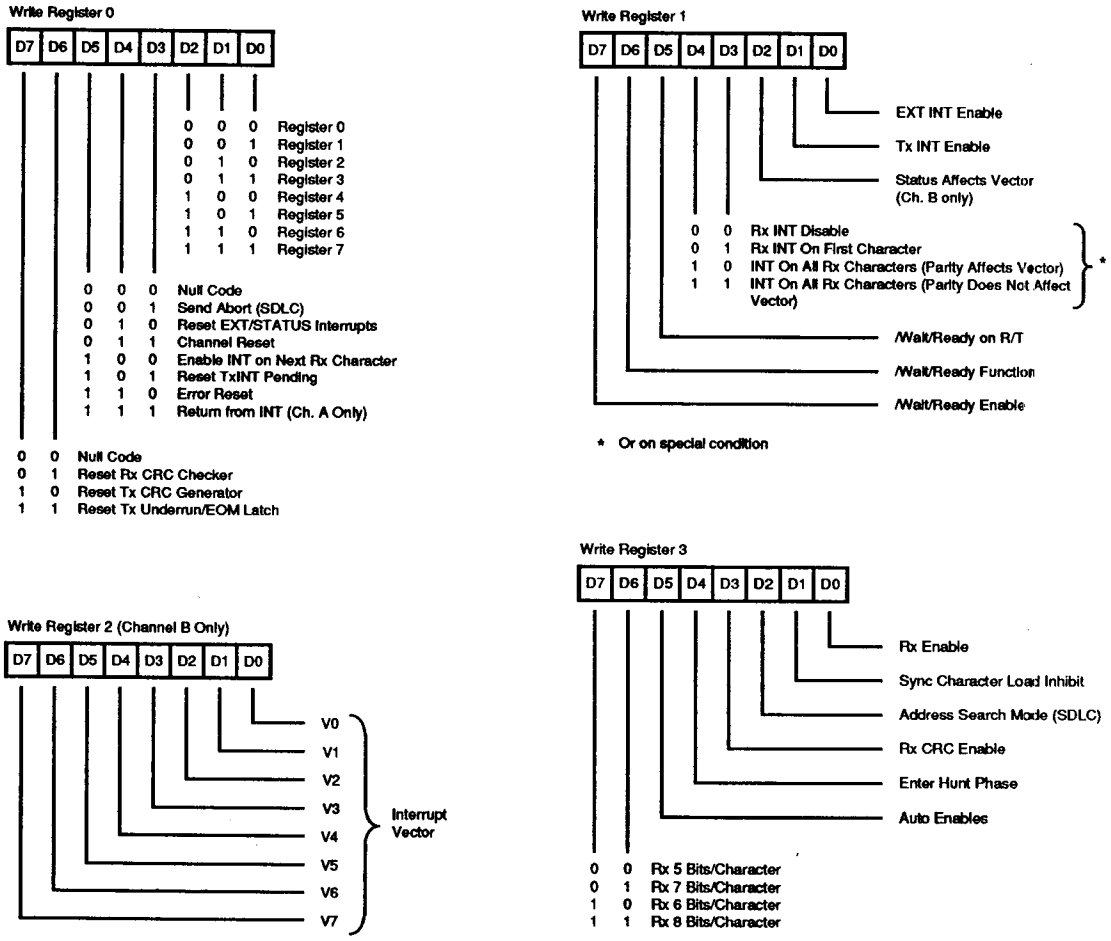


Figure 21. SIO Write Registers

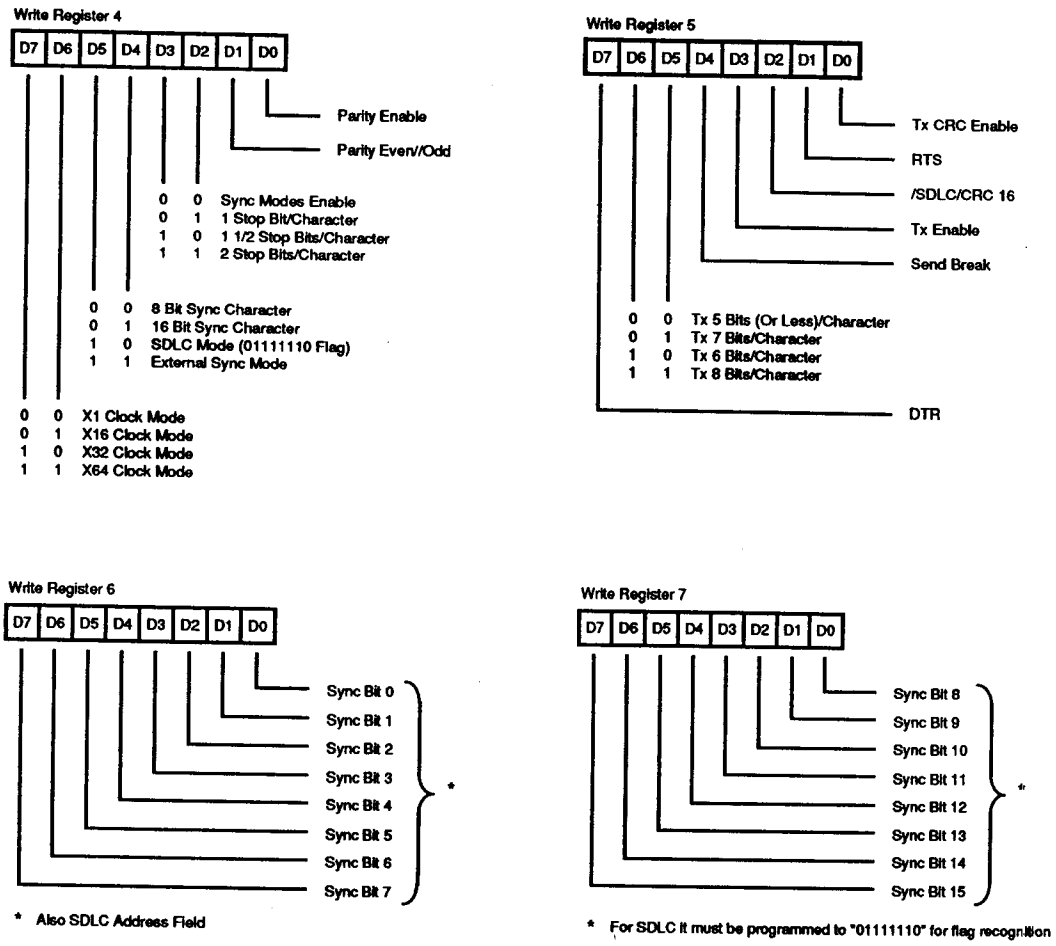


Figure 21. SIO Write Registers (Continued)

WATCH DOG CONTROL REGISTERS

There are two registers to control Watch Dog Timer operations. These are Watch Dog Timer Master Register (WDTMR; I/O Address F0h) and the WDT Command Register (WDTCR; I/O Address F1h). Watch Dog Timer Logic has a "double key" structure to prevent the WDT disabling error, which may lead to the WDT operation to stop due to program runaway. Programming the WDT follows this procedure. Also, these registers program the power-down mode of operation. The "Second key" is needed when turning off the Watch Dog Timer.

Enabling the WDT. The WDT is enabled by setting the WDT Enable Bit (D7:WDTE) to "1" and the WDT Periodic field (D5,D6:WDTP) to the desired time period. These command bits are in the Watch Dog Timer Master Register (WDTMR; I/O Address F0h).

Disabling the WDT. The WDT is disabled by clearing WDT Enable bit (WDTE) in the WDTMR to "0" followed by writing "B1h" to the WDT Command Register (WDTCR; I/O Address F1h).

Clearing the WDT. The WDT can be cleared by writing "4Eh" into the WDTCR.

Watch Dog Timer Master Register (WDTMR;I/O address F0h). This register controls the activities of the Watch Dog Timer and selects power-down mode of operation (Figure 22).

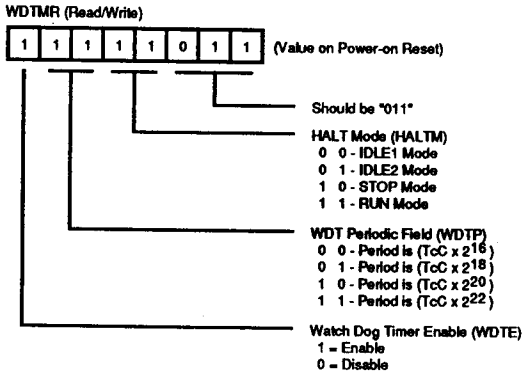


Figure 22. Watch Dog Timer Master Register

Bit D7. *Watch Dog Timer Enable* (WDTE). This bit controls the activities of Watch Dog Timer. The WDT can be enabled by setting this bit to "1". To disable WDT, write "0" to this bit followed by writing "B1h" in the WDT Command Register. Watch Dog Timer Logic has a "double key" structure to prevent the WDT disabling error, which may lead to the WDT operation to stop, due to program run-away. Upon Power-on reset, this bit is set to "1" and the WDT is enabled.

Bit D6-D5. *WDT Periodic field* (WDTP). This two bit field determines the desired time period. Upon Power-on reset, this field sets to "11".

00 - Period is (TcC * 2^{16})
01 - Period is (TcC * 2^{18})
10 - Period is (TcC * 2^{20})
11 - Period is (TcC * 2^{22})

Bit D4-D3. *HALT mode* (HALTM). This two bit field specifies one of four power-down modes. To change this field, write "DBh" to the WDT command register, followed by a write to this register. For detailed descriptions of this field, please refer to the section "Mode of operations." Upon Power-on Reset, this field is set to 11, which specifies "RUN mode."

00 - IDLE 1 Mode
01 - IDLE 2 Mode
10 - STOP Mode
11 - RUN Mode

Bit D2-D0. *Reserved.* These three bits are reserved and should always be programmed as "011". A read to these bit returns "011".

Watch Dog Timer Command Register (WDTCR; I/O address F1h). In conjunction with the WDTMR, this register works as a "Second key" for the Watch Dog Timer. This register is write only (Figure 23).

Write B1h after clearing WDTE to "0" - Disable WDT.
Write 4Eh - Clear WDT.
Write DBh followed by a write to HALTM - Change Power-down mode.

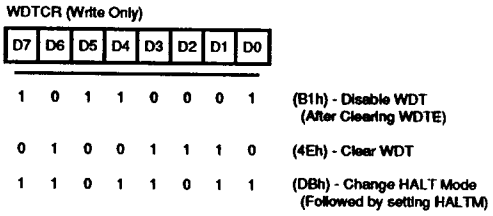


Figure 23. Watch Dog Timer Command Register

INTERRUPT PRIORITY REGISTER
(INTPR; I/O address F4h)

This register (write only) is provided to determine the interrupt priority for the CTC, SIO and the PIO (Figure 24).

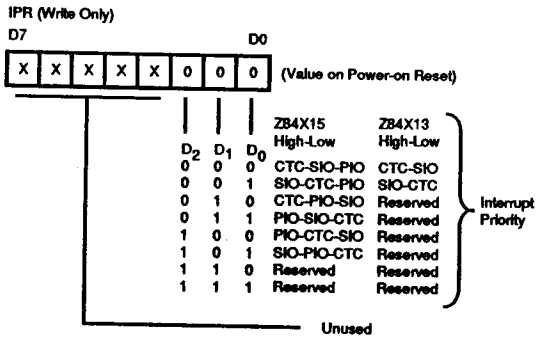


Figure 24. Interrupt Priority Register

Bit D7-D3. Unused

Bit D2-D0. This field specifies the order of the interrupt daisy chain. Upon Power-on Reset, this field is set to "000".

	Z84C15 High - Low	Z84C13 High - Low
000	CTC-SIO-PIO	CTC-SIO
001	SIO-CTC-PIO	SIO-CTC
010	CTC-PIO-SIO	Reserved
011	PIO-SIO-CTC	Reserved
100	PIO-CTC-SIO	Reserved
101	SIO-PIO-CTC	Reserved
110	Reserved	Reserved
111	Reserved	Reserved

REGISTERS FOR SYSTEM CONFIGURATION

(The following registers are not available on Z84013/015.) There are four indirectly accessible registers to determine System configuration with the Z84C13/C15. These indirectly accessible registers are: Wait State Control Register (WCR, Control Register 00h), Memory Wait Boundary Register (MWBR, Control Register 01h), Chip Select Boundary Register (CSBR, Control Register 02h) and Misc. Control Register (MCR, Control Register 03h). To access these registers, Z84C13/C15 writes "register number to be accessed" to the System Control Register Pointer (SCRP, I/O address EEh), and then accesses the target register through the System Control Data Port (SCDP, I/O address EFh). The pointer which writes into SCRP is kept until modified.

System Control Register Pointer (SCRP, I/O address EEh)
This register stores the pointer to access System Control Registers (WCR, MWBR, CSBR and MCR). This register is Read/Write and it holds the pointer value until modified. Upon Power-on Reset, all bits are cleared to zero. The pointer value, other than 00h to 03h is reserved and is not written. Upon Power-on Reset, this register is set to "00h" (Figure 25).

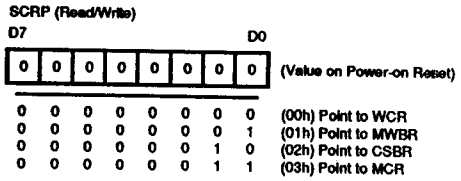


Figure 25. System Control Register Pointer

System Control Data Port (SCDP, I/O address EFh)
This register is to access WCR, MWBR, CSBR and MCR (Figure 26).

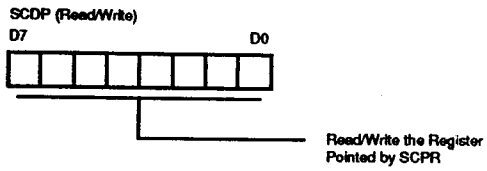


Figure 26. System Control Data Port

Wait State Control Register (WCR, Control Register 00h)
This register can be accessed through SCDP with the pointer value 00h in SCRP (Figure 27). To maintain compatibility with the Z84013/015, the Z84C13/C15 inserts the maximum number of wait states (set all bits of this register to one) for fifteen /M1 cycles after Power-on Reset. It automatically clears the contents of this register (move to no-wait state insertion) on the trailing edge of the 16th /M1 signal unless software has programmed a value. If automatic wait state insertion is needed, the wait state is programmed within this time period. A read to WCR during this period will return FFh, unless programmed.

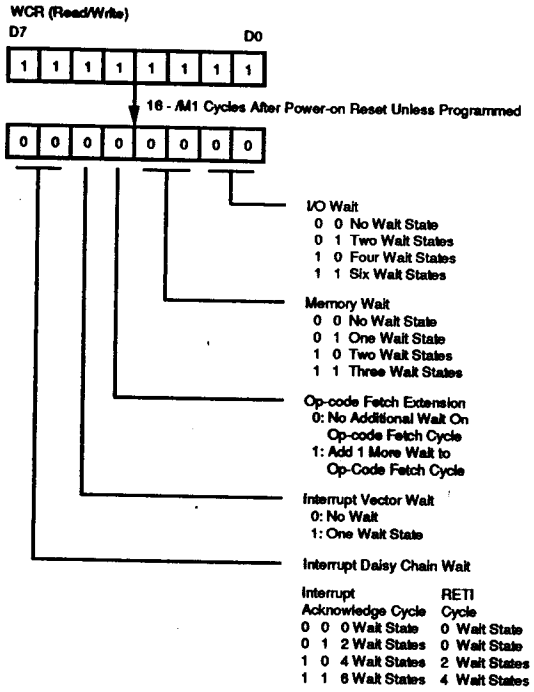


Figure 27. Wait State Control Register

This register has the following fields:

Bit 7-6. *Interrupt Daisy Chain Wait.* This 2-bit field specifies the number of wait states to be inserted during an Interrupt Daisy Chain settle period of the Interrupt Acknowledge cycle, which is/IORQ falls after the settling period from /M1 going active "0". Also, this field controls the number of wait states inserted during the RETI (Return From Interrupt) cycle. If specified to insert 4 or 6 wait states during Interrupt Acknowledge cycle, the Wait state generator also inserts wait states during RETI fetch sequence. This sequence is formed with two op-code fetch cycles (Op-code is EDh followed by 4Dh). It inserts 1 wait state if op-code followed by EDh is NOT 4Dh, and inserts 2 or 4 wait states, respectively, if the following op-code is 4Dh.

Interrupt Acknowledge	RETI cycle
00 - No Wait states	No Wait states
01 - 2 Wait states	No Wait states
10 - 4 Wait states	2 Wait states
11 - 6 Wait states	4 Wait states

For fifteen /M1 cycles from Power-on Reset, bits 7-6 are set to "11" . They clear to "00" on the trailing edge of the 16th /M1 signal unless programmed.

Bit 5. *Interrupt Vector Wait.* While this bit is set to one, the wait state generator inserts one wait state after the /IORQ signal goes active during the Interrupt acknowledge cycle. This gives more time for the vector read cycle. While this bit is cleared to zero, no wait state is inserted (standard timing). For fifteen /M1 cycles from Power-on Reset, this bit is set to "1", then cleared to "0" on the trailing edge of the 16th /M1 signal, unless programmed.

Bit 4. *Opcode Fetch Extension.* If this bit is set to "1", one additional wait state is inserted during the Op-code fetch cycle in addition to the number of wait states programmed in the Memory Wait field. For fifteen /M1 cycles from Power-on Reset, this bit is set to "1", then cleared to "0" on the trailing edge of the 16th /M1 signal, unless programmed.

Bit 3-2. *Memory Wait States.* This 2-bit field specifies the number of wait states to be inserted during memory Read/ Write transactions.

00 - No Wait states
01 - 1 Wait states
10 - 2 Wait states
11 - 3 Wait states

For fifteen /M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the16th /M1 signal, unless programmed.

Bit 1-0. *I/O Wait states.* This 2-bit field specifies the number of wait states to be inserted during I/O transactions.

00 - No Wait states
01 - 2 Wait states
10 - 4 Wait states
11 - 6 Wait states

For fifteen /M1 cycles from Power-on Reset, these bits are set to "11", then cleared to "00" on the trailing edge of the16th /M1 signal, unless programmed. For the accesses to the on-chip I/O registers, no Wait states are inserted regardless of the programming of this field.

Memory Wait Boundary Register (MWBR, Control Register 01h)

This register specifies the address range to insert memory wait states. When accessed memory addresses are within this range, the Memory Wait State generator inserts Memory Wait States specified in the Memory Wait field of WCR (Figure 28).

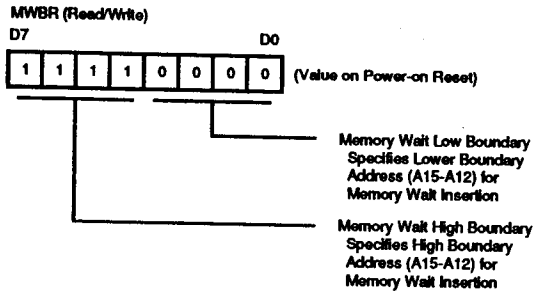


Figure 28. Memory Wait Boundary Register

Bit D7-D4. *Memory Wait High Boundary.* This field specifies A15-A12 of the upper address boundary for Memory Wait.

Bit D3-D0. *Memory Wait Low Boundary.* This field specifies A15-12 of the lower address boundary for Memory Wait.

Memory Wait states are inserted for the address range:

(D7-D4 of MWBR) ≥ A15-A12 ≥ (D3-D0 of MWBR)

This register is set to "F0h" on Power-on Reset, which specifies the address range for Memory Wait as "0000h to FFFFh".

Chip Select Boundary Register (CSBR, Control Register 02h)

This register specifies the address range for each chip select signal. When accessed memory addresses are within this range, chip select signals are active (Figure 29).

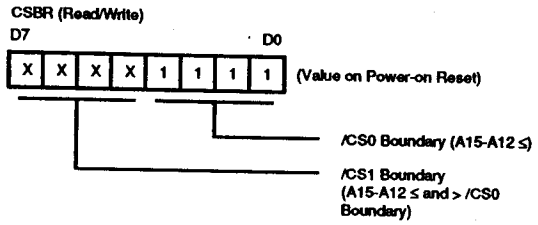


Figure 29. Chip Select Boundary Register

D7-D4. */CS1 Boundary Address.* These bits specify the boundary address range for /CS1. The bit values are ignored on power-up as the /CS1 enable bit is off. The /CS1 is asserted if the address lines A15-12 have an address value greater than the programmed value for /CS0, and less than or equal to the programmed value in these bits.

D3-D0. */CS0 Boundary Address.* These bits specify the boundary address range for /CS0. /CS0 is asserted if the address lines A15-12 have an address value less than or equal to the programmed boundary value. The /CS0 enable bit in the MCR must be set to 1. Upon Power-up reset, these bits come up as all 1's so that /CS0 is asserted for all addresses.

Chip Select signals are active for the address range:

/CS0: (D3-D0 of CSBR) ≥ A15-A12 ≥ 0
/CS1: (D7-D4 of CSBR) ≥ A15-A12 > (D3-D0 of CSBR)

This register is set to "xxxx1111b" on Power-on Reset, which specifies the address range of /CS0 for "0000h to FFFFh" (all Memory location) and /CS1 "undefined."

Misc Control Register (MCR, Control Register 03h)

This register specifies miscellaneous options on this device (Figure 30).

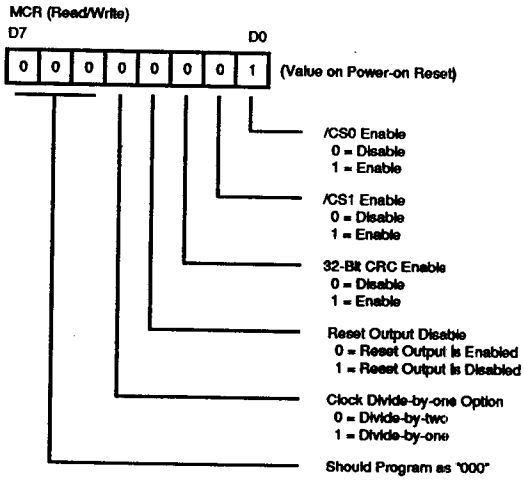


Figure 30. Misc Control Register

Bit D7-D5. *Reserved.* These three bits are reserved and are always programmed as "000".

Bit D4. *Clock Divide-by-one option.* "0"-Disable, "1"-enable. On-chip CGC unit has divide-by-two circuit. By setting this bit to one, this circuit is bypassed and CLKOUT is equal to X'tal oscillator frequency (or external clock input on the XTAL1 pin). This bit has no effect when the on-chip CGC unit is not in use and the external system clock is fed from CLKIN pin. Upon Power-on Reset, this bit is cleared to 0 and the clock is divided by two.

Bit D3. *Reset Output Disable.* "0"-Reset output is enabled, "1"-Reset output is disabled. This bit controls the /RESET signal and is driven out when reset input is used to take the Z84C13/C15 out of the "Halt" state. The reset pulse is driven out for 16-clock cycles from the falling edge of /RESET input, unless this bit is set. Upon Power-on reset, this bit is cleared to 0.

Bit D2. *32-Bit CRC enable.* "0"-Normal mode (16-bit CRC) "1"-32-bit CRC generation/Checking is enabled on SIO Channel A. This bit determines if the 32-bit CRC feature is enabled on Channel A of the SIO. If this bit is 0, the SIO is in a normal mode of operation. If this bit is set to 1, a normal CRC generator/checker is replaced with a 32-bit CRC generator/checker. Upon Power-on Reset, this bit is clear to "0".

Bit D1. */CS1 Enable. "0"-Disable, "1"-Enable.* This bit enables /CS1 output. While this bit is "0", /CS1 is forced to "1". While this bit is "1", /CS1 carries the address range specified in the CSBR. Upon Power-on Reset, this bit is cleared to "0".

Bit D0. */CS0 Enable. "0"-Disable, "1"-Enable.* This bit enables /CS0 output. While this bit is "0", /CS1 pin is forced to "1". While this bit is "1", the /CS0 carries address range specified in the CSBR. Upon Power-on Reset, this bit is set to "1".

Operation modes

There are four kinds of operation modes available for the IPC in connection with clock generation; RUN Mode, IDLE1/2 Modes and STOP Mode.

The Operation mode is effective when the HALT instruction is executed. Restart of the MPU from the stopped state under IDLE1/2 Mode or STOP mode is affected by inputting either /RESET or interrupt (/NMI or /INT). The mode selection of these power-down modes is made by programming the HALTM field (Bit D4-3) of WDTMR.

Setting Halt Mode

Duplicate control is provided to prevent the stopping of the WDT operation caused by the halt mode setting an error due to program runaway. As described in the programming section, changing the Halt Mode field of WDTMR is in two steps. First, write "DBh" to WDTCR followed by a write to the WDTMR with the value in HALTM. Table 2 has descriptions of each mode, and Table 3 has device status in the Halt state.

Table 2. Power-down Modes

(When using on-chip CGC unit; CLKOUT and CLKIN are tied together)

Operation Mode	WDTMR Bit D4	Bit D3	Description at HALT State
RUN Mode	1	1	The IPC continues the operation and continuously supplies a clock to the outside.
IDLE1 Mode	0	0	The internal oscillator's operation is continued. Clock output (CLKOUT) as well as internal clock to the CPU, PIO, SIO, CTC and the Watch Dog Timer is stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
IDLE2 Mode	0	1	The internal oscillator and the CTC's operation continues and supplies clock to the outside on the CLKOUT pin continuously. But the internal clock to the CPU, PIO, SIO and the Watch Dog Timer is stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
STOP Mode	1	0	All operations of the internal oscillator, clock (CLK) output, internal clock to the CPU, PIO, CTC, SIO and the Watch Dog Timer are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.

Table 3. Device status in Halt state
(When using on-chip CGC unit; CLKOUT and CLKIN are tied together)

Mode	CGC	CPU	CTC	PIO	SIO	WDT	CLKOUT
IDLE1	O	X	X	X	X	X	X
IDLE2	O	X	O	X	X	X	O
STOP	X	X	X	X	X	X	X
RUN	O	O	O	O	O	O	O

O: Operating
X: Stop

All of the operating modes listed here are valid with crystal input (Crystal connected between XTAL1/2 or external clock input on XTAL1). For the external clock on the CLKIN pin, only the IDLE2 and RUN modes are applicable.

TIMING

Basic Timing

The basic timing is explained here with emphasis placed on the halt function relative to the clock generator. The following items are identical to those for the Z84C00. Refer to the data sheet for the Z84C00.

- Operation code fetch cycle
- Memory Read/Write operation
- Input/Output operation
- Bus request/acknowledge operation
- Maskable interrupt request operation
- Non-Maskable interrupt request operation
- Reset Operation

Operation When HALT Instruction is Executed. When the CPU fetches a halt instruction in the operation code fetch cycle, /HALT goes active (Low) in synch with the falling edge of T4 state before the peripheral LSI and CPU stops the operation. After this, the system clock generation differs depending upon the operation mode (RUN Mode, IDLE1/2 Mode or STOP Mode). If the internal system clock is running, the CPU continues to execute NOP instruction even in the halt state.

RUN Mode (HALTM = 11). Shown in Figure 31 is the basic timing when the halt instruction is executed in RUN Mode.

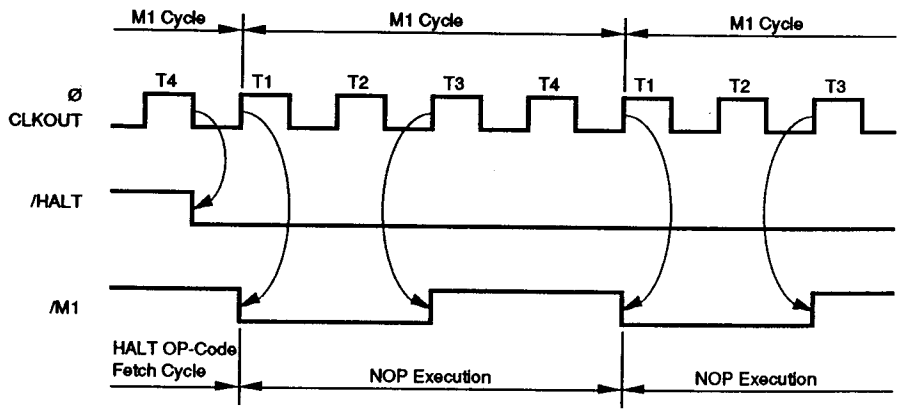


Figure 31. Timing of RUN Mode
(at Halt Instruction Command Execution)

In RUN Mode, output from the CGC unit (CLKOUT) is not stopped and the internal system clock (Ø) continues even after the halt instruction is executed. Therefore, until the halt state is released by the interrupt signal (/NMI or /INT) or /RESET signal, MPU continues to execute HALT instructions (internally executing NOP instructions).

IDLE1 Mode (HALTM=00). Shown in Figure 32 is the basic timing when the halt instruction is executed in IDLE1 Mode.

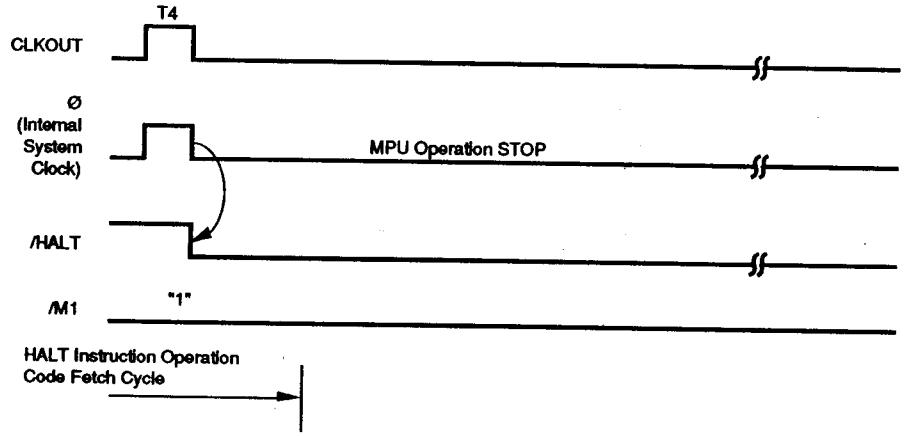


Figure 32. IDLE1 Mode Timing
(At Halt Instruction Execution)

In IDLE1 Mode, the internal oscillator continues to operate, but clock output (CLKOUT) is stopped at T4 Low state of HALT instruction execution. Then all components in the MPU stop their operation. This mode is not supported when the CGC unit is inactive and the external clock is fed from CLKIN pin; CLKOUT should be connected to CLKIN.

IDLE2 Mode (HALTM=01). Shown in Figure 33 is the basic timing when the halt instruction is executed in IDLE2 Mode.

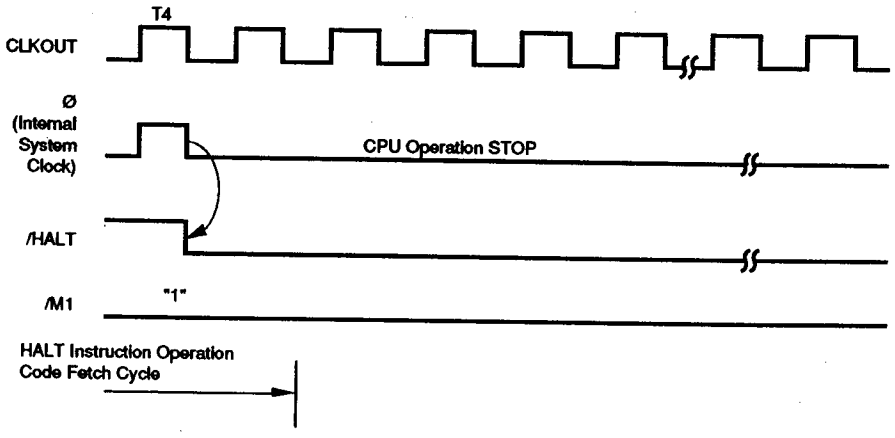


Figure 33. IDLE2 Mode Timing
(At Halt Instruction Execution)

In IDLE2 Mode, the internal oscillator and clock output (CLKOUT) continue to operate. The internal system clock, fed from CLKIN to the components other than CTC is stopped at the T4 Low state of HALT instruction execution.

STOP Mode (HALTM=10). Shown in Figure 34 is the basic timing when the halt instruction is executed in STOP Mode.

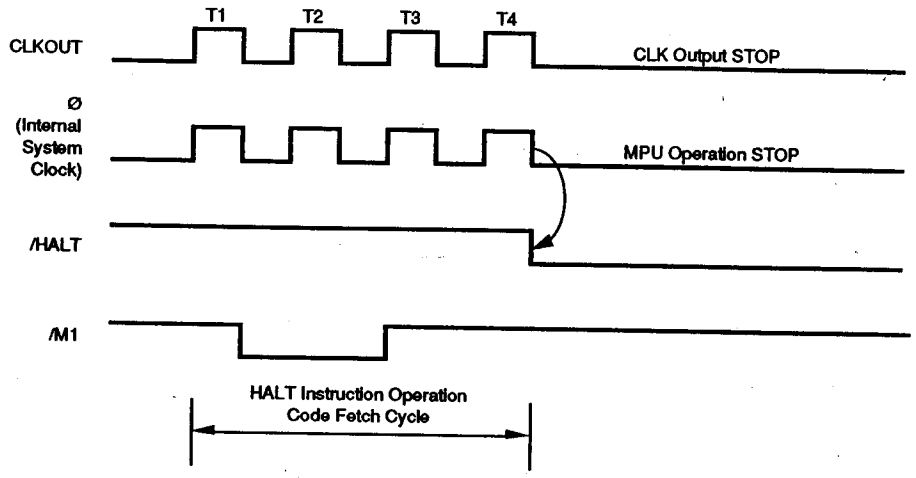


Figure 34. STOP Mode Timing
(At Halt Instruction Execution)

In STOP Mode, the on-chip CGC unit is stopped at T4 Low state of HALT instruction execution. Therefore, clock output (CLKOUT), operation of Watch Dog Timer, CPU, PIO, CTC, SIO are stopped.

Release from Halt State. The halt state of the CPU is released when "0" is input to the /RESET signal and the MPU is reset or an interrupt request is accepted. An interrupt request signal is sampled at the leading edge of the last clock cycle (T4 state) of NOP instruction. In case of the maskable interrupt, interrupt will be accepted by an active /INT signal ("0" level). Also, the interrupt enable flip-flop is set to "1". The accepted interrupt process is started from the next cycle.

Further, when the internal system clock is stopped (IDLE1/2 Mode, STOP Mode), it is necessary first to restart the internal system clock. The internal system clock is restarted when /RESET or interrupt signal (/NMI or /INT) is asserted.

RUN Mode (HALTM=11). The halt release operation is enabled by interrupt request in RUN Mode (Figure 35).

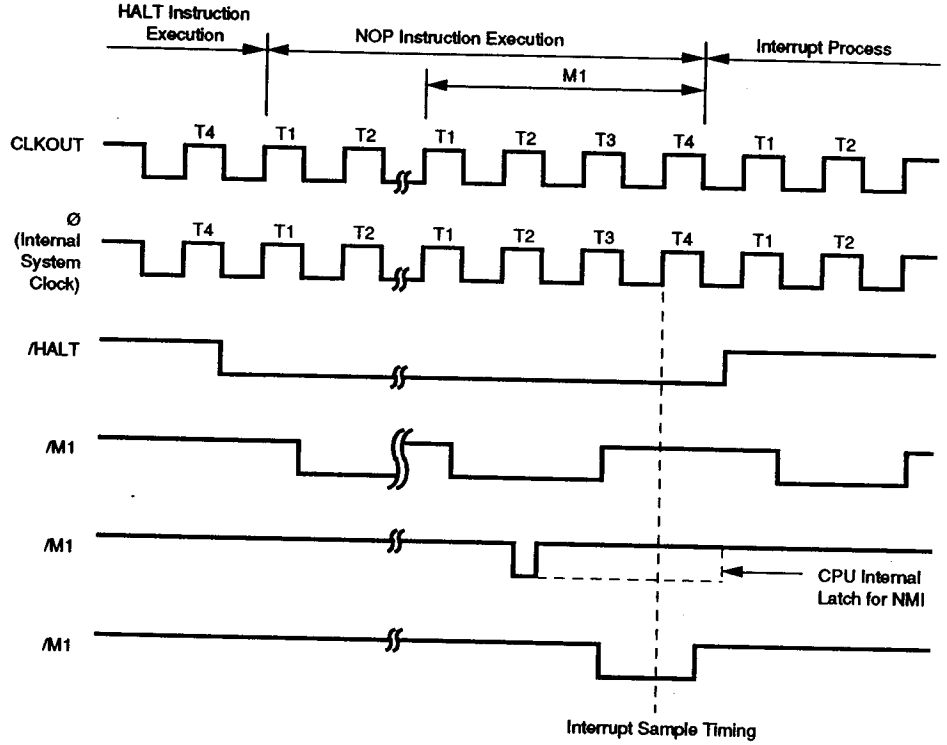


Figure 35. Halt Release Operation Timing By Interrupt Request Signal in RUN Mode

In RUN Mode the internal system clock is not stopped. If the interrupt signal is recognized on the rising clock edge of T4 of the continued NOP instruction, CPU will execute the interrupt process from the next cycle.

The halt release resets CPU in RUN Mode (Figure 36). After reset, CPU will execute an instruction starting from address 0000H. However, in order to reset the CPU it is necessary to keep /RESET signal at "0" for at least 3 system clock cycles. (For Z84C13/C15: 3 clock cycles if Reset output is disabled.) In addition, if /RESET signal becomes "1", after the dummy cycle for at least two T states, CPU executes an instruction from address 0000H.

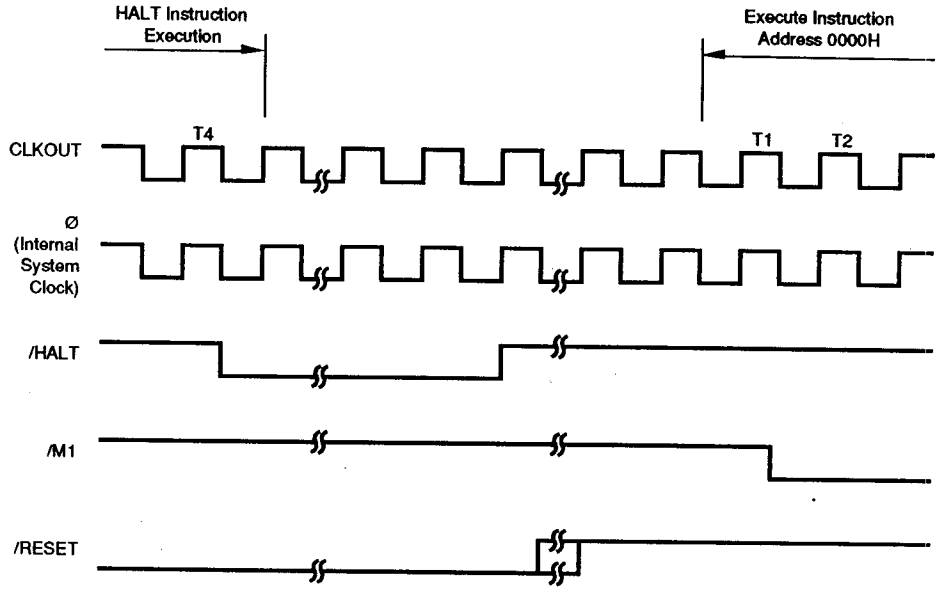


Figure 36. Halt Release Operation Timing By Reset in RUN Mode

IDLE1 Mode (HALTM=00), IDLE2 Mode (HALTM=01). The halt release operation by interrupt signal in IDLE1 Mode is shown in Figure 37 (a) and in IDLE2 Mode in Figure 37 (b).

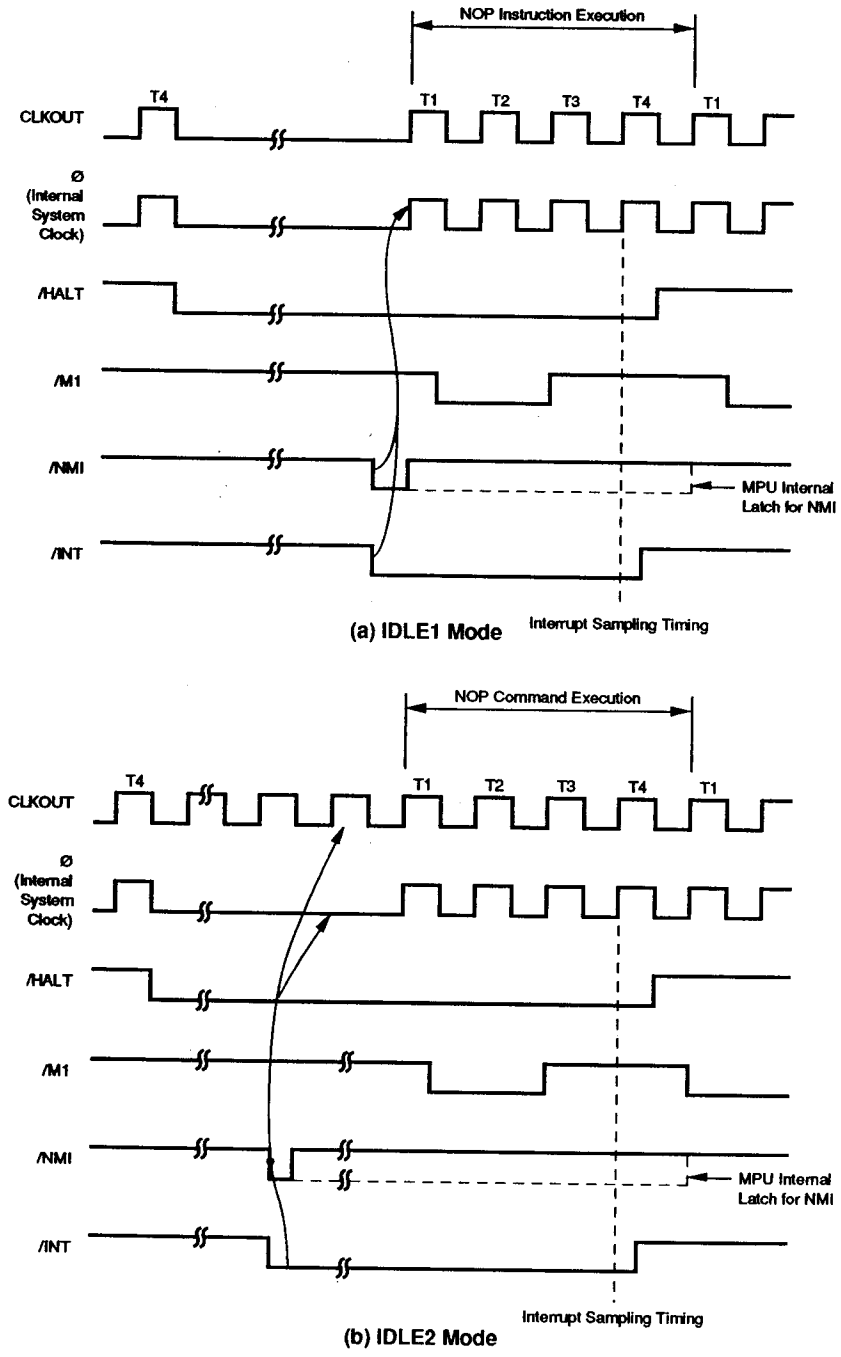


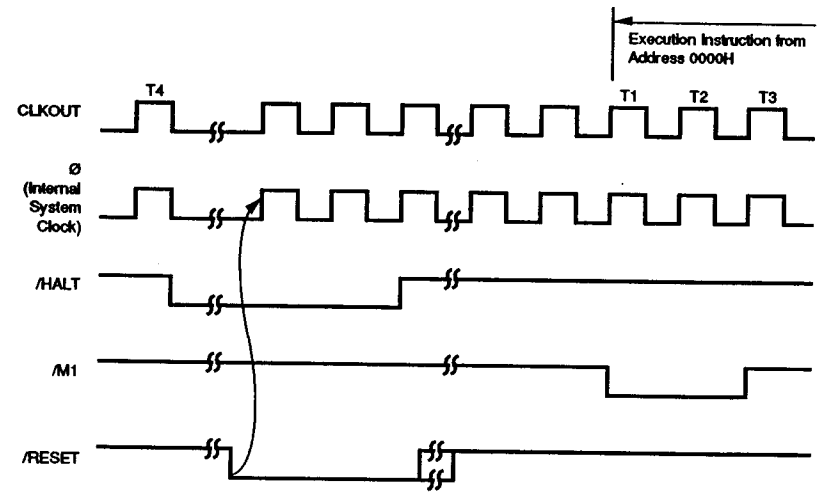
Figure 37. Halt Release Operation Timing By Interrupt Request Signal in IDLE1/2 Mode

When receiving /NMI or /INT signals, the stopped internal system clock starts to feed. In IDLE1 Mode, the IPC starts clock output on CLKOUT at the same time.

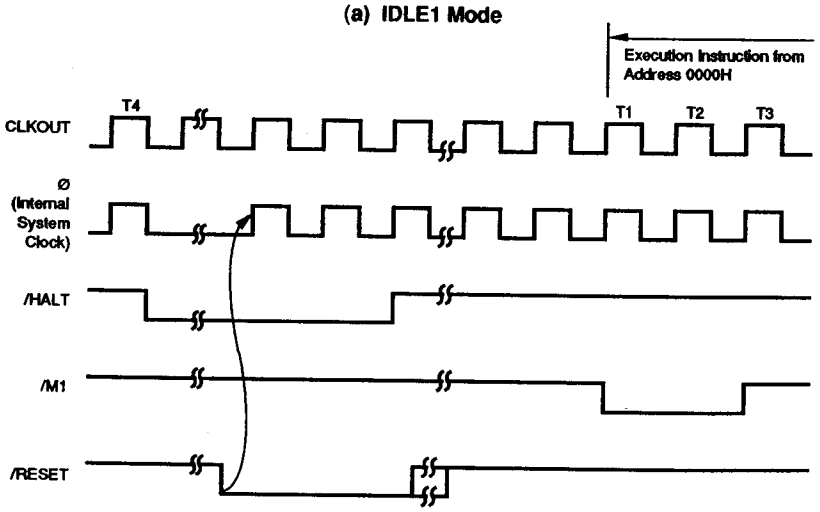
The operation stop of CPU in IDLE2 mode is taking place at "0" level during T4 state in the halt instruction op-code fetch cycle. Therefore, after being restarted by the interrupt signal, CPU executes one NOP instruction and samples an interrupt signal at the rise of T4 state during the execution of this NOP instruction, and executes the interrupt process from next cycle.

If no interrupt signal is accepted during the execution of the first NOP instruction after the internal system clock is restarted, CPU is not released from the halt state. It is placed in IDLE1/2 Mode again at "0" level during T4 state of the NOP instruction, stopping the internal system clock. If /INT signal is not at "0" level at the rise of T4 state, no interrupt request is accepted.

The halt release operation resets the IPC in IDLE1 Mode (Figure 38a) and in IDLE2 Mode (Figure 38b).



(a) IDLE1 Mode



(b) IDLE2 Mode

Figure 38. Halt Release Operation Timing By Reset in IDLE1/2 Mode

When /RESET signal at "0" level is input into the IPC, the internal system clock is restarted and the IPC will execute an instruction stored in address 0000H.

At time of /RESET signal input, it is necessary to take the same care as that in resetting the IPC in RUN Mode.

Halt release in STOP Mode (HALTM=10) by interrupt. The halt release operation by interrupt signal in STOP Mode is shown in Figure 39.

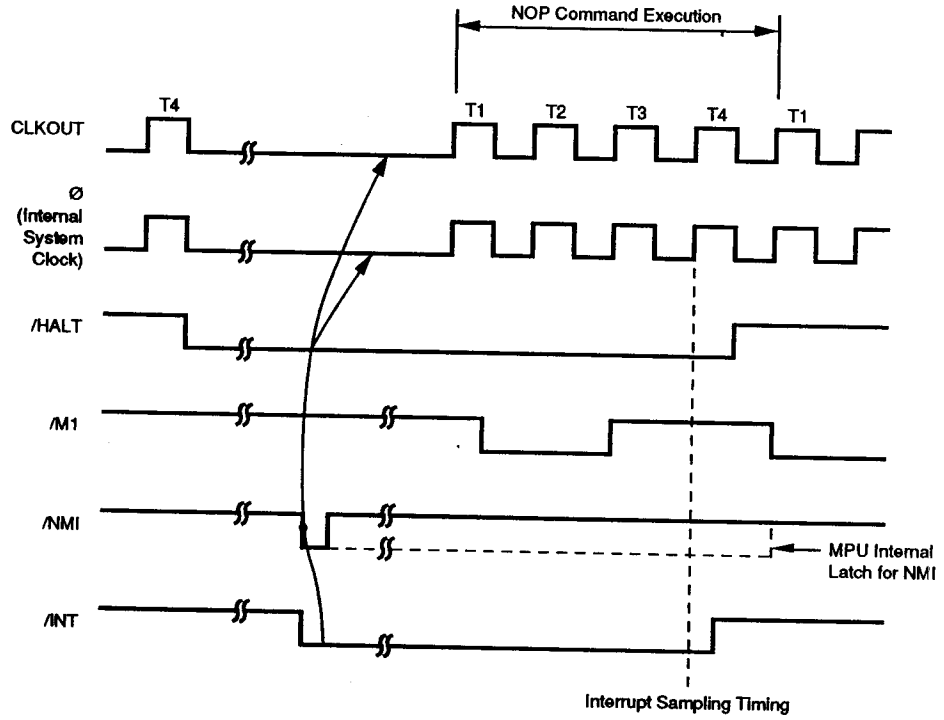


Figure 39. Halt Release Operation Timing By Interrupt Request Signal in STOP Mode

When the IPC receives an interrupt signal, the internal oscillator is restarted. To obtain stabilized oscillation, CLKOUT (and the internal system clock) are started after a start-up time of (2^{14}+2.5) TcC (TcC: Clock Cycle) by the internal counter.

CPU executes one NOP instruction after the internal system clock is restarted. At the same time, it samples an interrupt signal at the rise of T4 state during the execution of this NOP instruction. If the interrupt signal is accepted, CPU executes the interrupt process operation from the next cycle.

During interrupt signal input, it is necessary to take the same care as the interrupt signal input in IDLE1/2 Mode.

Halt release in STOP Mode (HALTM=10) by /RESET. When /RESET at "0" level is input into the IPC, the internal oscillator is restarted. However, the internal clock counter for warm-up does not operate. Therefore, the operation is not carried out properly due to unstable clock oscillation. It is necessary to hold /RESET at "0" level for sufficient time. The halt release operation by the IPC resetting in STOP Mode is shown in Figure 40.

Z84C13/C15 Only. The /RESET pulse is stretched to a minimum of 16 cycles and driven out of the Z84C13/C15 on the /RESET pin if Reset output is enabled (bit D3 of MCR is cleared to "0"). Setting bit D3 disables the driving out of /RESET. The values in the control registers (WDTMR, SCRP, WCR, MWBR, CSBR and MCR) are initialized to the default value on /RESET.

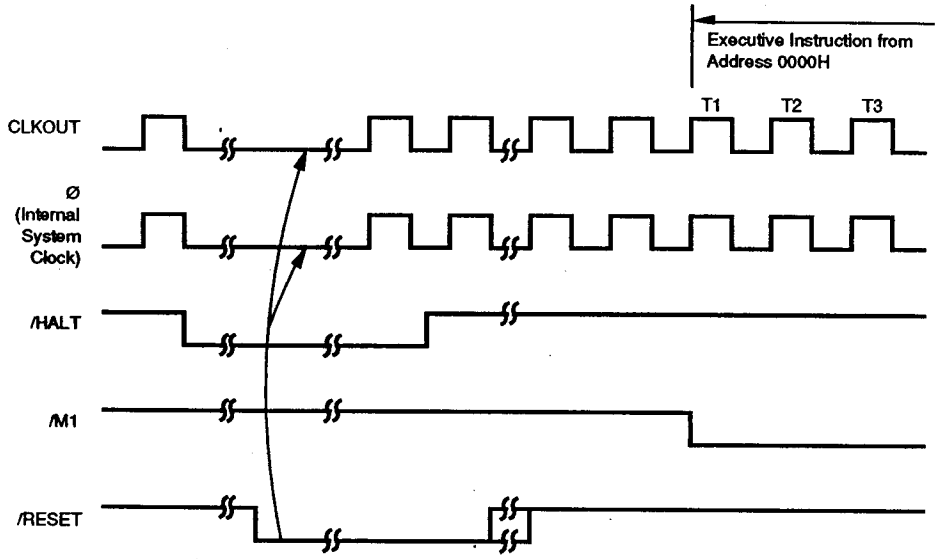


Figure 40. Halt Release Operation Timing By Reset in STOP Mode

Start-up Time at Time of Restart (STOP Mode). When the MPU is released from the halt state by accepting an interrupt request, it executes an interrupt service routine. Therefore, when an interrupt request is accepted, it starts generating clock on the CLKOUT pin, after a start-up time, by the internal counter [(2^{14}+2.5) TcC (TcC:Clock Cycle)]. This obtains a stabilized oscillation for operation.

Further, in case of restart by the /RESET signal, the internal counter does not operate.

Evaluation operation. Each of the CPU signals (A15-0, D7-0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1, /RFSH) can be 3-stated by activating the EV pin. The Z84C13/C15 enhances the counter part by eliminating the requirement of /BUSREQ to go active.

Instruction set. The instruction set of the IPC is the same for the Z84C00. For details, refer to the data sheet of the Z84C00 Technical Manual.

AC TIMING

The following section describes the timing of the IPC. The numbers appearing in the figures refer to the parameters on Table A - F.

CPU Timing
Parameters referenced in Figure 41 through Figure 48 appear in Table A.

The IPC's CPU executes instructions by proceeding through the following specific sequence of operations:

Memory read or write
I/O device read or write
Interrupt acknowledge

The basic clock period is referred to as a Time or Cycle and three or more T cycles make up a machine cycle (e.g., M1, M2 or M3). Machine cycles are extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

Instruction Op-code Fetch. The CPU places the contents of the Program Counter (PC) on the address bus at the start of the cycle (Figure 41). Approximately one-half clock cycle later, /MREQ goes active. When active, /RD indicates that the memory data can be enabled onto the CPU data bus.

The CPU samples the /WAIT input with the falling edge of clock state T2. During clock states T3 and T4 of an M1 cycle, dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction.

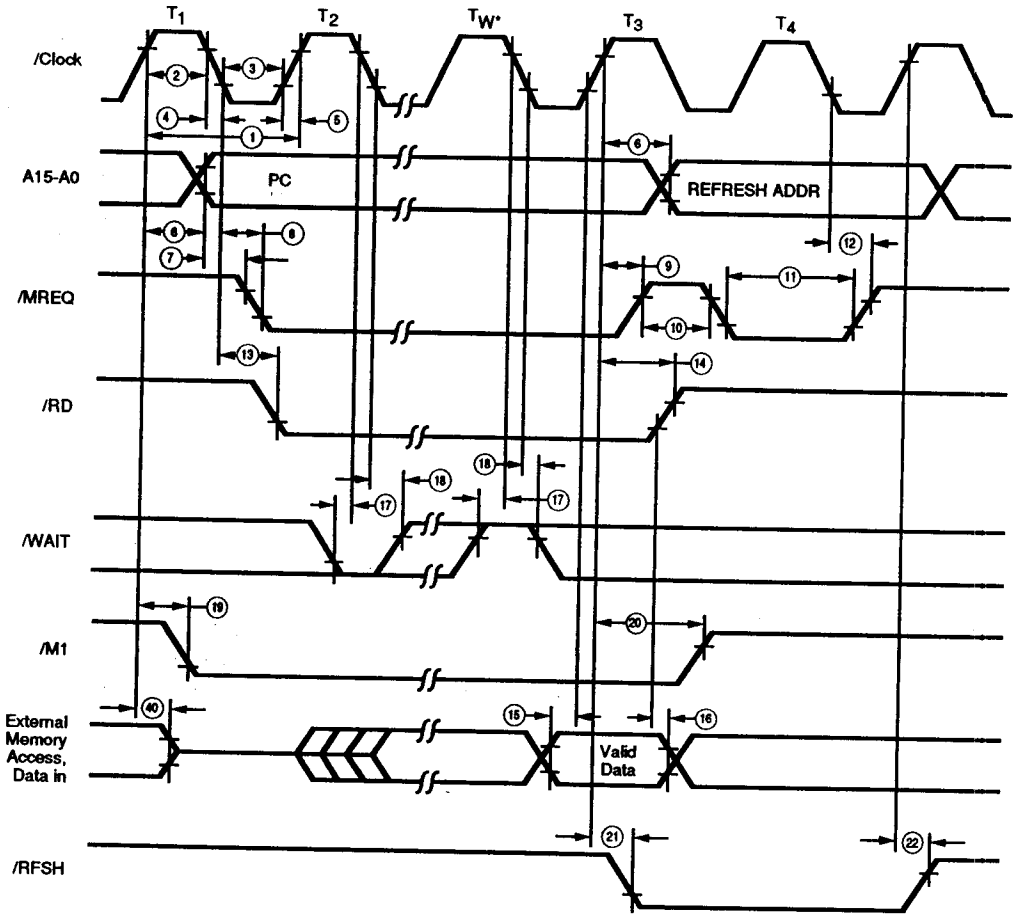


Figure 41. Instruction Op-code Fetch
(See Table A)

Memory Read or Write Cycles. Figure 42 shows the timing of memory read or write cycles other than an Op-code fetch (/M1) cycle. The /MREQ and /RD signals function like the Op-code fetch cycle.

In a memory write cycle, /MREQ also becomes active when the Address Bus is stable. The /WR line is active when the Data Bus is stable, so that it can be used directly as an R/W pulse to most semiconductor memories.

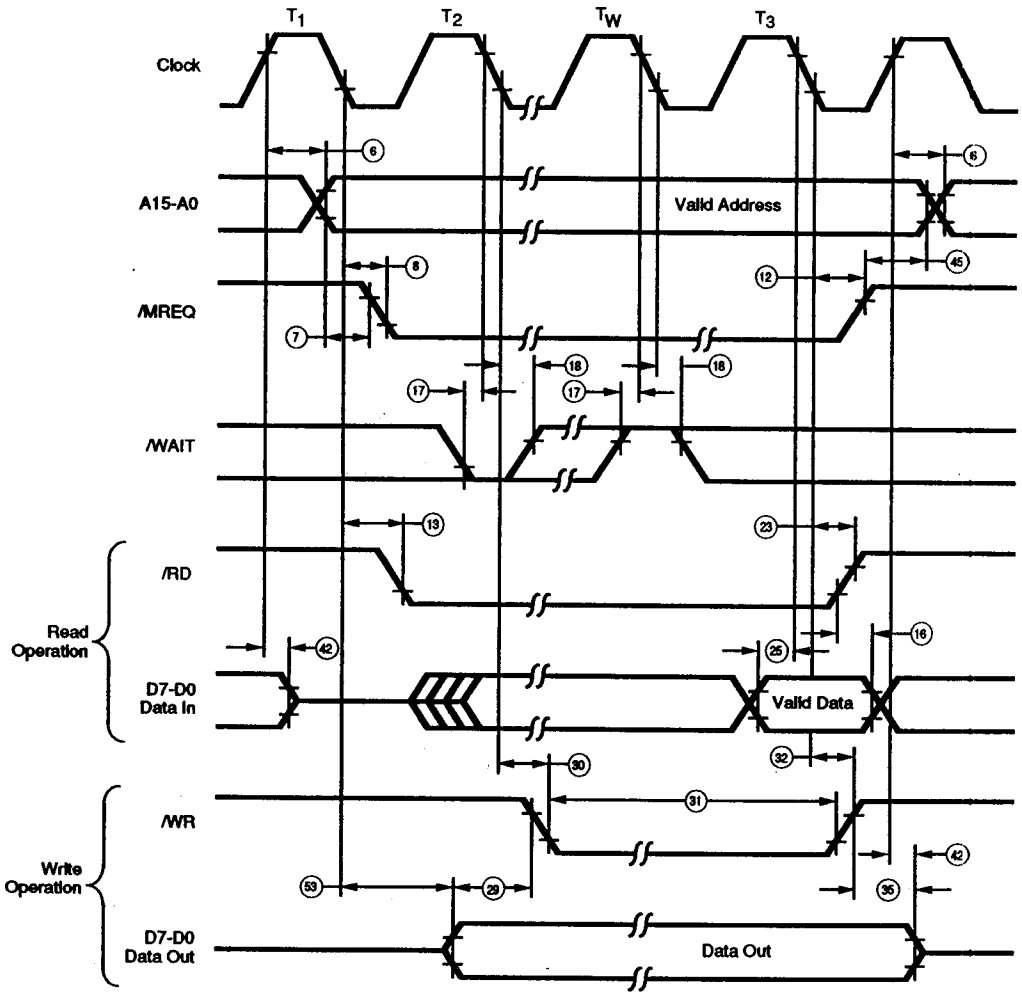
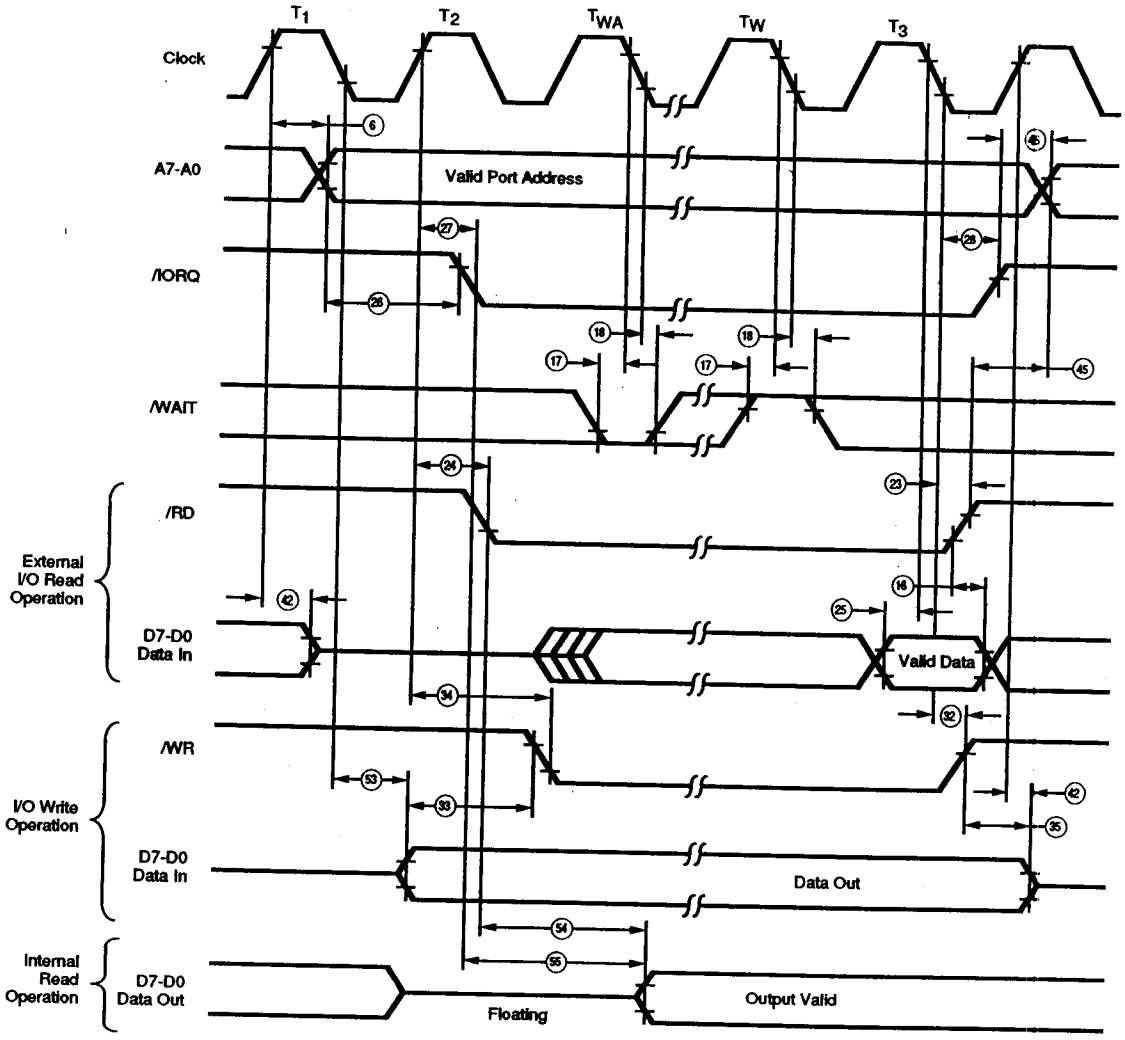


Figure 42. Memory Read or Write Cycle
(See Table A)

Input or Output Cycles. Figure 43 shows the timing for an I/O read or I/O write operation. During I/O operations, the CPU automatically inserts a single Wait state (T_{WA}). This extra Wait state allows sufficient time for an I/O port to decode the address from the port address lines.

When the CPU is accessing the on-chip I/O registers (PIO, CTC, SIO and system control registers), the data from/to these registers also appears on the data bus, or data bus is output during I/O cycle.



Note: T_{WA} = One wait cycle automatically inserted by CPU

Figure 43. Input or Output Cycle
(See Table A)

Interrupt Request/Acknowledge Cycle. The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Figure 44). When an interrupt is accepted, a special /M1 cycle is generated. During this /M1 cycle, /IORQ becomes active (instead of /MREQ) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two Wait states to this cycle.

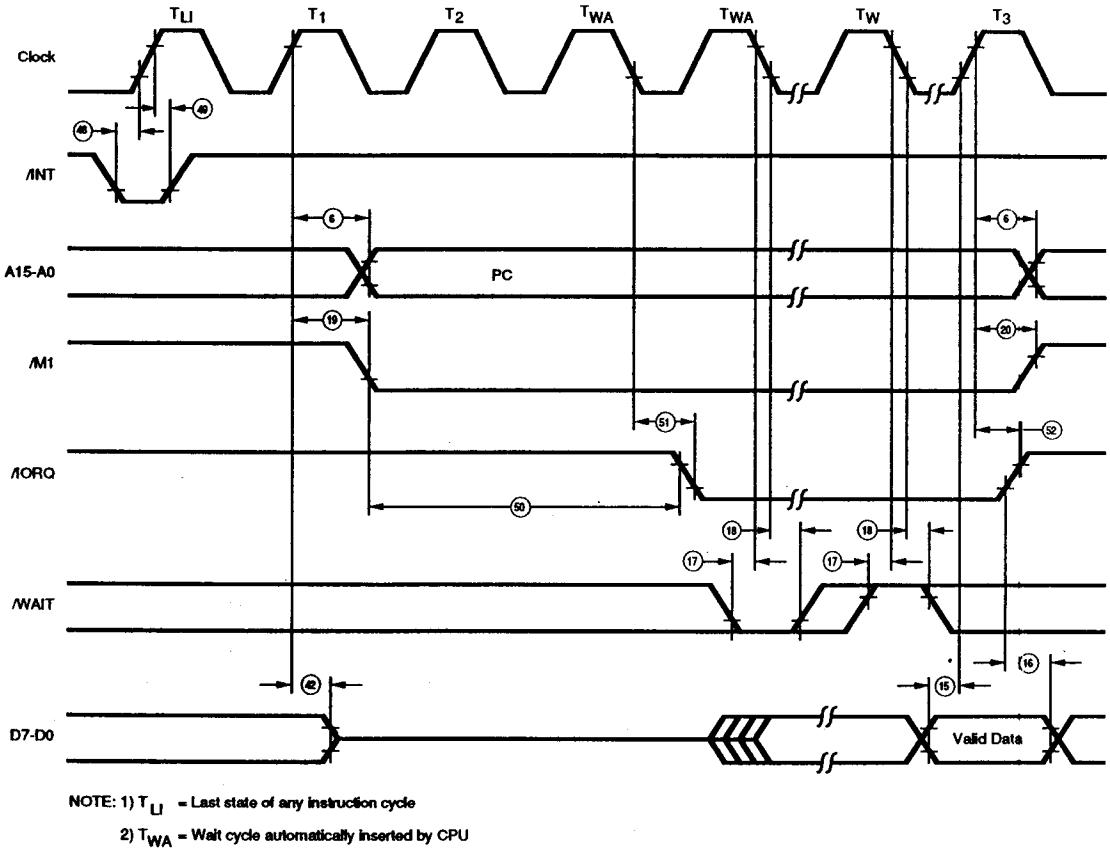
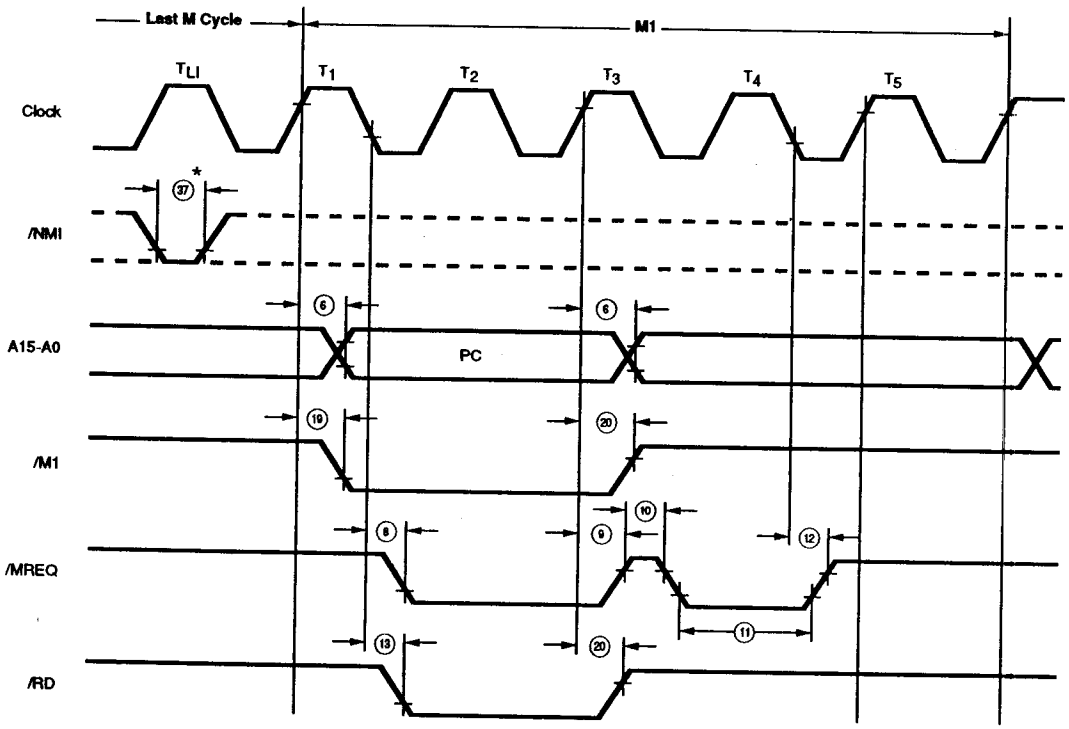


Figure 44. Interrupt Request/Acknowledge Cycle
(See Table A)

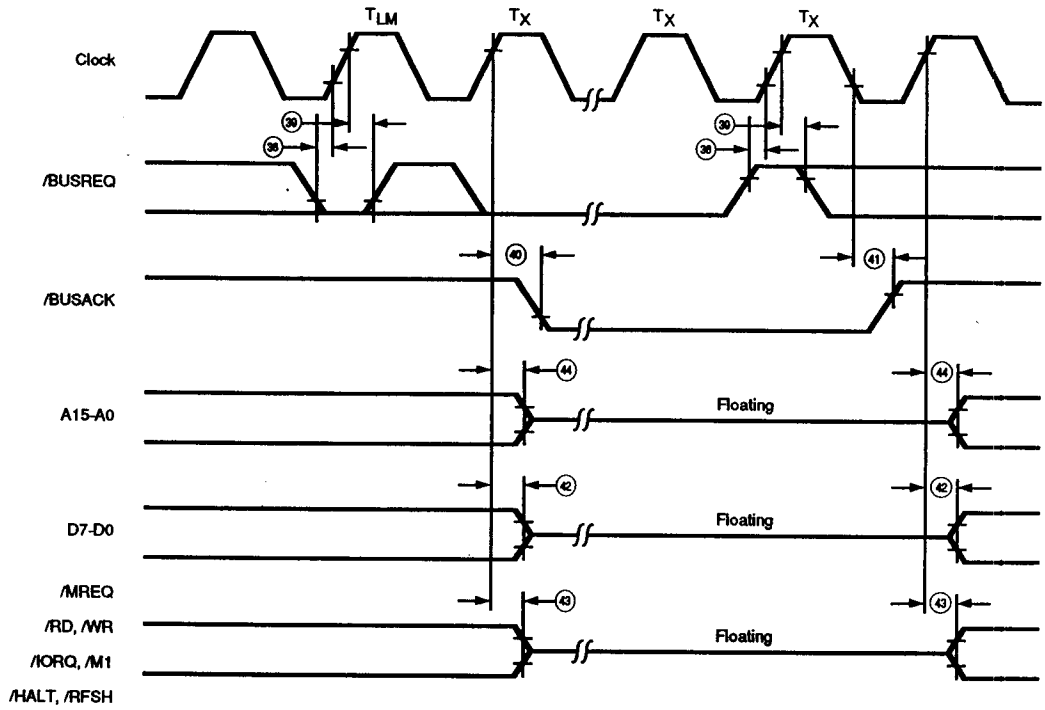
Non-Maskable Interrupt Request Cycle. /NMI is sampled at the same time as the maskable interrupt input /INT, but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal memory read operation except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the /NMI service routine located at the address 0066H (Figure 45).



* Although /NMI is an asynchronous input, to guarantee its being recognized on the following machine cycle, /NMI's falling edge must occur no later than the rising edge of the clock cycle preceding the last state of any instruction cycle (T_{LI}).

Figure 45. Non-Maskable Interrupt Request Operation
(See Table A)

Bus Request/Acknowledge Cycle. The CPU samples /BUSREQ with the rising edge of the last clock period of any machine cycle (Figure 46). If /BUSREQ is active, the CPU sets its address, data, and /MREQ to Inputs, and /IORQ, /RD and /WR lines set to an input for on-chip peripheral access from an external bus master with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices.

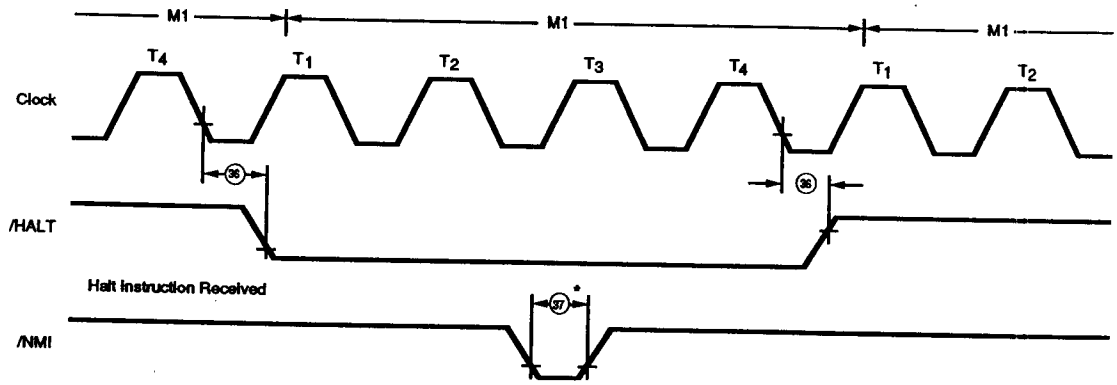


Notes: 1) T_{LM} = Last state of any M cycle

2) T_X = An arbitrary clock cycle used by requesting device

Figure 46. BUS Request/Acknowledge Cycle
(See Table A)

Halt acknowledge cycle. Figure 47 shows the timing for Halt acknowledge cycle.



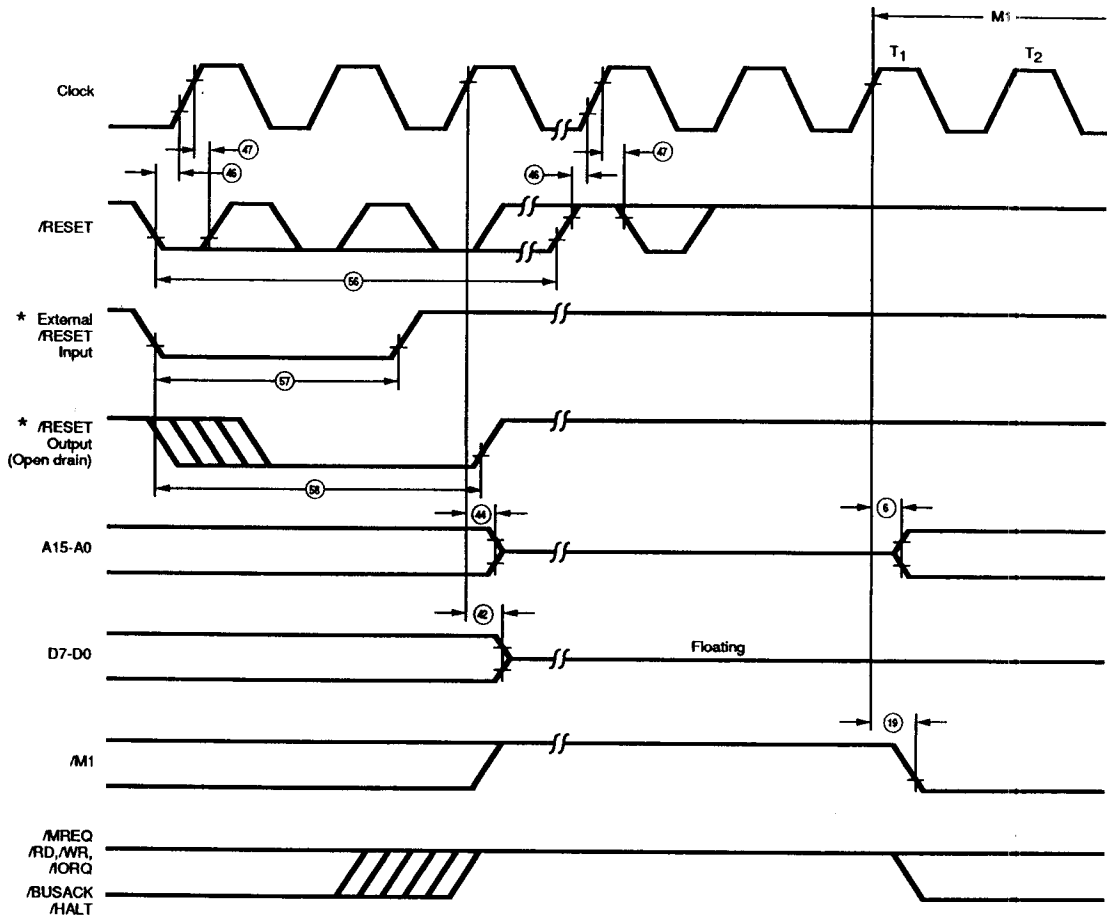
* Although /NMI is an asynchronous input, to guarantee its being recognized on the following machine cycle, /NMI's falling edge must occur no later than the rising edge of the clock preceding the last state of any instruction cycle (T_{LI}).

Figure 47. Halt Acknowledge
(See Table A)

Reset Cycle. /RESET must be active for at least three clock cycles for the CPU to properly accept it. As long as /RESET remains active, the address and data buses float, and the control outputs are inactive.

Once /RESET goes inactive, two internal T cycles are consumed before the CPU resumes normal processing operation. /RESET clears the PC register, so the first op-code fetch location is 0000H (Figure 48).

Z84C13/C15 Only. If Reset output is disabled, /RESET must be active for at least three clock cycles for the CPU to properly accept it. Otherwise, /RESET must be active for at least two clock cycles and the on-chip reset circuit extends /RESET signal to at least a minimum of 16-clock cycles.



* 84C13/15 Only Reset Output is Enabled

Figure 48. Reset Cycle
(See Table A)

CGC TIMING

Figure 49 to Figure 52 shows the timing related CGC and Power-On Reset circuit.

Parameters referenced in Figure 49 thru Figure 52 appear in Table B.

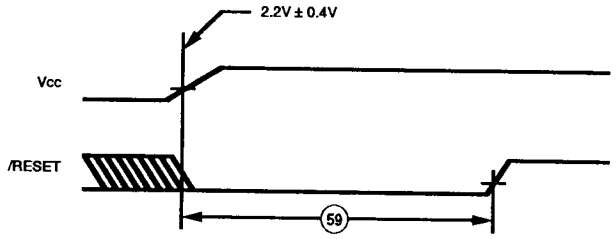


Figure 49. Reset on Power-up (Applies only for Z84C13/C15)
(See Table B)

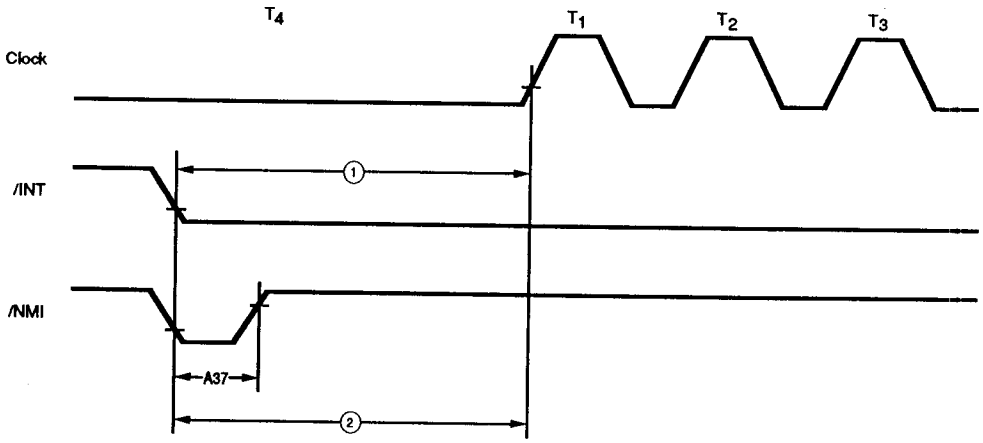
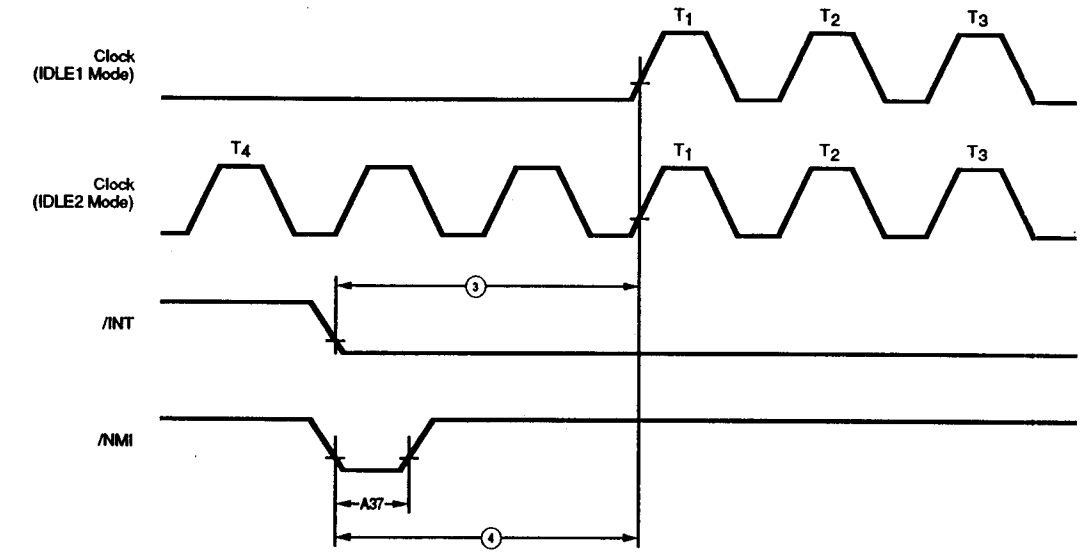
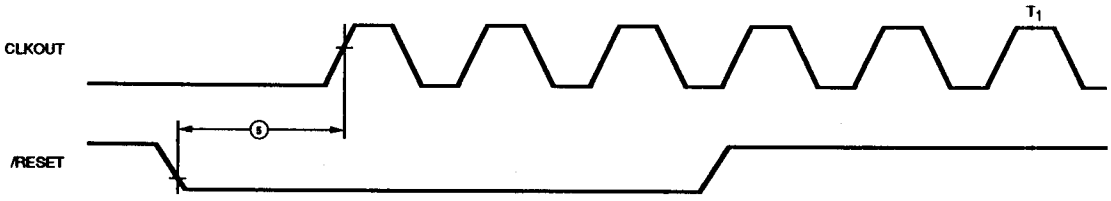


Figure 50. Clock Restart Timing by /INT, /NMI (STOP Mode)
(See Table B)

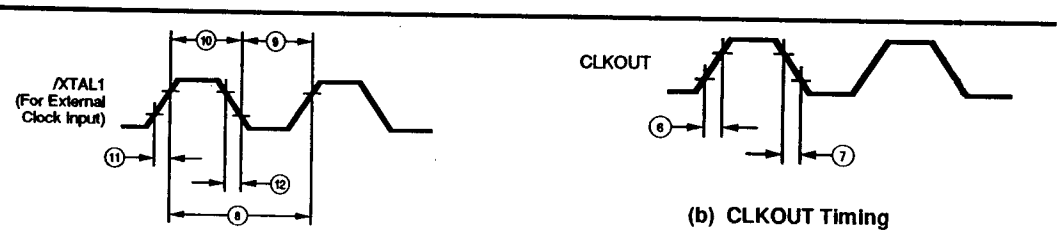


(a) Clock Restart Timing by /INT, /NMI (IDLE1/2 Mode)



(b) Clock Restart Timing by /RESET (IDLE 1/2 Mode)

Figure 51. Clock Restart Timing (IDLE1/2 Mode)
(See Table B)

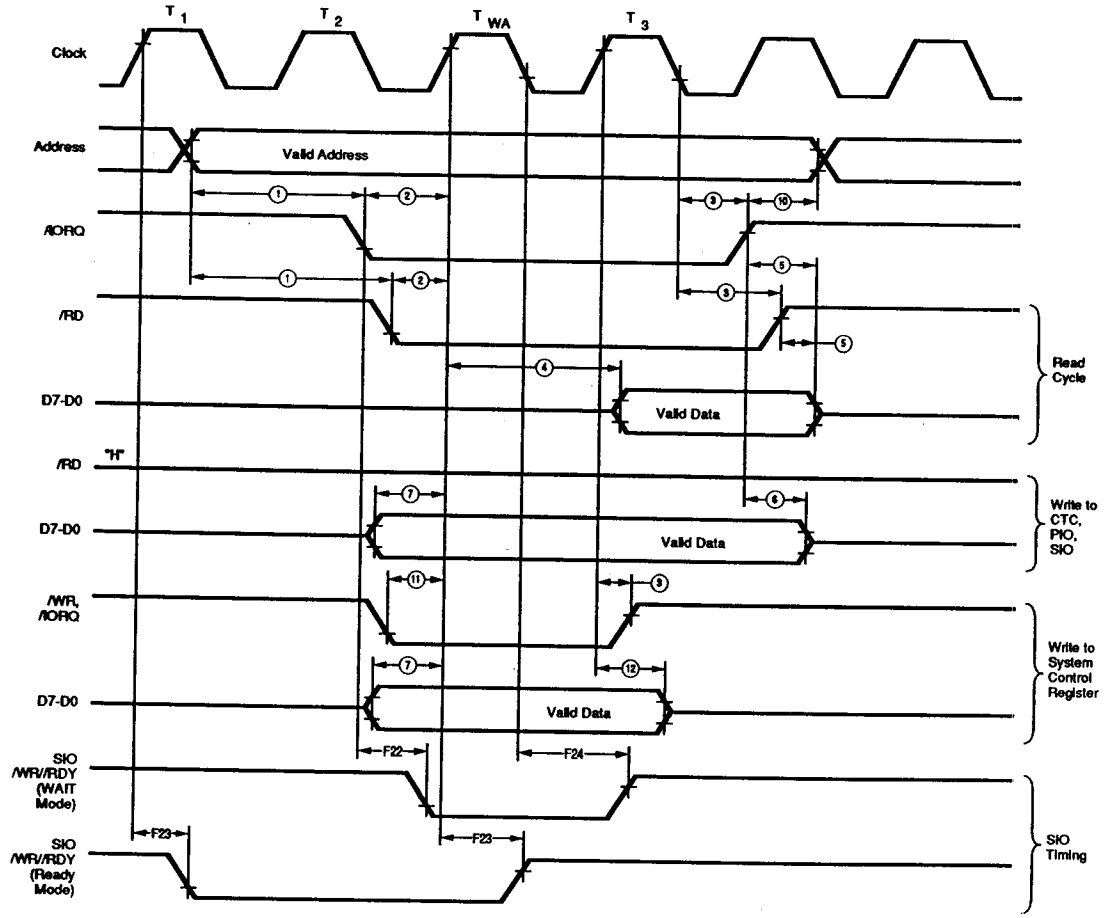


(a) XTAL1 Timing for External Clock Input

(b) CLKOUT Timing

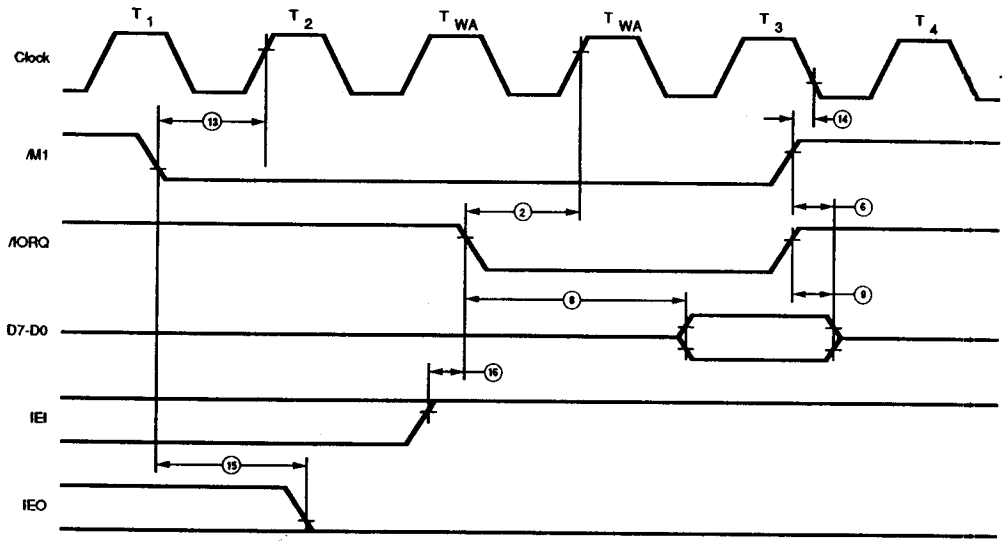
Figure 52. Clock Timing
(See Table B)

On-chip peripheral access from External Bus master. The timing for the on-chip I/O device access from the external bus master is shown in Figure 53. This timing also applies to the timing during EV mode of operation.

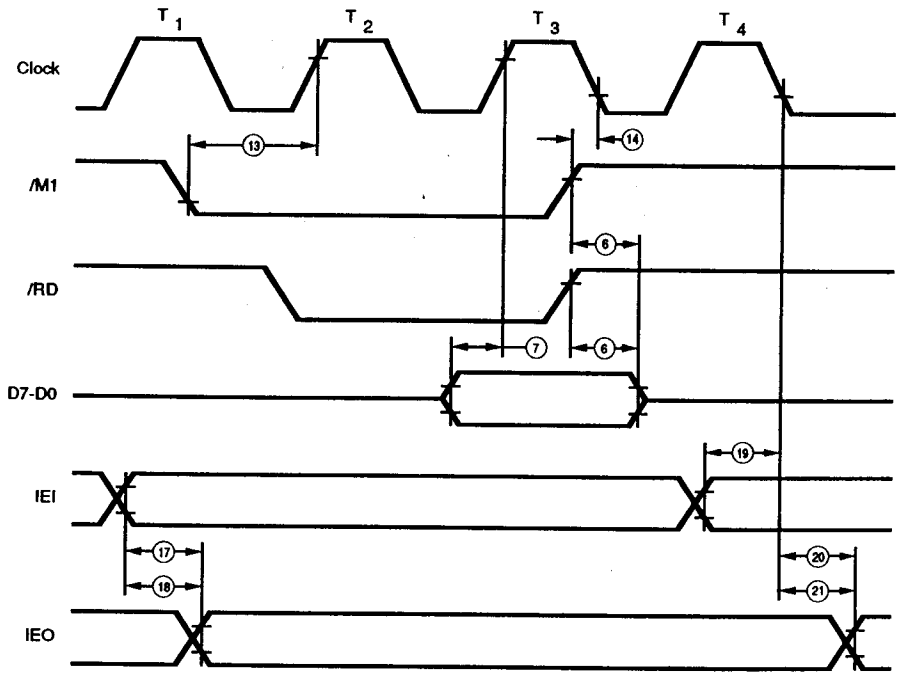


(a) On-chip peripheral I/O access from External Bus master
(See Tables C and F)

Figure 53. On-chip Peripheral Timing from External Bus master



(b) Interrupt Acknowledge Cycle Timing for On-chip peripheral from External Bus master
(See Table C)



(c) Op-code fetch Cycle Timing for On-chip peripheral from External Bus master
(See Table C)

Figure 53. On-chip Peripheral Timing from External Bus master (Continued)

PIO timing
(Not applicable on Z84x13) Figure 54 shows the timing for on-chip PIO.

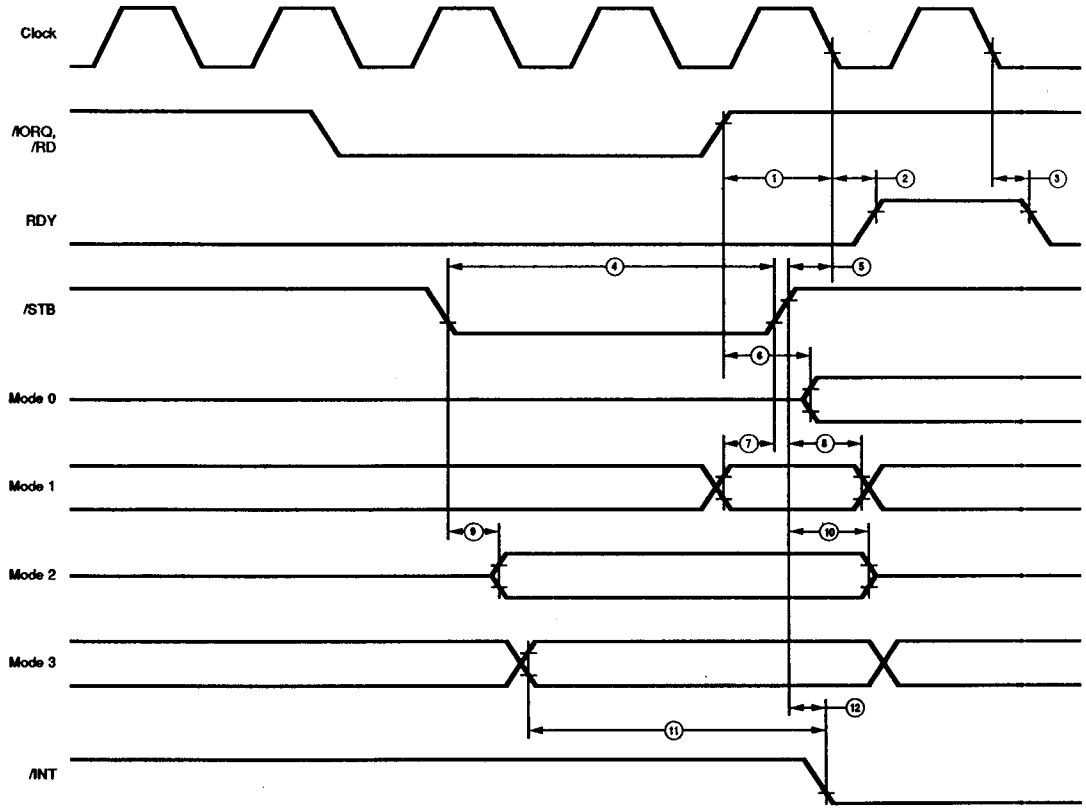


Figure 54. PIO Timing
(See Table D)

CTC Timing

Figure 55 shows the timing for on-chip CTC.

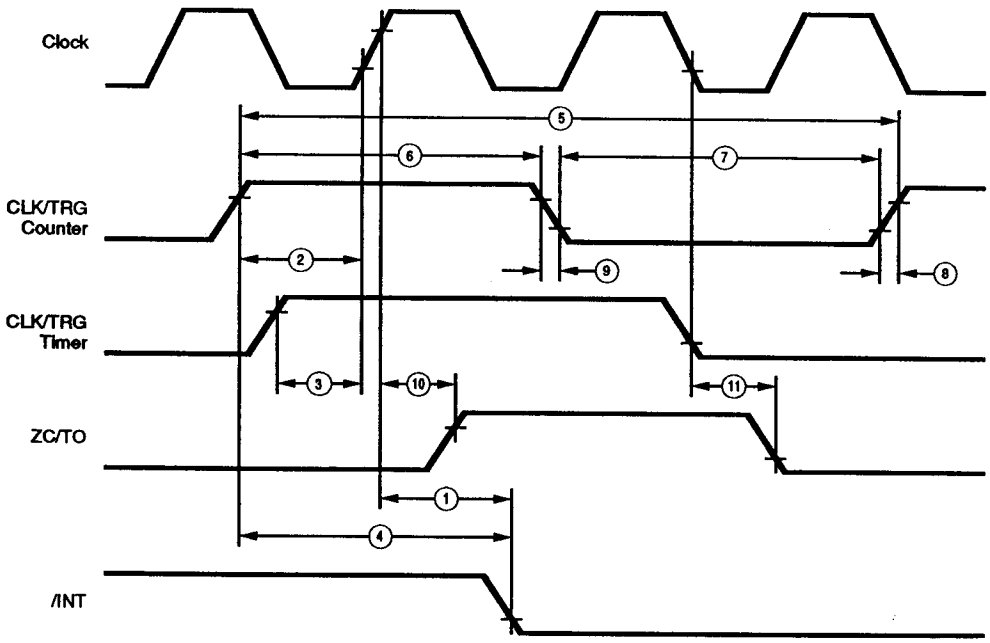


Figure 55. Counter/Timer Timing
(See Table E)

SIO Timing

Figure 56 shows the timing for on-chip SIO.

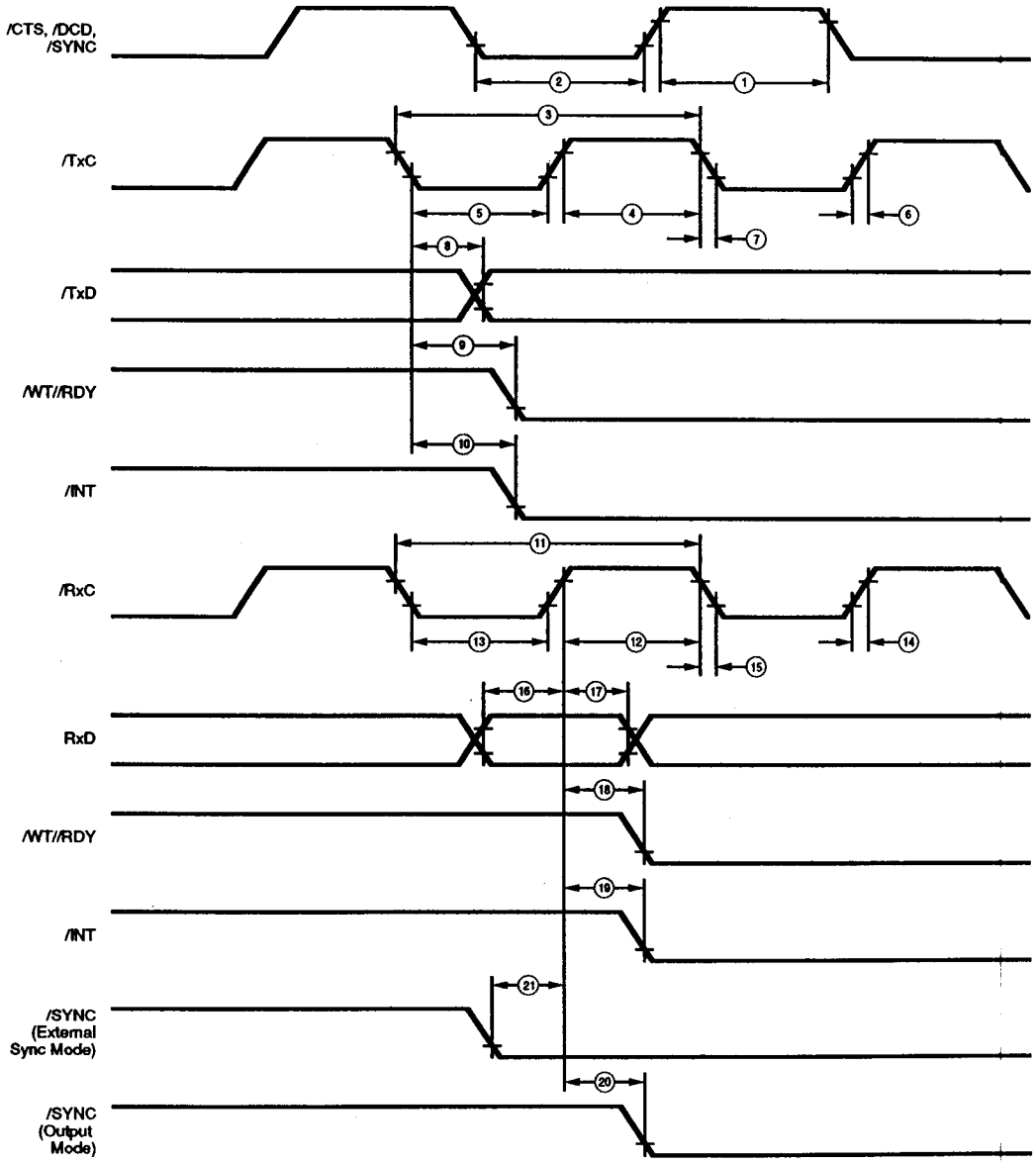


Figure 56. SIO Timing
(See Table F)

Watch-Dog Timer Timing
Figure 57 shows the timing for Watch-dog Timer.

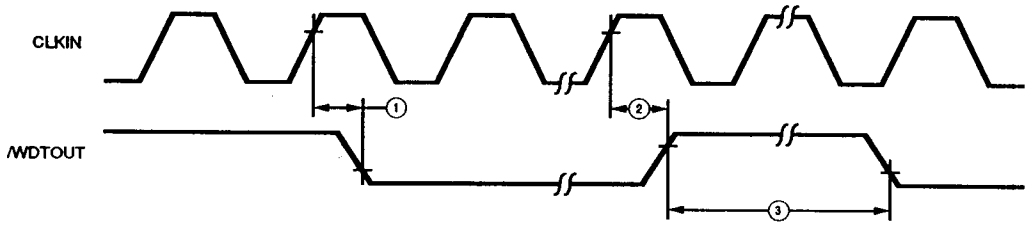


Figure 57. Watch-dog Timer Timing (See Table H)

PRECAUTIONS

(1) To release the HALT state by /RESET signal in STOP Mode, hold the /RESET signal at "0" until the output from the internal oscillator stabilizes.

Z84013/015 Only. To reset MPU, it is necessary to hold /RESET signal input at "0" level for at least three clocks.

Z84C13/C15 Only. If Reset output is disabled, /RESET must be active for at least three clock cycles for the CPU to properly accept it. Otherwise, the on-chip reset circuit extends /RESET signal to at least a minimum of 16-clock cycles.

(2) Releasing the MPU from the HALT state by the interrupt signal in IDLE1/2 Mode and STOP Mode, depends upon the HALT state and the internal system clock. They will stop unless an interrupt signal is accepted during the execution of NOP instruction, even when the internal system clock is restarted by the interrupt signal input. In particular, care must be taken when /INT is used.

Other precautions are identical to those for the Z84C00. Refer to the data sheet for the Z84C00.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Voltage on Vcc with respect to Vss .....-0.3V to +7.0V
Voltages on all inputs
with respect to Vss .....-0.3V to Vcc+0.3V
Operating Ambient
Temperature .....See Ordering Information
Storage Temperature .....-65 °C to + 150 °C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature range is:
E = -40°C to 100°C
Voltage Supply Range:
+4.50V ≤ Vcc ≤ + 5.50V

All AC parameters assume a load capacitance of 100 pf. Add 10 ns delay for each 50 pf increase in load up to a maximum of 150 pf for the data bus and 100 pf for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pf.

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

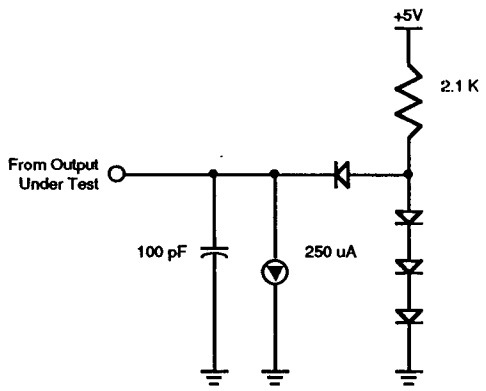


Figure 58. Standard Test Load

CAPACITANCE

Guaranteed by design and characterization

Symbol	Parameter	Min	Max	Unit
C_{CLOCK}	Clock Capacitance	35	pF	
C_{IN}	Input Capacitance	5	pF	
C_{OUT}	Output Capacitance	15	pF	

DC CHARACTERISTICS

V_{CC}=5.0V ± 10%, unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Condition
V_{OLC}	Clock Output High Voltage	V_{CC}-0.6		V	-2.0mA
V_{OHC}	Clock Output Low Voltage		0.4	V	+2.0mA
V_{IHC}	Clock Input High Voltage	V_{CC}-0.6		V	
V_{ILC}	Clock Input Low Voltage		0.4	V	
V_{IH}	Input High Voltage	2.2	V_{CC}	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{OL}	Output Low Voltage		0.4 [5]	V	I_{LO}=2.0mA
V_{OH1}	Output High Voltage	2.4		V	I_{OH}=-1.6mA
V_{OH2}	Output High Voltage	V_{CC}-0.8 [5]		V	I_{OH}=-250µA
I_{CC1}	Power Supply Current				V_{CC}=5V
	XTALIN =10MHz		50	mA	V_{IH}=V_{CC}-0.2V
	XTALIN = 6MHz		30	mA	V_{IL}=0.2V
I_{CC2}	Power Supply Current (STOP Mode)		50	µA	V_{CC}=5V
I_{CC3}	Power Supply Current (IDLE1 Mode)				V_{CC}=5V
	XTALIN =10MHz		6	mA	V_{IH}=V_{CC}-0.2V
	XTALIN = 6MHz		4	mA	V_{IL}=0.2V
I_{CC4}	Power Supply Current (IDLE2 Mode)				V_{CC}=5V
	XTALIN =10MHz		TBD [1]	mA	V_{IH}=V_{CC}-0.2V
	XTALIN = 6MHz		TBD [1]	mA	V_{IL}=0.2V
I_{LI}	Input Leakage Current	-10	10 [4]	µA	V_{IN}=0.4V to V_{CC}
$I_{L(SY)}$	SYNC pin Leakage Current	-40	10	µA	V_{OUT}=0.4V to V_{CC}
I_{LO}	3-state Output Leakage Current in Float	-10	10 [2]	µA	V_{OUT}=0.4V to V_{CC}
I_{OHD}	Darlington Drive Current				V_{OH}=1.5V
	(Port B and CTC ZC/TO)	-1.5		mA	REXT = 390 Ohms

Notes:

[1] Measurements made with outputs floating.

[2] A15-A0, D7-D0, /MREQ, /IORQ, /RD and /WR.

[3] I_{CC2} Standby Current is guaranteed when the /HALT pin is low in STOP mode.

[4] All Pins except XTALI, where I_{LI}=±25µA.

[5] A15-A0, D7-D0, /MREQ, /IORQ, /RD, /WR, /HALT, /M1 and /BUSACK.

AC CHARACTERISTICS

Table A. CPU Timing (See Figure 41 to 48)

No	Symbol	Parameter	Z84X1306 Z84X1506 Min	Max	Z84X1310 Z84X1510 Min	Max	Z84C1316* Z84C1516 Min	Max	Unit	Note
1	TcC	Clock Cycle time	162**	DC	100**	DC	61	DC	nS	[A1]
2	TwCh	Clock Pulse Width (High)	65	DC	40	DC	20	DC	nS	[A1]
3	TwCl	Clock Pulse Width (Low)	65	DC	40	DC	20	DC	ns	[A1]
4	TfC	Clock Fall time		20		10		6	ns	[A1]
5	TrC	Clock Rise time		20		10		6	ns	[A1]
6	TdCr(A)	Address Valid from Clock Rise		90		65		55	ns	
7	TdA(MREQf)	Address Valid to /MREQ Fall	35**		0**		-15		ns	
8	TdCf(MREQf)	Clock Fall to /MREQ Fall Delay		70		55		40	ns	
9	TdCr(MREQr)	Clock Rise to /MREQ Rise Delay		70		55		40	ns	
10	TwMREQh	/MREQ Pulse Width (High)	65**		30**		10		ns	[A2]
11	TwMREQl	/MREQ Pulse Width (Low)	132**		75**		25		ns	[A2]
12	TdCf(MERQr)	Clock Fall to /MREQ Rise Delay		70		55		40	ns	
13	TdCf(RDf)	Clock Fall to /RD Fall Delay		80		65		40	ns	
14	TdCr(RDr)	Clock Rise to /RD Rise Delay		70		55		40	ns	
15	TsD(Cr)	Data Setup Time to Clock Rise	30		25		10		ns	
16	ThD(RDr)	Data Hold Time After /RD Rise	0		0		0		ns	
17	TsWAIT(Cf)	/WAIT Setup Time to Clock Fall	60		20		75		ns	
18	ThWAIT(Cf)	/WAIT Hold Time After Clock Fall	10		10		10		ns	
19	TdCr(M1f)	Clock Rise to /M1 Fall Delay		80		65		40	ns	
20	TdCr(M1r)	Clock Rise to /M1 Rise Delay		80		65		40	ns	
21	TdCr(RFSHf)	Clock Rise to /RFSH Fall Delay		110		80		60	ns	
22	TdCr(RFSHr)	Clock Rise to /RFSH Rise Delay		100		80		60	ns	
23	TdCf(RDr)	Clock Fall to /RD Rise Delay		70		55		40	ns	
24	TdCr(RDf)	Clock Rise to /RD Fall Delay		70		55		40	ns	
25	TsD(Cf)	Data Setup to Clock Fall During M2, M3, M4 or M5 Cycles	40		25		12		ns	
26	TdA(IORQf)	Address Stable Prior to /IORQ Fall	107**		50**		0		ns	
27	TdCr(IORQf)	Clock Rise to /IORQ Fall Delay		65		50		40	ns	
28	TdCf(IORQr)	Clock Fall to /IORQ Rise Delay		70		55		40	ns	
29	TdD(WRf)	Data Stable Prior to /WR Fall	22**		40**		-10		ns	
30	TdCf(WRf)	Clock Fall to /WR Fall Delay		70		55		40	ns	
31	TwWR	/WR Pulse Width	132**		75**		25		ns	
32	TdCf(WRr)	Clock Fall to /WR Rise Delay		70		55		40	ns	
33	TdD(WRf)IO	Data Stable Prior to /WR Fall	-55**		-10**		-30		ns	
34	TdCr(WRf)	Clock Rise to /WR Fall Delay		60		50		40	ns	
35	TdWRr(D)	Data Stable from /WR Fall	30**		10**		0	0	ns	
36	TdCf(HALT)	Clock Fall to /HALT 0 or 1		260		90		70	ns	
37	TwNMI	/MNI pulse Width	60		60		60		ns	
38	TsBUSREQ(Cr)	/BUSREQ Setup Time to Clock Rise	50		30		15		ns	
39	ThBUSREQ(Cr)	/BUSREQ Hold Time after Clock Rise	10		10		10		ns	
40	TdCr(BUSACKf)	Clock Rise to /BASACK Fall Delay		90		75		40	ns	

AC CHARACTERISTICS (Continued)

Table A. CPU Timing (Continued)

No	Symbol	Parameter	Z84X1306 Z84X1506 Min	Z84X1306 Z84X1506 Max	Z84X1310 Z84X1510 Min	Z84X1310 Z84X1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Unit	Note
41	TdCf(BUSACKr)	Clock Fall to /BASACK Rise Delay		90		75		40	ns	
42	TdCr(Dz)	Clock Rise to Data Float Delay		80		65		40	ns	
43	TdCr(CTz)	Clock Rise to Control Outputs Float Delay (/MREQ, /IORQ, /RD and /WR)		70		65		40	ns	
44	TdCr(Az)	Clock Rise to Address Float Delay		80		75		40	ns	
45	TdCTr(A)	Address Hold Time from /MREQ, /IORQ, /RD or /WR	35**		20**			0	ns	
46	TsRESET(Cr)	/RESET to Clock Rise Setup Time	60		40		15		ns	
47	ThRESET(Cr)	/RESET to Clock Rise Hold Time	10		10		10		ns	
48	TsINTf(Cr)	/INT Fall to Clock Rise Setup Time	70		50		15		ns	
49	ThINTr(Cr)	/INT Rise to Clock Rise Hold Time	10		10		10		ns	
50	TdM1f(IORQf)	/M1 Fall to /IORQ Fall Delay	359**		220**		100		ns	
51	TdCf(IORQf)	Clock Fall to /IORQ Fall Delay		70		55		45	ns	
52	TdCf(IORQr)	Clock Rise to /IORQ Rise Delay		70		55		45	ns	
53	TdCf(D)	Clock Fall to Data Valid Delay		130		110		75	ns	
54	TRDf(D)	/RD Fall to Output Data Valid		TBD		60		40	ns	
55	TdIORQ(D)	/IORQ Fall to Output Data Valid		TBD		70		45	ns	
56	TwRESET	/RESET Pulse Width 013/015, or C13/C15 with RESET Output Disabled	3TcC		3TcC		3TcC		ns	
57	TwRESEToe	/RESET Pulse Width RESET Output Enabled	2TcC		2TcC		2TcC		ns	
58	TwRESETdo	/RESET Drive Duration RESET Output Enabled	16TcC		16TcC		16TcC		ns	
59	TwRESETpor	/RESET drive duration on Power-On Sequence	10	75	10	75	10	75	ms	

Notes:

* 16 MHz Timings are preliminary and subject to change. Only C version

** For clock period other than the minimum shown, calculate parameters using the formula on Table H.

[A1] These parameters apply to the external Clock input on CLKIN pin. For the cases where external Clock is fed from XTAL1, please refer to Table B.

[A2] For loading >= 50 pF, decrease width by 10 ns for each additional 50 pF.

Table H. Footnote to Table A.

No	Symbol	Parameter	Z84X1306 Z84X1506	Z84X1310 Z84X1510	Z84C1316* Z84C1516
1	TcC	TwCh + TwCl + TrC + TfC			
7	TdA(MREQf)	TwCh + TfC	-50	-50	-45
10	TwMREQh	TwCh + TfC	-20	-20	-20
11	TwMREQl	TcC	-30	-25	-25
26	TdA(IORQf)	TcC	-55	-50	-50
29	TdD(WRf)	TcC	-140	-60	-60
31	TwWR	TcC	-30	-25	-25
33	TdD(WRf)	TwCl + TrC	-140	-60	-60
35	TdWRr(D)	TwCl + TrC	-55	-40	-25
45	TdCTr(A)	TwCl + TrC	-50	-30	-30
50	TdM1f(IORQf)	2TcC + TwCh + TfC	-50	-30	-30

AC CHARACTERISTICS (Continued)

Table B. CGC Timing (See Figure 49 to 52)

No	Symbol	Parameter	Z84C1306 Z84C1506 Min	Z84C1306 Z84C1506 Max	Z84C1310 Z84C1510 Min	Z84C1310 Z84C1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Unit	Note
1	TRST(INT)S	Clock Restart Time by /INT (STOP Mode)	(Typ)2^{14}+2.5TcC		(Typ)2^{14}+2.5TcC		(Typ)2^{14}+2.5TcC		ns	
2	TRST(MNI)S	Clock Restart Time by /NMI (STOP Mode)	(Typ)2^{14}+2.5TcC		(Typ)2^{14}+2.5TcC		(Typ)2^{14}+2.5TcC		ns	
3	TRST(INT)I	Clock Restart Time by /INT (IDLE Mode)	2.5TcT		2.5TcT		2.5TcT		ns	
4	TRST(Nmi)I	Clock Restart Time by /NMI (IDLE Mode)	2.5TcT		2.5TcT		2.5TcT		ns	
5	TRST(RESET)I	Clock Restart Time by /RESET (IDLE Mode)	1TcC		1TcC		1TcC		ns	
6	TfCLKOUT	CLKOUT Rise Time		15		10		6	ns	
7	TrCLKOUT	CLKOUT Fall time		15		10		6	ns	
8	TcX1	XTAL1 Cycle Time (for External Clock Input on XTAL1)								
		Divide-by-Two Mode	81		50		31		ns	
		Divide-by-One Mode	162		100		61		ns	
9	TwlX1	XTAL1 Low Pulse Width (for External Clock Input on XTAL1)								
		Divide-by-Two Mode	35		15		10		ns	
		Divide-by-One Mode	65		40		25		ns	
10	TwhX1	XTAL1 High Pulse Width (for External Clock input on XTAL1)								
		Divide-by-Two mode	35		15		10		ns	
		Divide-by-One mode	65		40		25		ns	
11	TrX1	XTAL1 Rise Time (for External Clock Input on XTAL1)		25		25		15	ns	[B1]
12	TfX1	XTAL1 Fall Time (for External Clock Input on XTAL1)		25		25		15	ns	[B1]

Note:
[B1] If parameters 8 and 9 are not met, adjust parameters 11 and 12 to satisfy parameters 8 and 9.

Table C. Timing for on-chip peripheral access from external bus master and daisy chain timing (See Figure 53(a))

No	Symbol	Parameter	Z84C1306 Z84C1506 Min	Z84C1306 Z84C1506 Max	Z84C1310 Z84C1510 Min	Z84C1310 Z84C1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Unit	Note
1	TsA(Rlf)	Address Setup Time to /RD, /IORQ Fall	50		40		30		ns	
2	TsRI(Cr)	/RD, /IORQ Rise to Clock Rise Setup	60		50		40		ns	
3	Th	Hold time for Specified Setup	15		15		10		ns	
4	TdCr(DO)	Clock Rise to Data out delay		100		80	60		ns	
5	TdRIr(DOz)	/RD, /IORQ Rise to Data Out Float Delay		75		60	50		ns	
6	ThRDr(D)	/M1, /RD, /IORQ Rise to Data Hold	15	40	15	30		20	ns	[C1]
7	TsD(Cr)	Data In to Clock Rise Setup Time	30		25		15		ns	
8	TdIOf(DOI)	/IORQ Fall to Data Out Delay (INTACK cycle)		95		95	70		ns	
9	ThIOr(D)	/IORQ Rise to Data Hold	15		15		10		ns	
10	ThIOr(A)	/IORQ Rise to Address Hold	15		15		10		ns	
11	TsWIf(Cr)	/IORQ, /WR setup time to Clock Rise New parameter	20		20		15		ns	[C2]
12	ThWRr(Cr)	Clock Rise to /IORQ, /WR Rise hold time	0		0		0		ns	[C2]
13	TsM1f(Cr)	/M1 Fall to Clock Rise Setup Time	40		40		15		ns	
14	TsM1r(Cf)	/M1 Rise to Clock Rise Setup Time (/M1 cycle)	-15		-15		-10		ns	
15	TdM1f(IEOf)	/M1 Fall to IEO Fall delay (Interrupt Immediately Preceding /M1 Fall)		140		80		60	ns	
20	TdCf(IEOr)	Clock Fall to IEO Rise Delay	50		40			30	ns	
21	TdCf(IEOf)	Clock Fall to IEO Rise Delay		90		75		50	ns	

Notes:
[C1] For I/O write to PIO, CTC and SIO.
[C2] For I/O Write to system control registers.
[C3] For daisy-chain timing, please refer to the note on Page 356.

AC CHARACTERISTICS (Continued)

Table D. PIO Timing (Z84x15 only) (See Figure 54)

No	Symbol	Parameter	Z84C1506 Min	Z84C1506 Max	Z84C1510 Min	Z84C1510 Max	Z84C1516* Min	Z84C1516* Max	Unit	Note
1	TslOr(Cr)	/IORQ Rise to Clock Fall Setup Time (To Activate RDY on Next Clock Cycle)	100		100		100		ns	
2	TdCf(RDYr)	Clock Fall to RDY Rise Delay		100		115		30	ns	[D2]
3	TdCf(RDYf)	Clock Fall to RDY Fall Delay		100		115		30	ns	[D2]
4	TwSTB	/STB Pulse Width	100		80		50		ns	[D1]
5	TsSTBr(Cr)	/STB Rise to Clock Fall Setup Time (To Activate RDY on Next Clock Cycle)	100		100		70		ns	[D2]
6	TdIOr(PD)	/IORQ Rise to Port Data Stable Delay (Mode 0)		140		120		100	ns	[D2]
7	TsPD(STBr)	Port Data to /STB Rise Setup Time (Mode 1)	140		75		30		ns	
8	ThPD(STBr)	Port Data to /STB Rise Hold Time (Mode 1)	15		15		15		ns	
9	TdSTBf(PD)	/STB Fall to Port Data Stable (Mode 2)		150		120		30	ns	[D2]
10	TdSTBr(PDz)	/STB Rise to Port Data Float Delay (Mode 2)		140		120		50	ns	
11	TdPD(INTf)	Port Data Match to /INT Fall Delay (Mode 3)		250		200		40	ns	
12	TdSTBr(INTf)	/STB Rise to /INT Fall Delay		290		220		75	ns	

Notes:
[D1] For Mode 2: TwSTB >TsPD(STB).
[D2] Increase these values by 2 ns for 10 pF increase in loading up to 100 pF Max.

Table E. CTC Timing (Figure 55)

No	Symbol	Parameter	Z84C1306 Z84C1506 Min	Z84C1306 Z84C1506 Max	Z84C1310 Z84C1510 Min	Z84C1310 Z84C1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Unit	Note
1	TdCr(INTf)	Clock Rise to /INT Fall Delay		(TcC+100)		(TcC+80)		(TcC+30)		[E1]
2	TsCTR(Cc)	CLK/TRG to Clock Rise Setup Time for Immediate Count	90		90		40		ns	[E2]
3	TsCTR(Ct)	CLK/TRG to Clock Rise Setup Time for Enabling of Prescalor on Following Clock Rise	90		90		40		ns	[E1]
4	TdCTR(INTf)	CLK/TRG to /INT Fall Delay TsCTR(C) Satisfied		(1)+(3)		(1)+(3)		(1)+(3)	ns	[E2]
		TsCTR(C) not Satisfied		TcC+(1)+(3)		TcC+(1)+(3)		TcC+(1)+(3)	ns	[E2]
5	TcCTR	CLK/TRG Cycle time	(2TcC)	DC	(2TcC)	DC	(2TcC)	DC	ns	[E3]
6	TwCTRh	CLK/TRG Width (Low)	90	DC	90	DC	25	DC	ns	
7	TwCTRl	CLK/TRG Width (High)	90	DC	90	DC	25	DC	ns	
8	TrCTR	CLK/TRG Rise Time		30		30		15	ns	
9	TfCTR	CLK/TRG Fall Time		30		30		15	ns	
10	TdCr(ZCr)	Clock Rise to ZC/TO Rise Delay		80		80		25	ns	
11	TdCf(ZCf)	Clock Fall to ZC/TO Fall Delay		80		80		25	ns	

Notes:
[E1] Timer Mode.
[E2] Counter Mode.
[E3] Counter Mode only; when using a cycle time less than 3TcC, parameter #2 must be met.

Table F. SIO Timing (See Figures 53(a) and 56)

No	Symbol	Parameter	Z84C1306 Z84C1506 Min	Z84C1306 Z84C1506 Max	Z84C1310 Z84C1510 Min	Z84C1310 Z84C1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Unit	Note
1	TwPh	Pulse Width (High)	150		120		80		ns	
2	TwPl	Pulse Width (Low)	150		120		80		ns	
3	TcTxC	/TxC Cycle Time	250		200		120		ns	[F1]
4	TwTxCH	/TxC Width (High)	85		80		55		ns	
5	TwTxCL	/TxC Width (Low)	85		80		55		ns	
6	TrTxC	/TxC Rise Time		60		60		60	ns	
7	TfTxC	/TxC Fall Time		60		60		60	ns	
8	TdTxCf(TxD)	/TxC Fall to TxD Delay		160		120		40	ns	
9	TdTxCf(W/RRf) (Ready Mode)	/TxC Fall to /W//RDY Fall Delay	5	9	5	9	5	8	TcC	
10	TdTxCf(INTf)	/TxC Fall to /INT Fall Delay	5	9	5	9	5	9	TcC	
11	TcRxC	/RxC Cycle Time	250		200		120		ns	[F1]
12	TwRxCh	/RxC Width (High)	85		80		55		ns	
13	TwRxCl	/RxC Width (Low)	85		80		55		ns	
14	TrRxC	/RxC Rise Time		60		60		60	ns	
15	TfRxC	/RxC Fall Time		60		60		60	ns	
16	TsRxD(RxCr)	RxD to /RxC Rise Setup Time (X1 Mode)	0		0		0		ns	
17	ThRxCr(RxD)	/RxC Rise to RxD Hold Time (X1 Mode)	80		60			40	ns	
18	TdRxCr(W/RRf)	/RxC Rise to /W//RDY Fall Delay (Ready Mode)	10	13	10	13	10	13	TcC	
19	TdRxCr(INTf)	/RxC Rise to /INT Fall Delay	10	13	10	13	10	13	TcC	
20	TdRxCr(SYNCf)	/RxC Rise to /SYNC Fall Delay (Output Modes)	4	7	4	7	4	7	TcC	
21	TsSYNCf(RxCr)	/SYNC Fall to /RxC Rise Setup (External Sync Modes)	-100		-100		-100		ns	[F2]
22	TdIOf(W/RRf)	/IORQ Fall or Valid Address to /W//RDY Delay (Wait Mode)		130		110		40	ns	[F2]
23	TdCr(W/RRf)	Clock Rise to /W//RDY Delay (Ready Mode)		85		85		40	ns	[F2]
24	TdCf(W/Rz)	Clock Fall to /W//RDY Float Delay (Wait Mode)		90		80		40	ns	[F2]

Notes:
[F1] In all modes, the System Clock rate must be at least five times the maximum data rate.
[F2] Parameters 22 to 24 are on Figure 53a.

AC CHARACTERISTICS (Continued)

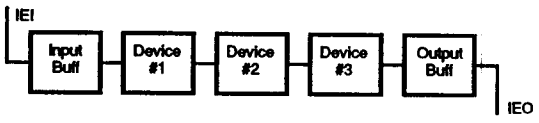
Table G. Watch Dog Timer Timing (See Figure 57)

No	Symbol	Parameter	Z84C1306 Z84C1506 Min	Z84C1306 Z84C1506 Max	Z84C1310 Z84C1510 Min	Z84C1310 Z84C1510 Max	Z84C1316* Z84C1516 Min	Z84C1316* Z84C1516 Max	Units
1	TdC(WDTf)	Clock Rise to /WDTOUT Fall Delay		160		160		160	ns
2	TdCr(WbTc)	Clock Rise to /WDTOUT Rise Delay		165		165		160	ns
3	TcWDT	/WDTOUT Cycle Time							
		WDTP = 00	(Typ)2^{16}TcC		(Typ)2^{16}TcC		(Typ)2^{16}TcC		ns
		WDTP = 01	(Typ)2^{18}TcC		(Typ)2^{18}TcC		(Typ)2^{18}TcC		ns
		WDTP = 10	(Typ)2^{20}TcC		(Typ)2^{20}TcC		(Typ)2^{20}TcC		ns
		WDTP = 11	(Typ)2^{22}TcC		(Typ)2^{22}TcC		(Typ)2^{22}TcC		ns

Notes:
* In all modes, the System Clock rate must be at least five times the maximum data rate.
RESET must be active a minimum of one complete clock cycle.
[1] Units equal to System Clock Periods.
[2] Units in nanoseconds (ns).

Additional information for note [C3]

Parameter #15, 16, 17 and 18 of Table C. These parameters are daisy-chain timing and calculated values, and vary depending on the inside daisy-chain configuration, which is specified in the Interrupt Priority Register. Inside the IPC, the daisy chain can be figured as follows:



Internal Daisy Chain Configuration

No	Parameter	6 MHz Min	6 MHz Max	10 MHz Min	10 MHz Max	16 MHz* Min	16 MHz* Max	Units
15	TdM1(IEO)		160		100		100	ns
16	TsIEI(IO) (PIO at #3)	160		100		100		ns
	(CTC at #3)	160		100		100		ns
	(SIO at #3)	160		100		100		ns
17	TdIEI(IEOf)		120		70		100	ns
18	TdIEI(IEOr)		120		70		100	ns

To calculate IPC daisy-chain timing, it can be treated as if there are Z80 PIO, CTC and SIO with Input buffer and look ahead circuit on the chain. Following are the calculation formulas:

Parameter Table C, #15, /M1 falling to IEO delay
TsM1(IEO) = Max[TdM1(IO)#1, TdM1(IO)#2, TdM1(IO)#3] + (look-ahead gate Delay)

Parameter Table C, #16, IEI to /IORQ falling setup time
TsIEI(IO) = TdIEI(IEO)#1 + TdIEI(IEO)#2 + TsIEI(IO)#3 + (Input Buffer delay)

Parameter Table C, #17, IEI falling to IEO falling delay
TdIEI(IEOf) = Max[TdIEI(IEOf)PIO, TdIEI(IEOf)CTC, TdIEI(IEOf)SIO] + (Input Buffer delay) + (look-ahead gate Delay)

Parameter Table C, #18, IEI rising to IEO rising delay (After ED decode) TdIEI(IEOr) = TdIEI(IEOr)PIO + TdIEI(IEOr)CTC + TdIEI(IEOr)SIO + (Input Buffer delay) + (look-ahead gate Delay)

* Where TdIEI(IEO) is worse number between TdIEI(IEOr) and TdIEI(IEOf)

	6MHz Min	Max	10MHz Min	Max	16MHz Min	Max
Input Buffer Delay	10nS		10nS		10 nS	
Look ahead gate delay	10nS		10nS		10 nS	

6MHz	PIO part Min	Max	CTC part Min	Max	SIO part Min	Max
TdM1(IEO)		90nS		130nS		150nS
TsIEI(IO)		90nS		100nS		70nS
TdIEI(IEOf)		100nS		90nS		50nS
TdIEI(IEOr)		130nS		90nS		50nS

10MHz	PIO part Min	Max	CTC part Min	Max	SIO part Min	Max
TdM1(IEO)		60nS		60nS		90nS
TsIEI(IO)		50nS		70nS		50nS
TdIEI(IEOf)		50nS		50nS		30nS
TdIEI(IEOr)		50nS		50nS		30nS

Preliminary

16MHz*	PIO part Min	Max	CTC part Min	Max	SIO part Min	Max
TdM1(IEO)		55nS		55nS		90nS
TsIEI(IO)		45nS		65nS		45nS
TdIEI(IEOf)		45nS		45nS		30nS
TdIEI(IEOr)		45nS		45nS		30nS

*** Note:**
16MHz is for C15 only.

If using an interrupt from only a portion of the IPC, these numbers are smaller than the values shown above. For more details about the "Z80 Daisy Chain Structure," please refer to the Application Note "Z80 Family Interrupt Structure" included in the Z80 Data book.