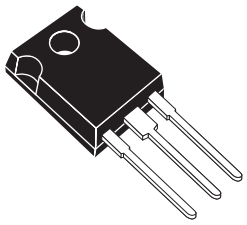
STW18NK80Z

N-channel 800V - 0.34Ω - 19A - TO-247
Zener-protected SuperMESH™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	P_W
STW18NK80Z	800V	<0.38Ω	19A	350W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatibility

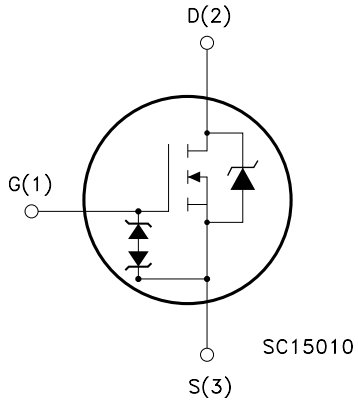


TO-247

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STW18NK80Z	W18NK80Z	TO-247	Tube

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2 Electrical characteristics 5
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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	800	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25°C	19	A
I_D	Drain current (continuous) at T_C = 100°C	12	A
I_{DM}(1)	Drain current (pulsed)	76	A
P_{tot}	Total dissipation at T_C = 25°C	350	W
	Derating Factor	2.4	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	6000	V
dv/dt(2)	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. I_{SD} ≤19A, di/dt ≤300A/µs, V_{DD} ≤V_{DD} < 800V, T_j ≤T_{JMAX}

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	0.36	°C/W
Rthj-amb	Thermal resistance junction-ambient max	50	°C/W
T_J	Maximum lead temperature for soldering purpose	300	°C

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	19	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	700	mJ

Table 4. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1mA (open drain)	30			V

1.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS} =0	800			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating, T_C = 125°C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 150µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 10A		0.34	0.38	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D = 10A		19		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		6100 500 100		pF pF pF
$C_{oss\ eq}$ (2)	Equivalent output capacitance	V_{GS} = 0V, V_{DS} = 0V to 640V		240		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 400V, I_D = 9A R_G = 4.7Ω V_{GS} = 10V (see *Figure 13*)		46 32 140 32		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 640V, I_D = 18A, V_{GS} = 10V (see *Figure 14*)		192 34 102	250	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Coss eq. is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				19 76	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 19A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 18A, di/dt = 100A/µs, V_{DD} = 40V, T_j = 25°C (see *Figure 15*)		920 11 24		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 18A, di/dt = 100A/µs, V_{DD} = 40V, T_j = 150°C (see *Figure 15*)		1160 15 25.8		ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

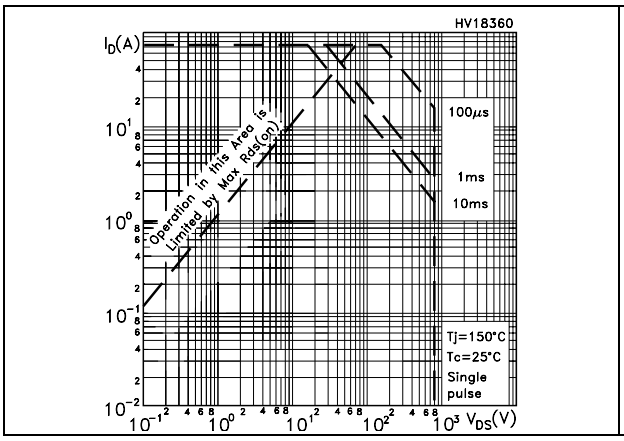


Figure 2. Thermal impedance

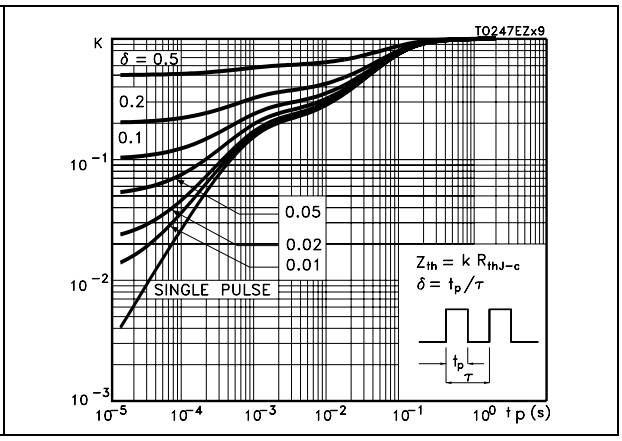


Figure 3. Output characterisics

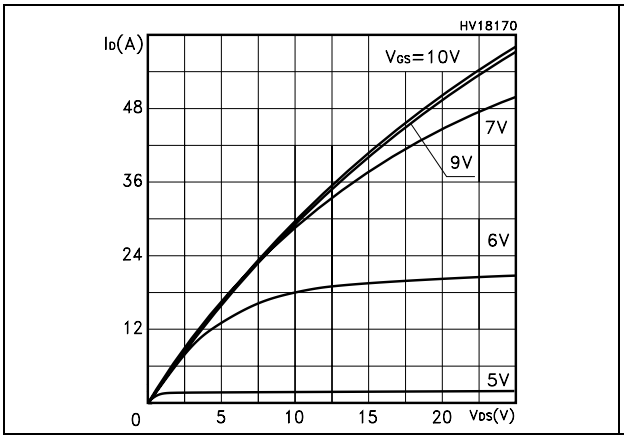


Figure 4. Transfer characteristics

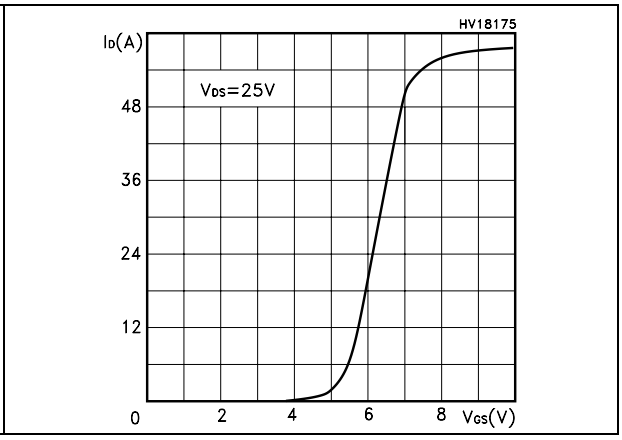


Figure 5. Transconductance

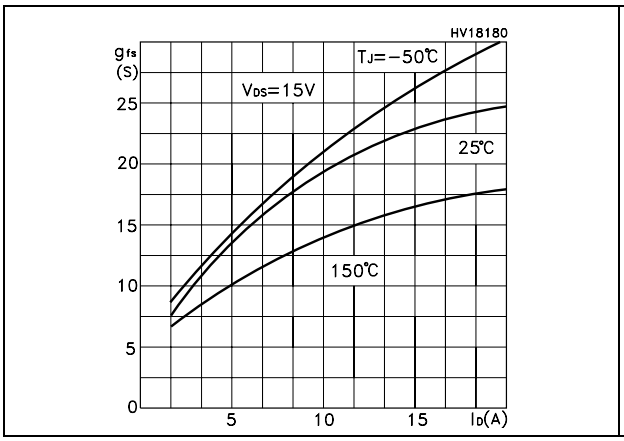


Figure 6. Static drain-source on resistance

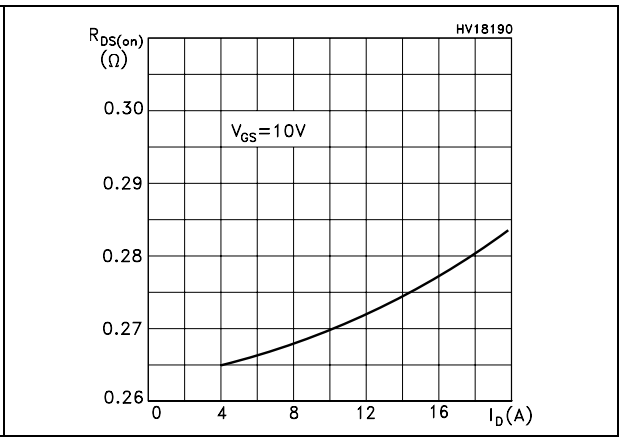


Figure 7. Gate charge vs gate-source voltage

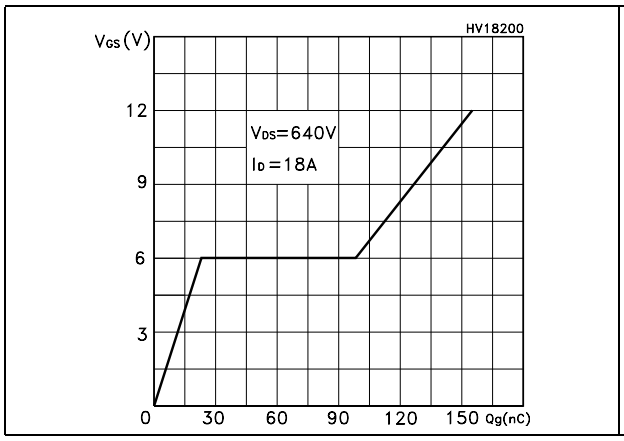


Figure 8. Capacitance variations

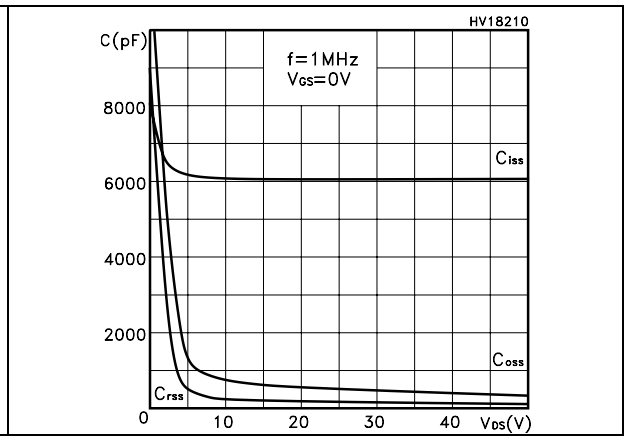


Figure 9. Normalized gate threshold voltage vs temperature

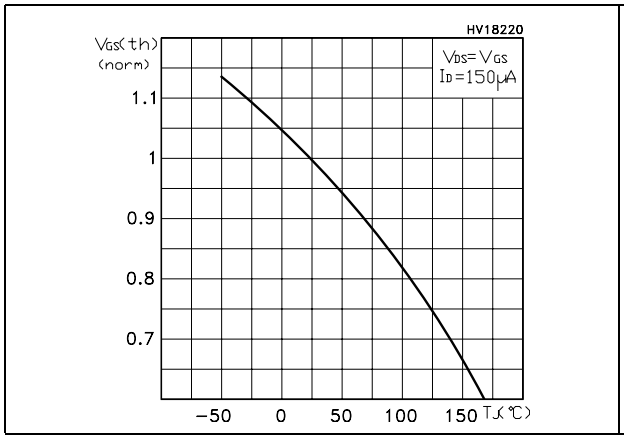


Figure 10. Normalized on resistance vs temperature

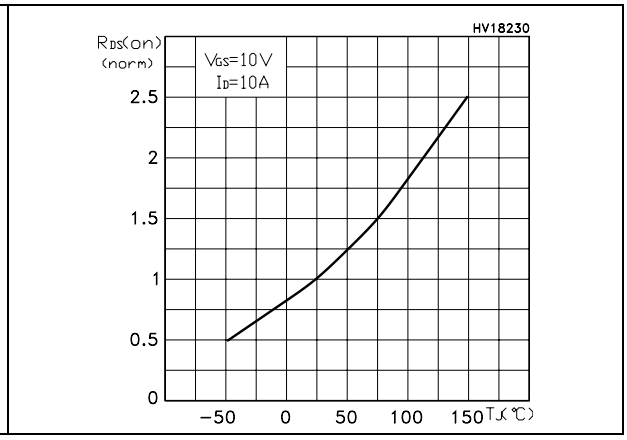


Figure 11. Source-drain diode forward characteristics

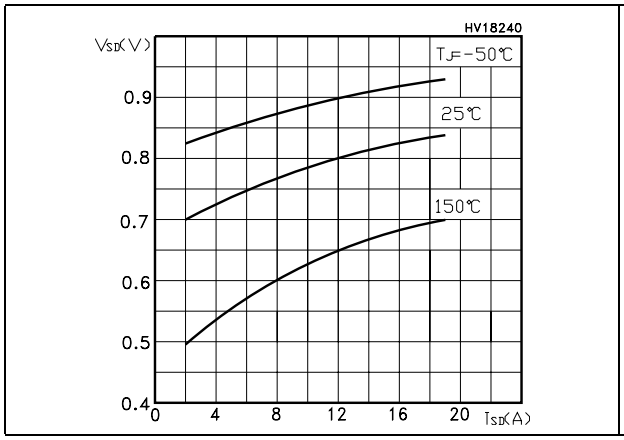
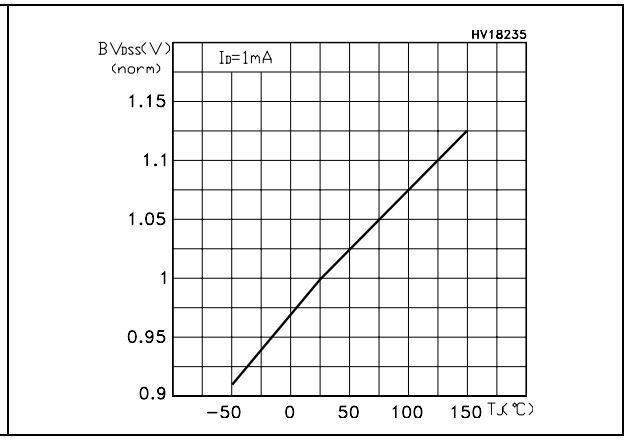


Figure 12. Normalized breakdown voltage vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

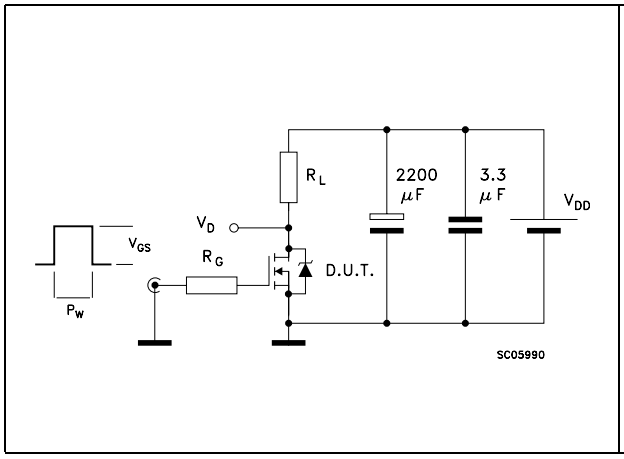


Figure 14. Gate charge test circuit

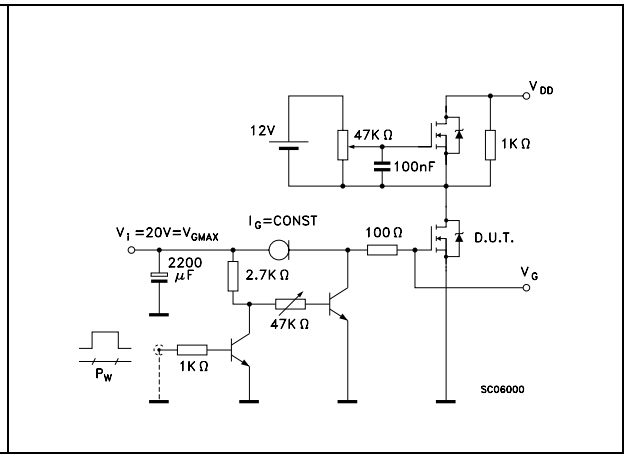


Figure 15. Test circuit for inductive load switching and diode recovery times

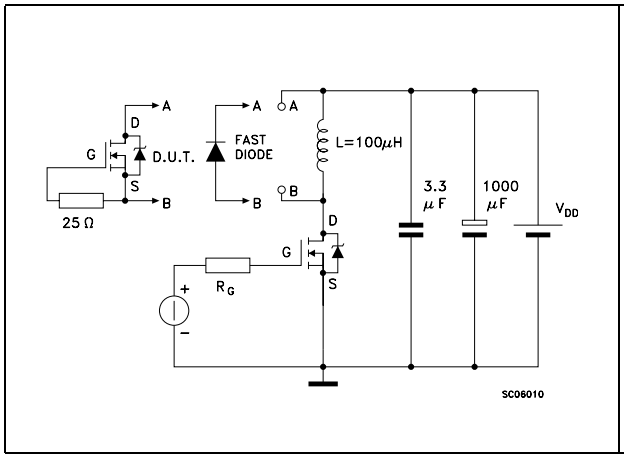


Figure 16. Unclamped Inductive load test circuit

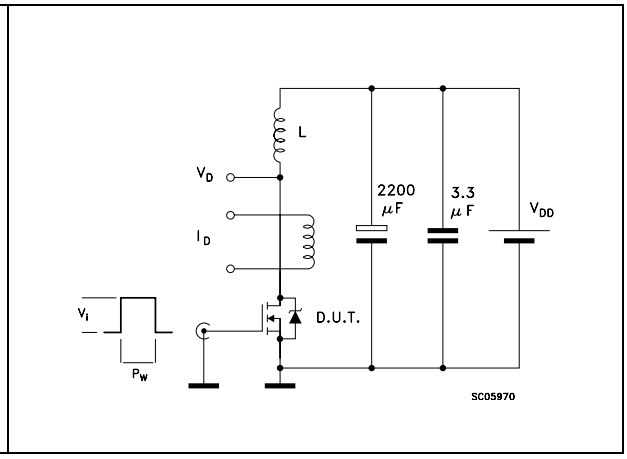


Figure 17. Unclamped inductive waveform

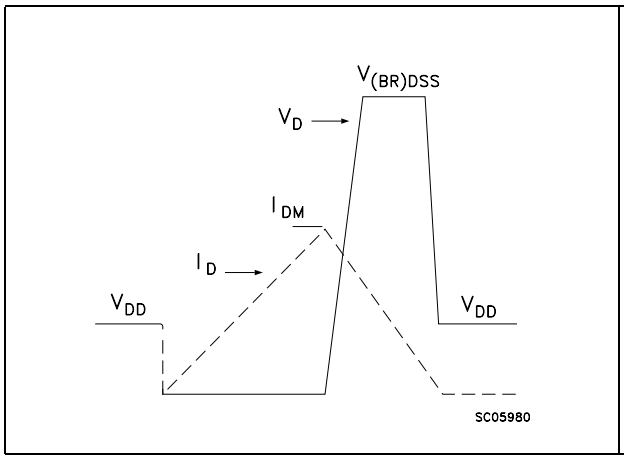
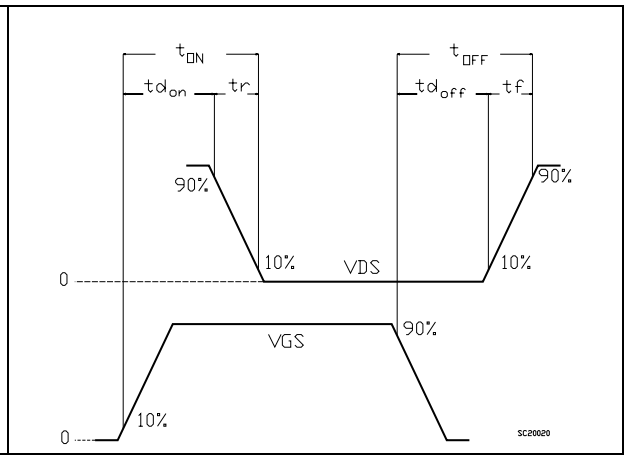


Figure 18. Switching time waveform

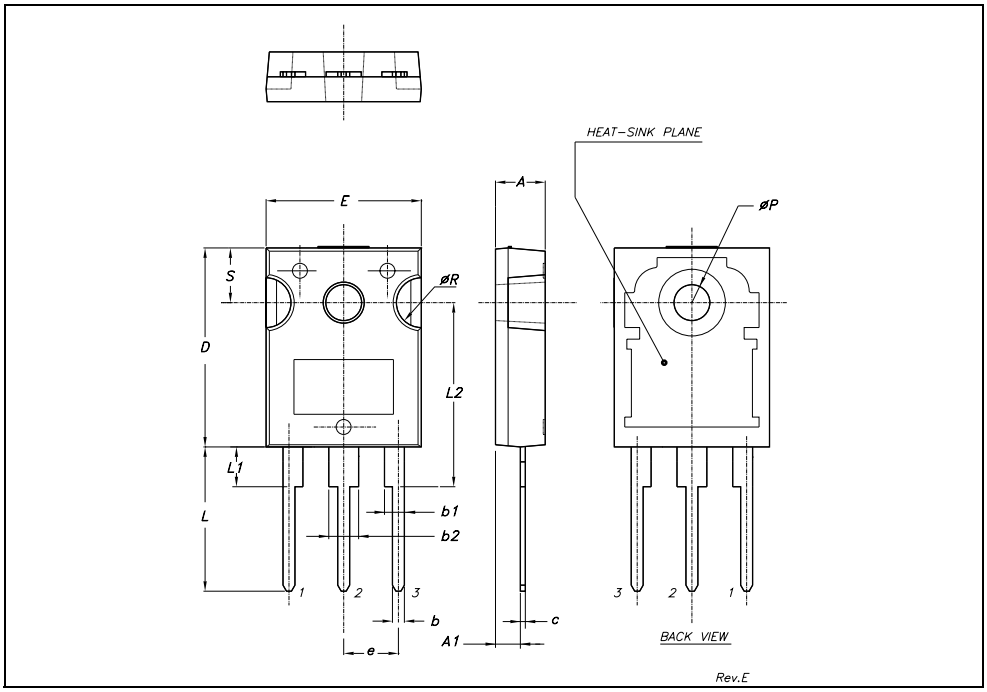


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



5 Revision history

Table 8. Revision history

Date	Revision	Changes
21-Jun-2004	3	Complete document
17-Oct-2006	4	New template, no content change

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