AN2482
Application note

PCLT (Programmable current limited termination)

Introduction

The purpose of this document is:

- To describe the PCLT behavior (refer also to data sheet)
- To give useful recommendations to achieve robust PCLT designs regarding EMI test (IEC 61000-4-5 and 4-4)
- To give information on thermal behavior of PCLT in its application
- To describe the demonstration board and recommendations for use

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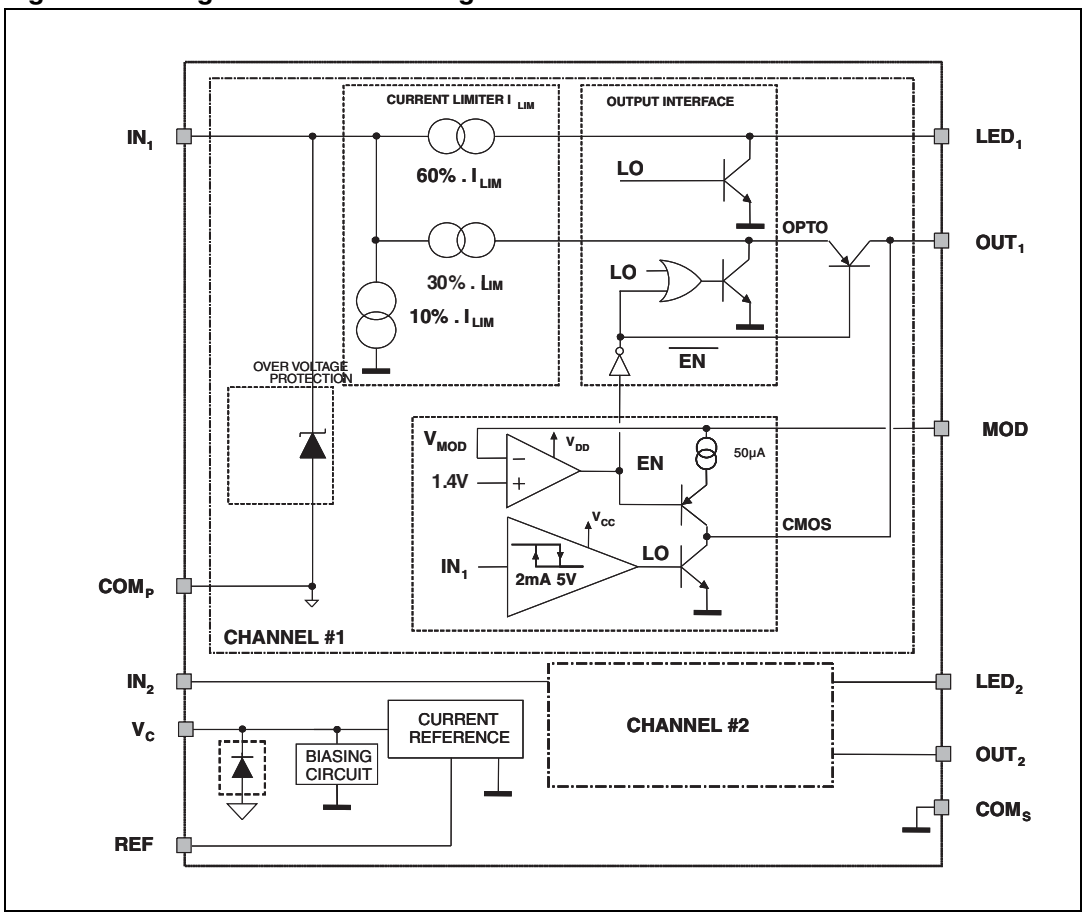
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1 PCLT Description

1.1 Main features

The PCLT (programmable current limited termination) is a dual input digital active termination device designed for 24 V DC input modules used in industrial automation. Each channel circuit terminates the connection between a high side proximity sensor and the I/O module.

Figure 1. Single channel bock diagram



The advanced features of the PCLT compared to the CLT3 are:

- The current limiter circuit can be programmed through an external resistance R_{REF} to meet type 2 (7.5 mA), type 3 and type 1 (2.5 mA) characteristics as specified in IEC 61131-2 standard.
- The possibility to drive either opto-couplers for isolated circuit or CMOS 3.3 V to 12 V for unisolated circuit.
- The additional outputs to drive status LEDs.

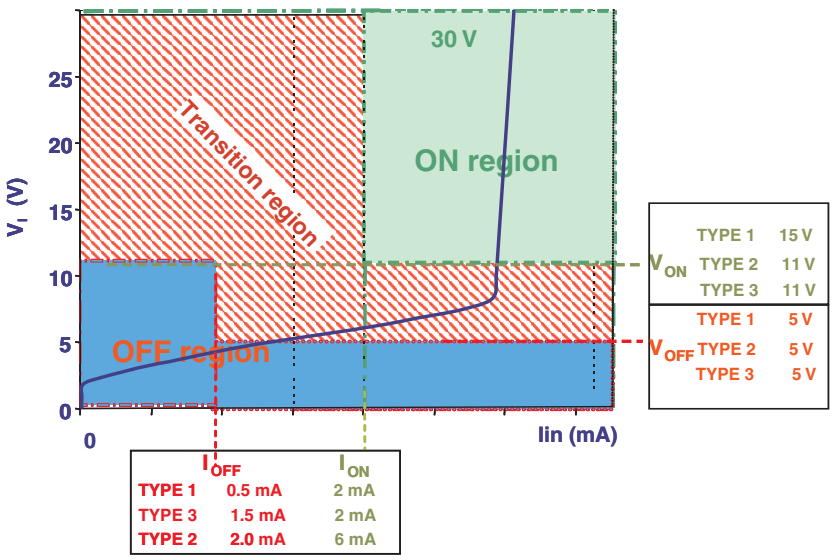
The PCLT also features an input voltage protection. This input protection makes this device robust against electromagnetic interferences as defined in IEC 61000-4-x standards: ESD, fast transient bursts, and voltage surges.

It is housed in a very low R_{TH} exposed pad surface mount TSS0P14 package to reduce the printed board size and the cooling pad.

1.2 Operating modes

Figure 2. gives the input limits and operating ranges defined by IEC 61131-2 standard and a typical PCLT characteristic.

Figure 2. EC61131-2 operating regions and PCLT2 characteristic



In accordance with IEC 61131-2 standard, for both opto-coupler and CMOS configuration modes, when the input current is less than 2 mA (type 2) or 1.5 mA (type 3) the output circuits divert all the input current and maintain both LED and output in OFF state (V_{OL} < 0.1 V for V_{MOD} = 0 and 20% V_{MOD} for V_{MOD} > 2.9 V).

When the module input voltage V_I (type 2), including the 750 Ω input resistor and the reverse diode (see *Figure 4.*), is higher than 11 V, i.e. the PCLT input voltage V_{IN} is higher than 5 V, both LED and output circuits are in ON states. The input current is then shared between the COMs (about 10%), the LED (about 60%), and the OUT (about 30%) pins in case of opto-coupler mode.

In CMOS mode, the CMOS output level is defined by the V_{MOD} voltage supplied by the external supply voltage V_{DD} of the bus controller. It can be in the range of 3.3 to 12 V. The output voltage is delivering 80% of V_{DD} for ON state and 20% of V_{DD} for OFF state.

When no LED diode is used, the LED outputs pin must be connected to the ground COM_P to allow the current to flow back to the power supply.

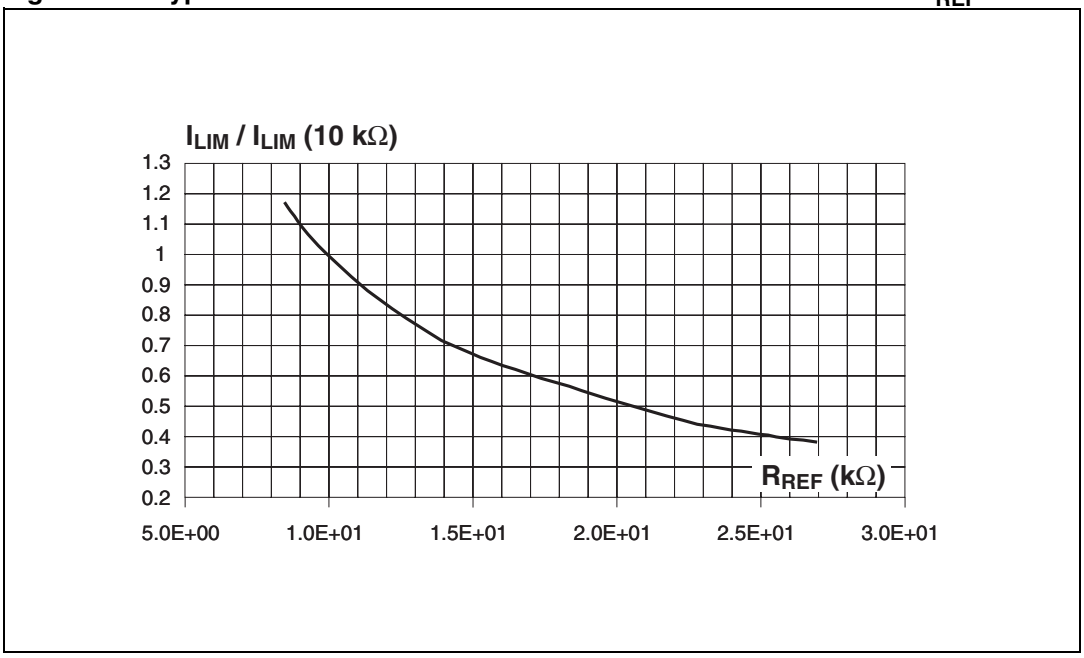
1.3 External biasing resistor settings

The PCLT operation mode can be set to the various logic input types defined by the IEC 61131-2 standard. The current reference of the input-limiting block of each channel is programmable by means of an external resistor R_{REF}. Moreover, because the operating current range is different for each type, the external input resistor R_I can be changed to improve the over-voltage robustness of the whole circuit. *Table 1.* defines the setting resistances for the types 1, 2, and 3 and the corresponding performances of the PCLT input and *Figure 3.* shows the current limiter variation versus the R_{REF} biasing resistor.

Table 1. Setting table

Type		1	3	2
Setting	**Unit**			
R_{REF}	KΩ	22		10
R_I	KΩ	2.2	1.2	0.75
R_C	KΩ	2.2		
Performances				
$I_{IN\ MIN}$	mA	2.2		6
$I_{IN\ TYP}$	mA	3		7.1
$I_{IN\ MAX}$	mA	4		8.5
$I_{LED\ TYP}$	mA	1.9		4
Surge with R_I	kV	1		0.5
ESD with R_I	kV	8 in contact, 15 in air (class4)		

Figure 3. Typical current limiter variation versus reference resistance R_{REF}



1.4 Protection against reverse polarity of power supply

A reverse diode should be connected between the module ground connection and the common pin COM of the PCLT2A device to protect the module against spurious reverse supply connection (refer to IEC 6131-2 section 5.3.3.1)

1.5 Opto-coupler and CMOS modes

The voltage V_{MOD} applied to the selector pin MOD allows the output OUT to be configured either in an opto-coupler driver mode (V_{MOD} < 0.75 V) (see *Figure 4.*) or in a CMOS output mode able to interface directly a bus controller circuit (V_{MOD} > 2.9 V) (see *Figure 5.*).

In CMOS mode, the V_{MOD} pin activates a CMOS compatible buffer output able to source a minimum current of 35 µA powered by the MOD pin.

Figure 4. Isolated digital input diagram with opto-coupler driving output

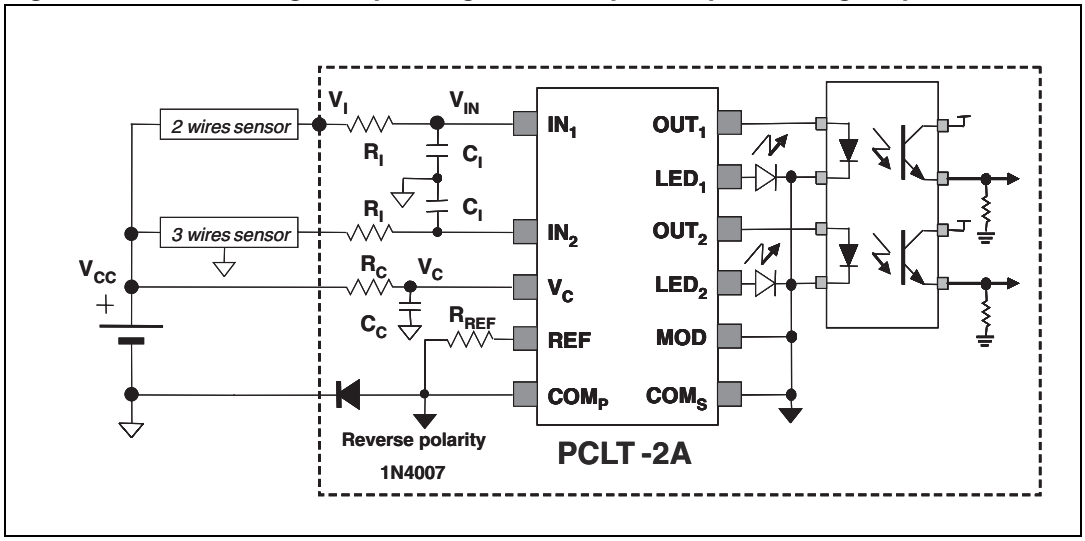
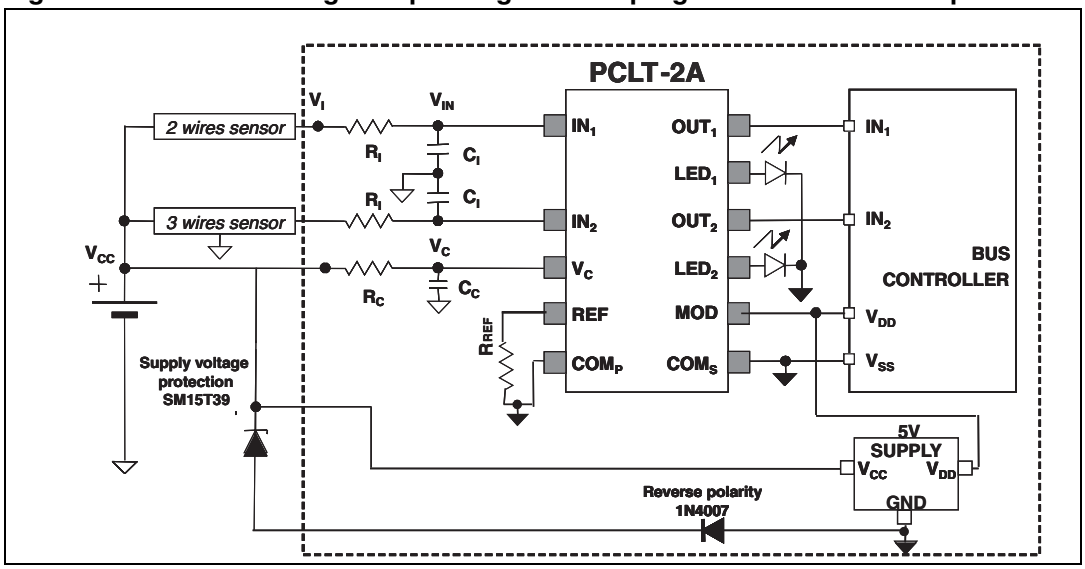


Figure 5. Unisolated digital input diagram with programmable CMOS output



2 Thermal dissipation calculation

2.1 Normal forward polarity of all inputs case

Referring to the PCLT diagram defined in *Figure 1.*, the dissipated power for both configurations can be calculated as follows:

$P_{OPTO_MODE} = V_C \cdot I_C + 2(V_{IN_LED} \cdot 0.6 \cdot I_{IN} + V_{IN_OUT} \cdot 0.3 \cdot I_{IN} + V_{IN} \cdot 0.1 \cdot I_{IN})$ if $V_{MOD} < 0.75V$

$P_{CMOS_MODE} = V_C \cdot I_C + V_{MOD} \cdot I_{DD} + 2(V_{IN_LED} \cdot 0.6 \cdot I_{IN} + V_{IN} \cdot 0.4 \cdot I_{IN})$ if $V_{MOD} > 2.9V$

$V_{IN} = V_{CC} - V_{SENSOR} - R_{IN} \cdot I_{IN}$ *where* V_{SENSOR} is the voltage drop of the input sensor

$V_{IN_OUT} = V_{IN} - V_{OUT}$ *where* V_{OUT} is the forward voltage drop of the opto coupler input

$V_{IN_LED} = V_{IN} - V_{LED}$ *where* V_{LED} is the forward voltage drop of the LED

The worst case scenario occurs when I_{IN} and I_{CC} are maximum (values are given in the datasheet):

$I_{IN_MAX} = 8.8mA$

$I_{C_MAX} = 2.0mA$

and when the voltage drops between PCLT input and output or LED_output.

With the conditions V_{CC} = 30 V, R_{REF} = 10 kΩ, V_{SENSOR} = 0 V, V_{OUT} = 0.9 V, R_{IN} = 750 Ω, and V_{OUT_LED} = 1.5 V

$P_{OPTO_MODE} = 430mW$

$P_{CMOS_MODE} = 440mW$

But this normal forward input polarity is not the worst case of PCLT power dissipation. See the next section.

2.2 Reverse polarity on a single input case

Each input of the PCLT circuit may be biased to a reverse polarity equal to - V_{CC}. This case corresponds to a connection mistake or a reverse biasing that is generated by the demagnetization of a **monitored** inductive solenoid.

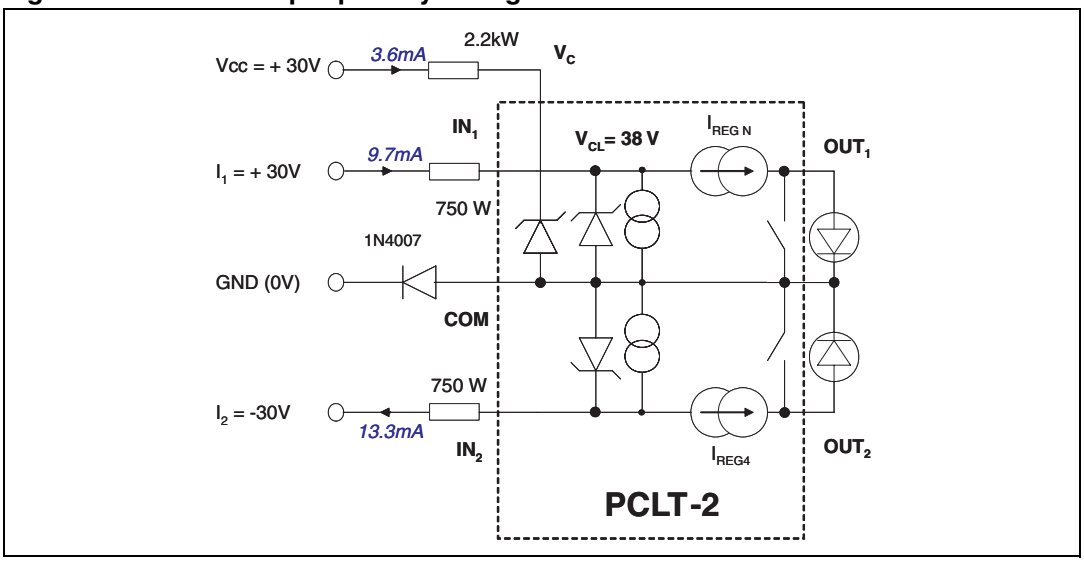
The involved input can withstand a high reverse current up to 20 mA. Its corresponding opto-coupler output is then OFF and is protected by the clamping input diode. The **other** input remains operational, and some power is dissipated in their clamping protections.

The losses in reverse input polarity configuration (see *Figure 6.*) are:

$Pdis_PCLT = P_{TOTdelivered} - P_{dis_RC} - P_{dis_RIN1} - P_{dis_RIN2}$

$Pdis_PCLT = 566mW$

Figure 6. Reverse input polarity configuration

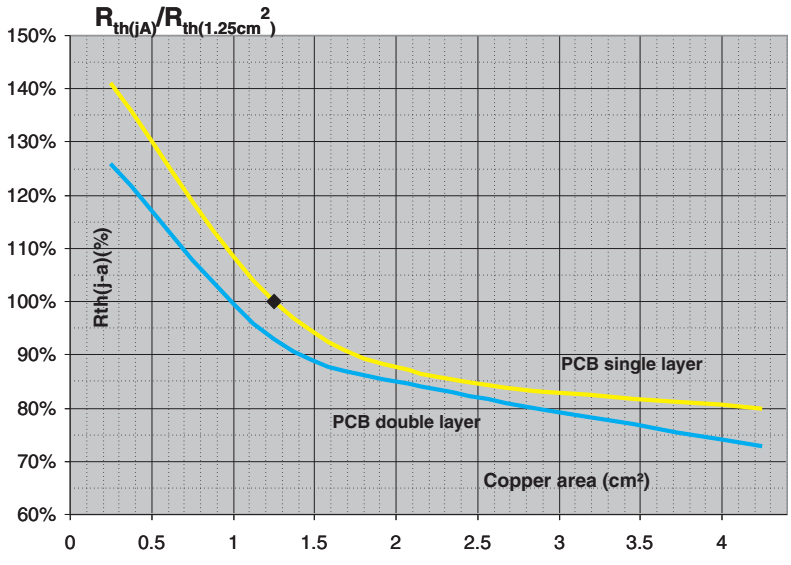


Taking into account this dissipated power worst case (reverse polarity on a single input) and with an ambient temperature of 85° C the thermal resistance must be lower than 115° C/W. The PCLT datasheet specifies a 100° C/W $R_{TH(JA)}$ with a copper area of 1.25cm^2 ensuring a safer cooling.

2.3 R_{TH} adjustment with PCB area

Figure 7. gives the relative junction to ambient thermal resistance as a function of the copper surface used as a heat sink (FR4 epoxy PCB, 35 µm for the thickness of the copper). The R_{THJA} can be deceased down to100° C/W with a 1.25 cm² copper area.

Figure 7. Thermal resistance variation versus copper area (35 µm layer thickness; 50 vias/cm^2 and 300 µm diameter in double layer)

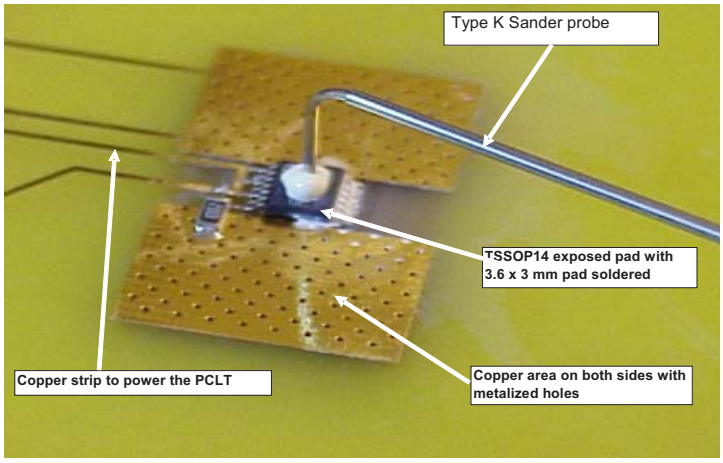


2.4 Experimental T_j measurement

The purpose is to estimate easily and experimentally the junction temperature T_J from the case temperature T_C measurement.

The case temperature is measured here with a Sander probe (K type, rounded contact, area 500 µm) as shown on *Figure 8.*

Figure 8. T_{CASE} measurements

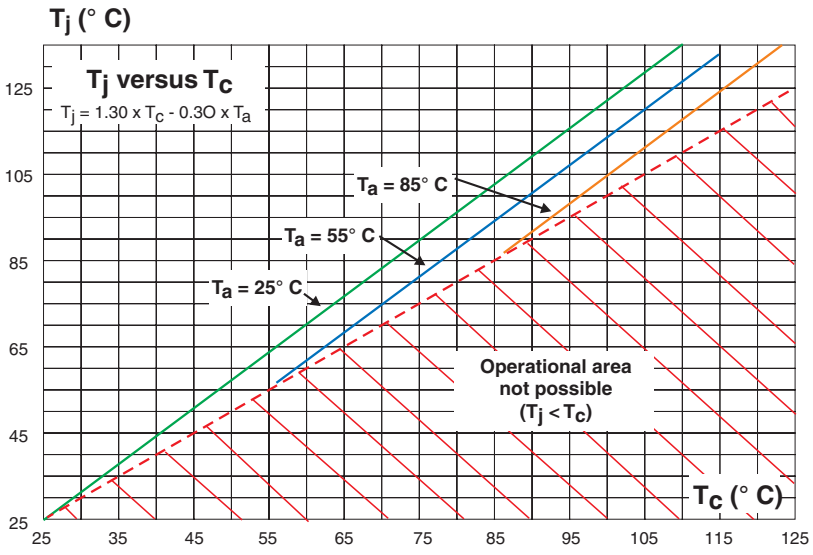


The PCLT has been submitted to two representative powers (380 mW and 670 mW), it has been soldered on different copper area sizes from 0.1 cm^2 (exposed pad size) to 2 cm^2 per side. The case and junction temperatures have been measured at three room temperatures, +25° C, +55° C and +85° C using only natural convection.

The junction temperature is calculated by means of an input diode protection used as a temperature sensor.

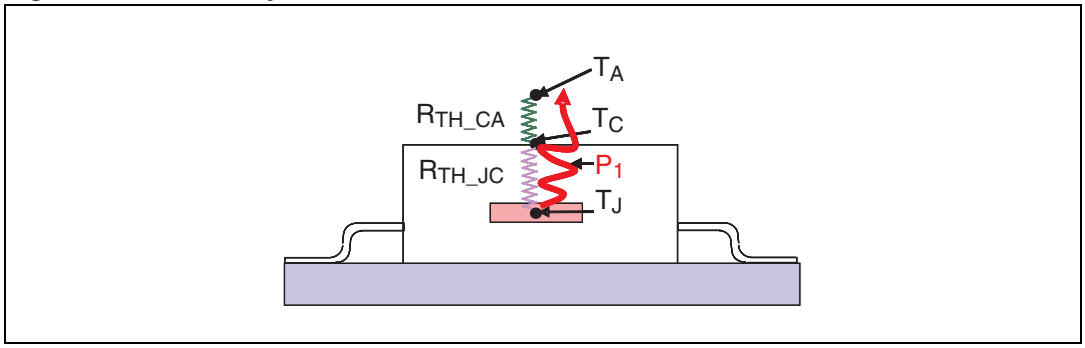
According to these experimental results, *Figure 9.* gives an evaluation of the junction temperature as a function of the case temperature for three ambient temperatures.

Figure 9. Junction temperature versus case and ambient temperatures



Junction and ambient temperatures can be found from the assembly model shown in *Figure 10.*

Figure 10. Assembly model



T_J = junction temperature
T_A = ambient temperature
T_C = case temperature

$$T_J - T_A = P_1\left(R_{TH_JC} + R_{TH_CA}\right)$$
$$T_J - T_C = P_1\left(R_{TH_JC}\right)$$
$$T_J = T_C + \left(T_J - T_A\right)\frac{R_{TH_JC}}{\left(R_{TH_JC} + R_{TH_CA}\right)}$$
$$T_J = T_C\left(1 + \frac{R_{TH_JC}}{R_{TH_CA}}\right) - T_A\frac{R_{TH_JC}}{R_{TH_CA}}$$

assu min *g* : $\frac{R_{TH_JC}}{R_{TH_CA}} = 0.30$ in accordance to the experimental results, the relation becomes :

$$T_J = 1.30 \bullet T_C - 0.30 \bullet T_A$$

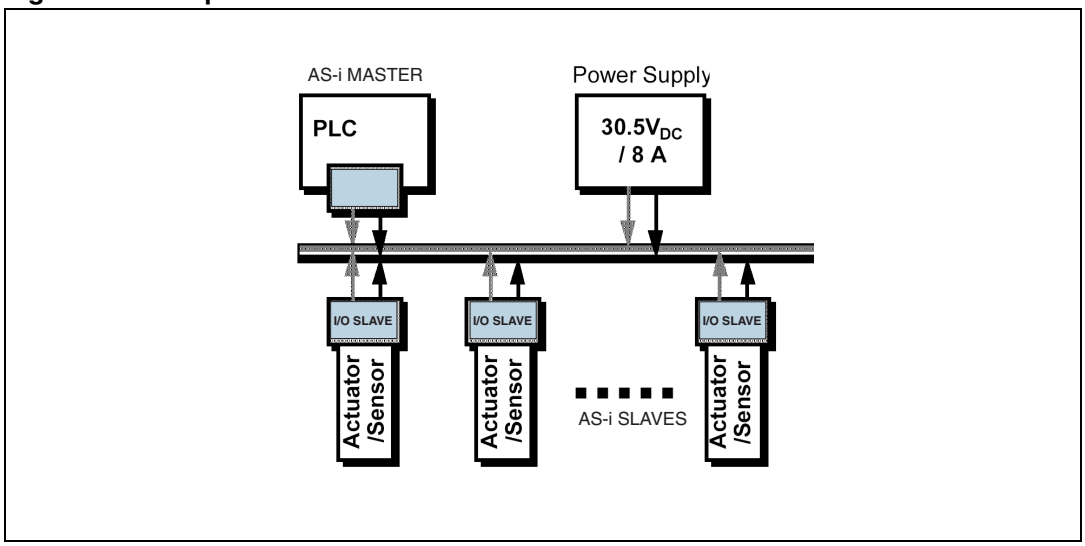
The accuracy of the T_J results are in the range of 5%

3 Unisolated AS-interface bus application

3.1 Application overview

The AS-Interface bus is a low-end field bus for actuators and sensors in manufacturing and industrial automation. Its electrical architecture uses an unshielded 2-wire yellow cable that transports both the 24 V power supply of the field nodes and the serial bidirectional data communication.

Figure 11. Simplified architecture of AS-interface Bus



The data communication is achieved with a current carrier modulation superimposed over the power wires. Therefore, the power bus terminals are filtered in order to maintain identical and calibrated differential and common mode impedances measured by both master and slave units.

3.2 Isolation of the sensor section and the supply from data/supply bus

The PCLT can be designed as an interface between a proximity sensor and its associated slave controller unit.

The sensor power supply is generated from the bus power supply with a filter and a regulator that are inserted in the slave unit. In the same manner, the sensor logic signal is isolated from the AS-Interface power supply bus to avoid any degradation of the data transmission.

A conventional way to achieve the interface with the PCLT and the AS-Interface controller is to insert an opto-coupler between the AS-Interface controller and the PCLT that runs in opto-coupler mode as shown on *Figure 4.* (MOD pin grounded).

3.3 Un-isolated connection of the PCLT with AS-Interface controller

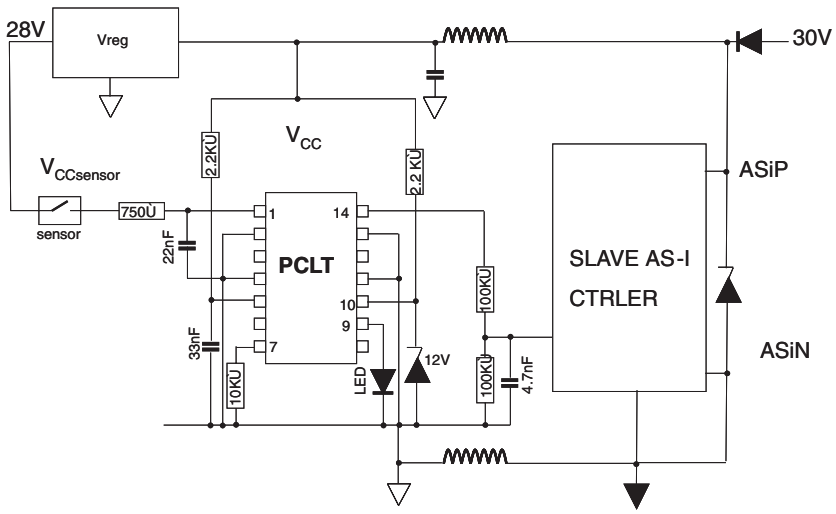
To remove the opto-coupler in lower cost versions, the operation of the PCLT has been extended to fit the AS-Interface application. A precaution is required on its interface with the bus controller: the impedance between the two circuits must be high in order to maintain the isolation.

To achieve this isolation impedance level, the PCLT runs in CMOS mode (MOD = V_{CC}) and the buffer operation is extended up to V_{CC} = 12 V. In the application, the V_{CC} voltage is generated with a Zener diode reference fed from the sensor bus.

Because of the buffer voltage increase, it becomes possible to insert a high impedance between the PCLT output and the AS-Interface bus controller input. Typically a 100 kΩ resistor is designed while keeping a 5 V CMOS operation on the input of the bus controller.

Figure 12. shows the application diagram where the PCLT is connected to the slave bus controller through a 100 kΩ resistor. The logic signal is transmitted with a low level of less than 20% of the V_{DD} supply voltage and a high level of at least 3.5 V. This high level is defined by the voltage drop across the 100 kΩ pull down resistor. (35 µA times 100 kΩ).

Figure 12. Un-isolated AS-Interface slave controller unit using the PCLT



4 Electromagnetic compatibility (EMC) requirements

The input and supply pins are designed to withstand electromagnetic interferences. They are protected by a clamping diode that is connected to the COM_P common pin. Combined with the serial input resistance R_I, this clamping diode is effective against the fast transient bursts (±4 kV, IEC 61000-4-4) and the voltage surges (±1kV, IEC 61000-4-5).

EMC test procedures are fully described in AN1608 CLT3-4BT6 application note. Refer to it to get detailed information. It covers IEC 61000-4.2 standard for ESD tests, IEC 61000-4.4 standard for fast transient burst tests, IEC 61000-4.5 standard for surge tests, IEC 61000-4-6 standard for conducted disturbance tests.

IEC 61131-2 standard for programmable controllers specifies (see section 7.3.3 of the standards document) a low profile requirement for digital inputs with:

- High energy Surge = 0.5 kV
- Fast Transient Burst = 1 kV
- Electrostatic Discharge = 4 kV
- Radio Frequency Interference = 3 V_{rms}.

But designers are requiring now improved robustness levels:

- 4 kV EFT burst;
- 500 V at least in surge
- ESD 15 kV air
- 10V_{rms} for conducted RFI.

The PCLT demo board described here sustains the levels given on *Table 2.*

Table 2. PCLT Immunity tests results

<table>
<tr><th rowspan="2"></th><th colspan="3">Minimum requirements of international standards</th><th colspan="4">Robustness of the PCLT demo board</th></tr>
<tr><th colspan="2">Test conditions</th><th>Levels</th><th colspan="2">Tests conditions</th><th>Levels</th><th>behavior of the PCLT</th></tr>
<tr><td rowspan="2">ESD test
IEC61000-4-2</td><td colspan="2">Air discharge</td><td>±8 kV</td><td colspan="2">R_C = 2.2 kΩ
R_{IN} = 750 Ω</td><td>±15 kV</td><td rowspan="2">No failure,
no disturbance.</td></tr>
<tr><td colspan="2">Contact discharge</td><td>±4 kV</td><td colspan="2">R_C = 2.2 kΩ
R_{IN} = 750 Ω</td><td>±8 kV</td></tr>
<tr><td rowspan="2">Burst test
IEC61000-4-4</td><td colspan="2">Analog Input</td><td>±1kV</td><td>R_{IN} = 750 Ω</td><td>C_{IN} = 22 nF
C_C =33 nF</td><td rowspan="2">±4 kV</td><td rowspan="2">No failure,
no disturbance.</td></tr>
<tr><td colspan="2">DC power line</td><td>±2 kV</td><td>R_C = 2.2 kΩ</td><td></td></tr>
<tr><td rowspan="4">Surge test
IEC61000-4-5</td><td rowspan="2">Analog Input</td><td rowspan="2">42 Ω: 0.5 µF differential and common mode</td><td rowspan="2">±0.5 kV</td><td rowspan="2">Analog Input</td><td>R_{IN} = 750 Ω</td><td>±0.5 kV</td><td rowspan="4">No failure,
temporary disturbance.</td></tr>
<tr><td>R_{IN} = 1.2 kΩ</td><td>±1 kV</td></tr>
<tr><td rowspan="2">dc power line</td><td>2 Ω; 18 µF differential mode</td><td>±0.5 kV</td><td rowspan="2">dc power line</td><td rowspan="2">R_C = 2.2 k</td><td>±1 kV</td></tr>
<tr><td>12 Ω; 9 µF common mode</td><td>±1 kV</td><td>±1 kV</td></tr>
<tr><td>Conducted disturbance test
IEC61000-4-6</td><td>150 kHz to 80 MHz</td><td>22 nF capacitors</td><td>3 V_{rms}
AM±80%</td><td>150 kHz to 80 MHz</td><td>R_{IN} = 750 Ω
C = 22 nF
At the input</td><td>10 V_{rms}
AM±80%</td><td>No failure,
No disturbance.</td></tr>
<tr><td>Reverse input polarity test</td><td colspan="3">-V_{cc} applied to one input during 10 s</td><td colspan="3">-30 V_{dc} applied to one input,
+30 V_{dc} on the others</td><td>No failure</td></tr>
</table>

5 Demo board

5.1 Description of the PCLT-2A demo board

This demonstration board allows the PCLT evaluation. It can be easily inserted in a real application, between sensors and digital bus controller. The LEDs monitors the logic state of each PCLT input.

The demonstration board schematics are shown on *Figure 13.* and *Figure 14.* It has been designed to present both opto-coupler and CMOS modes for type 2. The bill of material is given in *Table 3.*

For the opto-coupler driving mode, the PCLT pin 10 has been grounded, while for the CMOS driving mode the user has to supply the PCLT pin 10 through the OUTPUT_B connector.

The copper surface under the CLT device improves the thermal dissipation capability of the exposed pad TSSOP14 package. The copper area (cooling pad) on the PCB demo board is around 1cm², this decreases the package R_{THJA} below 110° C/W.

Figure 13. Electrical diagram of opto-coupler diving mode

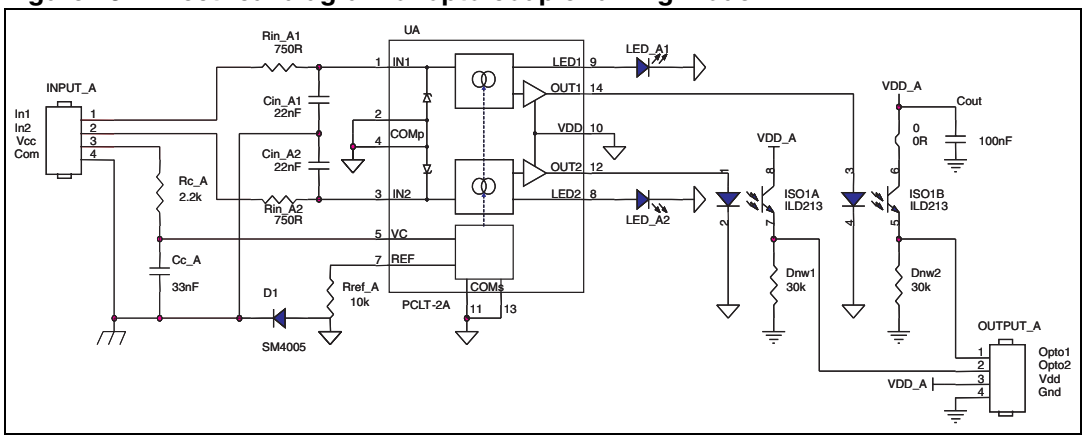


Figure 14. Electrical diagram of CMO driving mode

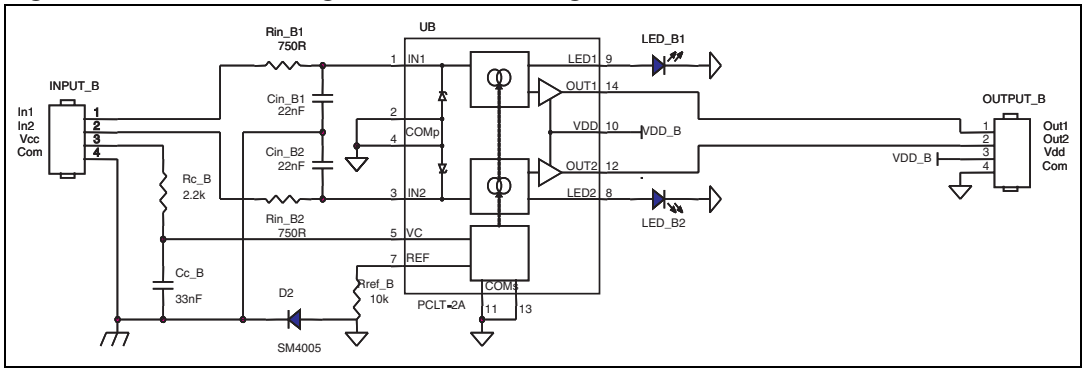


Table 3. Bill of material

Item	Quantity	Reference	Part	Package / comments
1	4	$R_{IN_}(A_1, A_2, B_1, B_2)$	750 ±1%	CMS MMB0207
2	2	$R_{C_}(A, B)$	2.2k ±1%	CMS MMB0207
3	2	$R_{REF_}(A, B)$	10k ±1%	CMS 0805
4	4	$C_{IN_}(A_1, A_2, B_1, B_2)$	22n ±5%	CMS 0805
5	2	$C_{C_}(A, B)$	33n ±5%	CMS 0805
6	1	C_{OUT}	100n ±5%	CMS 0805
7	2	D1, D2	BYD17J	CMS SOD-80
8	2	$D_{NW}(1, 2)$	33k ±%	CMS 1206
9	1	0_R	0 ±5%	CMS 1206
10	4	$LED_(A_1, A_2, B_1, B_2)$	Green	CMS PLCC-2
11	1	Opto-coupler	ILD213	SOIC-8
12	4	Bent connectors (INPUT_(A, B),OUTPUT_(A, B)	4 pins/connector	Bottom assembly
13	2	PCLT-2A	PCLT2A	TSSOP14
14	4	Nylon spacer		

5.2 Operating instructions of the PCLT-2A demo-board

This section provides some basic advice on using the demonstration board to evaluate the PCLT product.

5.2.1 Input connectors

The INPUT_A, INPUT_B connectors give access to:

- the 2 input signals of the module (In1, In2)
- the PCLT power supply (V_{CC} and Com_A, Com_B).

It is then easy to connect this module directly to any type of sensor, especially those specified by the EN60947-5-2 standard.

The V_{cc} power supply is typically 24 V DC (30 V max).

5.2.2 Output connectors

The OUTPUT_A connector gives access to:

- the 2 opto-coupler outputs of the module (Opto1, Opto2)
- the opto-coupler collector power supply (V_{dd} and Gnd) which is typically 5 V DC (this voltage has to be compatible with micro controllers being used; 12 V max).

It is then easy to connect the output of the module directly on a digital bus controller.

The OUTPUT_B connector gives access to:

- the 2 PCLT2 CMOS compatible outputs (out1, out2)
- the VDD supply (V_{dd} and Com), which is typically 5 V DC, can be in the range from 3.3 V to 12 V (This voltage has to be compatible with micro controllers being used)

This application allows a direct CMOS compatible connection to the digital bus controller but without any galvanic isolation.

5.2.3 Schematics components

The 22 nF input capacitors are used in order to improve the noise immunity of the whole module. Their function is to filter the high frequency electrical noise, and to secure the off state of the module.

Adding a 33 nF capacitor on V_C pin ensures high immunity against electrical noise such as the one described in the IEC 61131-2 standard.

The input resistors are used to limit the current that could appear in case of voltage surge clamped by the PCLT. These resistors can then withstand the high over voltage that may be applied to the module during surge tests.

The LEDs resistor value shall be set according to the input power supply value used, and the normal current of displaying LEDs. A resistor array can be used to control these low power LEDs (reduction of the PCB size).

The D1 diode used between the COM of the input power supply, and the COM of the PCLT-2A device can be a general purpose component such as a 1000 V, 1 A rectifier.

The opto-coupler must be chosen according to its input diode drop voltage. This drop voltage must not disturb the operation of the PCLT (see PCLT datasheet, “Absolute ratings table” for more details about V_{OM}).

Figure 15. Demo board assembly - top view

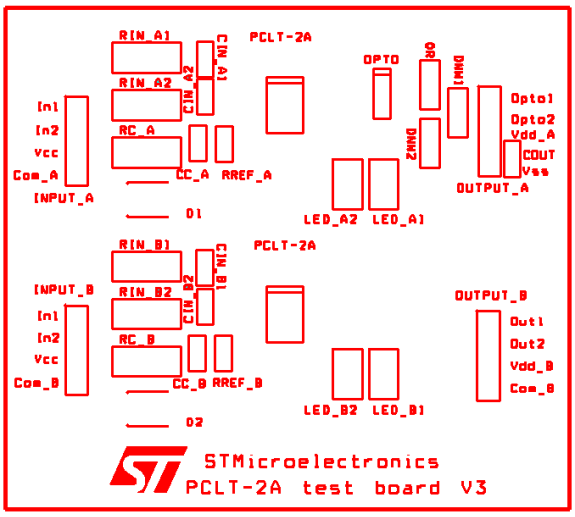
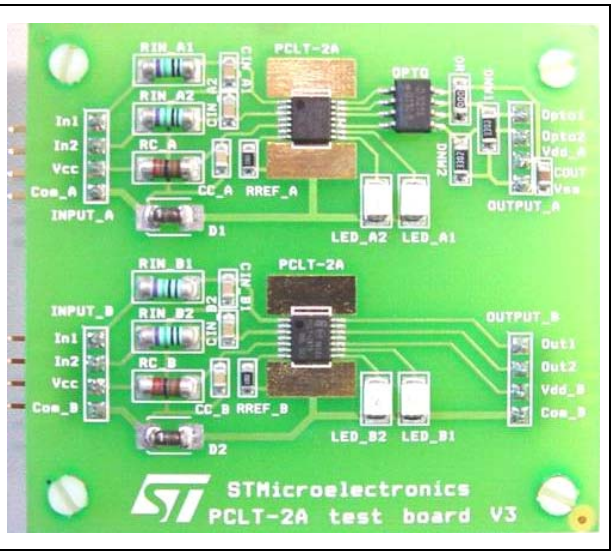


Figure 16. Demo board photograph



6 Conclusion

This application note illustrates how designers can maximize PCLT performance in its application especially in the field of thermal behavior and EMI robustness.

Designed for I/O module in factory automation, the PCLT is a low-loss EMI-proof solution showing high usage flexibility. Designers can develop a wide variety of input types in isolated and un-isolated versions.

To illustrate PCLT performance and advantages, a bread board is also proposed with an optimized lay-out.

With its robust protection and its current limiter, the PCLT is a low-loss EMI-proof solution for highly integrated module interfacing with proximity sensors.

7 Revision history

Date	Revision	Changes
08-Feb-2006	1	Initial release.

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