TLIN1441-Q1 Automotive Local Interconnect Network (LIN) Transceiver with Integrated Voltage Regulator and Watchdog

1 Features

- AEC Q100: Qualified for Automotive Applications
  - Device Temperature Grade 1: –40°C To 125°C T_A
- Local Interconnect Network (LIN) Physical Layer Specification ISO/DIS 17987–4.2 Compliant and Conforms to SAEJ2602 Recommended Practice for LIN
- Supports 12 V Applications
- Integrated Watchdog Supervisor Configurable by Pin or SPI
- Wide Operating Ranges
  - 5.5 V to 28 V Supply Voltage
  - ±42 V LIN Bus Fault Protection
  - LDO output supporting 3.3 V (TLIN14413-Q1) or 5 V (TLIN14415-Q1)
  - Sleep Mode: Ultra-Low Current Consumption Allows Wake Up Event From:
    - LIN Bus
    - Local Wake Up through EN
    - Local Wake Up through WAKE
  - Power Up and Down Glitch Free Operation
- Protection Features:
  - ESD Protection
  - Under Voltage Protection on V_{SUP}
  - TXD Dominant Time Out (DTO) Protection
  - Thermal Shutdown Protection
  - Unpowered Node or Ground Disconnection Failsafe at System Level
- V_{CC} sources 125 mA with 12 V_{SUP} at 100°C
- Available in Leadless VSON (14) Package with Improved Automated Optical Inspection (AOI) Capability

2 Applications

- Body Electronics and Lighting
- Hybrid, Electric and Power Train Systems
- Infotainment and Cluster
- Appliances

3 Description

The TLIN1441-Q1 is a Local Interconnect Network (LIN) physical layer transceiver with an integrated low dropout voltage regulator, wake up and protection features and is compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4.2 standards. The TLIN1441-Q1 integrates a window or timeout based watchdog supervisor that is PIN or SPI configurable and controlled. The TLIN1441-Q1 watchdog is controlled by PIN strapping or SPI depending upon the state of pin 9 at power up.

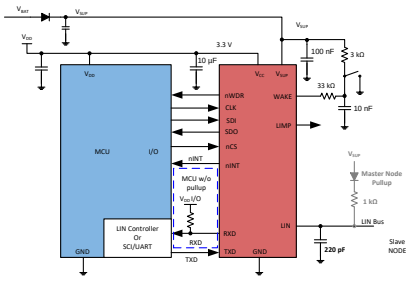
LIN is a single-wire bidirectional bus typically used for low speed in-vehicle networks using data rates up to 20 kbps. The LIN receiver supports data rates up to 100 kbps for end-of-line programming. The TLIN1441-Q1 converts the LIN protocol data stream on the TXD input into a LIN bus signal using a current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The receiver converts the data stream to logic level signals that are sent to the microprocessor through the open-drain RXD pin.

Device Information[1]

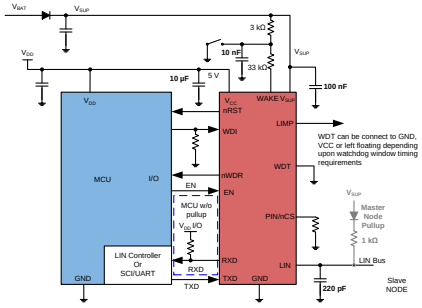
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLIN1441-Q1	VSON (14)	3.00 mm x 4.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematics, SPI Mode



Simplified Schematics, Pin Mode



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2018) to Revision A	Page
• Changed the document status From: *Advanced Information* To: *Production* data	1

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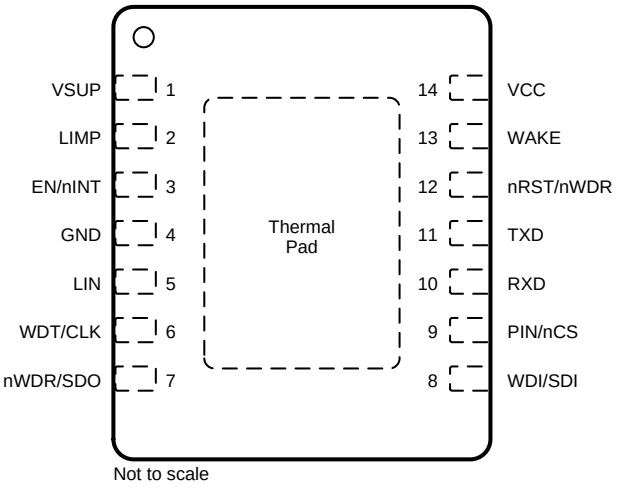
5 Description (continued)

Ultra-low current consumption is possible using the sleep mode which allows wake up via LIN bus or pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode. No external pull-up components are required for slave applications. Master applications required an external pull-up resistor (1 kΩ) plus a series diode per the LIN specification.

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6 Pin Configuration and Functions

DMT Package
14-Pin (VSON)
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V_{SUP}	HV Supply In	Device supply voltage (connected to battery in series with external reverse blocking diode)
2	LIMP	HV O	Used for LIMP home, watchdog event causes this pin to switch V_{SUP}
3	EN/nINT	D I/O	Enable Input when in Pin Mode/Processor Interrupt when in SPI Mode (open drain) - when EN - Enable input - Setting pin high place device into normal mode and setting low is sleep mode
4	GND, PAD	GND	Ground
5	LIN	HV I/O	LIN bus single-wire transmitter and receiver
6	WDT/CLK	D I	Programmable watchdog window set input (3 levels)/SPI Clock input
7	nWDR/SDO	D O	Watchdog output trigger when in Pin Mode / SPI Slave Data Output when in SPI Mode
8	WDI/SDI	D I	Watchdog timer trigger input active on both rising and falling edges when in Pin Mode (Must be driven at all times) /SPI Slave Data Input when in SPI Mode
9	PIN/nCS	D I	Watchdog Configuration Control Set at Power Up. When tied to GND at power up device is in Pin Mode. When High or in Z-State device is in SPI Mode and this pin becomes Chip Select
10	RXD	D O	RXD output (open-drain) interface reporting state of LIN bus voltage
11	TXD	D I	TXD input interface to control state of LIN output
12	nRST/nWDR	D O	Reset output (active low)/Watchdog output trigger if programmed in SPI Mode (active low)
13	WAKE	HV I	High Voltage Local wake up pin active Low
14	V_{CC}	Supply Out	Output voltage from integrated voltage regulator

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7 Specifications

7.1 ABSOLUTE MAXIMUM RATINGS

over operating T_A temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage range (ISO/DIS 17987)	–0.3	42	V
V_{LIN}	LIN Bus input voltage (ISO/DIS 17987)	–42	42	V
V_{CC50}	Regulated 5 V Output Supply	–0.3	6	V
V_{CC33}	Regulated 3.3 V Output Supply	–0.3	4.5	V
V_{WAKE}	WAKE pin input voltage range	–0.3	42	V
V_{LIMP}	LIMP pin output voltage range	–0.3	42 and $V_O \leq V_{SUP}+0.3$	V
V_{nRST}	Reset output voltage	–0.3	V_{CC} + 0.3	V
V_{LOGIC_INPUT}	Logic input voltage	–0.3	6	V
V_{LOGIC_OUTPUT}	Logic output voltage	–0.3	6	V
I_{VCC}	V_{CC} supply current		300	mA
I_O	Digital pin output current		8	mA
$I_{O(nRST)}$	Reset output current	–5	5	mA
T_A	Ambient temperature	–40	125	°C
T_J	Junction temperature	–55	150	°C
Storage temperature, T_{stg}	Storage temperature range	–65	165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD RATINGS

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) classification level H2, V_{SUP}, LIN, and WAKE, per AEC Q100-002(1)		±8000	V
		Human body model (HBM) classification level 3A, all other pins, per AEC Q100-002(1)		±4000	
		Charged device model (CDM) classification level C5, per AEC Q100-011	All pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 ESD RATINGS, IEC SPECIFICATION

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (1), LIN, V_{SUP} terminal to GND(2)	IEC 61000-4-2 contact discharge	±8000	V
		IEC 61000-4-2 air-gap discharge	±15000	
	Powered electrostatic discharge SAEJ2962-1(3)	SAEJ2962-1 contact discharge	±8000	V
		SAEJ2962-1 air discharge	±15000	
Transient	ISO7637-2 and IEC 62215-3 Transients according to IBEE LIN EMC test spec(4)	Pulse 1	-100	V
		Pulse 2a	75	
		Pulse 3a	-150	
		Pulse 3b	150	
Transient	ISO7637 Slow Transients Pulse	SAEJ2962-1(5) test spec and IBEE Zwickau	85	V

(1) IEC 61000-4-2 is a system-level ESD test. Results given here are specific to the IBEE LIN EMC Test specification conditions. Different system-level configurations may lead to different results
(2) Testing performed at 3rd party IBEE Zwickau test house, test report available upon request.
(3) SAEJ2962-1 Testing performed at 3rd party US3 approved EMC test facility, test report available upon request.
(4) ISO7637 is a system-level transient test. Results given here are specific to the IBEE LIN EMC Test specification conditions. Different system-level configurations may lead to different results.
(5) ISO7637 is a system-level transient test. Results given here are specific to the SAEJ2962-1 Test specification conditions. Different system-level configurations may lead to different results

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7.4 RECOMMENDED OPERATING CONDITIONS

over operating T_A temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage	5.5		28	V
V_{LIN}	LIN bus input voltage	0		28	V
V_{LOGIC5}	Logic pin voltage	0		5.25	V
$V_{LOGIC33}$	Logic pin voltage	0		3.465	V
$I_{OH(DO)}$	Digital terminal HIGH level output current	-2			mA
$I_{OL(DO)}$	Digital terminal LOW level output current			2	mA
$I_{O(LIMP)}$	LIMP output current			1	mA
$C_{(VSUP)}$	V_{SUP} supply capacitance	100			nF
$C_{(VCC)}$	V_{CC} supply capacitance; 500 µA to full load	1			µF
$C_{(VCC)}$	V_{CC} supply capacitance; no load to full load	10			µF
ESR_{CO}	Output ESR capacitance requirements	0.001		2	Ω
$\Delta t/\Delta V$	Input transition rise and fall rate (WDI, WDT, WDR)			100	ns/V
T_J	Operating junction temperature range	–40		150	°C

7.5 THERMAL INFORMATION

THERMAL METRIC(1)		TLIN1441x DMT 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 POWER SUPPLY CHARACTERISTICS

Over operating T_A temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT						
V_{SUP}	Operational supply voltage (ISO/DIS 17987 Param 10)	Device is operational beyond the LIN defined nominal supply voltage range See Figure 7 and Figure 8	5.5		36	V
V_{SUP}	Nominal supply voltage (ISO/DIS 17987 Param 10):	Normal and Standby Modes Normal Mode: Ramp VSUP while LIN signal is a 10 kHz square wave with 50 % duty cycle and 18 V swing. See Figure 7 and Figure 8	5.5		28	V
		Sleep Mode	5.5		28	V
UV_{SUPR}	Under voltage V_{SUP} threshold	Ramp Up		3.5	4.2	V
UV_{SUPF}	Under voltage V_{SUP} threshold	Ramp Down	1.8	2.1	2.5	V
U_{VHYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			1.5		V
I_{SUP}	Transceiver and LDO supply current	Transceiver normal mode dominant plus LDO output; where LDO load current is 125 mA			135	mA

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POWER SUPPLY CHARACTERISTICS (continued)

Over operating T_A temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SUPTRXDOM}$	Supply current transceiver only	Normal Mode: EN = V_{CC}, bus dominant: total bus load where R_{LIN} ≥ 500 Ω and C_{LIN} ≤ 10 nF		1.2	7.5	mA
		Standby Mode: EN = 0 V, bus dominant: total bus load where R_{LIN} ≥ 500 Ω and C_{LIN} ≤ 10 nF		1	2.1	mA
$I_{SUPTRXREC}$	Supply current transceiver only	Normal Mode: EN = V_{CC}, Bus recessive: LIN = V_{SUP},		450	775	µA
		Standby Mode: EN = 0 V, LIN = recessive = V_{SUP}		20	40	µA
		Added Standby Mode current through the RXD pull-up resistor with a value of 100 kΩ: EN = 0 V, LIN = recessive = VSUP, RXD = GND (1)			55	
$I_{SUPTRXSLP}$	Sleep mode supply current transceiver only	5.5 V < V_{SUP} ≤ 14 V, LIN = V_{SUP}, WAKE = V_{SUP}, EN = 0 V, TXD and RXD floating		9	15	µA
		14 V < V_{SUP} ≤ 28 V, LIN = V_{SUP}, WAKE = V_{SUP}, EN = 0 V, TXD and RXD floating		12	20	µA
REGULATED OUTPUT V_{CC}						
V_{CC}	Regulated output	V_{SUP} = 5.5 to 28 V, I_{CC} = 1 to 125 mA	–2%		2%	
$\Delta V_{CC(\Delta VSUP)}$	Line regulation	V_{SUP} = 5.5 to 28 V, ΔV_{CC}, I_{CC} = 10 mA			50	mV
$\Delta V_{CC(\Delta VSUPL)}$	Load regulation	I_{CC} = 1 to 125 mA, V_{SUP} = 14 V, ΔV_{CC}			50	mV
V_{DROP}	Dropout voltage	3.3 V and 5 V version, V_{SUP} – V_{CC}, I_{CC} = 125 mA; – 40 °C ≤ T_J ≤ 105 °C		300	600	mV
UV_{CC5R}	Under voltage 5 V V_{CC} threshold	Ramp Up		4.7	4.9	V
UV_{CC5F}	Under voltage 5 V V_{CC} threshold	Ramp Down	4.1	4.45		V
UV_{CC33R}	Under voltage 3.3 V V_{CC} threshold	Ramp Up		2.9	3.1	V
UV_{CC33F}	Under voltage 3.3 V V_{CC} threshold	Ramp Down	2.5	2.75		V
OV_{CC5R}	Over voltage 5 V VCC threshold	Ramp Up		5.6	6.0	V
OV_{CC5F}	Over voltage 5 V VCC threshold	Ramp Down	5.28	5.5		V
OV_{CC33R}	Over voltage 3.3 V VCC threshold	Ramp Up		3.79	3.98	V
OV_{CC33F}	Over voltage 3.3 V VCC threshold	Ramp Down	3.58	3.73		V
I_{CCOUT}	Output current	V_{CC} in regulation with 12 V V_{SUP}; T_A = 100°C	0		125	mA
I_{CCOUTL}	Output current limit	V_{CC} short to ground			275	mA
PSRR	Power supply rejection ripple rejection	V_{RIP} = 0.5 V_{PP}, Load = 10 mA, f = 100 Hz, CO = 10 µF, V_{SUP} = 12 V and temperature = 27 ℃		60		dB
T_{SDR}	Thermal shutdown temperature	Internal junction temperature; rising	165			°C
T_{SDF}	Thermal shutdown temperature	Internal junction temperature; falling			150	°C
T_{SDHYS}	Thermal shutdown hysteresis	V_{SUP} = 12 V and temperature = 27 ℃		10		°C

(1) RXD pin is an open drain output. In standby mode RXD is pulled low which has the device pulling current through V_{SUP} through the pull-up resisitor to V_{CC}. The value of the pull-up resistor impacts the standby mode current. A 10 kΩ resistor value can add as much at 500 µA of current.

7.7 ELECTRICAL CHARACTERISTICS

over operating T_A temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RXD OUTPUT TERMINAL (OPEN DRAIN)					

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ELECTRICAL CHARACTERISTICS (continued)

over operating T_A temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output low voltage	Based upon a 2 kΩ to 10 kΩ external pull-up to V_{CC}			0.2	V_{CC}
I_{OL}	Low level output current, open drain	LIN = 0 V, RXD = 0.4 V	1.5			mA
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, RXD = V_{CC}	–5	0	5	µA
TXD INPUT TERMINAL						
V_{IL}	Low level input voltage		–0.3		0.8	V
V_{IH}	High level input voltage		2		5.5	V
I_{IH}	High level input leakage current	TXD = high	–5	0	5	µA
R_{TXD}	Internal pull-up resistor value		125	350	800	kΩ
LIN TERMINAL (REFERENCED TO V_{SUP})						
V_{OH}	HIGH level output voltage	LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 5.5 V to 36 V	0.85			V_{SUP}
V_{OL}	LOW level output voltage	LIN dominant, TXD = low, V_{SUP} = 5.5 V to 36 V			0.2	V_{SUP}
$V_{SUP_NON_OP}$	V_{SUP} where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11)	TXD & RXD open V_{LIN} = 5.5 V to 45 V	–0.3		45	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987 Param 12)	TXD = 0 V, V_{LIN} = 36 V, R_{MEAS} = 440 Ω, V_{SUP} = 36 V, V_{BUSdom} < 4.518 V; Figure 12	40	90	200	mA
$I_{BUS_PAS_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 13)	V_{LIN} = 0 V, V_{SUP} = 12 V Driver off/recessive; Figure 13	–1			mA
$I_{BUS_PAS_rec1}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	$V_{LIN} \geq V_{SUP}$, 5.5 V ≤ V_{SUP} ≤ 36 V Driver off; Figure 14			20	µA
$I_{BUS_PAS_rec2}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V_{LIN} = V_{SUP}, Driver off; Figure 14	–5		5	µA
$I_{BUS_NO_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15)	GND = V_{SUP}, V_{SUP} = 12 V, 0 V ≤ V_{LIN} ≤ 28 V; Figure 15	–1		1	mA
$I_{BUS_NO_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 16)	0 V ≤ V_{LIN} ≤ 28 V, V_{SUP} = GND; Figure 16			5	µA
V_{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 17)	LIN dominant (including LIN dominant for wake up); Figure 9, Figure 10			0.4	V_{SUP}
V_{BUSrec}	High level input voltage (ISO/DIS 17987 Param 18)	LIN recessive; Figure 9, Figure 14	0.6			V_{SUP}
V_{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19)	V_{BUS_CNT} = (V_{IL} + V_{IH})/2; Figure 9, Figure 14	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20)	V_{HYS} = (V_{IL} - V_{IH}); Figure 9, Figure 14			0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN term pull-up path (ISO/DIS 17987 Param 21)	By design and characterization	0.4	0.7	1.0	V
R_{SLAVE}	Pull-up resistor to V_{SUP} (ISO/DIS 17987 Param 26)	Normal and Standby modes	20	45	60	kΩ
I_{RSLEEP}	Pull-up current source to V_{SUP}	Sleep mode, V_{SUP} = 12 V, LIN = GND	–20		–2	µA
$C_{LIN,PIN}$	Capacitance of the LIN pin	By design and characterization			45	pF
EN INPUT TERMINAL						
V_{IH}	High level input voltage		2		5.5	V
V_{IL}	Low level input voltage		0		0.8	V
V_{HYS}	Hysteresis voltage	By design and characterization	30		500	mV
I_{IL}	Low level input current	EN = Low	–5	0	5	µA
R_{EN}	Internal pull-down resistor		125	350	800	kΩ
LIMP OUTPUT TERMINAL (HIGH VOLTAGE OPEN DRAIN OUTPUT)						
ΔV_H	High level voltage drop LIMP with respect to V_{SUP}	I_{LIMP} = - 0.5 mA		0.5	1	V

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ELECTRICAL CHARACTERISTICS (continued)

over operating T_A temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LKG(LIMP)}$	Leakage current	LIMP = 0 V, Sleep Mode	–0.5		0.5	µA
WAKE INPUT TERMINAL						
V_{IH}	High-level input voltage	Selective Wake-up or Standby Mode, WAKE pin enabled	V_{SUP} – 2			V
V_{IL}	Low-level input voltage	Selective Wake-up or Standby Mode, WAKE pin enabled			V_{SUP} – 3	V
I_{IH}	High-level input leakage current	WAKE = V_{SUP} - 1 V	–25	–15		µA
I_{IL}	Ligh-level input leakage current	WAKE = 1 V		15	25	µA
t_{WAKE}	WAKE hold time	Wake up time from a wake edge on WAKE; Standby or Sleep mode	5		50	µs
WDI, SDI, SCK, nCS INPUT TERMINAL						
V_{IH}	High-level input voltage		2.19			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input leakage current	Inputs = V_{CC}	–1		1	µA
I_{IL}	Low-level input leakage current	Inputs = 0 V, V_{CC} = Active	–50		-5	µA
C_{IN}	Input Capacitance	4 MHz		10	15	pF
$I_{LKG(OFF)}$	Unpowered leakage current	Inputs = 5.25/3.465 V, V_{CC} = V_{SUP} = 0 V	–1		1	µA
WDT INPUT TERMINAL						
V_{IH}	High-level input voltage	Inputs = V_{CC}	0.8			V_{CC}
V_{IL}	Low-level input voltage	Inputs = V_{CC}			0.2	V_{CC}
$V_{IM(WDT)}$	WDT Mid-level input voltage(1)	Inputs = V_{CC}	0.4	0.5	0.6	V_{CC}
I_{IH}	High-level input leakage current	Inputs = V_{CC}	2.5		25	µA
I_{IL}	Low-level input leakage current	Inputs = 0 V, V_{CC} = Active	–25		–2.5	µA
$I_{LKG(OFF)}$	Unpowered leakage current	Inputs = 5.25/3.465 V, V_{CC} = V_{SUP} = 0 V	–1		1	µA
SDO OUTPUT TERMINAL						
V_{OH}	High level output voltage	I_O = 2 mA, V_{CC} = Active	0.8			V_{CC}
V_{OL}	Low level output voltage	I_O = 2 mA, V_{CC} = Active			0.2	V_{CC}
$I_{LKG(OFF)}$	Unpowered leakage current	Outputs = 5.25/3.465 V, V_{CC} = V_{SUP} = 0 V	–1		1	µA
nRST, nWDR (SPI Mode) TERMINAL (OPEN DRAIN OUTPUT)						
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, nRST = V_{CC}	–5		5	µA
V_{OL}	Low-level output voltage	Based upon external pull up to V_{CC}			0.2	V_{CC}
I_{OL}	Low-level output current, open drain	LIN = 0 V, nRST = 0.4 V	1.5			mA
nINT, nWDR (Pin Mode) TERMINAL (OPEN DRAIN OUTPUT)						
V_{OL}	Low-level output voltage				0.2	V_{CC}
I_{OL}	Low-level output current, open drain	LIN = 0 V, nINT = 0.4 V	1.5			mA
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, nINT = V_{CC}	–5		5	µA
WDI, WDT TIMING and SWITCHING CHARACTERISTIC (RL = 1 MΩ, CL = 50 pF and T_A = -40°C to 125°C)						
t_W	WDI pulse width; see Figure 25	Filter time to avoid false input	30			µs
t_d	nWDR pulse width delay time that sets the lower window boundry starting point; see Figure 25	Time from nWDR low to high	2	4	6	ms
t_{WINDOW}	Closed Window + Open Window; See Figure 25	WDT = GND	32	40	48	ms
		WDT = V_{CC}	480	600	720	ms
		WDT = Floating	4.8	6	7.2	s

(1) This is the measured voltage at the WDT pin when left floating. The WDT pin should be connected directly to V_{CC}, GND or left floating.

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ELECTRICAL CHARACTERISTICS (continued)

over operating T_A temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WDOUT}	Watchdog timeout window (Open Window); See Figure 25	WDT = GND	16	20	24	ms
		WDT = V_{CC}	240	300	360	ms
		WDT = Floating	2.4	3	3.6	s
t_{PHL}	Propagation delay time high to low level output (V_{CC} to nWDR delay)	V_{CC} = Active		40	65	µs
DUTY CYCLE CHARACTERISTICS						
$D1_{12V}$	Duty Cycle 1 (ISO/DIS 17987 Param 27)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 5.5 V to 18 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 17, Figure 18)	0.396			
$D2_{12V}$	Duty Cycle 2 (ISO/DIS 17987 Param 28)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 5.5 V to 18 V, t_{BIT} = 50 µs (20 kbps), D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 17, Figure 18)			0.581	
$D3_{12V}$	Duty Cycle 3 (ISO/DIS 17987 Param 29)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 5.5 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 17, Figure 18)	0.417			
$D4_{12V}$	Duty Cycle 4 (ISO/DIS 17987 Param 30)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.251 x V_{SUP}, V_{SUP} = 5.5 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 17, Figure 18)			0.59	

7.8 AC SWITCHING CHARACTERISTICS

over operating T_A temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE SWITCHING CHARACTERISTICS						
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	RRXD = 2.4 kΩ, CRXD = 20 pF (See Figure 19, Figure 20)			6	µs
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time (ISO/DIS 17987 Param 32)	Rising edge with respect to falling edge, (t_{rx_sym} = t_{rx_pdf} – t_{rx_pdr}), R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (Figure 19, Figure 20)	–2		2	µs
t_{LINBUS}	LIN wakeup time (minimum dominant time on LIN bus for wakeup)	See Figure 23, Figure 30 and Figure 31	25	100	150	µs
t_{CLEAR}	Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See Figure 31	10		60	µs
t_{DST}	Dominant state time out		20	45	80	ms
t_{MODE_CHANGE}	Mode change delay time	Time to change from normal mode to sleep mode through EN pin: See Figure 21			15	µs
	Mode change delay time sleep mode to normal mode	Time to change from sleep mode to normal mode through EN pin and not due to a wake event; RXD pulled up to V_{CC}: See Figure 21			800	µs

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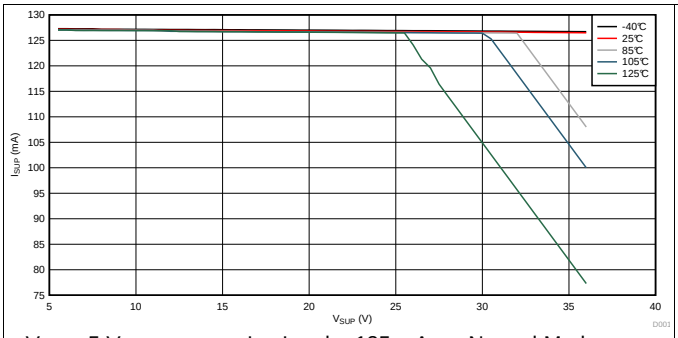
AC SWITCHING CHARACTERISTICS (continued)

over operating T_A temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{NOMINT}	Normal mode initialization time	Time for normal mode to initialize and data on RXD pin to be valid, includes t_{MODE_CHANGE} for standby mode to normal mode See Figure 21			45	µs
t_{INACT_FS}	Timer for inactivity coming out of sleep mode and when coming out of failsafe mode to determine if caused event has been cleared		250			ms
t_{PWR}	Power up time	Upon power up time it takes for valid data on RXD			1.5	ms
SPI SWITCHING CHARACTERISTICS						
f_{SCK}	SCK, SPI clock frequency				5	MHz
t_{SCK}	SCK, SPI clock period	See Figure 24	200			ns
t_{RSCK}	SCK rise time	See Figure 24			40	ns
t_{FSCK}	SCK fall time	See Figure 24			40	ns
t_{SCKH}	SCK, SPI clock high	See Figure 24	80			ns
t_{SCKL}	SCK, SPI clock low	See Figure 24	80			ns
t_{ACC}	First read access time from chip select	See Figure 24	50			ns
t_{CSS}	Chip select setup time	See Figure 24	100			ns
t_{CSH}	Chip select hold time	See Figure 24	100			ns
t_{CSD}	Chip select disable time	See Figure 24	500			ns
t_{SISU}	Data in setup time	See Figure 24	30			ns
t_{SIH}	Data in hold time	See Figure 24	40			ns
t_{SOV}	Data out valid	See Figure 24			80	ns
t_{RSO}	SO rise time	See Figure 24			40	ns
t_{FSO}	SO fall time	See Figure 24			40	ns

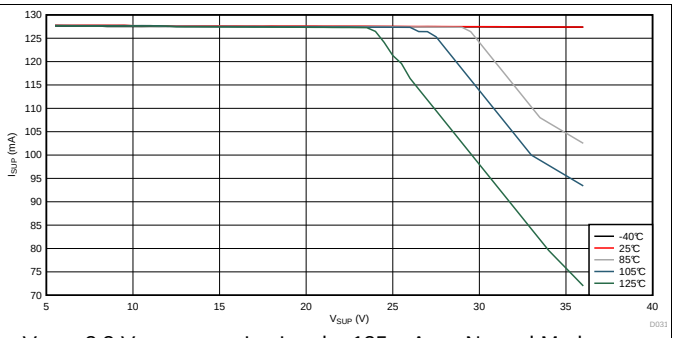
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7.9 Typical Characteristics



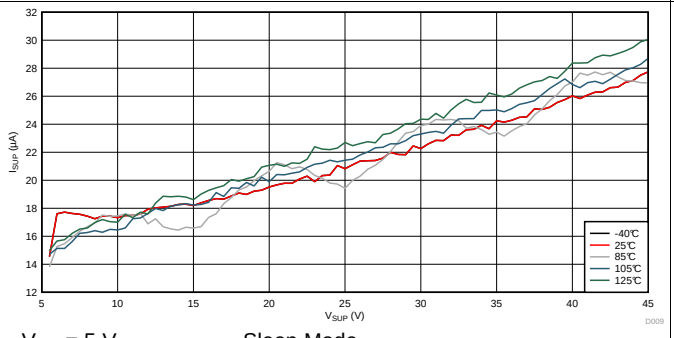
V_{CC} = 5 V I_{CC} Load = 125 mA Normal Mode

Figure 1. I_{SUP} vs V_{SUP} Across Temperature



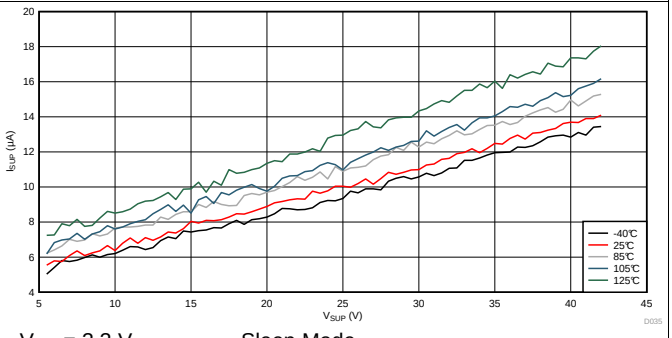
V_{CC} = 3.3 V I_{CC} Load = 125 mA Normal Mode

Figure 2. I_{SUP} vs V_{SUP} Across Temperature



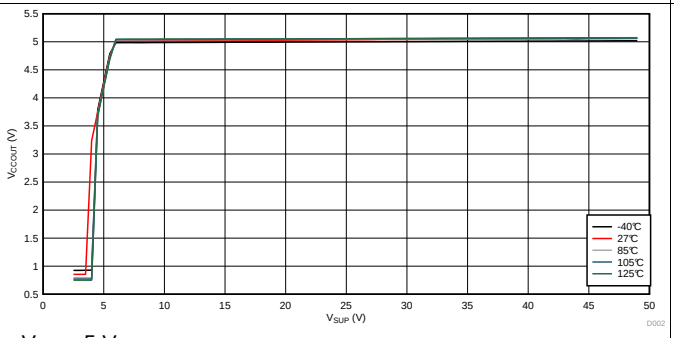
V_{CC} = 5 V Sleep Mode

Figure 3. I_{SUP} vs V_{SUP} Across Temperature



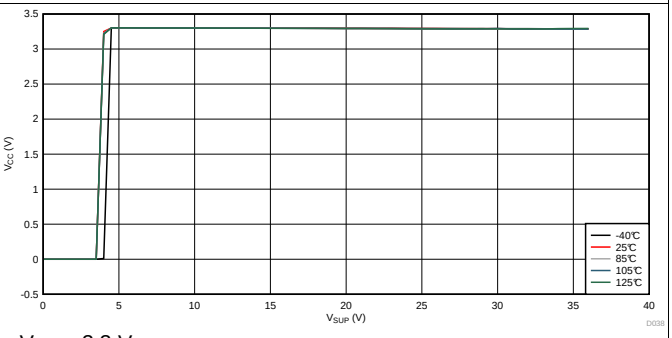
V_{CC} = 3.3 V Sleep Mode

Figure 4. I_{SUP} vs V_{SUP} Across Temperature



V_{CC} = 5 V

Figure 5. V_{CC} vs V_{SUP} Across Temperature



V_{CC} = 3.3 V

Figure 6. V_{CC} vs V_{SUP} Across Temperature

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8 Parameter Measurement Information

8.1 Test Circuit: Diagrams, Waveforms and Tables

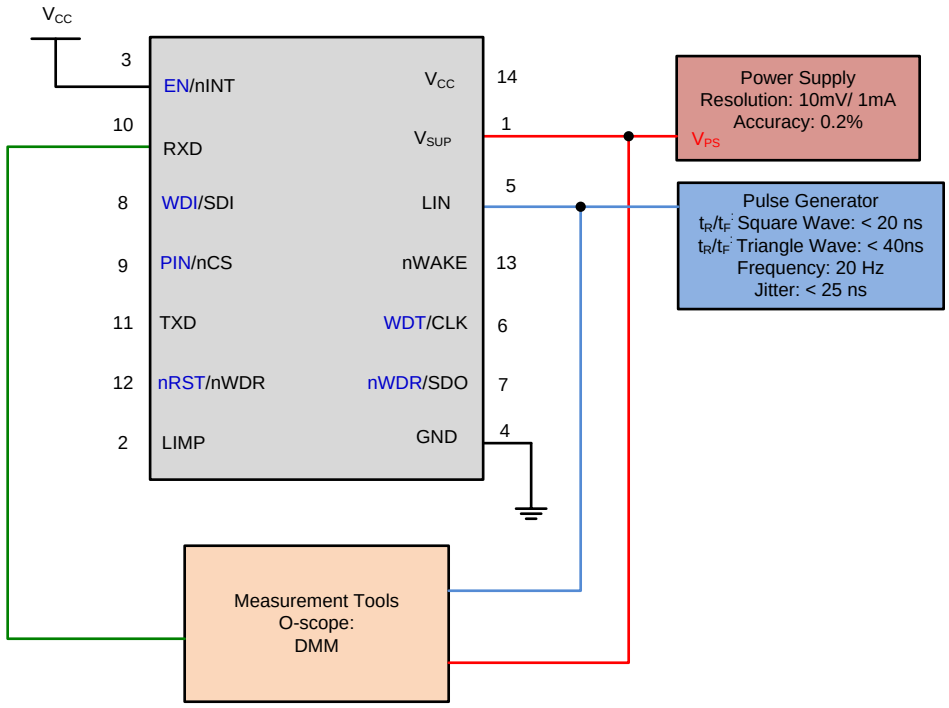


Figure 7. Test System: Operating Voltage Range with RX and TX Access

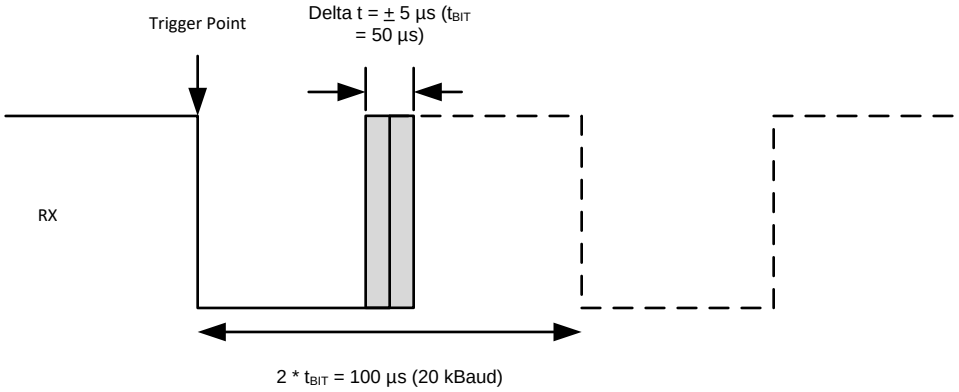


Figure 8. RX Response: Operating Voltage Range

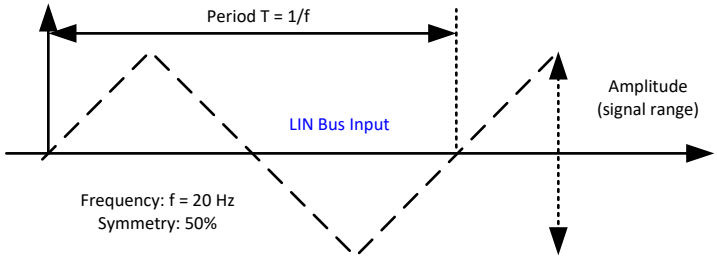


Figure 9. LIN Bus Input Signal

Test Circuit: Diagrams, Waveforms and Tables (continued)

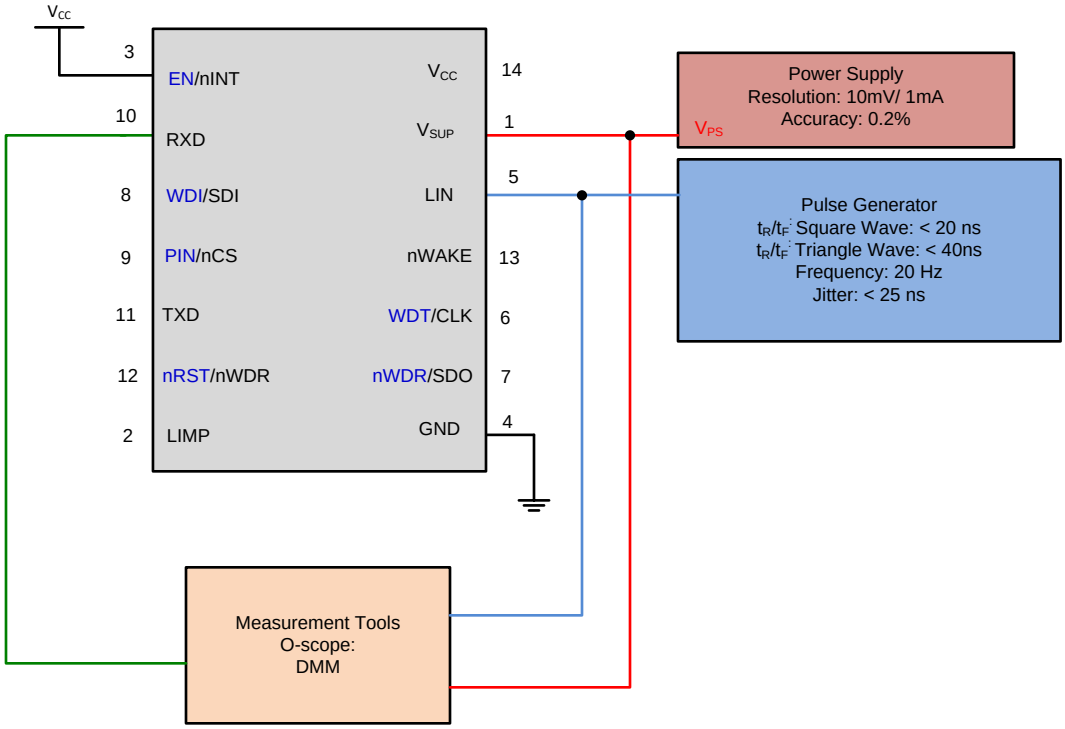


Figure 10. LIN Receiver Test with RX access

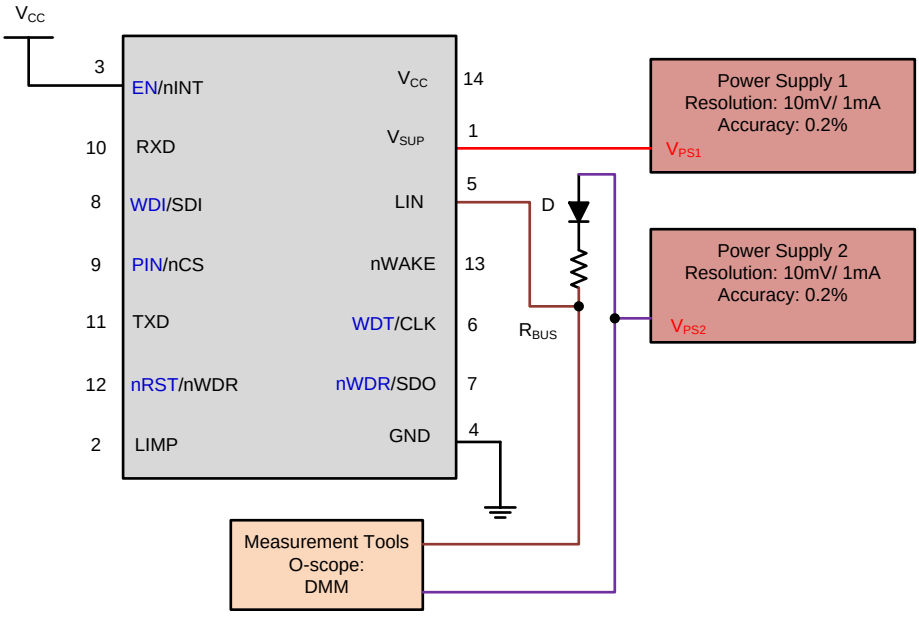


Figure 11. $V_{SUP_NON_OP}$ Test Circuit

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Test Circuit: Diagrams, Waveforms and Tables (continued)

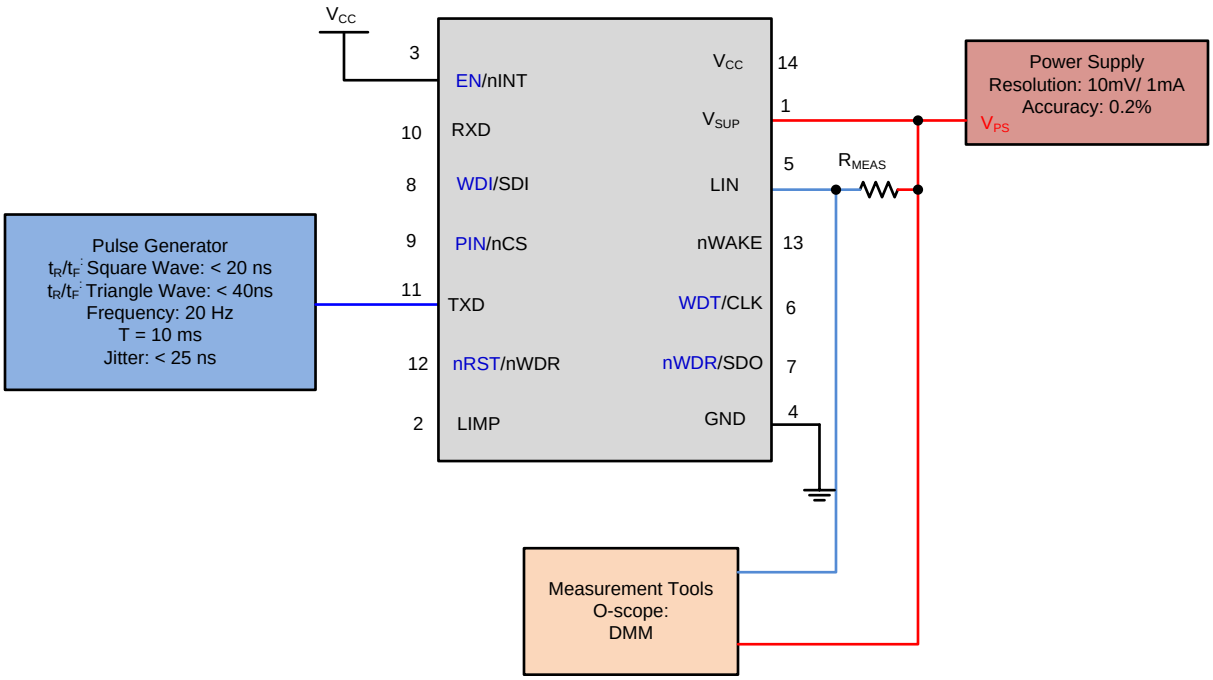


Figure 12. Test Circuit for I_{BUS_LIM} at Dominant State (Driver on)

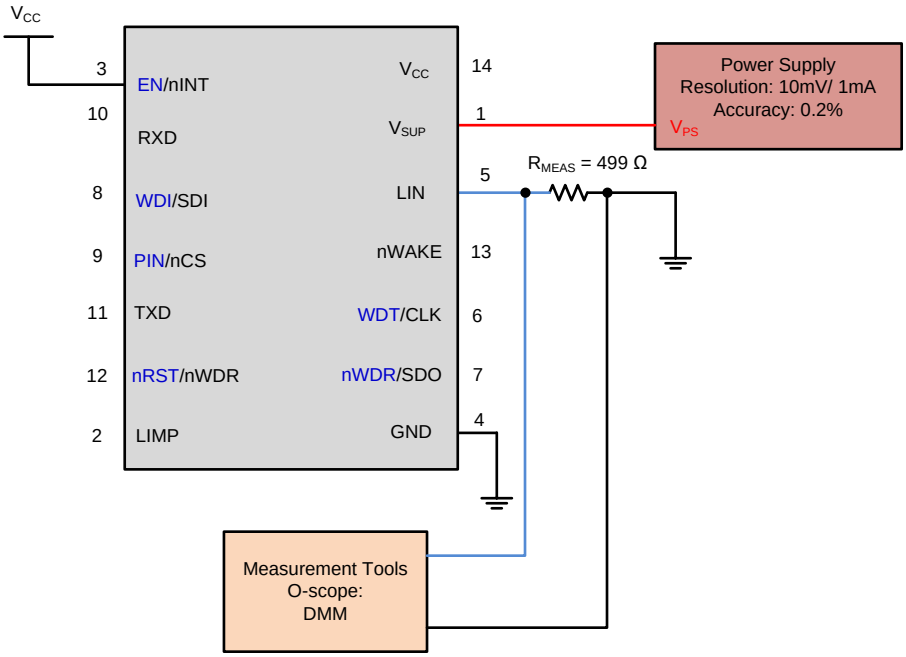


Figure 13. Test Circuit for $I_{BUS_PAS_dom}$; TXD = Recessive State V_{BUS} = 0 V

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Test Circuit: Diagrams, Waveforms and Tables (continued)

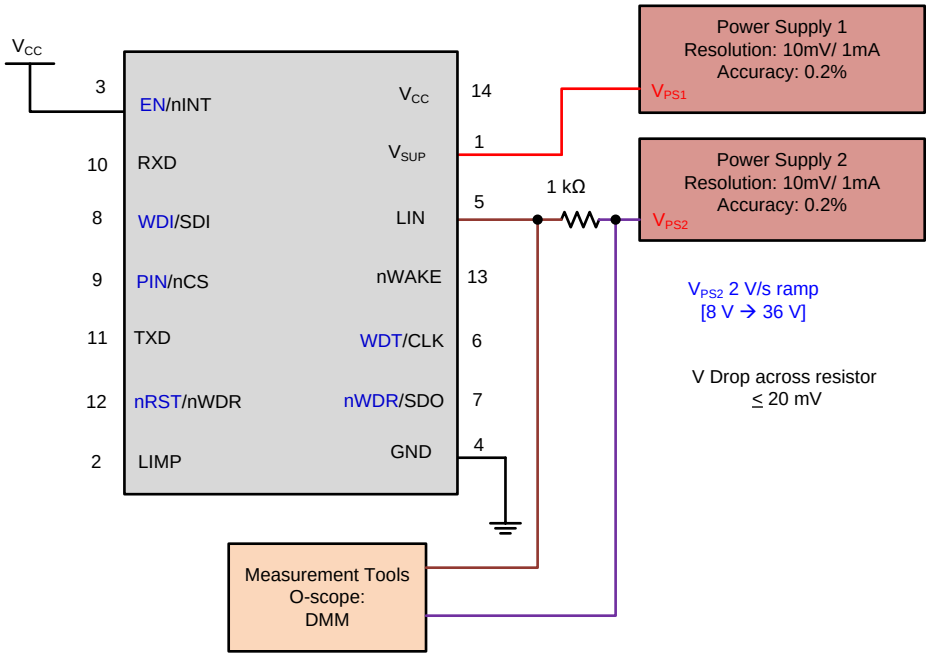


Figure 14. Test Circuit for $I_{BUS_PAS_rec}$

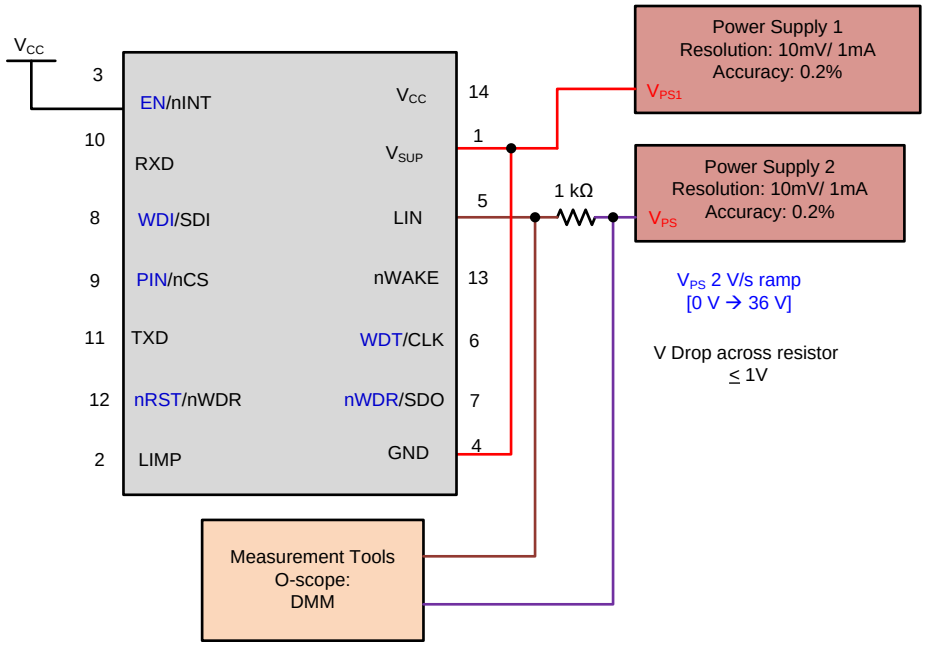


Figure 15. Test Circuit for $I_{BUS_NO_GND}$ Loss of GND

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Test Circuit: Diagrams, Waveforms and Tables (continued)

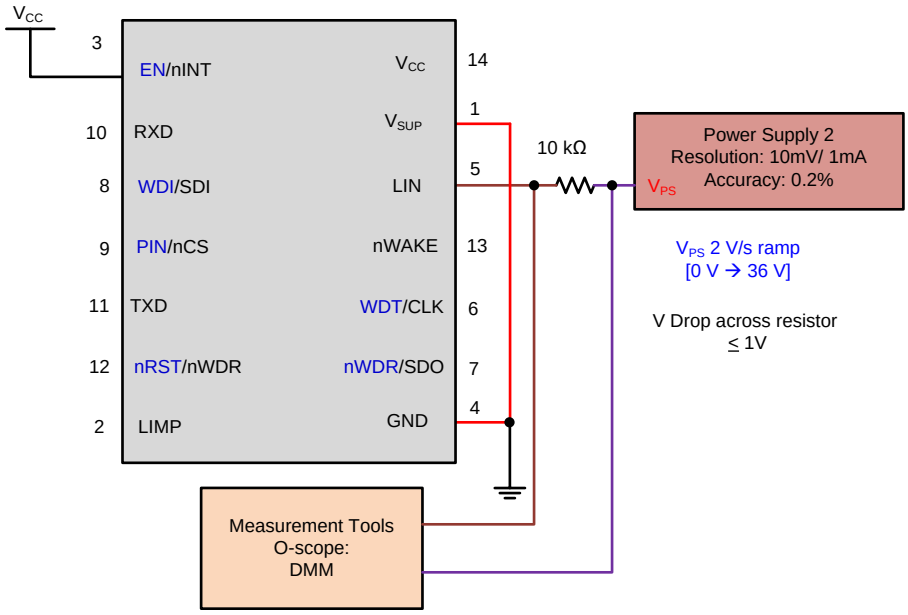


Figure 16. Test Circuit for $I_{BUS_NO_BAT}$ Loss of Battery

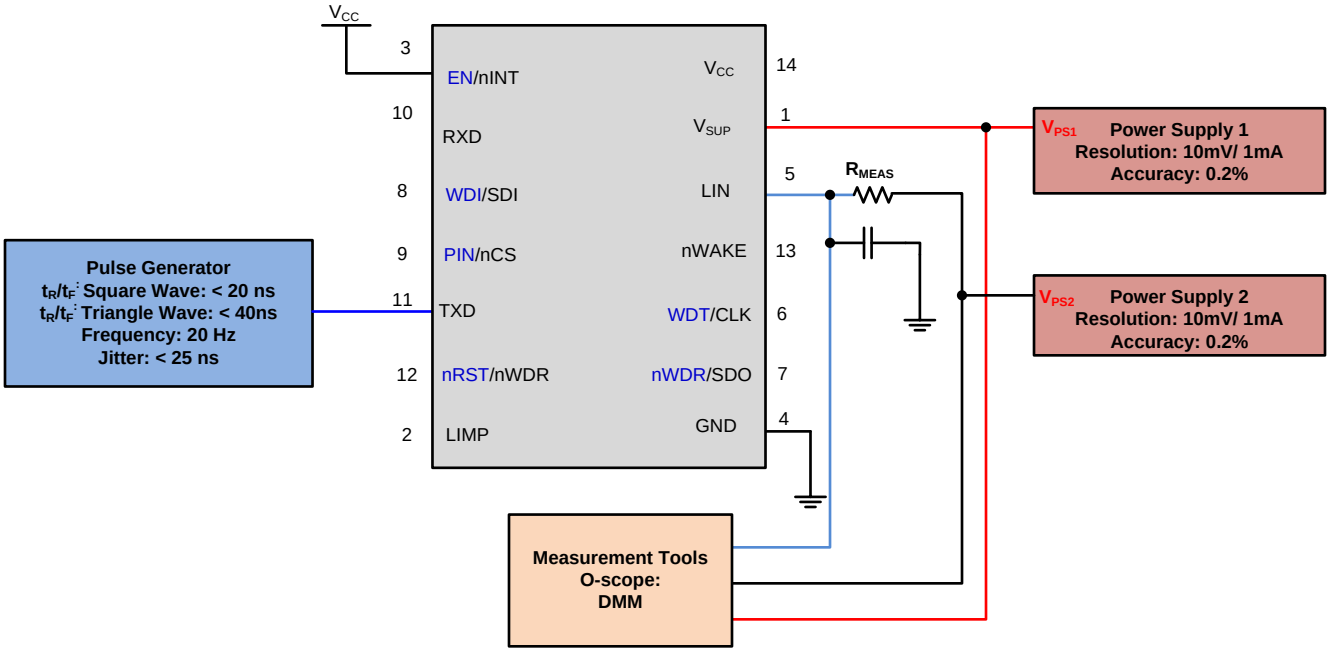


Figure 17. Test Circuit Slope Control and Duty Cycle

Test Circuit: Diagrams, Waveforms and Tables (continued)

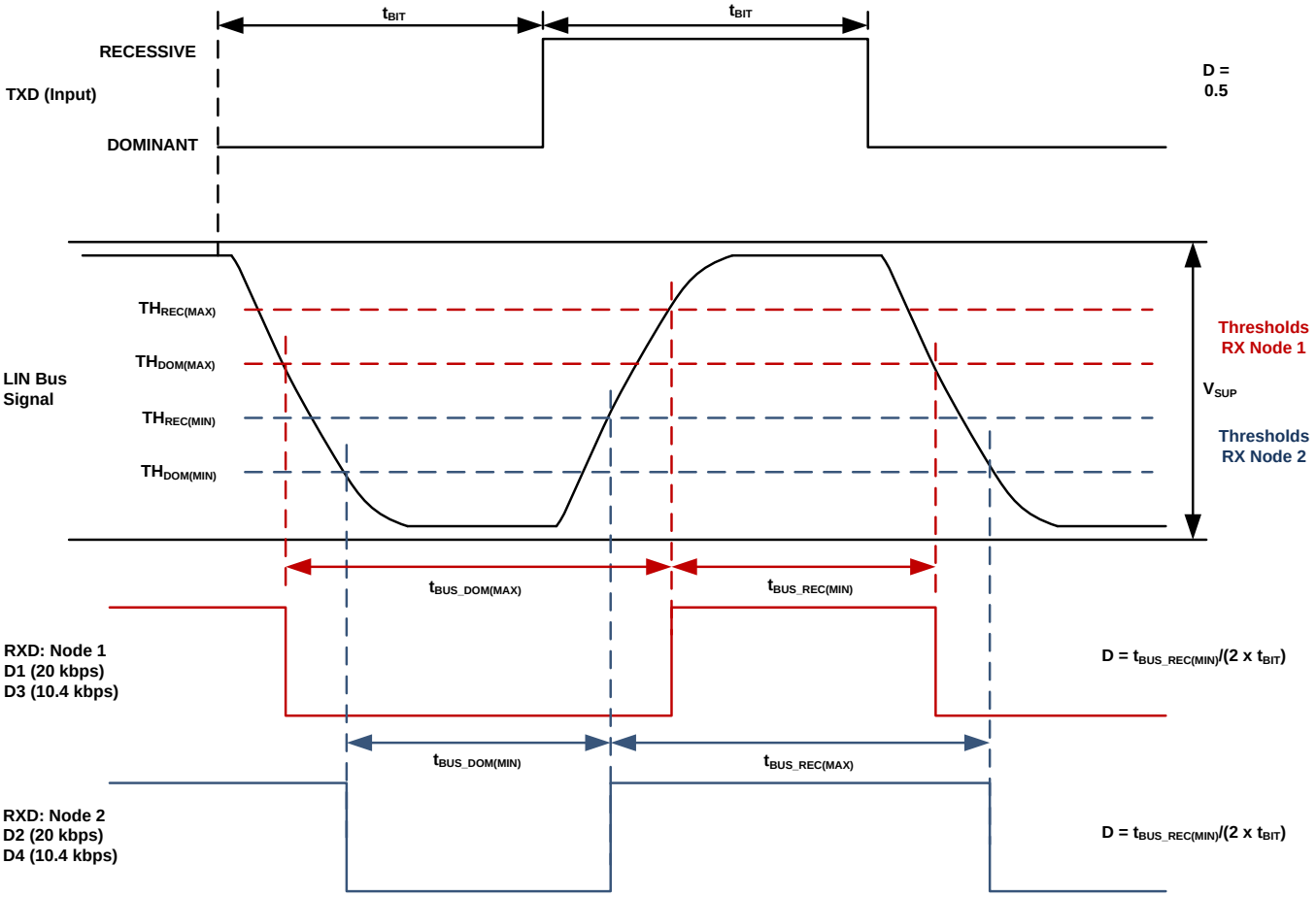


Figure 18. Definition of Bus Timing

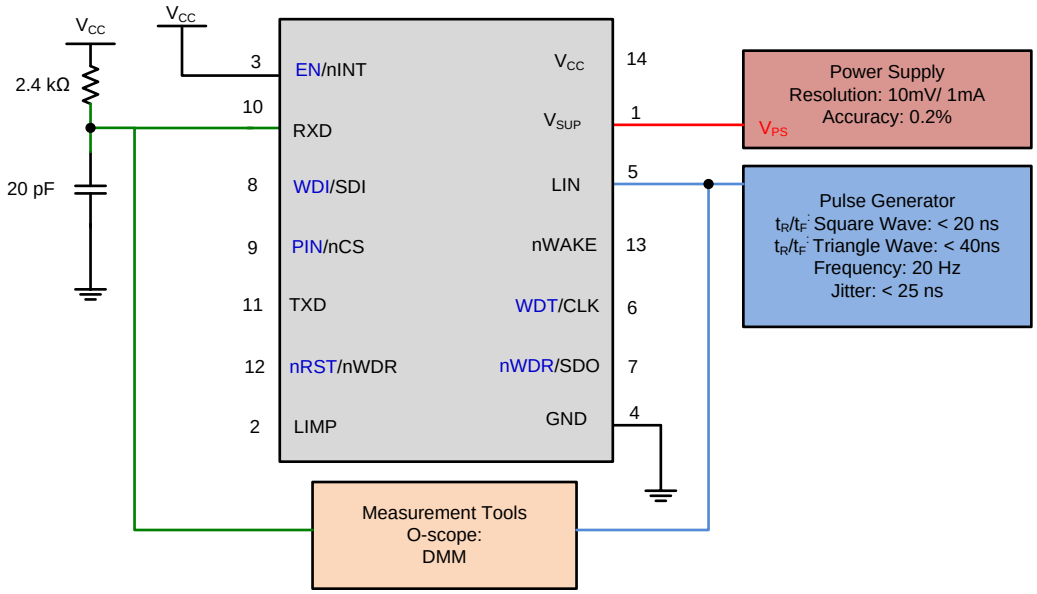
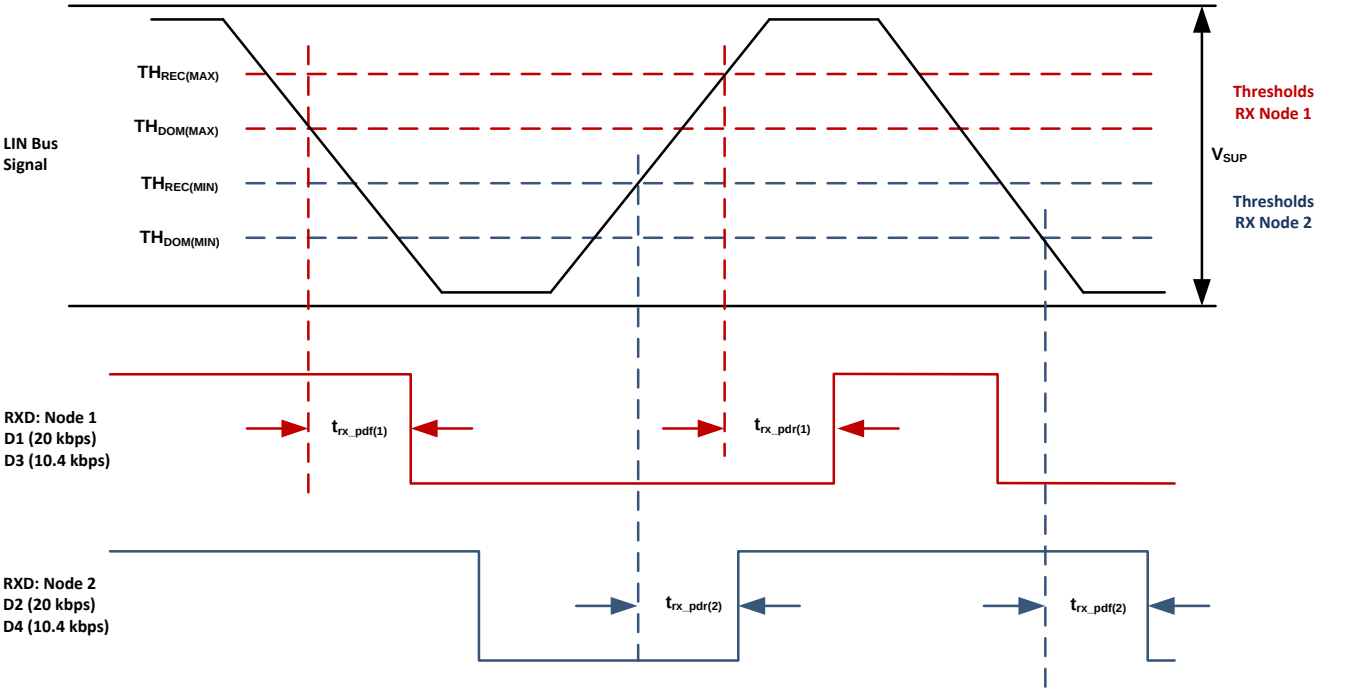


Figure 19. Propagation Delay Test Circuit

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Test Circuit: Diagrams, Waveforms and Tables (continued)



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Figure 20. Propagation Delay

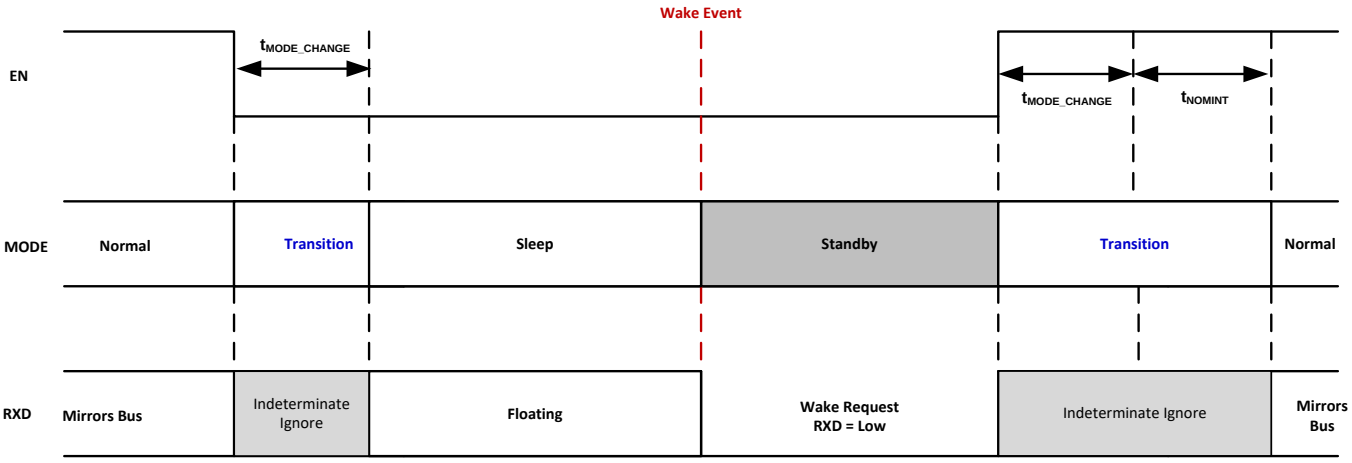


Figure 21. Mode Transitions

Test Circuit: Diagrams, Waveforms and Tables (continued)

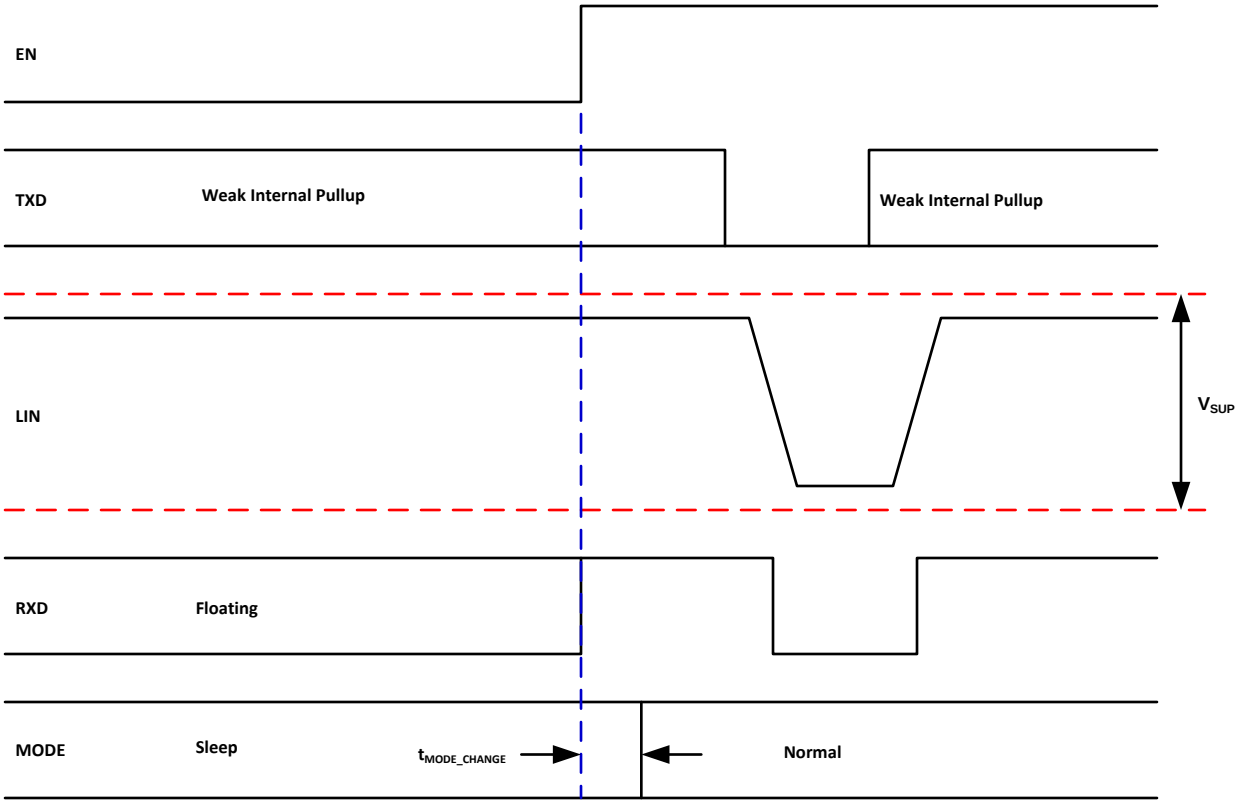


Figure 22. Wakeup Through EN

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Test Circuit: Diagrams, Waveforms and Tables (continued)

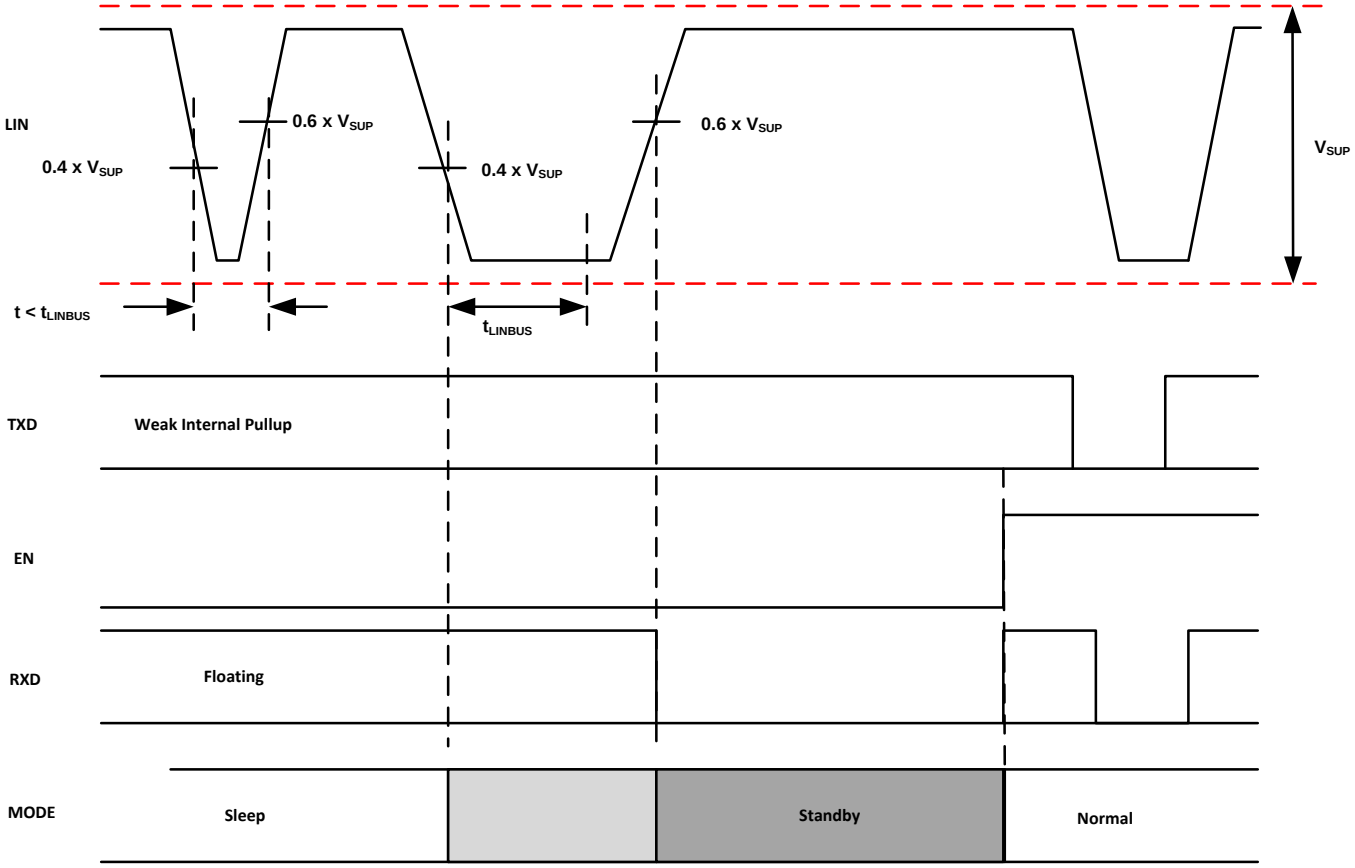


Figure 23. Wakeup through LIN

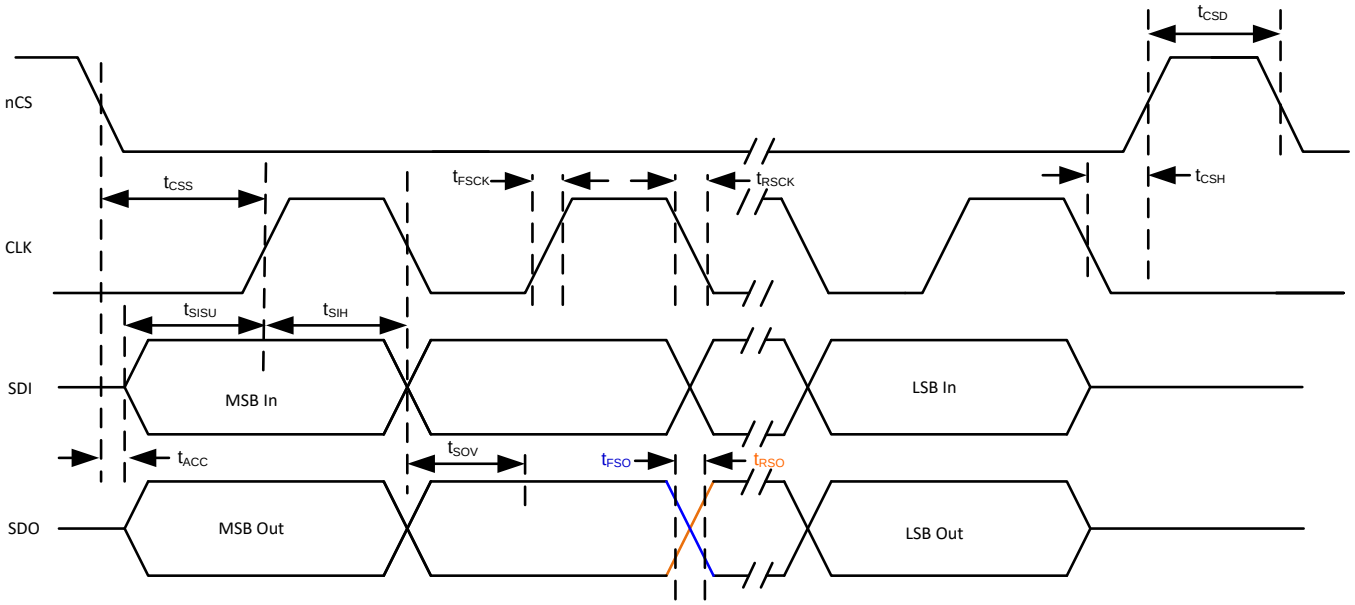


Figure 24. SPI AC Characteristic for Read and Write

Test Circuit: Diagrams, Waveforms and Tables (continued)

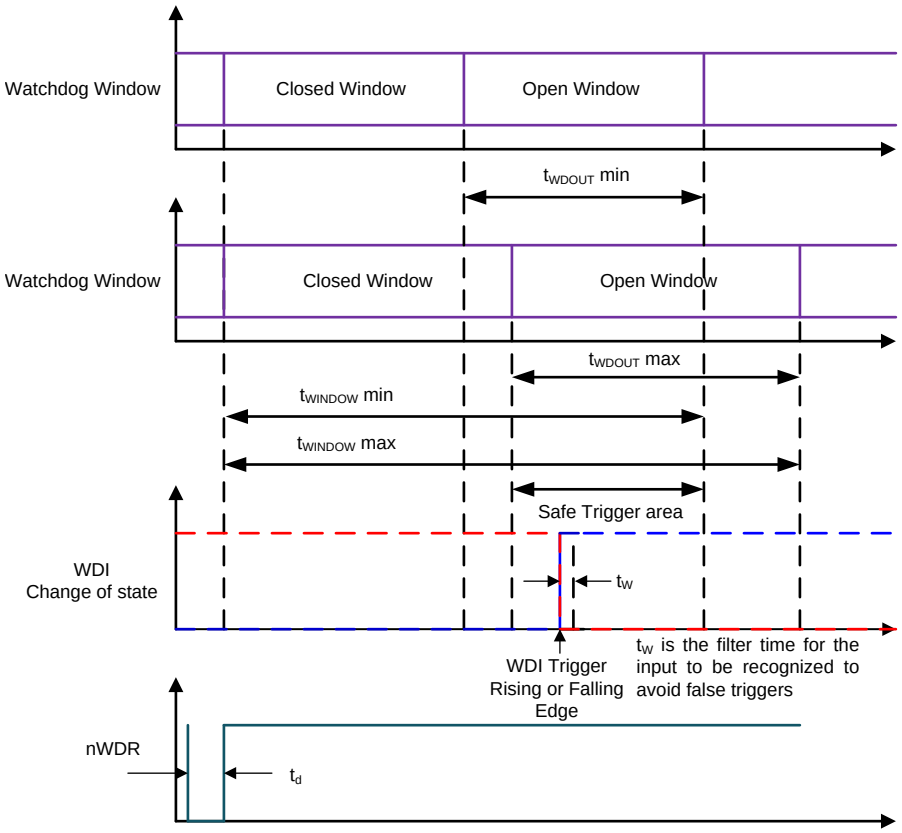


Figure 25. Watchdog Window Timing Diagram

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9 Detailed Description

9.1 Overview

The TLIN1441-Q1 LIN transceiver is a Local Interconnect Network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4.2 with integrated wake-up and protection features. The LIN bus is a single-wire, bi-directional bus that typically is used in low speed in-vehicle networks with data rates that range up to 20 kbps. The device LIN receiver works up to 100 kbps supporting in-line programming. The device converts the LIN protocol data stream on the TXD input into a LIN bus signal using a current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The receiver converts the data stream to logic level signals that are sent to the microprocessor through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode.

Ultra-low current consumption is possible using the sleep mode. TheTLIN1441-Q1 provides three methods to wake up from sleep mode: EN pin, WAKE pin and LIN bus. The device integrates a low dropout voltage regulator with a wide input from V_{SUP} providing 5 V ±2% or 3.3 V ±2% with up to 125 mA of current depending upon system implementation.

The TLIN1441-Q1 integrates a window based watchdog supervisor which has a programmable delay and window ratio determined by pin strapping or SPI communication. The device watchdog is controlled by pin configuration or SPI depending upon the state of pin 9 at power up. At power up, if pin 9 is externally pulled to ground, the device is configured for pin control of the device. If pin 9 is connected to the nCS pin of the processors and not driven at power up, the internal pull up configures the device for 3.3 V SPI control. If the processor uses 5 V IO a 500k Ω pull up resistor to V_{CC} is used for the 5 V version of the device. This allows the 5 V version of the device to work with both 3.3 V SPI or 5 V SPI. SPI communication is used for device configuration. In pin configuration nRST is asserted high when V_{CC} increases above UV_{CC} and stays high as long as V_{CC} is above this threshold.

When the watchdog is controlled by the device pins, the state of the WDT pin determines the window time. WDI is used as the watchdog input trigger which is expected in the open window. If a watchdog event takes place, the nWDR pin goes low to reset the processors. When using SPI writing FFh to register 15h, WD_TRIG, during the open window restarts the watchdog timer. The supervised processor must trigger the WDI pin or WD_TRIG register within the defined window. When using SPI, the nRST pin becomes the watchdog event output trigger for the processor. The watchdog timer does not start until after the first input trigger on WDI or the WD_TRIG register.

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9.2 Functional Block Diagram

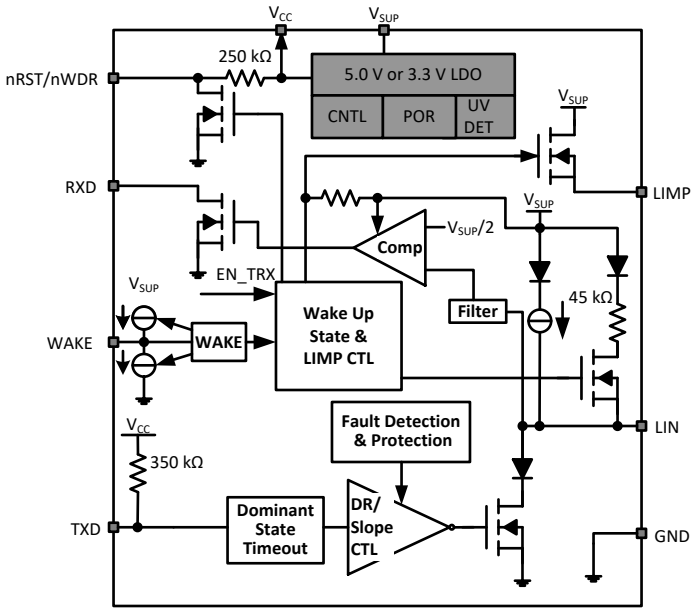


Figure 26. Transceiver plus VREG Functional Block Diagram

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Functional Block Diagram (continued)

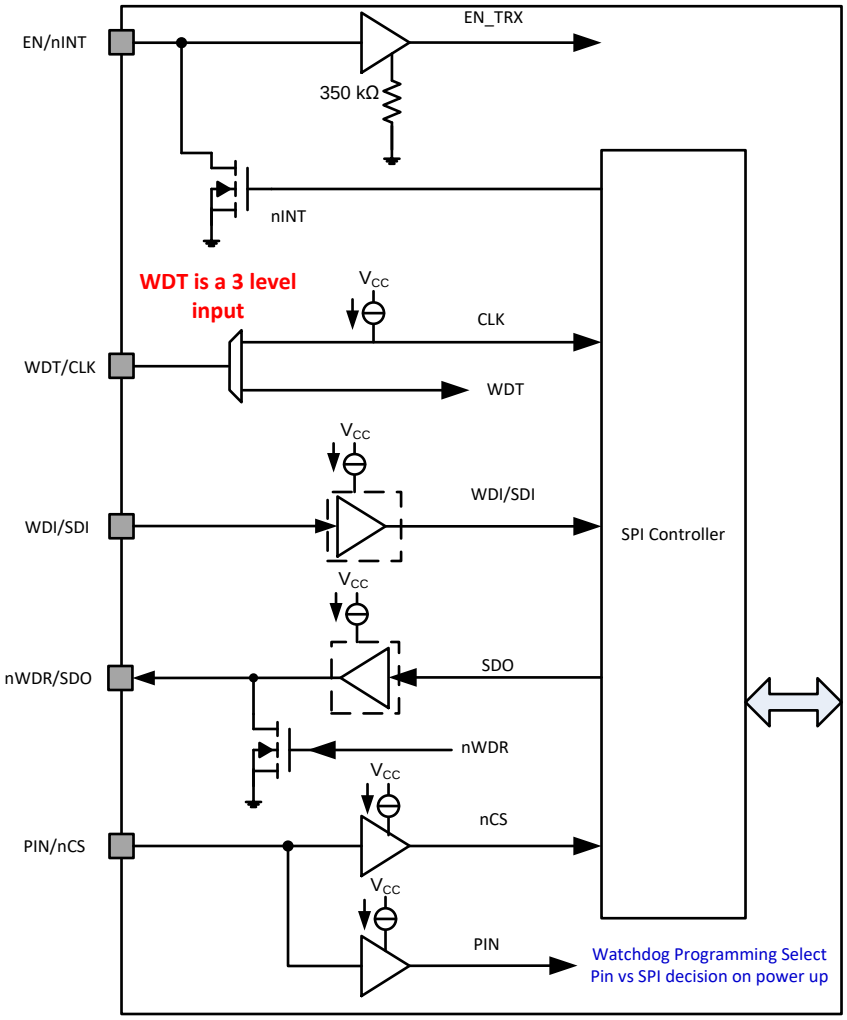


Figure 27. Input and Output High Level Functional Block Diagram

9.3 Feature Description

9.3.1 LIN (Local Interconnect Network) Bus

This high voltage input or output pin is a single wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 42 V. Reverse currents from the LIN to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

9.3.1.1 LIN Transmitter Characteristics

The transmitter meets thresholds and AC parameters according to the LIN specification. The transmitter is a low side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor and series diode to V_{SUP} must be added when the device is used for a master node application.

9.3.1.2 LIN Receiver Characteristics

The receiver's characteristic thresholds are ratio-metric with the device supply pin according to the LIN specification.

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Feature Description (continued)

The receiver is capable of receiving higher data rates (> 100 kbps) than supported by LIN or SAEJ2602 specifications. This allows the TLIN1441-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

9.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN slave mode applications. An external pull-up resistor (1 kΩ) and a series diode to V_{SUP} must be added when the device is used for master node applications as per the LIN specification.

Figure 28 shows a Master Node configuration and how the voltage levels are defined

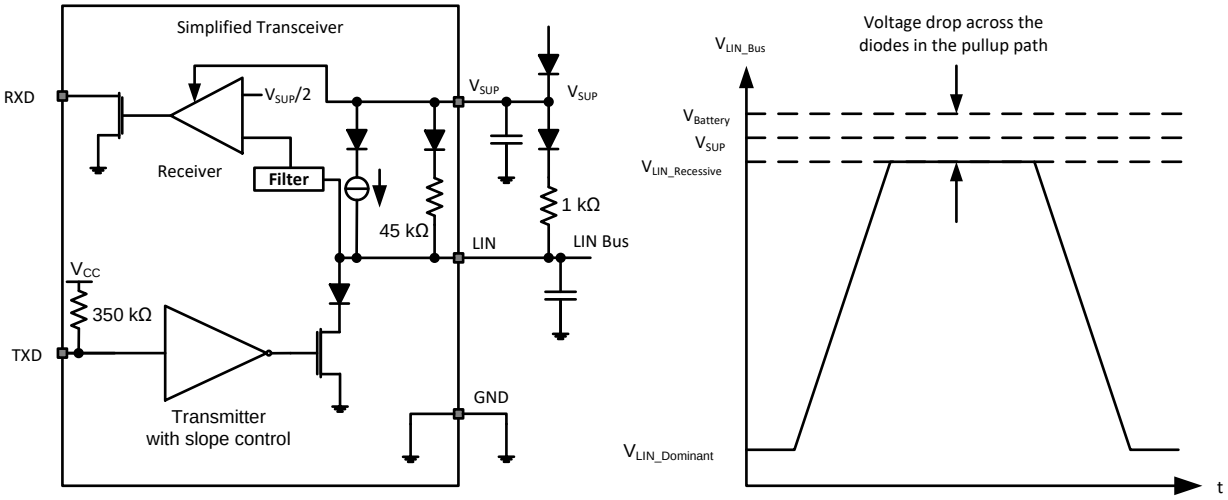


Figure 28. Master Node Configuration with Voltage Levels

9.3.2 TXD (Transmit Input and Output)

TXD is the interface to the node processors's LIN protocol controller that is used to control the state of the LIN output. When TXD is low, the LIN output is dominant (near ground). When TXD is high, the LIN output is recessive (near V_{SUP}). See Figure 28. The TXD input structure is compatible with processors with 3.3 V and 5 V_I and V_O. TXD has an internal pull-up resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state timer-out timer.

9.3.3 RXD (Receive Output)

RXD is the interface to the processors's LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near V_{SUP}) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3 V and 5 $V_{I/O}$ processors. If the processors RXD pin does not have an integrated pull-up, an external pull-up resistor to the processors I and O supply voltage is required. In standby mode, the RXD pin is driven low to indicate a wake up request from the LIN bus.

9.3.4 WAKE (High Voltage Local Wake Up Input)

WAKE pin is used for a high voltage device local wake up (LWU). This function is explained further in docato-extra-info-title Local Wake Up (LWU) via WAKE Terminal, see Local Wake Up (LWU) via WAKE Terminal section. The pin is both rising and falling edge trigger, meaning it recognizes a LWU on either edge of WAKE pin transition.

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Feature Description (continued)

9.3.5 WDT/CLK (Pin Programmable Watchdog Delay Input/SPI Clock)

When PIN/nCS is connected to ground at power up, this pin becomes the pin programmable watchdog delay input. This pin sets the upper boundary of the window watchdog. It can be connected to V_{CC}, GND or left floating. When connected directly to V_{CC} or GND or left open, the window frame will take on one of three value ranges: GND – 32 ms to 48 ms, VCC – 480 ms to 720 ms or left open – 4.8 s to 7.2 s. The closed versus open windows are based upon 50%/50%.

When PIN/nCS is connected to a high-Z output pin from a processor this pin becomes the SPI input clock.

9.3.6 WDI/SDI (Watchdog Timer Input/SPI Serial Data In)

When PIN/nCS is connected to ground at power up, this pin becomes the watchdog timer input trigger. This resets the timer with either a positive or negative transition from the processor. A filter time of t_W is used to avoid false triggers.

When PIN/nCS is connected to a high-Z output pin from a processor, this pin becomes the SPI serial data input pin for programming the device and providing a trigger event for the watchdog same as the WDI.

9.3.7 PIN/nCS (Pin Watchdog Select/SPI Chip Select)

This pin determines if the TLIN1441-Q1 watchdog is programmed by pin strapping or by SPI. At power up, the device monitors this pin and determine which method is to be used. When tied to GND, the device is pin programmable, and when connected to a high-Z processor I/O pin, the device is set up to support SPI. In SPI mode if the LDO is being used to power up other circuitry than the processor a mismatch can take place if using the 5 V version of the device and the processor supports 3.3 V. All I/O in the device are set up to work with a 3.3 V processor but if the 5 V LDO is being used for the processor requiring the I/O to be 5 V then an external resistor pulled up to VCC. This will make the I/O 5 V.

NOTE

The behavior of the microprocessor used must be understood if connecting to this pin to control whether the device is to be pin controlled or SPI controlled. There is an internal pull-up that will set the device in SPI control mode. If the processor pin drives low during power up, the device is in pin control mode. To specify pin control mode place and external pull-down resister to ground.

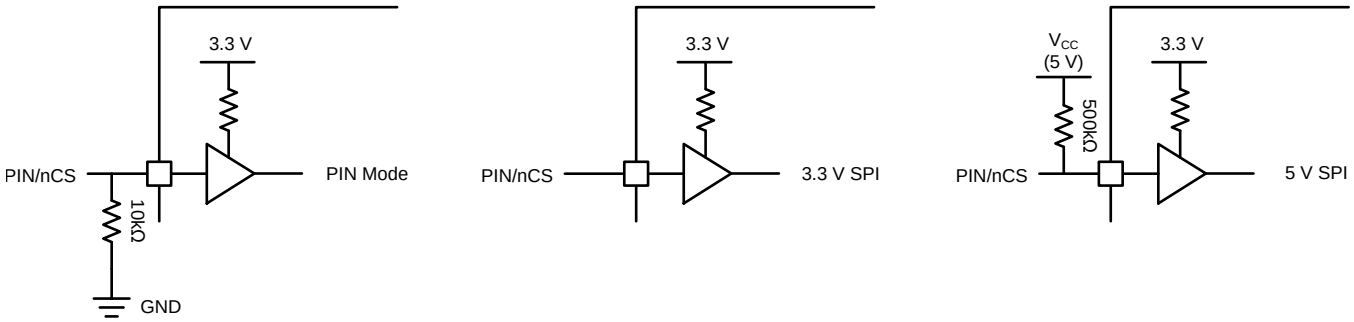


Figure 29. PIN/nCS Configuration

9.3.8 LIMP (LIMP Home output – High Voltage Open Drain Output)

This pin is connected to external circuitry for a limp home mode if the watchdog has timed out causing a reset. For the Limp pin to be turned off, the watchdog error counter must reach zero from correct input triggers in both pin control and SPI control modes. In SPI control Mode, other options can be selected in reg'h0B[4:3]. This feature can be disabled in SPI mode by setting reg'h0B[5] = 1. The only two modes that the LIMP pin changes state are in normal and failsafe modes. When in normal mode the LIMP pin is off unless there is a watchdog failure event that triggers it on. If programmed by SPI any event that trigger the failsafe mode will also turn on the LIMP pin.

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Feature Description (continued)

9.3.9 nWDR/SDO (Watchdog Timeout Reset Output/SPI Serial Data Out)

When PIN/nCS is connected to ground at power up, this pin becomes the watchdog timeout reset output pin. When the watchdog times out, this pin goes low for time of t_d and then release back to V_{CC}.

When PIN/nCS is connected to a high-Z output pin from a processor, this pin becomes the SPI serial data output pin.

9.3.10 V_{SUP} (Supply Voltage)

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse battery-blocking diode (see Figure 28). The V_{SUP} pin is a high-voltage-tolerant pin. Decoupling capacitors with a values of 100 nF is recommended to be connected close to this pin to better the transient performance. If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied). When V_{SUP} drops low enough the regulated output will drop out of regulation. The LIN bus works with a V_{SUP} as low as 5.5 V, but at a lower voltage, the performance is indeterminate and not ensured. If V_{SUP} voltage level drops enough, it triggers the UV_{SUP}, and if it keeps dropping, at some point it passes the POR threshold.

9.3.11 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.12 EN/nINT (Enable Input/Interrupt Output in SPI Mode)

When PIN/nCS is connected to ground at power up, this pin becomes the transceiver enable control. EN controls the operational modes of the device. When EN is high, the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low, the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after wake up. EN has an internal pull-down resistor to ensure the device remains in low power mode even if EN floats.

When PIN/nCS is connected to a high-Z output pin from a processor, this pin becomes processor interrupt output pin in SPI communication mode. When the TLIN1441-Q1 requires the attention of the processor, this pin is pulled low.

9.3.13 nRST/nWDR (Reset Output/Watchdog Timeout Reset Output)

The nRST pin serves as a V_{CC} monitor for under voltage events in Pin Control Mode and is the default function for SPI mode. This pin is internally pulled up to V_{CC}. When used a nRST and an under voltage event takes place, the signal is pulled low. The signal returns to V_{CC} value once the voltage on V_{CC} exceeds the under voltage threshold. If a thermal shutdown event takes place, the signal is pulled to ground. When the device is configured by SPI, the pin can be programmed to become the watchdog output trigger to reset the processor. When the watchdog times out, this signal is pulled low for time of t_d and then released back to V_{CC}. If both are needed for SPI configuration it is recommended to add an external circuit off the LIMP pin to serve as the watchdog output trigger to reset the processor. Note the LIMP pin output is a high voltage output based upon V_{SUP} and care must be taken when connecting to a lower voltage device.

9.3.14 V_{CC} (Supply Output)

The V_{CC} terminal can provide 5 V or 3.3 V with up to 125 mA from 12 V_{SUP} at 100°C to power up external devices when using high-k boards and thermal management best practices.

9.3.15 Protection Features

The device has several protection features that are described as follows.

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Feature Description (continued)

9.3.15.1 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than t_{DST}, the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the t_{DST} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-up to ensure the device fails to a known recessive state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of stated request on EN), the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on. The TLIN1441-Q1 can turn off this feature when in SPI mode by using register h0B[0].

9.3.15.2 Bus Stuck Dominant System Fault: False Wake Up Lockout

The device contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current use. Figure 30 and Figure 31 show the behavior of this protection.

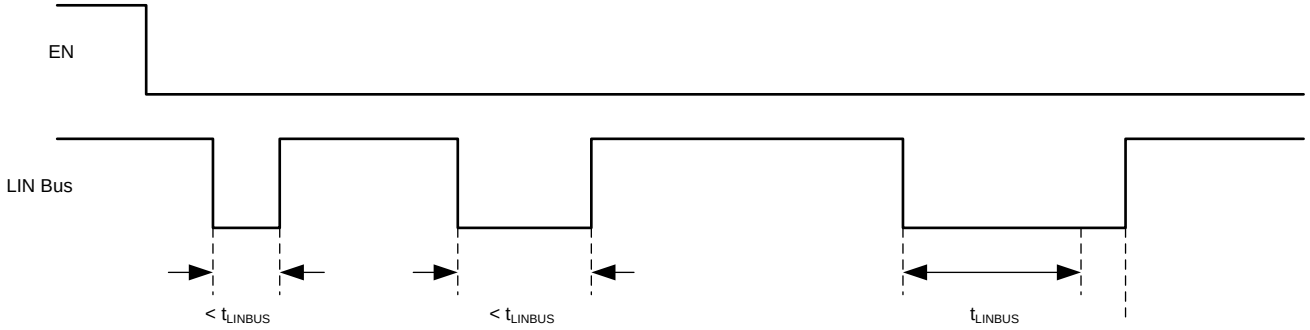


Figure 30. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wakeup

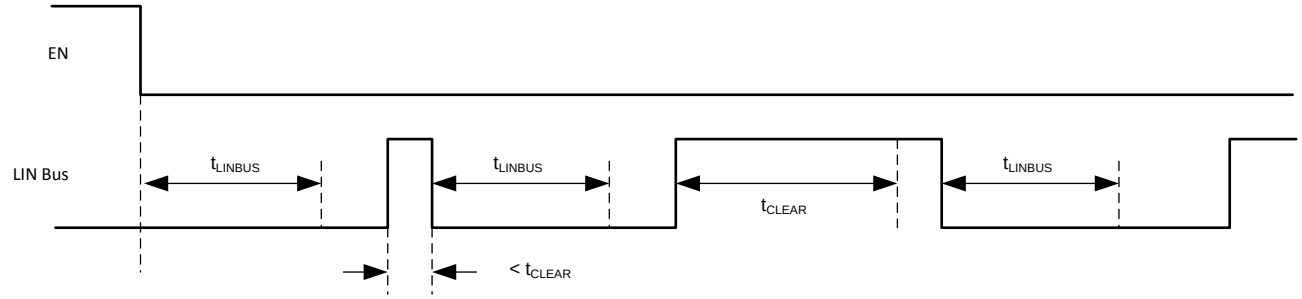


Figure 31. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wakeup

9.3.15.3 Thermal Shutdown

The LIN transmitter is protected by limiting the current; however, if the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state and turns off the V_{CC} regulator. The nRST pin is pulled to ground during a TSD event. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled. During this fault the device enters a TSD off mode. Once the junction temperature cools, the device enters standby mode as per the state diagram. In SPI mode the device can be configured to support a failsafe mode. If programmed the device will enter this mode upon an TSD event which puts the device into a sleep mode with LIMP turned on, see .

9.3.15.4 Under Voltage on V_{SUP}

The device contains a power on reset circuit to avoid false bus messages during under voltage conditions when V_{SUP} is less than UV_{SUP}.

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Feature Description (continued)

9.3.15.5 Unpowered Device and LIN Bus

In automotive applications, some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remains powered by the battery. The device has extremely low unpowered leakage current from the bus, so an unpowered node does not affect the network or load it down.

9.4 Device Functional Modes

The TLIN1441-Q1 has three functional modes of operation, normal, sleep, and standby. The next sections will describe these modes as well as how the device moves between the different modes. graphically shows the relationship while shows the state of pins.

Table 1. Operating SPI Mode

Mode	RXD	LIN BUS Termination	Transmitter	Watchdog	SPI Pins	nINT Pin	nRST/ nWDR Pin	WAKE Pin	LIMP	Comment
Sleep	Floating	Weak current pull-up	Off	Off	Off	On	Floating	On	Off	nRST is internally connected to the LDO output which in sleep mode is off
Standby	Low	45 kΩ (typical)	Off	Off	On	On	On	On	Previous state prior to entering STBY	Wake up event detected, waiting on processors to set EN
Normal	LIN Bus Data	45 kΩ (typical)	On	On	On	On	On	On	Off but can be active	LIN transmission up to 20 kbps
TSD Off	NA	Floating	45 kΩ (typical)	Off	On	On	Floating	On	Off	nRST will be floating but if OV_{CC} is reached this value may show up on nRST pin
Failsafe	Floating	Weak current pull-up	Off	Off	Off	On	Floating	On	On	Failsafe mode is sleep mode with LIMP on

Table 2. Operating PIN Mode

Mode	EN	RXD	LIN BUS Termination	Transmitter	Watchdog	nRST Pin	WAKE Pin	LIMP	Comment
Sleep	Low	Floating	Weak current pull-up	Off	Off	Floating	On	Off	nRST is internally connected to the LDO output which in sleep mode is off
Standby	Low	Low	45 kΩ (typical)	Off	Off	On	On	Previous state prior to entering STBY	Wake up event detected, waiting on processors to set EN
Normal	High	LIN Bus Data	45 kΩ (typical)	On	On	On	On	Off but can be active	LIN transmission up to 20 kbps
TSD Off	NA	Floating	45 kΩ (typical)	Off	Off	Floating	On	Off	nRST will be floating but if OV_{CC} is reached this value may show up on nRST pin

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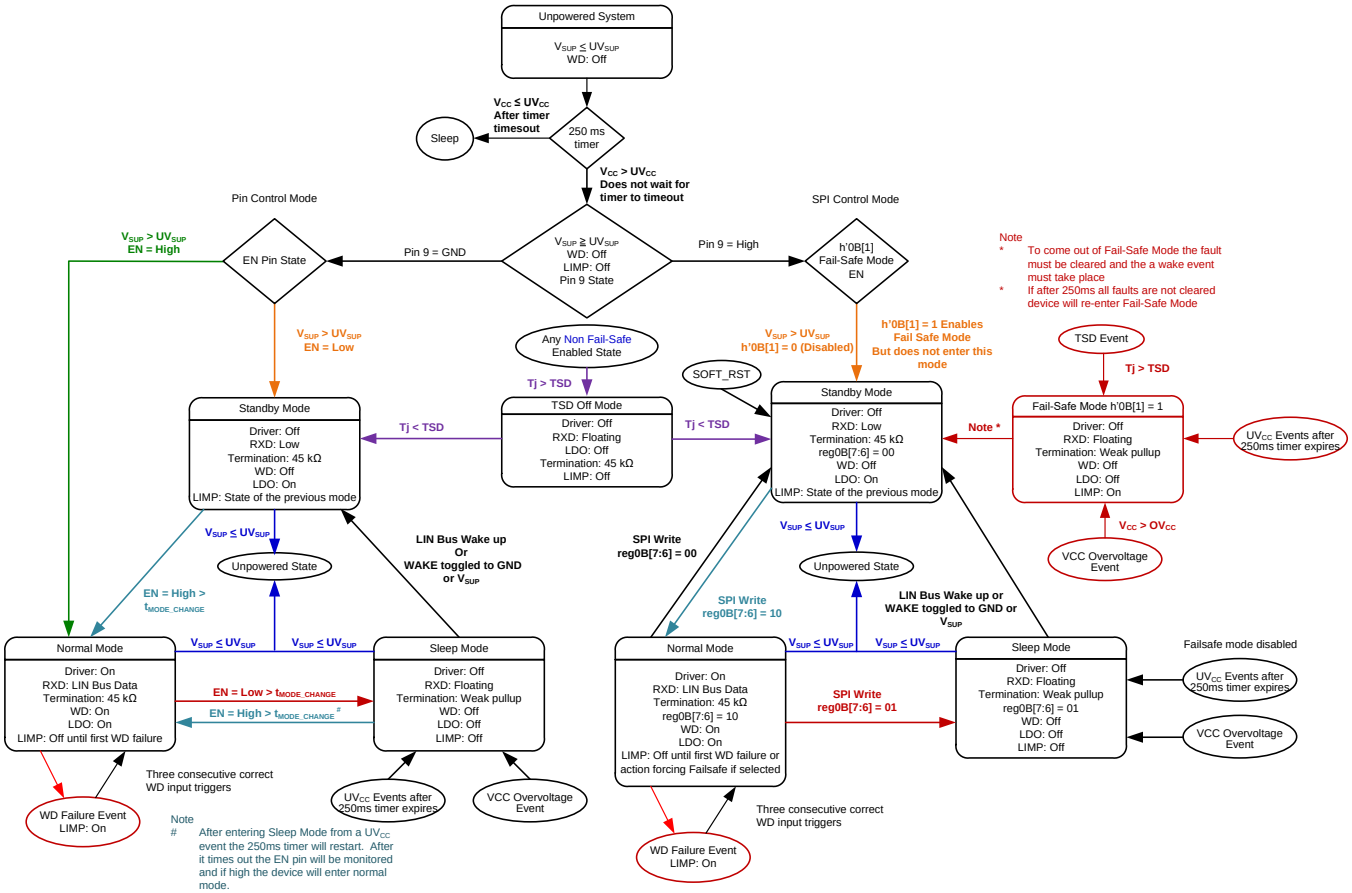


Figure 32. State Diagram with Failsafe

9.4.1 Normal Mode

If the EN pin is high at power up, the device powers up in normal mode and if low powers up in standby mode. In normal operational mode, the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a digital high and a dominant signal on the LIN bus is a digital low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high in Pin control mode or if reg0B[7:6] = 10 in SPI communication Mode. While in Pin control the device is in sleep or standby mode for > t_{MODE_CHANGE}.

9.4.2 Sleep Mode

Sleep Mode is the power saving mode for the TLIN1441-Q1. Even with extremely low current consumption in this mode, the device can still wake up from the LIN bus through a wake up signal or if EN is set high for > t_{MODE_CHANGE} for the device. There is a 250 ms timer, t_{INACT_FS}, that if UV_{CC} is still present after this time the device will re-enter sleep mode. The LIN bus is filtered to prevent false wake up events. The wake up events must be active for the respective time periods (t_{LINBUS}).

The sleep mode is entered by setting EN low for longer than t_{MODE_CHANGE} when in pin control mode or by setting reg0B[7:6] = 01 in SPI communication mode. In SPI control mode the device enters sleep mode through a SPI write to the MODE register 8'h0B[7:6].

While the device is in sleep mode, the following conditions exist.

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.

- EN (in Pin Control Mode) input and LIN wake up receiver are active.
- WAKE pin is active.

9.4.3 Standby Mode

This mode is entered whenever a wake up event occurs through LIN bus while the device is in sleep mode. The LIN bus slave termination circuit is turned on when standby mode is entered. Standby mode is signaled through a low level on RXD. See *Standby Mode Application Note* for more application information.

When EN (in Pin Control Mode) is set high for longer than t_{MODE_CHANGE} while the device is in standby mode the device returns to normal mode and the normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

During power up if EN is low the device goes into standby mode and if EN is high the device goes into normal mode. EN has an internal pull-down resistor ensuring EN is pulled low if the pin is left floating in the system.

When in SPI communication mode the TLIN1441-Q1 enters standby mode by writing a 00 to reg0B[7:6] from normal mode.

9.4.4 Failsafe Mode

When the TLIN1441-Q1 has certain fault conditions the device will enter a failsafe mode if this feature is enabled. This mode turns on LIMP and brings all other function into lowest power mode state. Fault conditions are over voltage on V_{CC}, thermal shutdown, and four consecutive V_{CC} undervoltage events. Once the fault conditions are cleared the device can be put back into standby mode from a wake event. If a fault condition is still in effect the device will re-enter failsafe mode after 250 ms, t_{INACT_FS}.

9.4.5 Wake Up Events

There are three ways to wake up from sleep mode:

- Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on the LIN bus where the dominant state is held for t+he t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake up event eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Local wake up through EN being set high for longer than t_{MODE_CHANGE}.
- Local wake up through WAKE pin being set high for longer than t_{MODE_CHANGE}.

9.4.5.1 Wake Up Request (RXD)

When the TLIN1441-Q1 encounters a wake up event from the LIN bus, RXD goes low and the device transitions to standby mode until EN is reasserted high and the device enters normal mode. Once the device enters normal mode, the RXD pin releases the wake up request signal and the RXD pin then reflects the receiver output from the LIN bus.

9.4.5.2 Local Wake Up (LWU) via WAKE Terminal

The WAKE terminal is a high voltage input terminal which can be used for local wake up (LWU) request via a voltage transition. The terminal triggers a LWU event on a high to low or low to high transition. This terminal may be used with a switch to ground or V_{SUP}. If the terminal is not used, it should be connected to V_{SUP} to avoid unwanted parasitic wake up.

The LWU circuitry is active in sleep mode and standby mode. If a valid LWU event occurs, the device transitions to standby mode. The LWU circuitry is not active in normal mode. To minimize system level current consumption, the internal bias voltages of the terminal follows the state on the terminal with a delay of $t_{WAKE(MIN)}$. A constant high level on WAKE will have an internal pull up to V_{SUP} and a constant low level on WAKE has an internal pull-down to ground. On power up, this may look like a LWU event and could be flagged as such.

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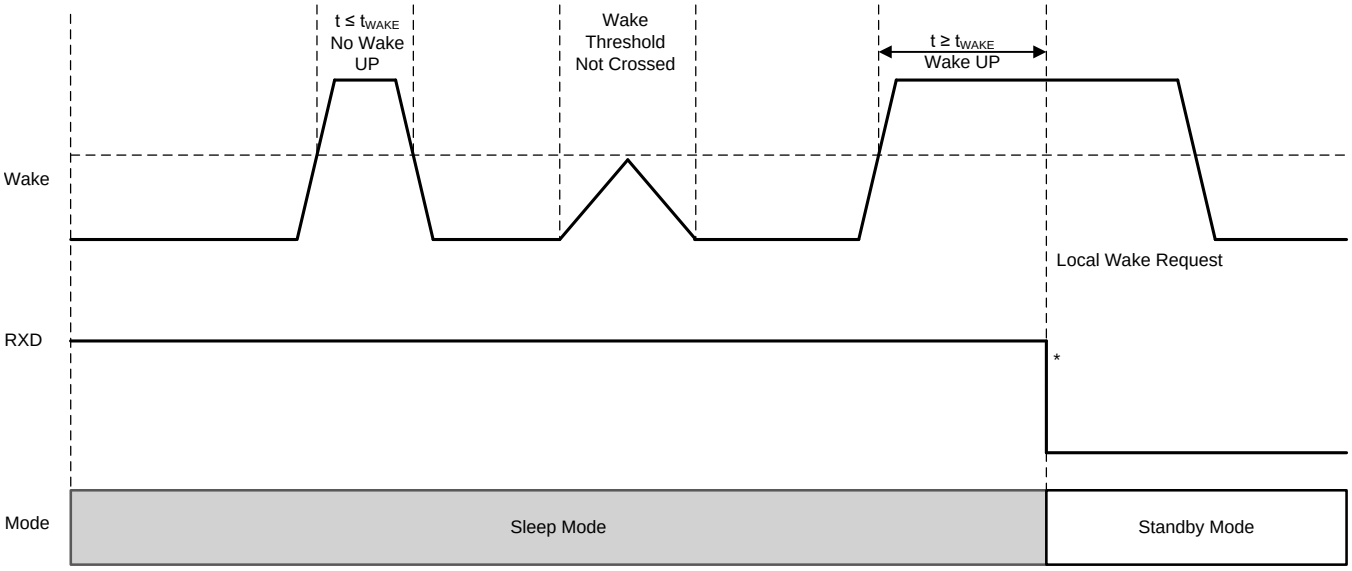


Figure 33. Local Wake Up (LWU) - Rising Edge

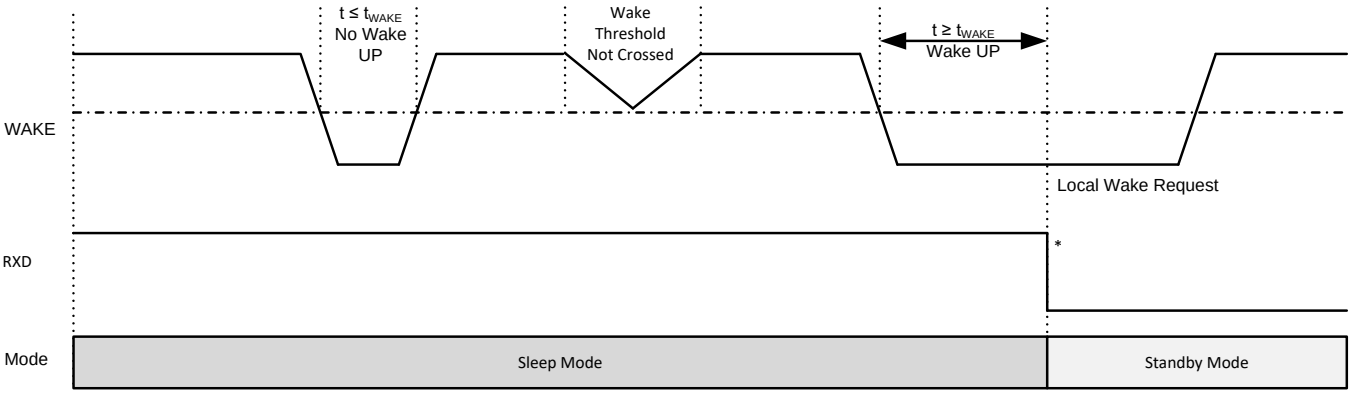


Figure 34. Local Wake Up (LWU) - Falling Edge

9.4.6 Mode Transitions

When the device is transitioning between modes, the device needs the time t_{MODE_CHANGE} and t_{NOMINT} to allow the change to fully propagate from the EN pin through the device into the new state.

9.4.7 Voltage Regulator

The device has an integrated high-voltage LDO that operates over a 5.5 V to 24 V input voltage range for both 3.3 V and 5 V V_{CC}. The device has an output current capability of 125 mA and support fixed output voltages of 3.3 V (TLIN14413-Q1) or 5 V (TLIN14415-Q1). It features thermal shutdown and short-circuit protection to prevent damage during over-temperature and over current conditions

9.4.7.1 V_{CC}

The V_{CC} pin is the regulated output based on the required voltage. The regulated voltage accuracy is ± 2%. The output is current limited. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UV_{SUP} threshold, the regulator shuts down until the input voltage returns above the UV_{SUPR} level. The device monitors situations where V_{CC} may drop below the UV_{CC} level thus causing the nRST pin to be pulled low. If after t_{INACT_FS} timer times out and UV_{CC} is still present the device will enter sleep mode. This timer is approximately 250ms at a minimum. When in PIN mode the timer restarts and once times out will determine the state of the EN pin and enter the mode based

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upon this state. In SPI mode and failsafe is turned off it will enter sleep mode. If failsafe is turned on the device will enter failsafe mode. An over voltage on V_{CC}, OV_{CC} is also monitored. If the device is in Pin mode it will enter sleep mode. Once in sleep mode the device will wait for 250 ms and then check the status of the EN pin. If high the device will enter normal mode. If the OV_{CC} event is still present, the device will enter sleep mode and wait for 250 ms and check the EN pin status. This will continue until either the EN pin is low or the OV_{CC} event is cleared. If the device is in SPI mode the state the device will enter depends upon whether failsafe is enabled. It enabled the device will enter failsafe mode, if not it will enter sleep mode. If the voltage exceeds the absolute max on the V_{CC} pin the device could be damaged.

9.4.7.2 Output Capacitance Selection

For stable operation over the full temperature range and with load currents up to 125 mA on V_{CC} a certain capacitance is expected and depends upon the minimum load current. To support no load to full load a value of 10 µF and ESR smaller than 2 Ω is needed. For 500 µA to full load an 1 µF capacitance can be used. The low ESR recommendation is to improve the load transient performance.

9.4.7.3 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (IL) and switch resistor. This tracking allows for a smaller input capacitance and can possibly eliminate the need for a boost converter during cold-crank conditions.

9.4.7.4 Power Supply Recommendation

The device is designed to operate from an input-voltage supply range between 5.5 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device. The recommended minimum capacitance at the pin is 100 nF . The max voltage range is for the LIN functionality. Exceeding 24V for the LDO will reduce the effective current sourcing capability due to thermal considerations.

9.4.8 Watchdog

The TLIN1441-Q1 has an integrated watchdog function. This can be programmed by pin control or SPI communication control based upon the state of the PIN/nCS pin at power up. The device provides a default window based watchdog as well as a selectable time-out watchdog using the SPI programming. The watchdog timer will not start until the first input trigger event when in normal operation mode. The watchdog timer is only operational in normal mode and is off in standby and sleep modes. The LIMP pin provides a limp home capability when connected to external circuitry. When in sleep or standby mode, the limp pin is off. When the error counter reaches the watchdog trigger event level, the LIMP pin turns on connecting V_{SUP} to the pin as described in the LIMP pin section.

9.4.8.1 Watchdog Error Counter

The TLIN1441-Q1 has a watchdog error counter. This counter is an up down counter that increments for every missed window or incorrect input watchdog trigger event. For every correct input trigger, the counter decrements but does not drop below zero. The default trigger for this counter to trigger a nWDR output trigger is for every event. On every WD error event, the nWDR pin goes low as a watchdog error output trigger. For Pin control, the value is on every event. In SPI communication mode, this counter can be changed to the fifth or ninth consecutive incorrect input trigger. The error counter can be read at register 8'14[4:1].

The error counter is set at four by default. This means that when the watchdog error count is set at five and the first input failure will be treated as if the fifth event has taken place. When set at nine and no correct inputs the fifth event will be treated as the failure event. This allows the system to check the counter after the first input trigger to see if a valid input was sent. nINT will be pulled low on each incorrect watchdog input while V_{CC} and nWDR will behave according to register configuration

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9.4.8.2 Pin Control Mode

When using pin control for programming the watchdog, the WDT pin is used for this function. WDT sets the total window size of the window watchdog. It can be connected to VCC, GND or left open. The electric table provides the window values. The ratio between the upper (open window) and lower (closed window) is 50/50. WDI pin is used by they controller to trigger the watchdog input. The WDI input is an edge-triggered event and supports both rising and falling edges. A filter time of t_W is used to avoid noise or glitches causing a false trigger. A pulse would be treated as a two input trigger events and cause the nWDR pin to be pulled low. nWDR pin is connected to the controller reset pin and if a watchdog event happens this pin is pulled low.

9.4.8.3 SPI Control Programming

When pin 9 (PIN/nCS) is connected to a high-Z processor I/O the device is configured for SPI communication. Registers 8'h13 through 8'h15 control the watchdog function when the device is in SPI communication mode. These register are provided in table Table 6 . The device watchdog can be set as a time-out watchdog or window watchdog by setting 8'h13[6] to the method of choice. The timer is based upon reg8'h13[3:2] WD prescaler and reg8'h14[7:5] WD timer and is in ms. See Table 3 for the achievable times.

Table 3. Watchdog Window and Time-out Timer Configuration (ms)

WD_TIMER (ms)	reg13[5:4] WD_PRE			
reg14[7:5]	00	01	10	11
000	4	8	12	16
001	32	64	96	128
010	128	256	384	512
011	256	384	512	768
100	512	1024	1536	2048
101	2048	4096	6144	8192
110	10240	20240	RSVD	RSVD
1111	RSVD	RSVD	RSVD	RSVD

9.4.8.4 Watchdog Timing

The TLIN1441-Q1 provides two methods for setting up the watchdog when in SPI communication mode, Window or Time-out. If more frequent, < 64 ms, input trigger events are desired it is suggested to us the Time-out timer. When using Time-out watchdog the input trigger can occur anywhere before the timeout and is not tied to an open window.

When using the window watchdog it is important to understand the closed and open window aspects. The device is set up with a 50%/50% open and closed window and is based on an internal oscillator with a ± 10% accuracy range. To determine when to provide the input trigger, this variance needs to be taken into account. Using the 64 ms nominal total window provides a closed and open window that are each 32 ms. Taking the ± 10% internal oscillator into account means the total window could be 57.6 ms or 70.4 ms. The closed and open window would then be 22.4 ms or 35.2 ms. From the 57.6 ms total window and 35.2 ms closed window the total open window is 22.4 ms. The trigger event needs to happen at the 46.4 ms ± 11.2 ms. The same method is used for the other window values. Figure 25 provides the above information graphically.

9.5 Programming

The TLIN1441-Q1 is 7 bit address access SPI communication port.

The Addresses for each area of the device are as follows

- Register 8'h00 through 0A are Device ID and Revision Registers
- Register 8'h0B through 10 are device configuration registers and Interrupt Flags
- Register 8'h11 through 12 are for read and write scratch pad
- Register 8'h13 through 15 are for the watchdog read and write scratch pad

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Programming (continued)

9.5.1 SPI Communication

The SPI communication uses a standard SPI interface. Physically the digital interface pins are nCS (Chip Select Not), SDI (SPI Data In), SDO (SPI Data Out) and CLK (SPI Clock). Each SPI transaction is an 8 bit word containing a seven bit address with a R/W bit followed by a data byte. The data shifted out on the SDO pin for the transaction always starts with the register h'0C[7:0] which is the interrupt register. This register provides the high level interrupt status information about the device. The data byte which are the 'response' to the address and R/W byte are shifted out next. Data bytes shifted out during a write command is content of the registers prior to the new data being written and updating the registers. Data bytes shifted out during a read command are the content of the registers and the registers will not be updated.

The SPI data input data on SDI is sampled on the low to high edge of CLK. The SPI output data on SDO is changed on the high to low edge of CLK.

9.5.1.1 Chip Select Not (nCS)

This input pin is used to select the device for a SPI transaction. The pin is active low, so while nCS is high the SPI Data Output (SDO) pin of the device is high impedance allowing an SPI bus to be designed. When nCS is low the SDO driver is activated and communication may be started. The nCS pin is held low for a SPI transaction. A special feature on this device allows the SDO pin to immediately show the Global Fault Flag on a falling edge of nCS.

9.5.1.2 Serial Clock Input (CLK)

This input pin is used to input the clock for the SPI to synchronize the input and output serial data bit streams. The SPI Data Input is sampled on the rising edge of CLK and the SPI Data Output is changed on the falling edge of the CLK. See .

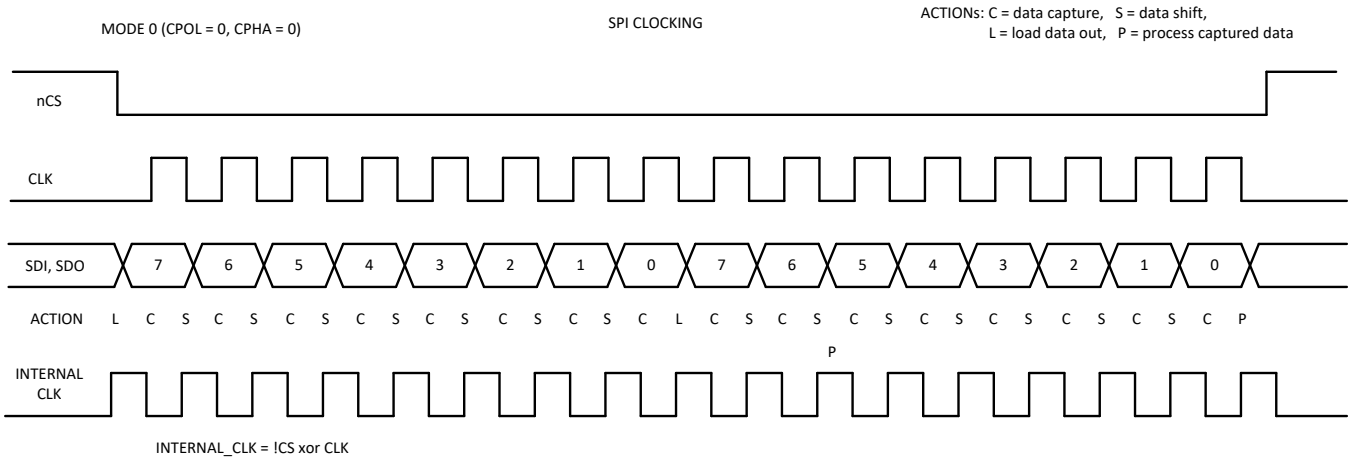


Figure 35. SPI Clocking

9.5.1.3 Serial Data Input (SDI)

This input pin is used to shift data into the device. Once the SPI is enabled by a low on nCS, the SDI samples the input shifted data on each rising edge of the SPI clock (SCK). The data is shifted into an 8 bit shift register. After eight (8) clock cycles and shifts, the addressed register is read giving the data to be shifted out on SDO. After eight clock cycles, the shift register is full and the SPI transaction is complete. If the command code was a writes the new data is written into the addressed register only after exactly 8 bits have been shifted in by CLK and the nCS has a rising edge to deselect the device. If there are not exactly 8 bits shifted in to the device the during one SPI transaction (nCS low), the SPI command is ignored, the SPIERR flag is set and the data is not written into the device preventing any false actions by the device.

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Programming (continued)

9.5.1.4 Serial Data Output (SDO)

This pin is high impedance until the SPI output is enabled via nCS. Once the SPI is enabled by a low on nCS, the SDO is immediately driven high or low showing the Global Fault Flag status which is also the first bit (bit 7) to be shifted out if the SPI is clocked. On the first falling edge of CLK, the shifting out of the data continues with each falling edge on CLK until all 8 bits have been shifted out the shift register.

See and for read and write method.

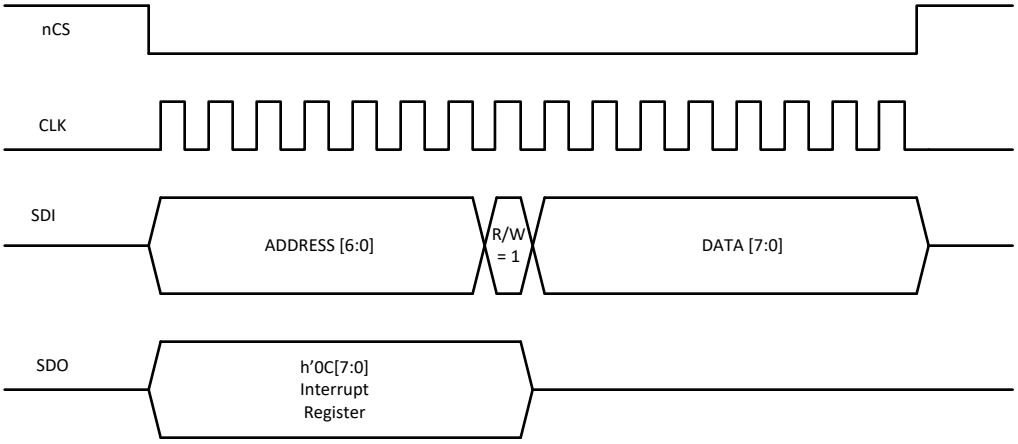


Figure 36. SPI Write

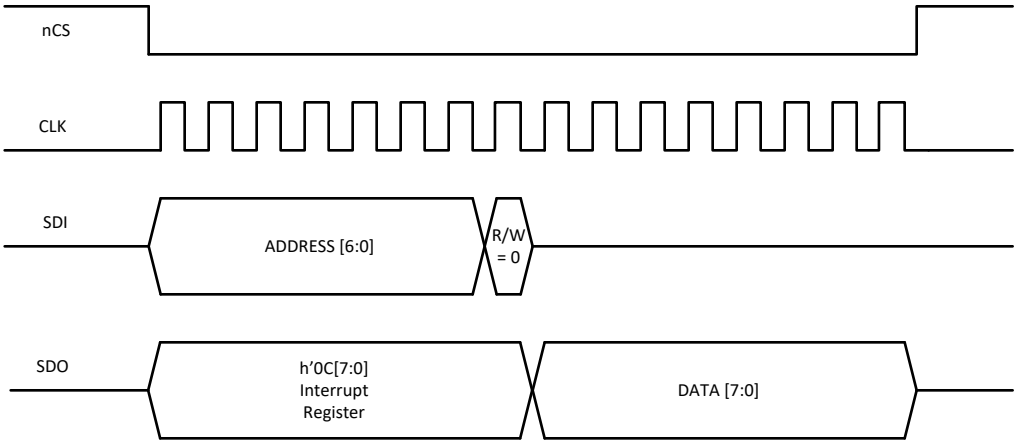


Figure 37. SPI Read

9.6 Registers

The following tables contain the registers that the device use during SPI communication

Table 4. Device ID and Revision

ADDRESS	REGISTER	VALUE	ACCESS
‘h00	Reserved	54	R
‘h01	Reserved	43	R
‘h02	Reserved	41	R
‘h03	Reserved	4E	R
‘h04	Reserved	32	R
‘h05	DEVICE_ID[7:0] "4"	34	R
‘h06	DEVICE_ID[7:0] "4"	34	R
‘h07	DEVICE_ID[7:0] "1"	31	R
‘h08	DEVICE_ID[7:0] “3” "5"	33,35	R
‘h09	Rev_ID Major	01	R
‘h0A	REV_ID Minor	00	R

Table 5. Device Configuration and Flag Registers

ADDRESS	BIT(S)	DEFAULT	DESCRIPTION	ACCESS
'h0B	7:6	2'b00	MODE: Modes of Operation 00 = Standby Mode 01 = Sleep Mode 10 = Normal Mode 11 = Reserved	R/W/U
	5	1'b0	LIMP_DIS: LIMP Disable 0 = LIMP Enabled 1 = LIMP Disabled	R/W/U
	4:3	2'b00	LIMP_SEL_RESET: Selects the method LIMP is reset/turned off 00 = On the third successful input trigger the error counter receives 01 = First correct input trigger 10 = SPI write 1 to h'0B[2] 11 = Reserved	R/W
	2	1'b0	LIMP Reset - Writing a one resets LIMP but then clears	R/WC
	1	1'b0	FAILSAFE_EN: Fail safe mode enable 0 = Disabled 1 = Enabled	R/W
	0	1'b0	DTO_DIS: Dominant timeout Disable 0 = DTO Enabled 1 = DTO Disabled	R/W
'h0C	7	1'b0	DTO Interrup	R/WC
	6	1'b0	UVCC Interrupt	R/WC
	5	1'b0	TSD Interrupt	R/WC
	4	1'b0	SPIERR Interrupt	R/WC
	3	1'b0	WDERR Interrupt	R/WC
	2	1'b0	OVCC Interrupt	R/WC
	1	1'b0	LWU Interrupt	R/WC
	0	1'b0	WUP Interrupt	R/WC
'h0D	7:0	8'h00	Reserved	R

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Table 5. Device Configuration and Flag Registers (continued)

ADDRESS	BIT(S)	DEFAULT	DESCRIPTION	ACCESS
'h0E	7	1'b1	DTO Interrupt Mask	R/W
	6	1'b1	UVCC Interrupt Mask	R/W
	5	1'b1	TSD Interrupt Mask	R/W
	4	1'b1	SPIERR Interrupt Mask	R/W
	3	1'b1	WDERR Interrupt Mask	R/W
	2	1'b1	OVCC Interrupt Mask	R/W
	1	1'b1	LWU Interrupt Mask	R/W
	0	1'b1	WUP Interrupt Mask	R/W
'h0F	7:0	8'h00	Reserved	R
'h10	7:4	4'b0000	Reserved	R
	3:2	1'b0	nRST_nWDR_SEL: Pin 12 configuration select when in SPI mode. 00 = nRST (Default) 01 = nWDR 10 = Both nRST for UV_{CC} and nWDR for watchdog failure event 11 = Reserved	R/W
	1	1'b0	Reserved	R
	0	1'b0	SOFT_RST: Soft reset of device. Writing a 1 resets the registers to default values	R/WC

Table 6. Device Watchdog Registers

ADDRESS	BIT(S)	DEFAULT	DESCRIPTION	ACCESS
'h11	7:0	8'h00	Read and Write Capable Scratch Pad	R/W
'h12	7:0	8'h00	Read and Write Capable Scratch Pad	R/W
'h13	7	1'b0	WD_DIS - Watchdog Function Disable 0 = Enabled 1 = Disabled	R/W
	6	1'b0	WD_WINDOW_TIMEOUT_SEL: Configures Watchdog as either a Window or Time-out watchdog 0 = Window 1 = Timeout	R/W
	5:4	2'b00	WD_PRE: Watchdog prescalar 00 = Factor 1 01 = Factor 2 10 = Factor 3 11 = Factor 4	R/W
	3:2	2'b00	WD_ERR_CNT_SET Sets the watchdog event error counter that upon overflow the watchdog output trigger event will take place. Increases with each error and decreases with each correct WD trigger. Will not go below zero. 00 = Immediate trigger on each WD event 01 = 2-Bit: Triggers on the fifth error event 10 = 3-Bit: Triggers on the ninth error event 11 = Reserved	R/W
	1:0	2'b10	WD_ACTION: Selection Action when Watchdog times out or misses a window 00 = nINT will be pulled low 01 = V_{CC} will be turned off for 100 ms and turned back on 10 = nWDR will be toggled high → low → high 11 = Reserved	R/W

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Table 6. Device Watchdog Registers (continued)

ADDRESS	BIT(S)	DEFAULT	DESCRIPTION	ACCESS
'h14	7:5	3'b000	WD_TIMER - Sets the window or timeout times and is based upon the WD_PRE setting - See Table 3	R/W
	4:1	4'b0100	WD_ERR_CNT: Watchdog error counter: Keeps a running count of the errors up to 15 errors	R
	0	1'b0	Reserved	R
'h15	7:0	8'h00	WD_TRIG: Writes to these bits resets the watchdog timer (FF)	WC

NOTE

For WD_ACTION turning off VCC for 100 ms and turning it back on will cause SPI communication to stop during the off time.

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10 Application and Implementation

NOTE

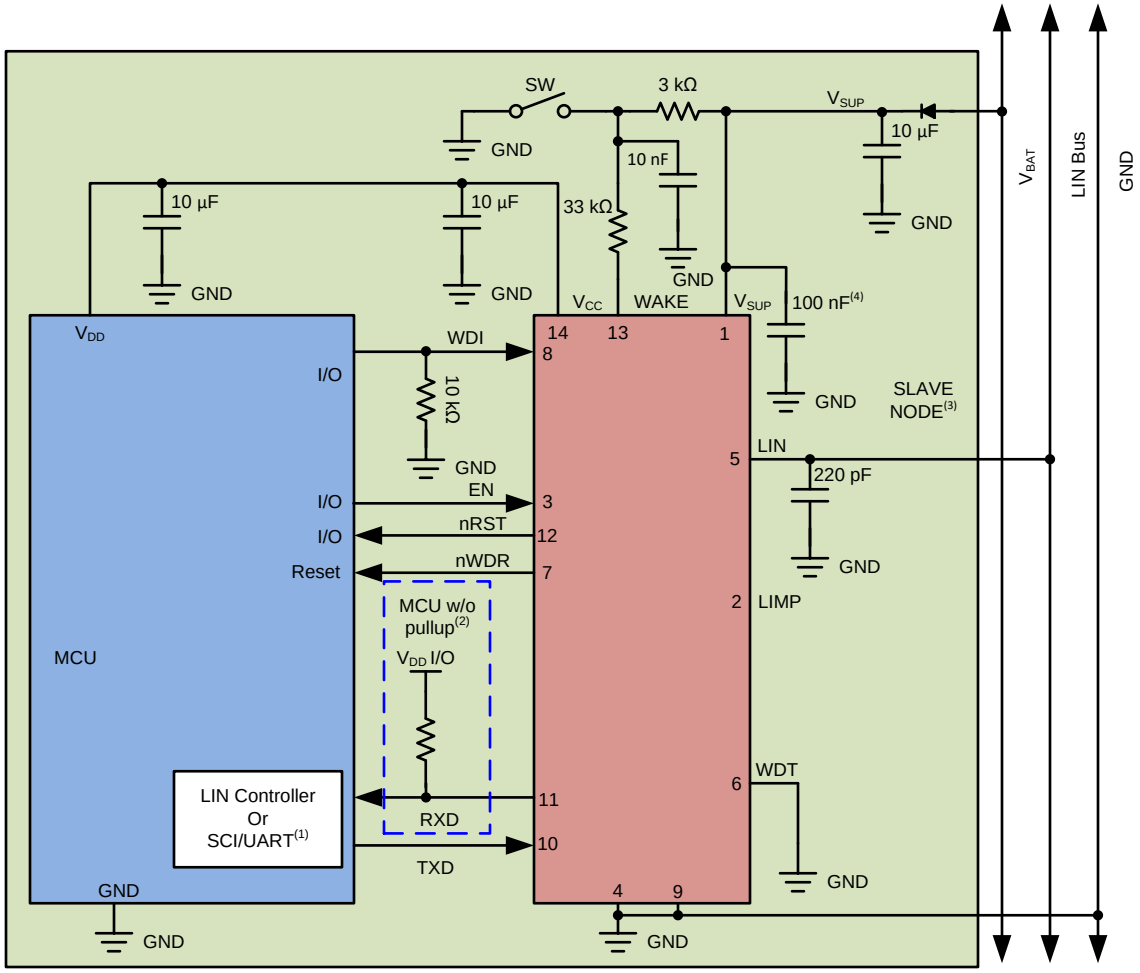
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TLIN1441-Q1 can be used as both a slave device and a master device in a LIN network. The device comes with the ability to support remote wake up request and local wake up request. It can provide the power to the local processor as well as providing watchdog supervision for the processor.

10.2 Typical Application

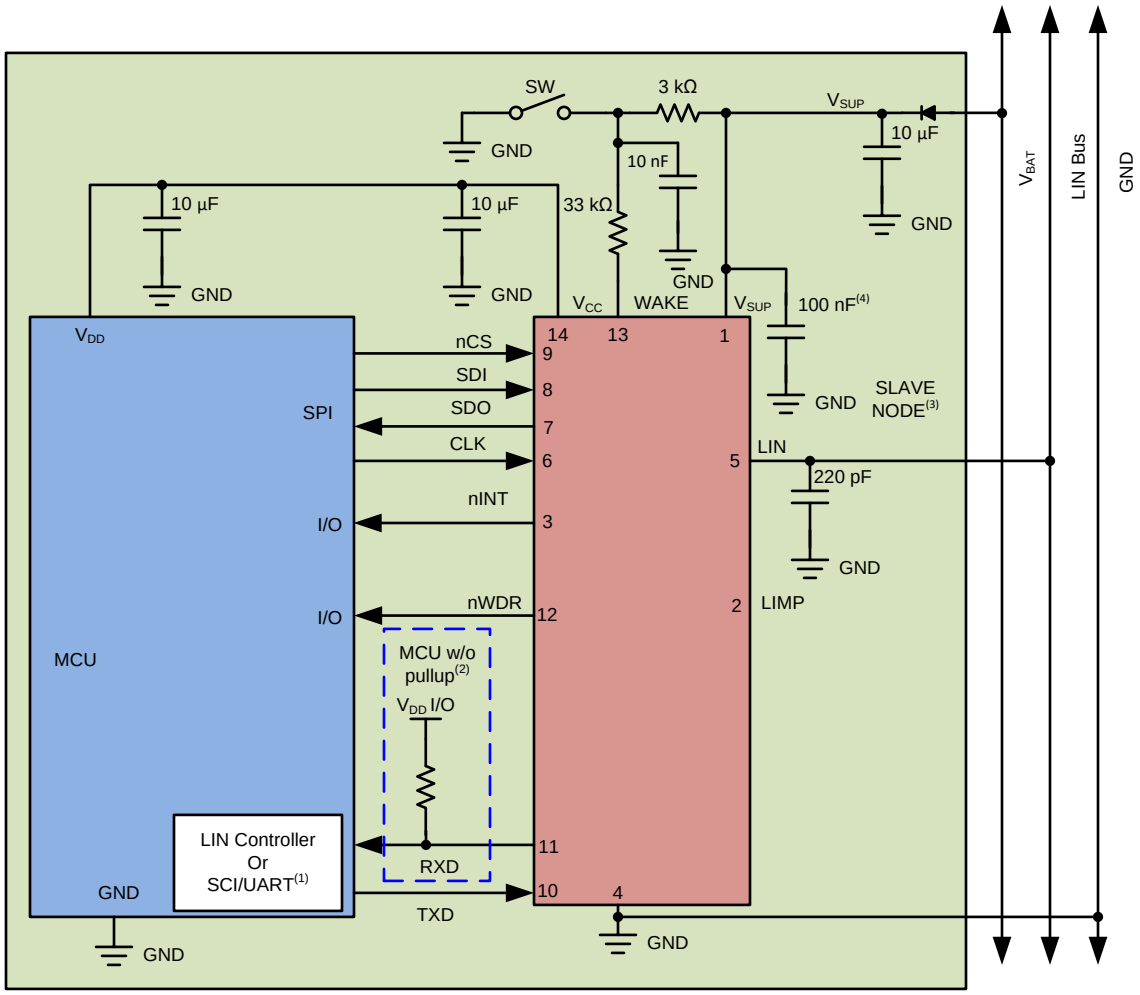
The device comes with an integrated 45 kΩ pull-up resistor and series diode for slave applications. For master applications an external 1 kΩ pull-up resistor with series blocking diode can be used. Figure 38 show the device in pin control mode for a slave application. Figure 39 shows the device in SPI control mode in a slave application.



(1) If RXD on MCU or LIN slave has internal pullup; no external pullup resistor is needed.
(2) If RXD on MCU or LIN slave does not have an internal pullup requires external pullup resistor.
(3) Master node applications require and external 1 kΩ pullup resistor and serial diode.
(4) Decoupling capacitor values are system dependent but usually have 100 nF, 1 µF and ≥10 µF

Figure 38. Typical LIN Slave in Pin Control Mode

Typical Application (continued)



(1) If RXD on MCU or LIN slave has internal pullup; no external pullup resistor is needed.
(2) If RXD on MCU or LIN slave does not have an internal pullup requires external pullup resistor.
(3) Master node applications require and external 1 kΩ pullup resistor and serial diode.
(4) Decoupling capacitor values are system dependent but usually have 100 nF, 1 µF and ≥10 µF

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Figure 39. Typical LIN Slave in SPI Control Mode

Typical Application (continued)

10.2.1 Design Requirements

10.2.1.1 Normal Mode Application Note

When using the TLIN1441-Q1 in systems which are monitoring the RXD pin for a wake up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake up request until t_{MODE_CHANGE}. This is shown in Figure 21 When transitioning to normal mode there is an initialization period shown as $t_{NOMINIT}$.

10.2.1.2 Standby Mode Application Note

If the TLIN1441-Q1 detects an under voltage on V_{SUP}, the RXD pin transitions low and would signal to the software that the device is in standby mode and should be returned to sleep mode for the lowest power state.

10.2.1.3 TXD Dominant State Timeout Application Note

The maximum dominant TXD time allowed by the TXD dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for master and slave applications; thus, there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

10.2.2 Detailed Design Procedures

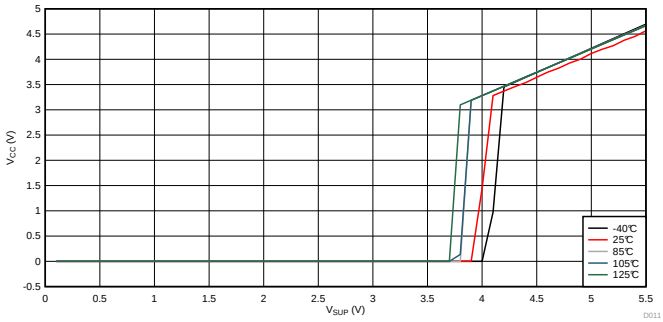
RXD on processors or LIN slave has internal pull-up; no external pull-up resistor is need. RXD on processors or LIN slave without internal pull-up requires external pull-up resistor. Master node applications require and external 1 kΩ pull-up resistor and serial diode.

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Typical Application (continued)

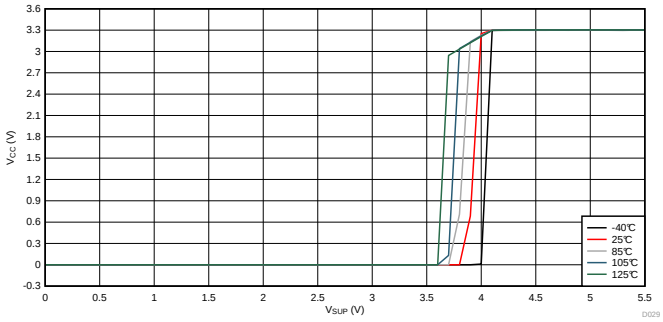
10.2.3 Application Curves

Characteristic curves below show the LDO performance between 0 V and 5.5 V when ramping up and ramping down.



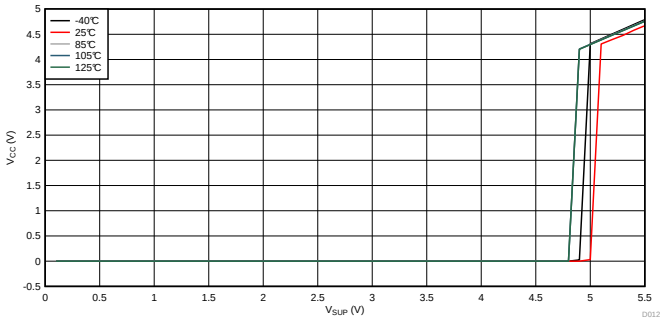
V_{CC} = 5 V I_{CC} Load = 125 mA Ramp Up

Figure 40. V_{CC} vs V_{SUP} Across Temperature



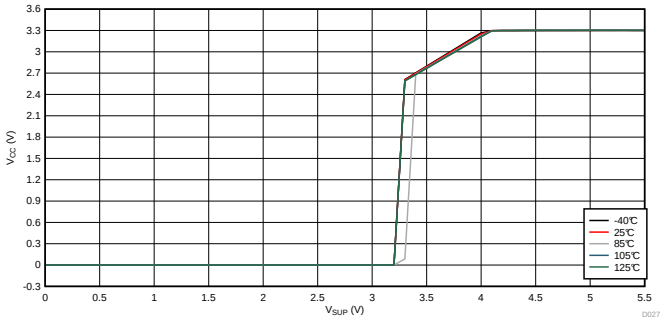
V_{CC} = 3.3 V I_{CC} Load = 125 mA Ramp Up

Figure 41. V_{CC} vs V_{SUP} Across Temperature



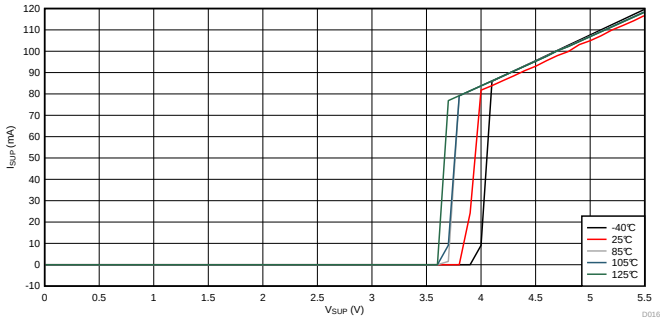
V_{CC} = 5 V I_{CC} Load = 125 mA Ramp Down

Figure 42. V_{CC} vs V_{SUP} Across Temperature



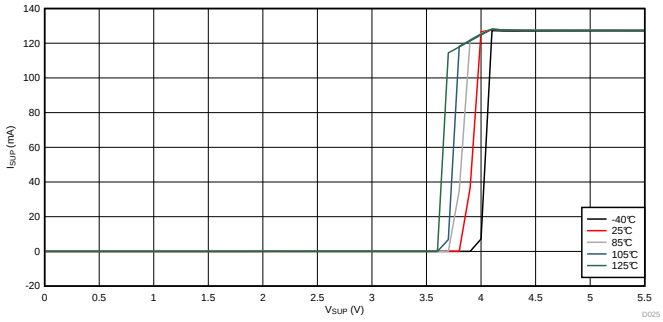
V_{CC} = 3.3 V I_{CC} Load = 125 mA Ramp Down

Figure 43. V_{CC} vs V_{SUP} Across Temperature



V_{CC} = 5 V I_{CC} Load = 125 mA Ramp Up

Figure 44. I_{SUP} vs V_{SUP} Across Temperature

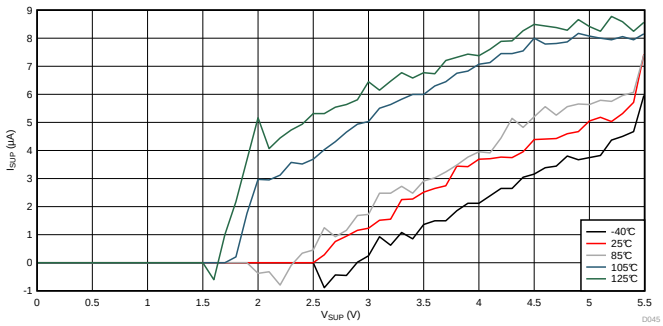


V_{CC} = 3.3 V I_{CC} Load = 125 mA Ramp Up

Figure 45. I_{SUP} vs V_{SUP} Across Temperature

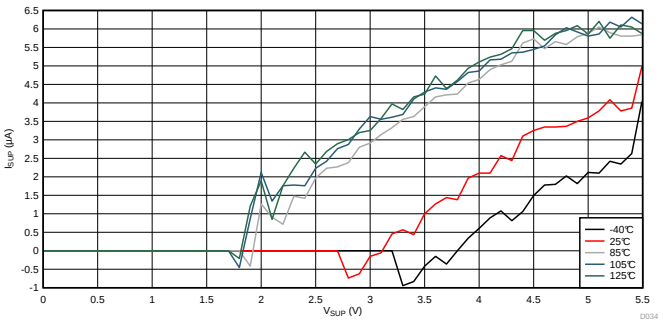
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Typical Application (continued)



V_{CC} = 5 V Sleep Mode Ramp Down

Figure 46. I_{SUP} vs V_{SUP} Across Temperature



V_{CC} = 3.3 V Sleep Mode Ramp Down

Figure 47. I_{SUP} vs V_{SUP} Across Temperature

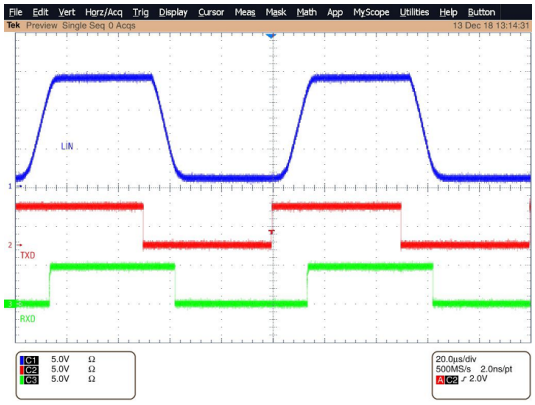


Figure 48. LIN Bus Performance

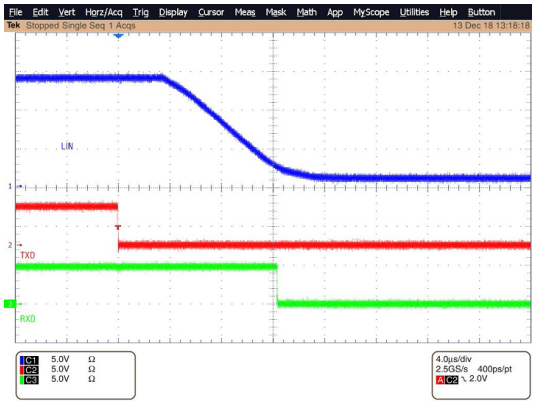


Figure 49. Dominant to Recessive Propagation Delay

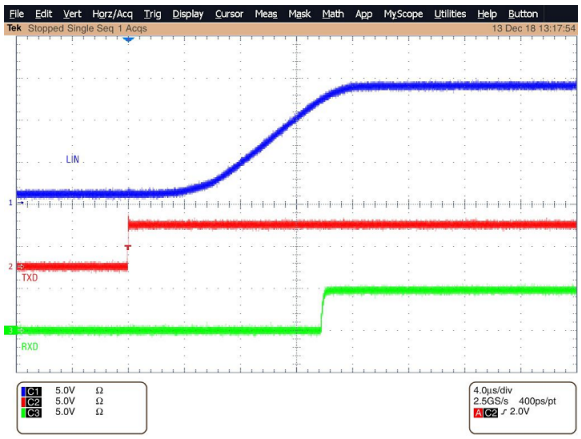


Figure 50. Recessive to Dominant Propagation Delay

11 Power Supply Recommendations

The TLIN1441-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 5.5 V to 36 V . A 100 nF decoupling capacitor should be placed as close to the V_{SUP} pin of the device as possible.

12 Layout

PCB design should start with design of the protection and filtering circuitry because ESD and EFT have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

12.1 Layout Guidelines

- **Pin 1 (V_{SUP}):** This is the supply pin for the device. A 100 nF decoupling capacitor should be placed as close to the device as possible.
- **Pin 2 (LIMP):** This pin is connected to external circuitry for a limp home mode if the watchdog has timed out causing a reset
- **Pin 3 (EN/nINT):** When in pin control mode, this pin is the EN and is an input pin that is used to place the device in a low power sleep mode. If this feature is not used, the pin should be pulled high to the regulated voltage supply of the microprocessor through a series resistor, values between 1 kΩ and 10 kΩ. Additionally, a series resistor may be placed on the pinto limit current on the digital lines in the event of an over voltage fault. When in SPI communication mode, this pin becomes an output interrupt pin that is provided to the processor.
- **Pin 4 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 5 (LIN):** This pin connects to the LIN bus. For slave applications, a 220 pF capacitor to ground is implemented. For master applications, an additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin. See
- **Pin 6 (WDT/CLK):** In pin control mode, this pin can be connected to VCC, GND or left open. In SPI communication mode, this pin is connected directly to the processor as the SPI CLK input.
- **Pin 7 (nWDR/SDO):** In pin control mode. this pin is connected to the processors reset pin. In SPI communication mode. this pin is connected directly to the processor as the SPI serial data output from the TLIN1441-Q1
- **Pin 8 (WDI/SDI):** In pin control mode, this input pin is connected to the processor. A 10 kΩ resistor should be connected to GND to avoid false triggers upon power up. In SPI communication mode, this pin is connected directly to the processor as the SPI serial data input into the TLIN1441
- **Pin 9 (PIN/nCS):** For pin control mode, this pin should be connected directly to ground. For SPI communication mode, this pin should be connected directly to the processor.
- **Pin 10 (RXD):** The pin is an open drain output and requires and external pull-up resistor in the range of 1 kΩ to 10 kΩ to function properly. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external resistor should be placed between RXD and the regulated voltage supply for the microprocessor. If RXD is connected to the V_{CC} pin a higher pull-up resistor value can be used to reduce standby current.
- **Pin 11 (TXD):** The TXD pin is the transmit input signal to the device from the processors. A series resistor can be placed to limit the input current to the device in the event of an over voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 12 (nRST/nWDR):** By default this pin connects to the processors GPIO to function as an interrupt or reset pin for an under voltage event. For SPI communication mode, this pin can be programmed as a processor reset due to a watchdog failure event.
- **Pin 13 (WAKE):**This pin connects to V_{SUP} through a resistor divider with the center tap connected to a switch to ground or VV_{SUP} and is used as the local wake up pin. A 10 nF capacitor to ground should be placed at this center tap as shown in the application drawings.
- **Pin 14 (V_{CC}):** Output source, either 3.3 V or 5 V depending upon the version of the device and has decoupling capacitors to ground.

NOTE

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

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12.2 Layout Example

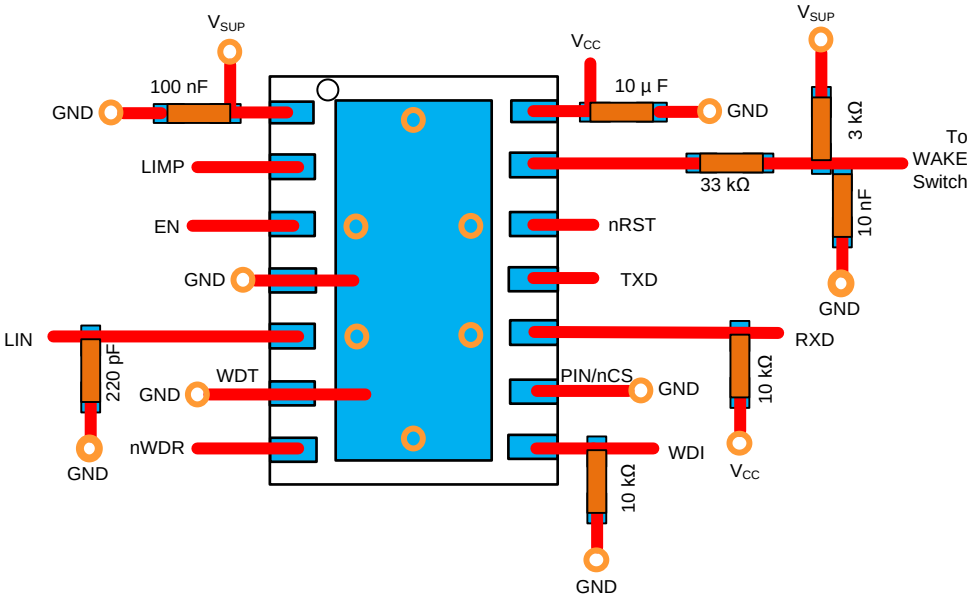


Figure 51. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

LIN Standards:

- ISO/DIS 17987-1.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
- ISO/DIS 17987-4.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V/24V
- SAEJ2602-1: LIN Network for Vehicle Applications
- LIN2.0, LIN2.1, LIN2.2 and LIN2.2A specification

EMC requirements:

- SAEJ2962-2: TBD
- HW Requirements for CAN, LIN, FR V1.3: German OEM requirements for LIN
- ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
- ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
- ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
- ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
- IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
- IEC 61000-4-2
- IEC 61967-4
- CISPR25

Conformance Test requirements:

- ISO/DIS 17987-7.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
- SAEJ2602-2: LIN Network for Vehicle Applications Conformance Test

TLINx441 LDO Performance, SLLA427

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

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All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLIN14415DMTTQ1	ACTIVE	VSON	DMT	14	250	TBD	Call TI	Call TI	-40 to 125		Samples
TLIN14413DMTRQ1	PREVIEW	VSON	DMT	14	3000	TBD	Call TI	Call TI	-40 to 125	TL413	
TLIN14413DMTTQ1	PREVIEW	VSON	DMT	14	250	TBD	Call TI	Call TI	-40 to 125	TL413	
TLIN14415DMTRQ1	PREVIEW	VSON	DMT	14	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TL415	
TLIN14415DMTTQ1	PREVIEW	VSON	DMT	14	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TL415	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

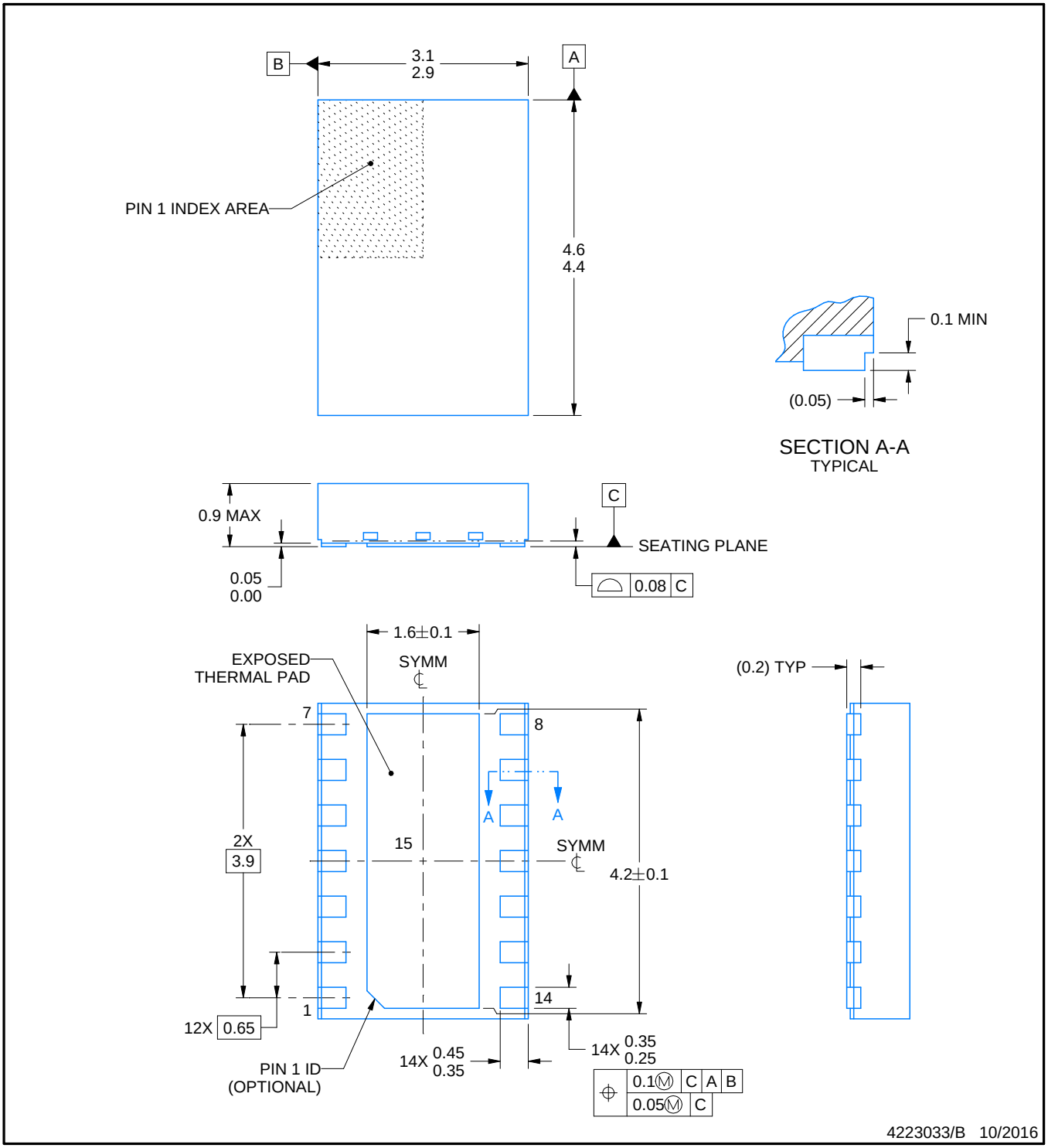
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

DMT0014A

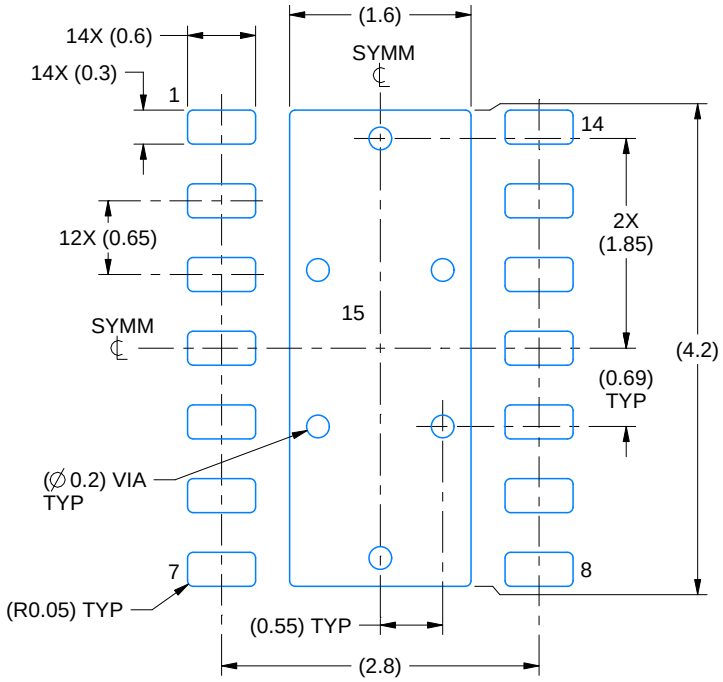
VSON - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

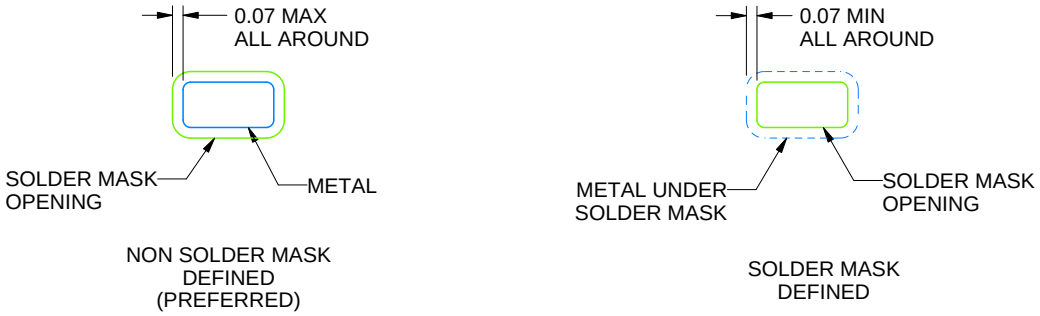


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

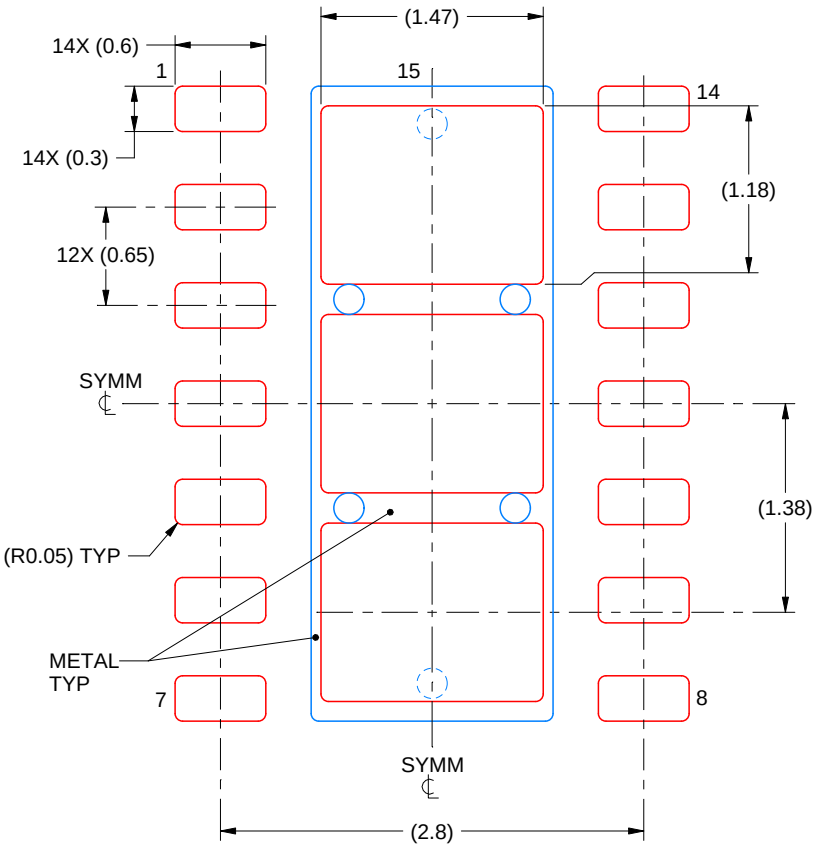


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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