TEXAS INSTRUMENTS

LP8728B-Q1

ZHCSDB0 – FEBRUARY 2015

LP8728B-Q1 四路输出降压 DC-DC 转换器

1 特性

- LP8728B-Q1 是一款经 AECQ-100 1 级认证的汽车级产品
- 四个高效降压 DC-DC 转换器：
  - 93% 峰值效率（V_{IN} = 5V，V_{OUT} = 3.3V）
  - 最大输出电流 1A
  - 强制脉宽调制 (PWM) 运行
  - 软启动控制
  - V_{OUT1} = 3.3V
  - V_{OUT2} = 1.2V
  - V_{OUT3} = 1.8V 或 2.65V（可由引脚选择）
  - V_{OUT4} = 1.5V
- 针对每个转换器控制的独立输入使能
- 针对每个转换器的独立电源正常输出
- 输出过流和输入过压保护
- 过热保护
- 欠压闭锁 (UVLO)

2 应用

- 现场可编程门阵列 (FPGA)，数字信号处理器 (DSP) 内核电源
- 移动器件的处理器电源
- 外设 I/O 电源
- 汽车安全摄像头
- 车用信息娱乐

3 说明

LP8728B-Q1 是一款四路输出电源管理单元 (PMU)，针对面向汽车应用的低功耗现场可编程门阵列 (FPGA)、微处理器以及数字信号处理器 (DSP) 进行了优化。 此器件在单一封装内集成了四个高效降压 DC-DC 转换器。 每个转换器都具有高电流驱动能力以及独立控制，这使得器件能够灵活适应多类应用。 所有转换器均以 3.2MHz 固定开关频率工作于 AM 波段之上。 每个转换器的高侧开关导通时间会进行相移，以最大程度减少输入电流尖峰。
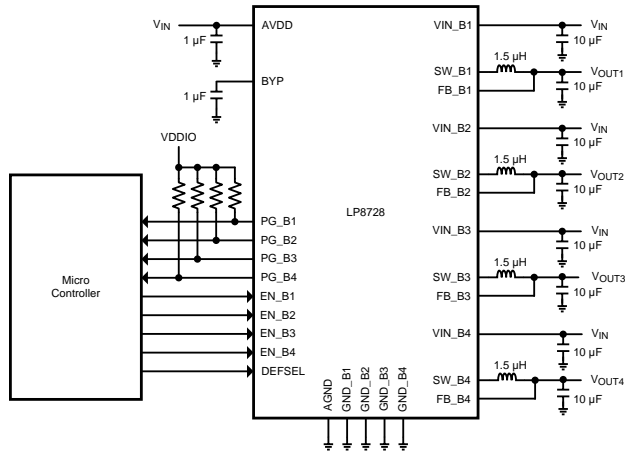
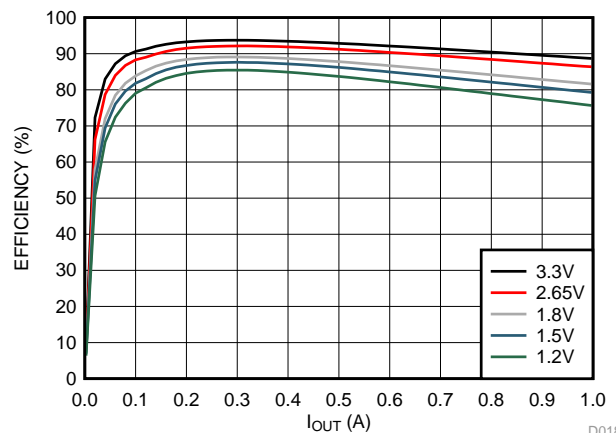保护特性包括输出短路保护、开关电流限制、输入过压保护、输入欠压闭锁和热关断功能。 启动期间，此器件会控制输出转换率以最大限度减少输出电压过冲和输入浪涌电流。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
LP8728B-Q1	WQFN (28)	5.00mm x 5.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图

效率

English Data Sheet: SNVSA70

目录

4 修订历史记录

日期	修订版本	注释
2015 年 2 月	*	最初发布。

5 Pin Configuration and Functions

WQFN (RSG) Package
28 Pins
TOP VIEW
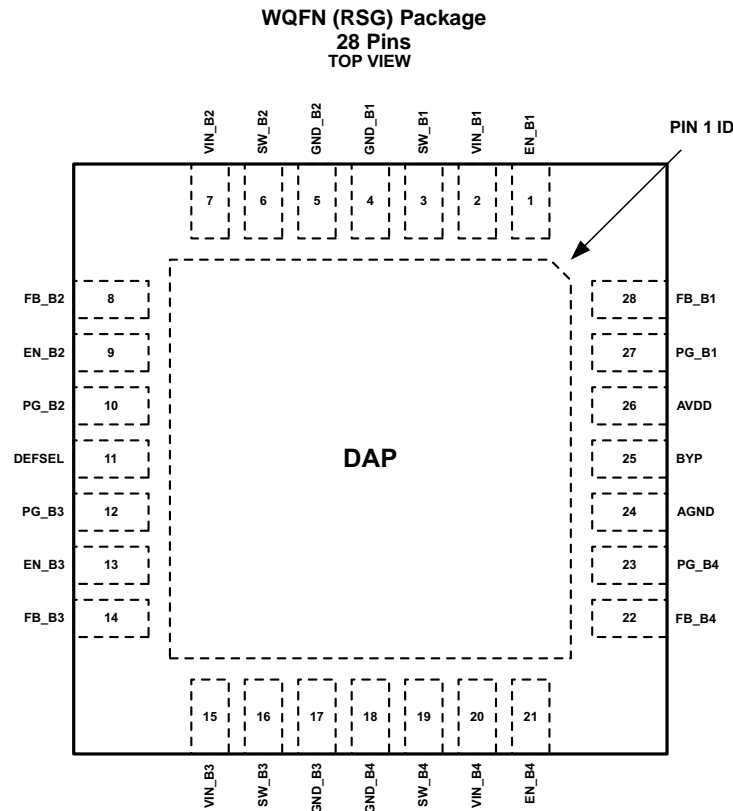
Pin Functions

PIN		TYPE[1]	DESCRIPTION
NUMBER	NAME		
1	EN_B1	D/I	Enable Buck 1
2	VIN_B1	P	Positive power supply input for Buck 1
3	SW_B1	P	Switch node for Buck 1
4	GND_B1	G	Power ground for Buck 1
5	GND_B2	G	Power ground for Buck 2
6	SW_B2	P	Switch node for Buck 2
7	VIN_B2	P	Positive power supply input for Buck 2
8	FB_B2	A	Feedback pin for Buck 2. Referenced against AGND.
9	EN_B2	D/I	Enable Buck 2
10	PG_B2	D/O	Open-drain Power Good output for Buck 2
11	DEFSEL	D/I	Buck 3 output voltage selection pin
12	PG_B3	D/O	Open-drain Power Good output for Buck 3
13	EN_B3	D/I	Enable Buck 3
14	FB_B3	A	Feedback pin for Buck 3. Referenced against AGND.
15	VIN_B3	P	Positive power supply input for Buck 3
16	SW_B3	P	Switch node for Buck 3
17	GND_B3	G	Power ground for Buck 3
18	GND_B4	G	Power ground for Buck 4
19	SW_B4	P	Switch node for Buck 4

(1)   A: Analog Pin, G: Ground Pin, P: Power Pin, O: Output Pin, D/I: Digital Input, D/O: Digital Output.

Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NUMBER	**NAME**		
20	VIN_B4	P	Positive power supply input for Buck 4
21	EN_B4	D/I	Enable Buck 4
22	FB_B4	A	Feedback pin for Buck 4. Referenced against AGND.
23	PG_B4	D/O	Open-drain Power Good output for Buck 4
24	AGND	G	Analog ground
25	BYP	A	Internal 1.8-V supply voltage capacitor pin. A ceramic low-ESR 1-µF capacitor should be connected from this pin to AGND. The BYP voltage is generated internally, do not supply or load this pin externally.
26	AVDD	P	Analog positive power supply pin (V_{IN} level)
27	PG_B1	D/O	Open-drain Power Good output for Buck 1
28	FB_B1	A	Feedback pin for Buck 1. Referenced against AGND.
DAP	Die Attachment Pad		Exposed die attachment pad should to be connected to GND plane with thermal vias to improve the thermal performance of the system.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{IN}	Voltage on power pins (AVDD, VIN_Bx)	−0.3	6	V
V_{FB}	Voltage on feedback pins (FB_Bx)	−0.3	6	V
V_{SW}	Voltage on buck converter switch pins (SW_Bx)	(GND_Bx – 0.2 V) to (VIN_Bx + 0.2 V) with 6 V max		V
V_{DIG}	Voltage on digital pins (PG_Bx, EN_Bx, DEFSEL)	(AGND – 0.2V) to (AVDD + 0.2 V) with 6 V max		V
V_{BYP}	Voltage on BYP pin	−0.3	2	V
$T_{J(MAX)}$	Maximum operating junction temperature[2]		150	°C
	Maximum lead temperature (Soldering)	See[3]		
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typical) and disengages at T_J = 130°C (typical).
(3) For detailed soldering specifications and information, please refer to Texas Instruments Application Note *Leadless Leadframe Package (LLP)* SNOA401.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage on AVDD, VIN_B1, VIN_B2, VIN_B3 and VIN_B4 pins	4.5	5	5.5	V
T_A	Operating ambient temperature[2]	−40		125	°C
C_{OUT}	Effective output capacitance during operation. Min value over T_A –40°C to 125°C.	5	10	12	µF
C_{IN}	Effective input capacitance during operation. 4.5 V ≤ V_{IN_Bx} ≤ 5.5 V. Min value over T_A –40°C to 125°C.	2.5	10		µF
L	Effective inductance during operation Min value over T_A –40°C to 125°C.	0.47	1.5	2	µF

(1) All voltage values are with respect to network ground terminal.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_{D(max)})$

6.4 Thermal Information

	THERMAL METRIC[1]	LP8728-Q1 WQFN (RSG) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	37.7	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	24.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	10.8	
Ψ_{JT}	Junction-to-top characterization parameter	0.3	
Ψ_{JB}	Junction-to-board characterization parameter	10.8	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Calculated using 4-layer standard JEDEC thermal test board with 5 thermal vias between the die attach pad in the first copper layer and second copper layer.

6.5 Electrical Characteristics[1][2]

Unless otherwise noted, V_{IN} = 5 V, typical values apply for T_A = 25°C, and minimum/maximum limits apply over junction temperature range, T_J = –40°C to 125°C.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SHDN}	Shutdown supply current into power connections	EN_Bx = 0 V		1	6	µA
I_{OP}	Operating current	All buck-converters active, I_{OUT} = 0 mA		20		mA
LOGIC INPUTS (EN_Bx, DEFSEL)						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.6			V
R_{PD_DI}	EN_Bx and DEFSEL internal pulldown resistance		300	520	820	kΩ
T_{H_MIN}	Minimum EN_Bx high time			1		ms
T_{L_MIN}	Minimum EN_Bx low time			10		µs
LOGIC OUTPUTS (PG_Bx)						
V_{OL}	Output low level	I_{SINK} = 3 mA			0.4	V
R_{PU}	Recommended pullup resistor			10		kΩ
BUCK CONVERTERS						
V_{OUT1}	Output voltage for Buck 1	Fixed voltage		3.3		V
V_{OUT2}	Output voltage for Buck 2	Fixed voltage		1.2		V
V_{OUT3}	Output voltage for Buck 3	DEFSEL = 1		2.65		V
		DEFSEL = 0		1.8		
V_{OUT4}	Output voltage for Buck 4	Fixed voltage		1.5		V
V_{FB_Bx}	Output voltage accuracy		–3%		3%	
ΔV_{OUT}	Line regulation	4.5 V ≤ V_{IN_Bx} ≤ 5.5 V, I_{LOAD} = 10 mA		3		mV
	Load regulation	V_{IN} = 5 V, 100 mA ≤ I_{LOAD} ≤ 900 mA		3		mV
I_{OUT}	Output current	DC load T_A = 25°C			1000	mA
f_{SW}	Switching frequency		3.03	3.2	3.37	MHz
GBW	Gain bandwidth			300		kHz
I_{LIMITP}	High-side switch current limit		1200	1500	1800	mA
I_{LIMITN}	Low-side switch current limit	Reverse current		500		mA
R_{DSONP}	Pin-pin resistance for PFET	I_{OUT} = 200 mA		210	300	mΩ
R_{DSONN}	Pin-pin resistance for NFET	I_{OUT} = 200 mA		140	240	mΩ
I_{LK_SW}	Switch pin leakage current	V_{OUT} = 1.8V			1	µA

(1) All voltage values are with respect to network ground terminal.
(2) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis. Typical (Typ) numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = 5 V and T_J = 25°C.

Electrical Characteristics[(1)(2)] (continued)

Unless otherwise noted, V_{IN} = 5 V, typical values apply for T_A = 25°C, and minimum/maximum limits apply over junction temperature range, T_J = –40°C to 125°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PD_FB}	Pulldown resistor from FB_Bx pin to GND	Only active when converter disabled. All limits apply for T_A = 25°C	40	70	100	Ω
K_{RAMP}	Slew rate control	DEFSEL from 0 to 1		10		mV/μs
T_{START}	Start-up time	Time from first EN_Bx high to start of switching		420		μs
K_{START}	Soft-start VOUT slew rate			18		mV/μs
VOLTAGE MONITORING						
V_{PG}	Power good threshold voltage	Power good threshold for voltage rising	93.5%	96%	98%	
		Power good threshold for voltage falling	91%	93%	95%	
V_{OVP}	Input overvoltage protection trigger point	Voltage monitored on AVDD Pin, voltage rising	5.5	5.7	5.9	V
		Hysteresis		80		mV
V_{UVLO}	Input undervoltage lockout (UVLO) threshold.	Voltage monitored on AVDD Pin, voltage falling		2.7		V
		Hysteresis		80		mV
THERMAL SHUTDOWN AND MONITORING						
TSD	Thermal shutdown	Threshold, temperature rising		150		°C
		Hysteresis		20		

6.6 System Characteristics[(1)(2)(3)]

Typical values apply for T_A = 25°C. Unless otherwise noted, V_{IN} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{OUT}	Load transient response	I_{OUT} 10% max load → 90% max load, 1-μs load step		70		mV
		I_{OUT} 90% max load → 10% max load, 1-μs load step		70		mV
	Line transient response	V_{IN_Bx} stepping 4.5 V ↔ 5.5 V, t_{RISE} = t_{FALL} = 10 μs, I_{OUT} = 400 mA		20		mV
V_{RIPPLE}	Output voltage ripple	C_{OUT} ESR = 10 mΩ, I_{OUT} = 200 mA		10		mV_{PP}
η	Efficiency	V_{OUT} = 3.3 V, I_{OUT} = 300 mA		94%		
		V_{OUT} = 2.65 V, I_{OUT} = 300 mA		92%		
		V_{OUT} = 1.8 V, I_{OUT} = 300 mA		89%		
		V_{OUT} = 1.5 V, I_{OUT} = 300 mA		87%		
		V_{OUT} = 1.2 V, I_{OUT} = 300 mA		85%		

(1) All voltage values are with respect to network ground terminal.
(2) Minimum (Min) and Maximum (Max) limits are specified by design, test, or statistical analysis. Typical (Typ) numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = 5 V and T_J = 25°C.
(3) System Characteristics are highly dependent on external components and PCB layout. System Characteristics are verified using inductor type: TOKO MDT2520-CN1R5M, input and output capacitor type: MuRata GRM21BR71A106KE51L.

6.7 Typical Characteristics

Unless otherwise noted, V_{IN} = 5 V, T_A = 25°C, inductor type: TOKO MDT2520-CN1R5M, input and output capacitor type: MuRata GRM21BR71A106KE51L.
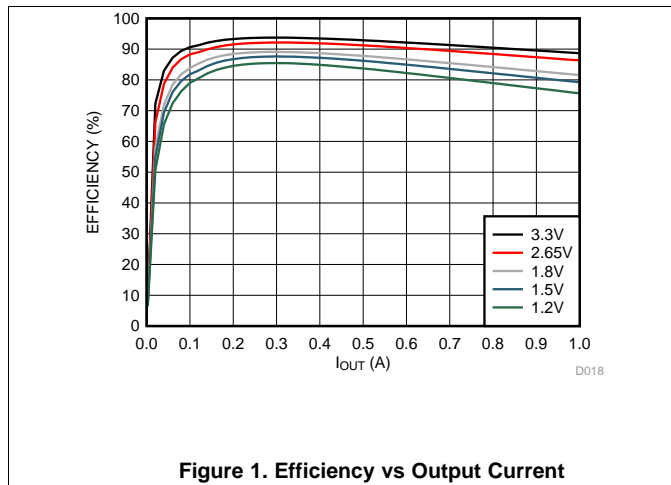
Figure 1. Efficiency vs Output Current

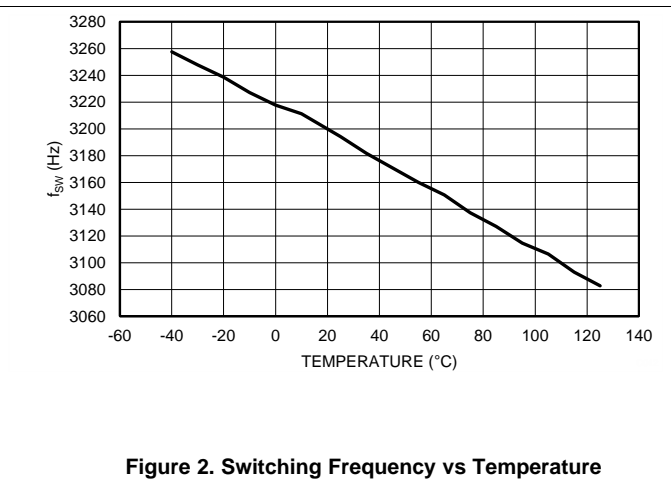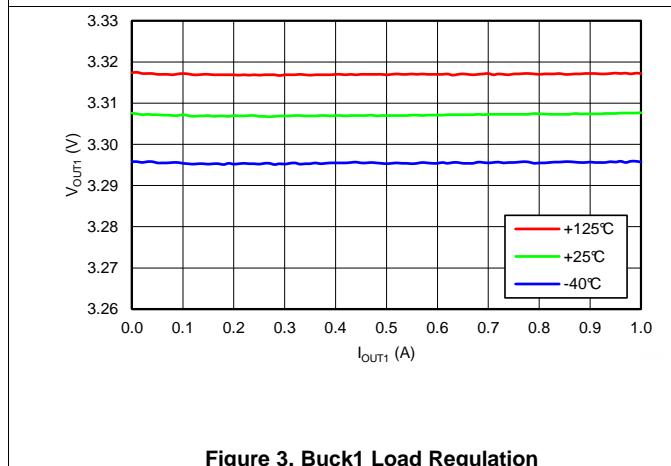**Figure 2. Switching Frequency vs Temperature**
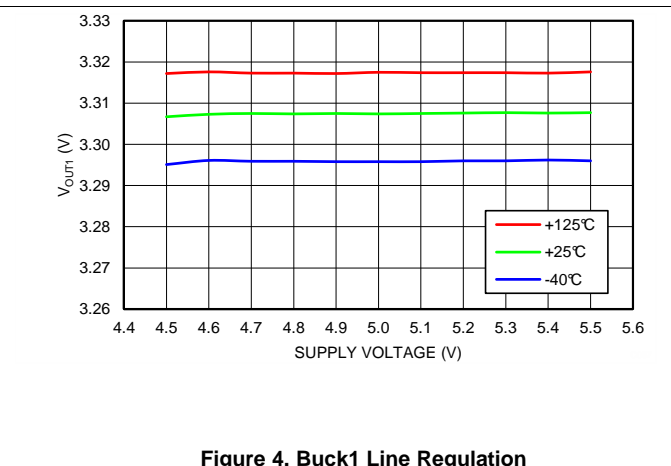
Figure 3. Buck1 Load Regulation

Figure 4. Buck1 Line Regulation
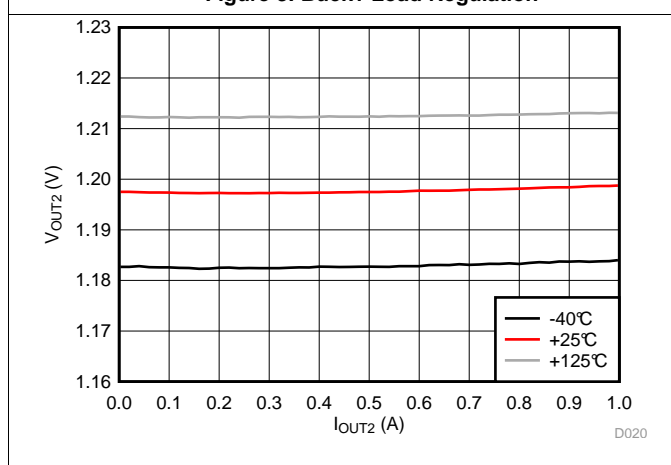
Figure 5. Buck2 Load Regulation
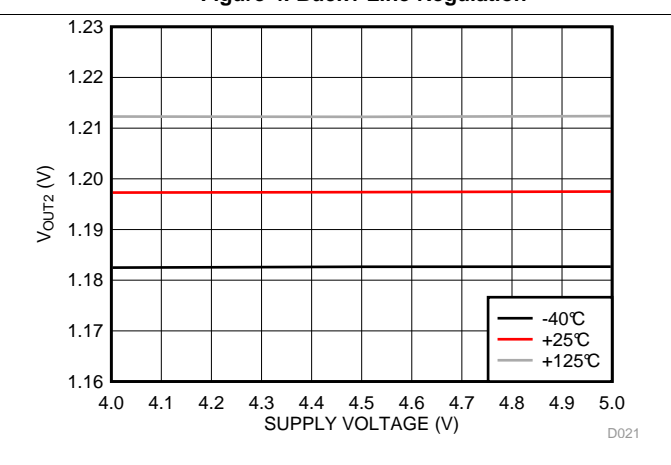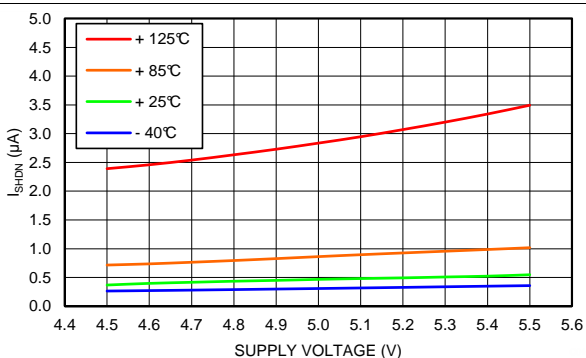
Figure 6. Buck2 Line Regulation

Typical Characteristics (continued)

Unless otherwise noted, V_{IN} = 5 V, T_A = 25°C, inductor type: TOKO MDT2520-CN1R5M, input and output capacitor type: MuRata GRM21BR71A106KE51L.

Figure 7. Shutdown Current Consumption
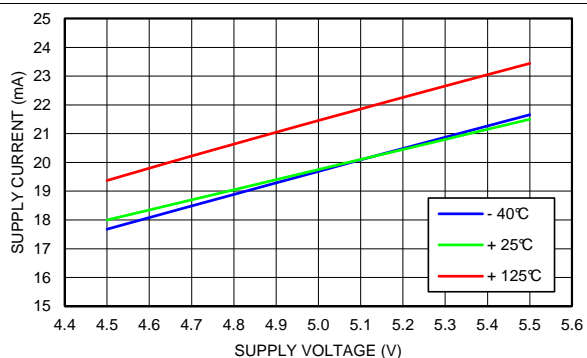
**Figure 8. Active Mode Current Consumption
(All Bucks Active)**

7 Detailed Description

7.1 Overview

The LP8728B-Q1 has four integrated high-efficiency buck converters. Each buck converter has individual enable input and power good output pins. When the first enable pin is pulled high there is a 420-µs start-up delay when the device wakes up from the shutdown mode and all internal reference blocks are started up. Once reference blocks have settled, the corresponding buck converter turns on. Buck cores utilize the soft-start feature to limit the inrush current during start-up. Once a buck output reaches 96% (typical) of the desired output voltage, the power-good pin is pulled high (see Figure 9). When at least one buck core is active, the remaining buck converters will start up without any start-up delay.

If the output voltage drops below 93% (typical) of desired voltage due to, for example, an overload condition, the corresponding power-good pin is pulled low. The power-good signal is always held low for at least 50 ms. When the enable pin is pulled low, the corresponding buck converter's power good signals are set low, and the buck converter is instantly shut down. An output capacitor is then discharged through an internal 70-Ω (typical) pulldown resistor. The pulldown resistor is connected between buck feedback pin and ground and is only active when the enable pin is set low. When all enable signals are pulled low, the LP8728B-Q1 enters a low current shutdown mode.

7.2 Functional Block Diagram
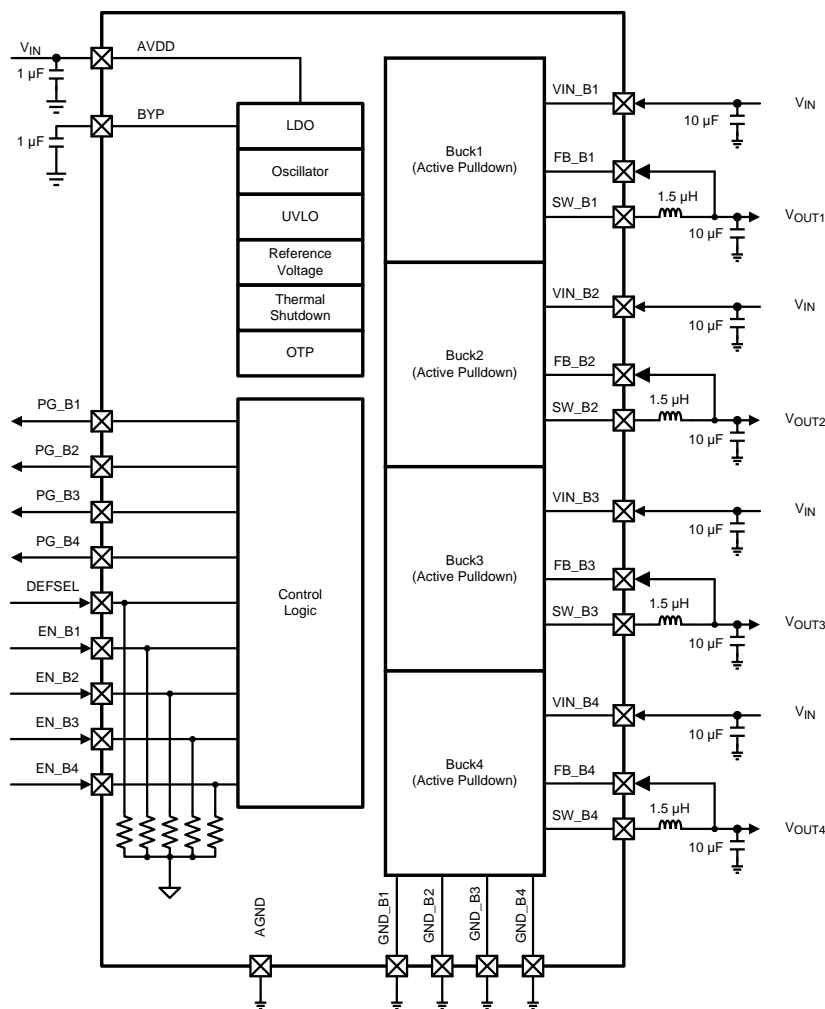
7.3 Feature Description

7.3.1 Buck Information

The buck converters are operated in a forced PWM mode. Even with light load a minimum switching pulse is generated with every switching cycle. Each buck converter's high-side switch turn-on time is phase shifted to minimize the input current ripple (see Figure 20).

7.3.1.1 *Features*

The following features are supported for all converters:

- Synchronous rectification
- Current mode feedback loop with PI compensator
- Forced PWM operation
- Soft start
- Power-good output
- Overvoltage comparator

In addition to the aforementioned features, Buck3 output voltage can be selected with the DEFSEL pin. If the DEFSEL pin is pulled low, V_{OUT3} is set to 1.8 V. If DEFSEL is pulled high, V_{OUT3} is set to 2.65 V.
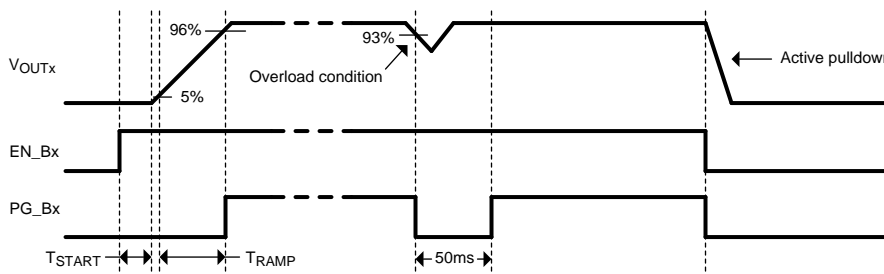
Figure 9. Buck Converter Start-up And Shutdown

7.3.2 Thermal Shutdown (TSD)

Thermal shutdown function shuts down all buck regulators if the device's junction temperature T_J rises above 150°C (typ.). All power-good signals are pulled low 5 ms before the buck regulators are shut down. Once T_J falls below 130°C (typical), the LP8728 will automatically start up the buck regulators. There is a 2-second safety delay included in the restart function. Buck regulators are not restarted until 2 seconds have elapsed after T_J falls below 130°C (typical). To minimize the inrush current during restarting, regulators are started in a Buck1 → Buck2 → Buck3 → Buck4 sequence. A 500-µs delay is included between each buck start-up.
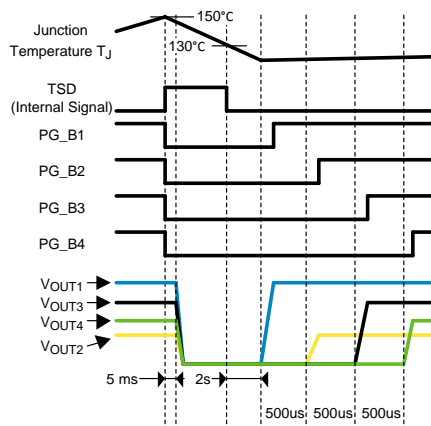
Figure 10. TSD Timing Diagram

Feature Description (continued)

7.3.3 Undervoltage Lockout (UVLO)

If input voltage drops below 2.7 V (typ.) the PG_Bx pins are pulled low and the buck converters are shut down. (Figure 11). The PG_Bx pins are always held low for at least 50 ms. The buck converters are restarted once the input voltage rises above UVLO level.

If a UVLO condition has lasted less than 50 ms, the PG_Bx pins are released high once 50 ms has elapsed and corresponding output voltage has settled. If an overvoltage condition has lasted more than 50 ms, the PG_Bx pins are released high once corresponding output voltage has settled.

Regulators are always restarted in a Buck1 → Buck2 → Buck3 → Buck4 sequence. A 500-µs delay is included between each buck start-up.
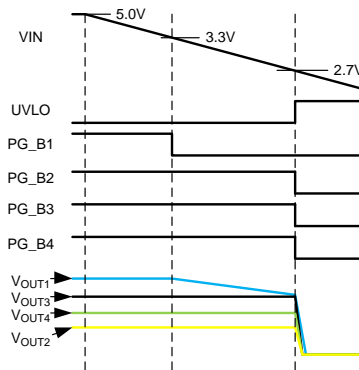
Figure 11. UVLO Operation

7.3.4 Overvoltage Protection (OVP)

Overvoltage protection protects the device in case of an overvoltage condition. If input voltage exceeds 5.7 V (typical), all PG_Bx pins are pulled low. the PG_Bx pins are always held low for at least 50 ms. Once the PG_Bx pins are pulled low, the system has 5 ms time to power down. After an overvoltage condition has lasted for 5 ms, all buck converters are shut down. The buck converters are restarted once input voltage falls below 5.62 V (typical). The buck converters are started in a Buck1 → Buck2 → Buck3 → Buck4 sequence. A 500-µs delay is included between each buck start-up.

If an overvoltage condition lasted more than 5 ms, but less than 50 ms, the PG_Bx pins are released high once 50 ms has elapsed and the corresponding output voltage has settled (Figure 12).
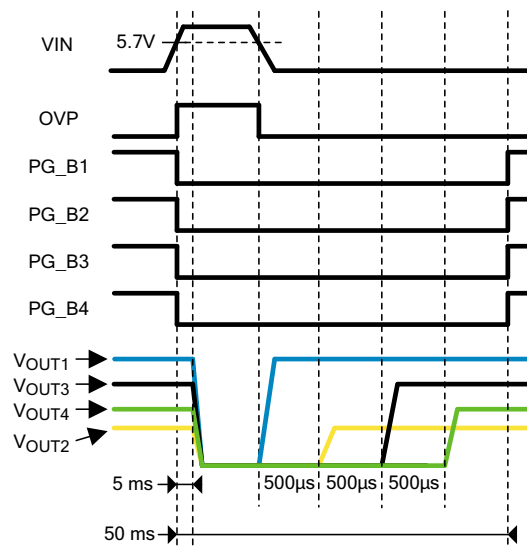

Figure 12. OVP Duration Less Than 50 ms

Feature Description (continued)

If an overvoltage condition has lasted more than 50 ms, the power-good signals are released high once the corresponding output voltage has settled. Regulators are started in a buck1 → buck2 → buck3 → buck4 sequence. A 500-µs delay is included between each buck start-up (Figure 13). If an overvoltage condition has lasted less than 5 ms, the buck converters are not shut down. Even in this case the PG_Bx pins are held low for 50 ms.

> **NOTE**
>
> Since the regulators are allowed to operate for 5 ms during overvoltage condition it is the system designer's responsibility to verify that input voltage doesn't exceed limits stated in *Absolute Maximum Ratings*. Exceeding these limits may cause permanent damage to the device.
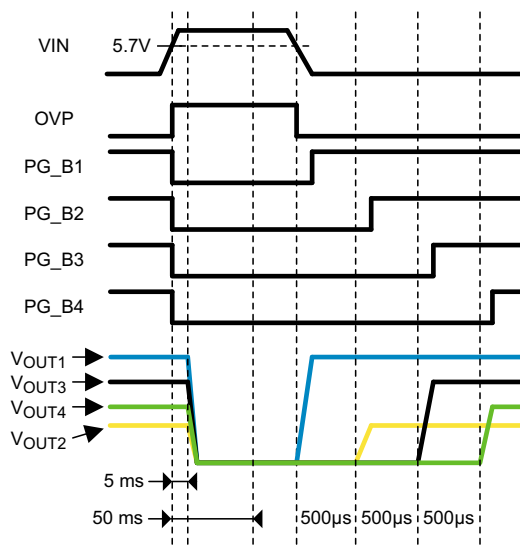

Figure 13. OVP Duration More Than 50 ms

7.4 Device Functional Modes

7.4.1 Shutdown Mode

When all EN_Bx inputs are low, the device is in a Shutdown mode. This is a low-power mode when all buck-regulators and all internal blocks are disabled.

7.4.2 Active Mode

When the first enable pin is pulled high there is a 420-µs start-up delay when the device wakes up from the Shutdown; mode and all internal reference blocks are started up. Once the reference blocks have settled, the corresponding buck converter turns on. Buck cores utilize the soft-start feature to limit the inrush current during start-up. Once a buck output reaches 96% (typical) of the desired output voltage, the power-good pin is pulled high. When at least one buck converter is active device is in a Active mode. When device is in Active mode, the remaining buck converters will start up without any start-up delay when EN_Bx pin is pulled high. When EN_Bx pin is set low the corresponding buck converter will shut down. When all EN_Bx pins are set low the device shuts down all internal reference blocks and enters Shutdown mode.

If output voltage of a buck regulator falls below 93% (typical) of desired voltage due to, for example, an overload condition, the corresponding power good pin is pulled low. Once the output voltage rises back above 96% (typical) of desired voltage power good pin is set back high. Power good signal is held low for at least 50 ms.

Device Functional Modes (continued)

If OVP, or TSD fault occurs during normal operation, all power good pins are pulled low. Once fault condition has lasted for 5 ms all buck converters are shut down. In case of UVLO fault buck regulators are instantly shut down. Once fault condition has ended buck converters are restarted in a Buck1 → Buck2 → Buck3 → Buck4 power-up sequence. A 500-µs delay is included between each buck start-up. In case of TSD fault there is a 2-second safety delay before power-up sequence.
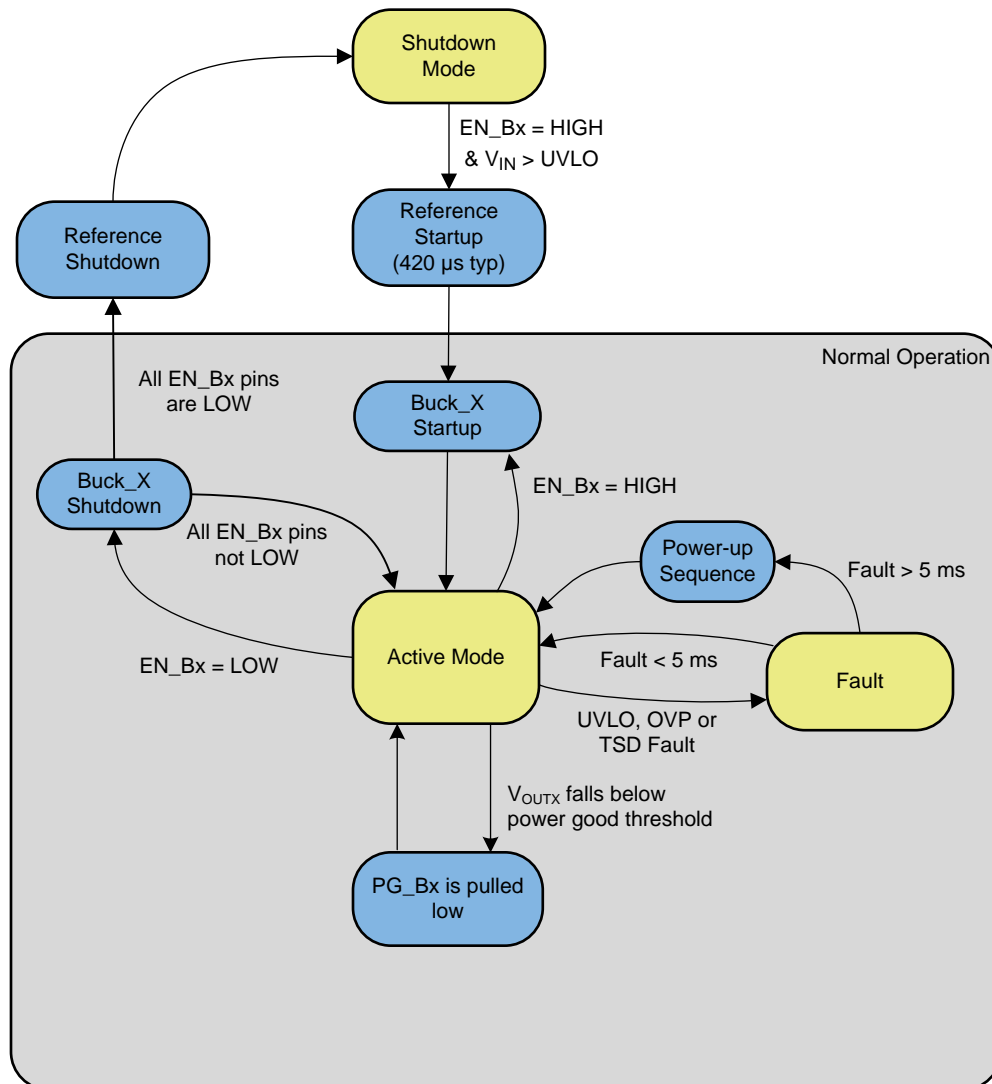
Figure 14. Device Functional Modes

8 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP8728B-Q1 is a quad-output Power Management Unit (PMU), optimized for low-power FPGAs, microprocessors, and DSPs.

8.2 Typical Application

Figure 15 shows an example of a typical application. A microcontroller controls each buck converter with separate enable signals. All four power good signals are connected to a microcontroller with dedicated pullup resistors. If only one master power good signal is required all power good signals can be connected in parallel and pulled up with a single pullup resistor. V_{OUT3} output voltage can be selected with a DEFSEL input. If V_{OUT3} output voltage control is not required during operation, output voltage can be selected by connecting DEFSEL pin to VDDIO or to GND.
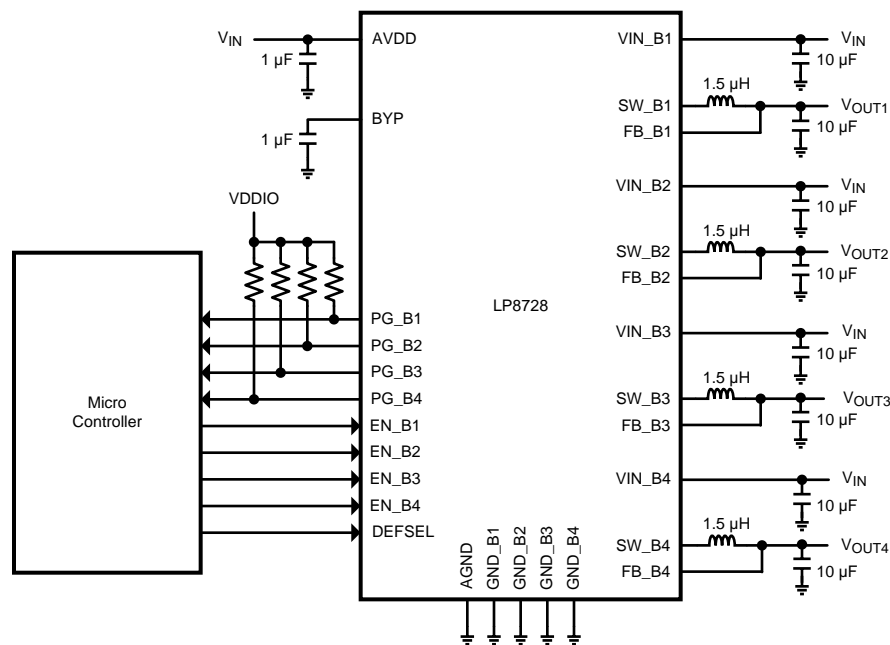
Figure 15. LP8728B-Q1 Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range (V_{IN})	4.5 V to 5.5 V
Buck converter output current	1 A maximum
Buck converter input capacitance	10 µF, 6.3 V
Buck converter output capacitance	10 µF, 6.3 V
Buck converter inductor	1.5 µH, 1.5 A
AVDD pin bypass capacitor	1 µF, 6.3 V
BYP pin bypass capacitor	1 µF, 6.3 V

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor

The four converters operate with 1.5-µH inductors. The inductor has to be selected based on the DC resistance and saturation current. The DC resistance of the inductor directly effects the efficiency of the converter. Therefore, an inductor with the lowest possible DC resistance should be selected for good efficiency. The inductor should have a saturation current rating equal or higher than the high-side switch current limit (1500 mA). To minimize radiated noise shielded inductor should be used. The inductor should be placed as close to the LP8728B-Q1 as possible, and the trace from the inductor to the buck converter switch pin needs to be wide enough to withstand the high switching currents.

8.2.2.2 Input and Output Capacitors

Because buck converters have a discontinuous input current, a low equivalent series resistance (ESR) input capacitor is required for the best input-voltage filtering and to minimize interference with other circuits caused by high input voltage spikes. Each DC-DC converter requires a 10-µF ceramic input capacitor on its input pin VIN_Bx. The input capacitor capacitance can be increased without any limit for better input voltage filtering. Voltage rating of the capacitors should be at least 10V. A small 100-nF capacitor can be used in parallel to minimize high-frequency interferences. Input capacitors should be placed as close to the VIN_Bx pins as possible. Routing from input capacitor to VIN_Bx pins should be done on top layer without using any vias.

An output capacitor with a typical value of 10 µF is recommended for each converter. Ceramic capacitors with low ESR value have lowest output voltage ripple and are recommended.
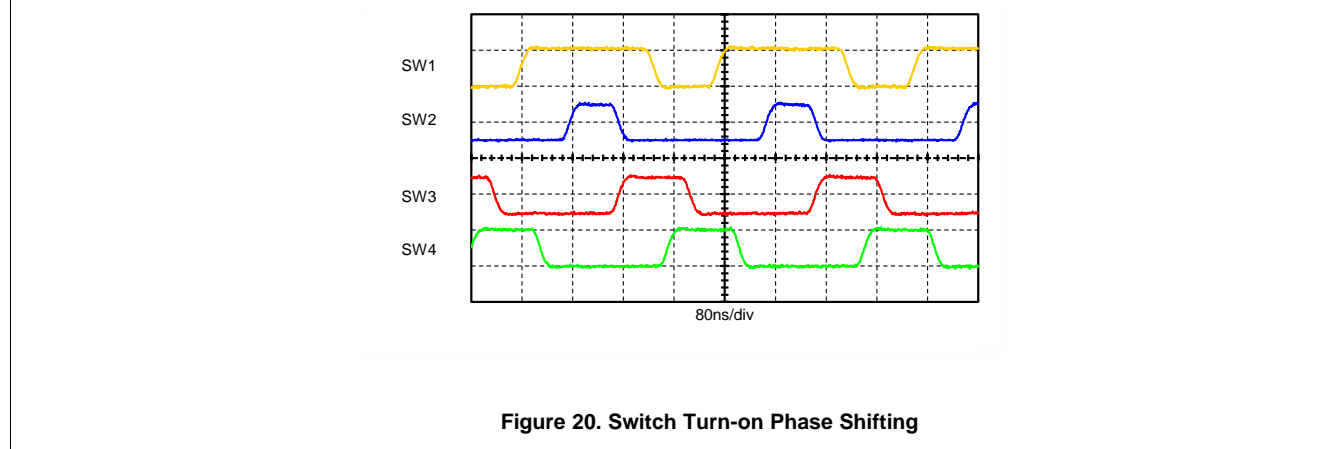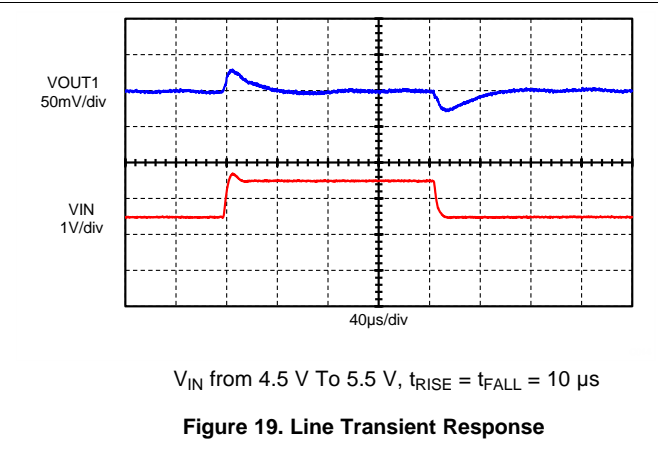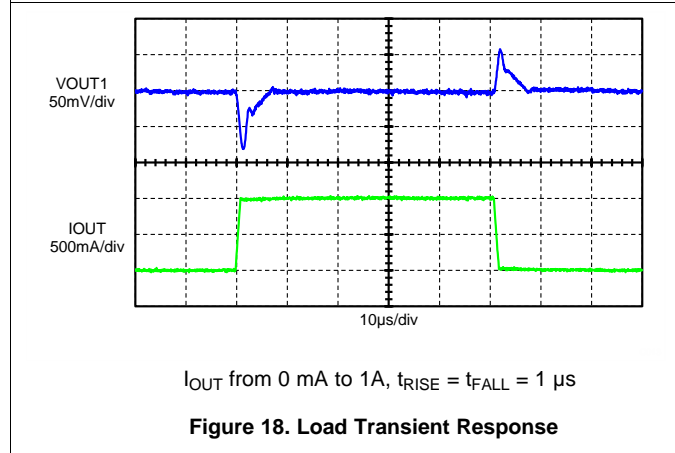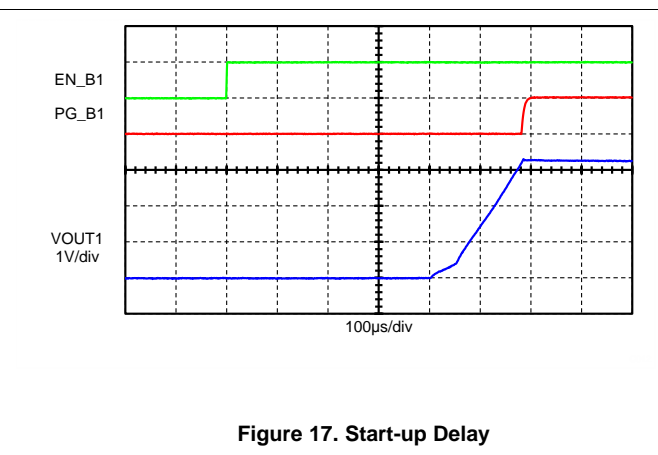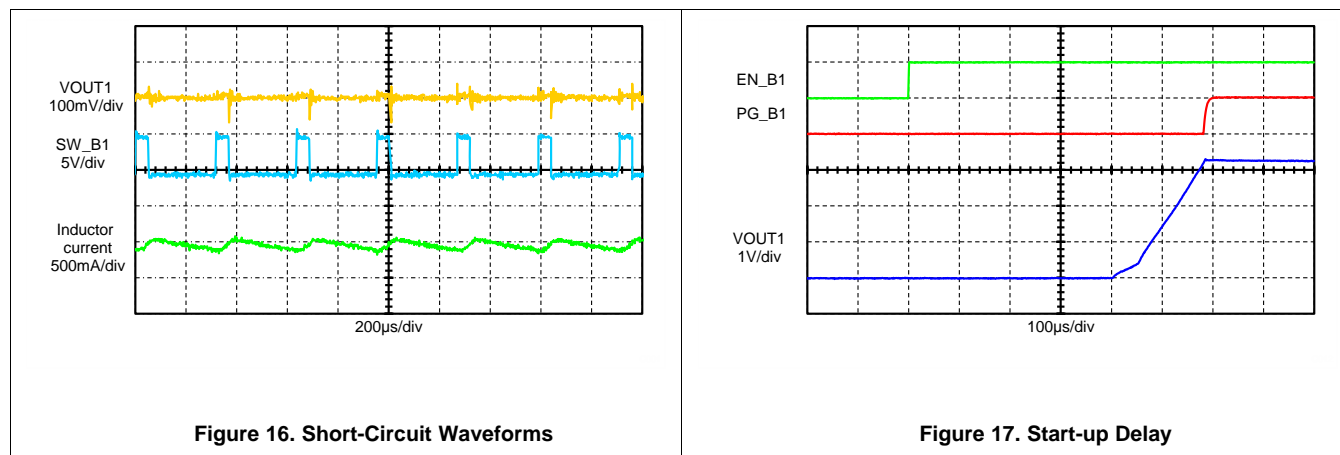
Some ceramic capacitors, especially those in small packages, exhibit a strong capacitance reduction with the increased applied DC voltage (DC bias effect). The capacitance value can fall below half of the nominal capacitance. This needs to be taken into consideration and, if necessary, use a capacitor with higher value or higher voltage rating.

Table 1. Recommended External Components

COMPONENT	DESCRIPTION	VALUE	TYPE	EXAMPLE
$C_{IN\_B1,2,3,4}$	Buck regulator input capacitor	10 µF	Ceramic, 10 V, X7R	MuRata, GRM21BR71A106KE51L
$C_{OUT\_B1,2,3,4}$	Buck regulator output capacitor	10 µF	Ceramic, 10 V, X7R	MuRata, GRM21BR71A106KE51L
C_{AVDD}	AVDD pin input capacitor	1 µF	Ceramic, 10 V, X7R	MuRata, GRM188R71A105KA61D
C_{BYP}	Internal LDO bypass capacitor	1 µF	Ceramic, 10 V, X7R	MuRata, GRM188R71A105KA61D
$L_{SW1,2,3\ 4}$	Buck regulator inductor	1.5 µH	I_{SAT} >1.5 A, DCR < 100 mΩ	TOKO MDT2520-CN1R5M

8.2.3 Application Performance Plots

Unless otherwise noted, V_{IN} = 5 V, T_A = 25°C, inductor type: TOKO MDT2520-CN1R5M, input and output capacitor type: MuRata GRM21BR71A106KE51L.

Figure 16. Short-Circuit Waveforms

Figure 17. Start-up Delay

I_{OUT} from 0 mA to 1A, t_{RISE} = t_{FALL} = 1 µs

Figure 18. Load Transient Response

V_{IN} from 4.5 V To 5.5 V, t_{RISE} = t_{FALL} = 10 µs

Figure 19. Line Transient Response

Figure 20. Switch Turn-on Phase Shifting

9 Power Supply Recommendations

The LP8728B-Q1 is designed to operate from an input voltage supply range between 4.5 V and 5.5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

- AVDD and BYP pins must be bypassed to ground. 1-µF ceramic capacitor is recommended. Place the capacitors close to the AVDD, BYP, and AGND pins.
- AGND pin must be tied to the PCB ground plane. Use multiple vias to minimize the inductance.
- AVDD pin must be connected to PCB VIN plane. Use multiple vias to minimize the inductance.
- Place the buck converter input capacitors as close to the buck input voltage and buck ground pins as possible.
- Place the buck converter output capacitors and inductors so that the buck converter switching loops can be routed on top layer. Try to minimize the area of the switching loops.
- Keep the trace width from switch pin to inductor wide enough to withstand the switching currents. Avoid any excess copper on the switch node to minimize parasitic switch node capacitance.
- Connect the exposed thermal pad to ground plane with multiple thermal vias.
- Avoid routing digital signals directly under the switching loops to avoid interferences.
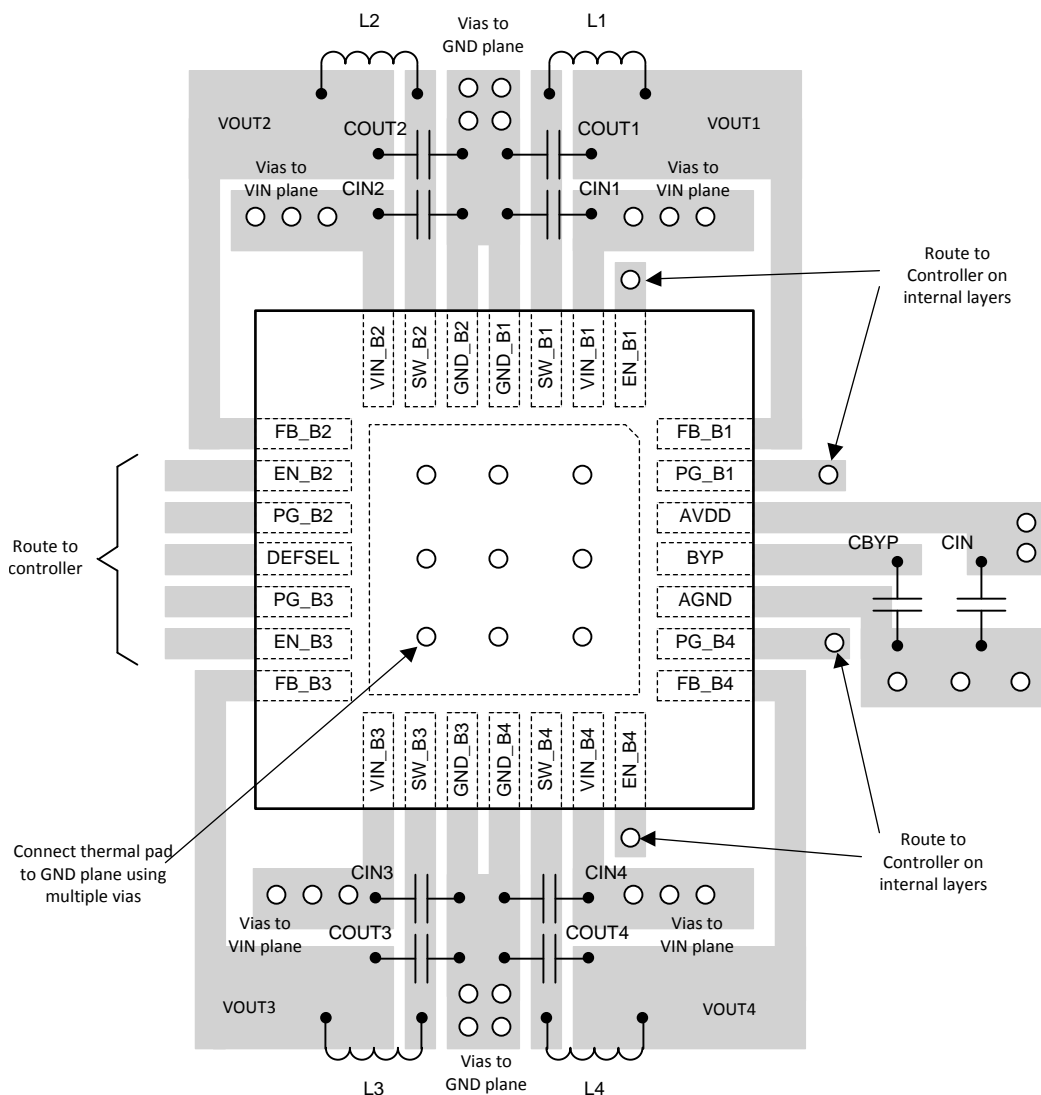
10.2 Layout Example

Figure 21. LP8728B-Q1 Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.2 相关文档

相关文档如下：

德州仪器 (TI) 应用手册 1187《无引线框架封装 (LLP)》（文献编号：SNOA401）。

有关 LP8728 评估模块的更多信息，请参见《使用 LP8728EVM 评估模块》（文献编号：SNVU231）。

11.3 商标

All trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 术语表

SLYZ022 — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或"增强型塑料"的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

产品		应用	
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8728QSQX-B/NOPB	ACTIVE	WQFN	RSG	28	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	8728Q-B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RSG (S−PWQFN−N28)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 ID
(OPTIONAL)

1   7

Exposed Thermal Pad

28   8

2,80±0,10

22   14

21   15

2,80±0,10

Bottom View
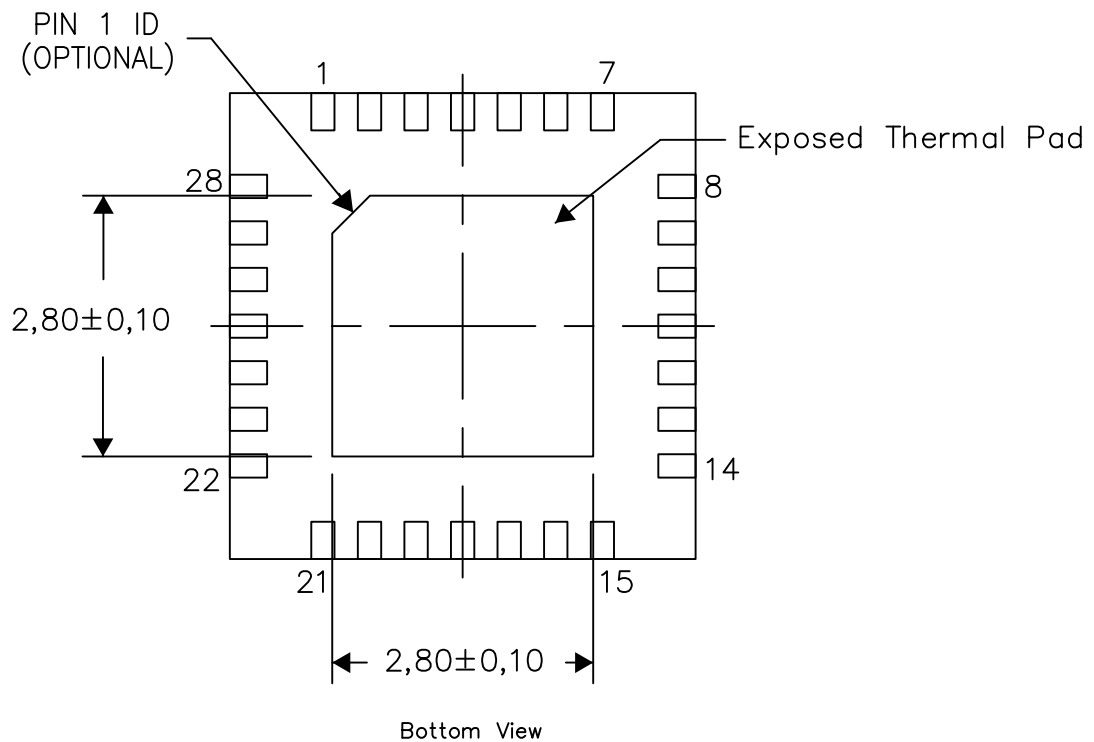
Exposed Thermal Pad Dimensions

4221534−3/B 04/15

NOTE: All linear dimensions are in millimeters

重要声明和免责声明