256MB - 32M x 64 BUFFERED SDRAM MODULE

FEATURES

- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V ± 0.3V Power Supply
- 168 pin DIMM JEDEC

DESCRIPTION

The W3DG6430V is a 32M x 64 synchronous DRAM module which consists of sixteen 32Mx4 SDRAM components in TSOP II package, three very high speed buffers for reduced input capacitance, and one 2K EEPROM in an 8 pin TSSOP package for Serial Presence Detect which are mounted on a 168 pin DIMM multilayer FR4 Substrate.

* This product is not fully qualified or characterized and is subject to change without notice.

PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

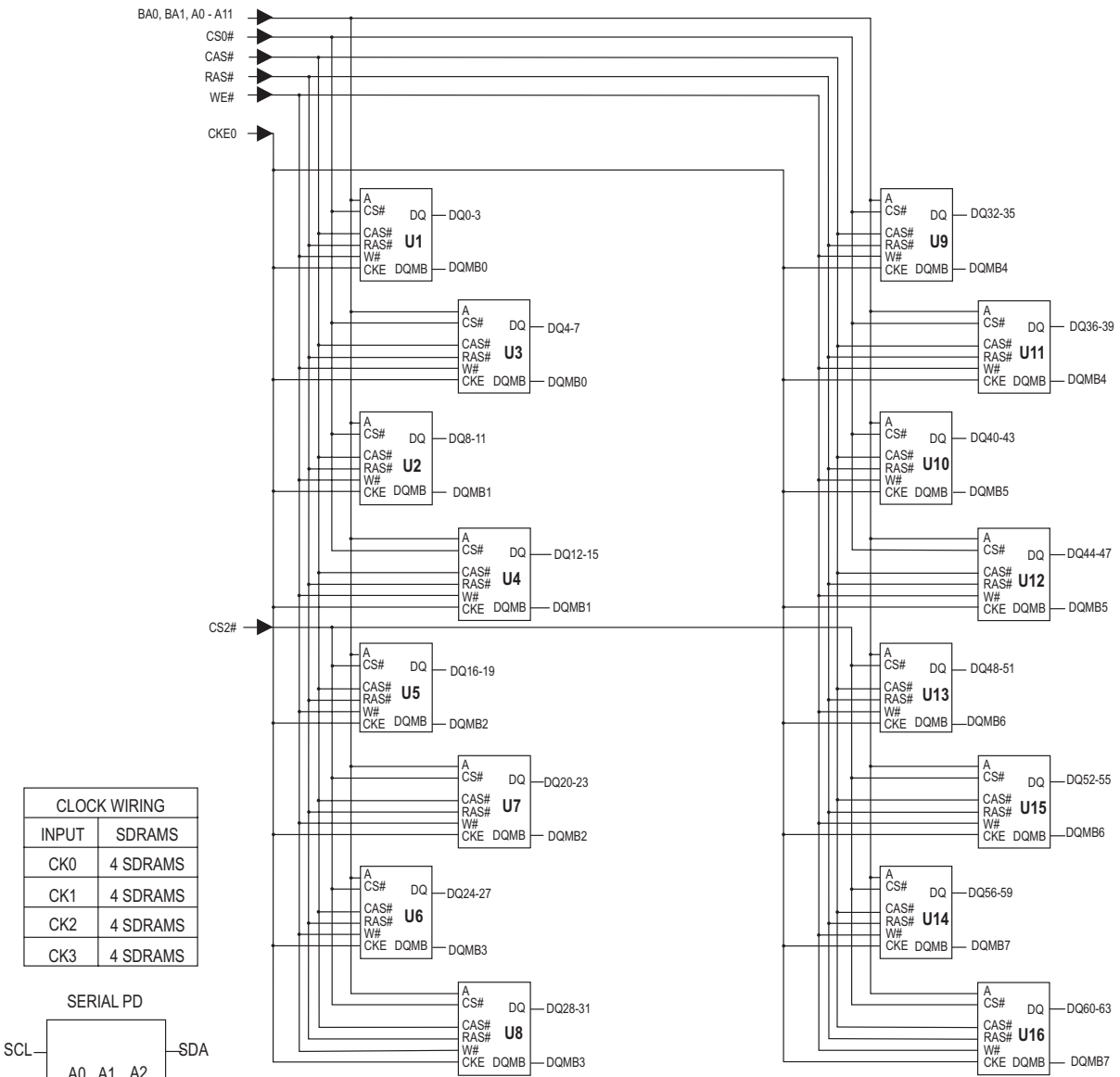
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V_{SS}	29	DQM1	57	DQ18	85	V_{SS}	113	DQM5	141	DQ50
2	DQ0	30	CS0#	58	DQ19	86	DQ32	114	NC	142	DQ51
3	DQ1	31	DNU	59	V_{CC}	87	DQ33	115	RAS#	143	V_{CC}
4	DQ2	32	V_{SS}	60	DQ20	88	DQ34	116	V_{SS}	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V_{CC}	34	A2	62	NC	90	V_{CC}	118	A3	146	NC
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	V_{SS}	92	DQ37	120	A7	148	V_{SS}
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	V_{SS}	40	V_{CC}	68	V_{SS}	96	V_{SS}	124	V_{CC}	152	V_{SS}
13	DQ9	41	V_{CC}	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	NC	154	DQ57
15	DQ11	43	V_{SS}	71	DQ26	99	DQ43	127	V_{SS}	155	DQ58
16	DQ12	44	DNU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2#	73	V_{CC}	101	DQ45	129	NC	157	V_{CC}
18	V_{CC}	46	DQM2	74	DQ28	102	V_{CC}	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DNU	76	DQ30	104	DQ47	132	NC	160	DQ62
21	NC	49	V_{CC}	77	DQ31	105	NC	133	V_{CC}	161	DQ63
22	NC	50	NC	78	V_{SS}	106	NC	134	NC	162	V_{SS}
23	V_{SS}	51	NC	79	CK2	107	V_{SS}	135	NC	163	CLK3
24	NC	52	NC	80	NC	108	NC	136	NC	164	NC
25	NC	53	NC	81	NC	109	NC	137	NC	165	SA0
26	V_{CC}	54	V_{SS}	82	**SDA	110	V_{CC}	138	V_{SS}	166	SA1
27	WE#	55	DQ16	83	**SCL	111	CAS#	139	DQ48	167	SA2
28	DQM0	56	DQ17	84	V_{CC}	112	DQM4	140	DQ49	168	V_{CC}

PIN NAMES

A0 – A11	Address input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CLK0,CLK3	Clock input
CKE0	Clock Enable input
CS0#-CS2#	Chip select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-7	DQM
V_{CC}	Power Supply (3.3V)
V_{SS}	Ground
SDA	Serial data I/O
SCL	Serial clock
DNU	Do not use
NC	No Connect
SA0-SA2	Address in EEPROM

** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM



CLOCK WIRING	
INPUT	SDRAMS
CK0	4 SDRAMS
CK1	4 SDRAMS
CK2	4 SDRAMS
CK3	4 SDRAMS

NOTE: A0-A11, BA0-BA1, WE, RAS, CAS, CS0, CS2, CKE0 are buffered, not registered. 10 ohm registors are in series with all DQ's.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 ~ 4.6	V
Storage Temperature	T_{STG}	-55 ~ +150	°C
Power Dissipation	P_D	8	W
Short Circuit Current	I_{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: V_{SS} = 0V, 0°C ≤ T_A ≤ 70°C

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH}= -2mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL}= -2mA
Input Leakage Current	I_{LI}	-20	—	20	A	1

Note: 1. Any input 0V ≤ V_{IN} ≤ V_{CC} Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

T_A = 23°C, f = 1MHz, V_{CC} = 3.3V, V_{REF}=1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A11)	C_{IN1}	20	pF
Input Capacitance (RAS#,CAS#,WE#)	C_{IN2}	20	pF
Input Capacitance (CKE0)	C_{IN3}	20	pF
Input Capacitance (CLK0,CLK2)	C_{IN4}	13	pF
Input Capacitance (CS0#,CS2#)	C_{IN5}	15	pF
Input Capacitance (DQM0-DQM7)	C_{IN6}	10	pF
Input Capacitance (BA0-BA1)	C_{IN7}	20	pF
Data input/output capacitance (DQ0-DQ63)	C_{OUT}	12	pF

OPERATING CURRENT CHARACTERISTICS

V_{CC} = 3.3V, 0°C ≤ T_A ≤ 70°C

Parameters	Symbol	Conditions	Versions	Units	Note
			100		
Operating Current (One bank active)	I_{CC1}	Burst Length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0mA	1700	mA	1
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	40	mA	
	I_{CC2PS}	CKE & CK ≤ V_{IL}(max), t_{CC} = ∞	40	mA	
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), t_{CC} =10ns Input signals are charged one time during 20	350	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CK ≤ V_{IL}(max), t_{CC}= ∞ Input signals are stable	180	mA	
Active standby current in power-down mode	I_{CC3P}	CKE ≥ V_{IL}(max), t_{CC} = 10ns	90	mA	
	I_{CC3PS}	CKE & CK ≤ V_{IL}(max), t_{CC} = ∞	90		
Active standby in current non power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), t_{CC} = 10ns Input signals are charged one time during 20ns	500	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CK ≤ V_{IL}(max), t_{CC} = ∞ input signals are stable	500	mA	
Operating current (Burst mode)	I_{CC4}	Io = mA Page burst 4 Banks activated t_{CCD} = 2CK	1700	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3300	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	40	mA	

Notes: 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noticed, input swing level is CMOS (V_{IH}/V_{IL} = V_{CC}/V_{SSQ})

AC CHARACTERISTICS

			133MHz component timing			
Paramater		**Symbol**	**Min**	**Max**	**Units**	**Notes**
Access time from CLK	CL = 2	t_{AC}		5.4	ns	
Address hold time		t_{AH}	0.8		ns	
Address setup time		t_{AS}	1.5		ns	
CLK high level width		t_{CH}	2.5		ns	
CLK low level width		t_{CL}	2.5		ns	
Clock cycle time	CL = 2	t_{CK}	7.5		ns	1
CKE hold time		t_{CKH}	0.8		ns	
CKE setup time		t_{CKS}	1.5		ns	
CS, RAS, CAS, WE, DQM hold time		t_{CMH}	0.8		ns	
CS, RAS, CAS, WE, DQM setup time		t_{CMS}	1.5		ns	
Data-in hold time		t_{DH}	0.8		ns	
Data-in setup time		t_{DS}	1.5		ns	
Data-out high-impedance time	CL = 2	t_{HZ}		5.4	ns	2
Data-out low-impedance time		t_{LZ}	1		ns	
Data-out hold time (load)		t_{OH}	3		ns	
Data-out hold time (no load)		t_{N}	1.8		ns	3
Active to Precharge command		t_{RAS}	37	120,000	ns	
Active to Active command period		t_{RC}	60		ns	
Active to Read or Write delay		t_{RCD}	15		ns	
Refresh period		t_{REF}		64	ms	
Auot refresh period		t_{RFC}	66		ns	
Precharge command period		t_{RP}	15		ns	
Active bank a to Active bank b command		t_{RRD}	14		ns	
Transition time		t_{T}	0.3	1.2	ns	4
Write recovery time		t_{WR}	1 CLK + 7ns		ns	5
					ns	6
Exit Self Refresh to Active command		t_{XSR}	67		ns	7

Notes:
1. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including WR and Precharge commands). CKE may be used to reduce the data rate.
2. t_{HZ} defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet t_{OH} before going High-Z.
3. Paramater guaranteed by design
4. AC characteristics assume t_T = 1ns
5. Auto precharge mode only) The precharge timing budget (t_{RP}) begins 7ns after the first clock delay, after the last Write is executed.
6. Precharge mode only.
7. CLK must be toggled a minimum of two times during this period.

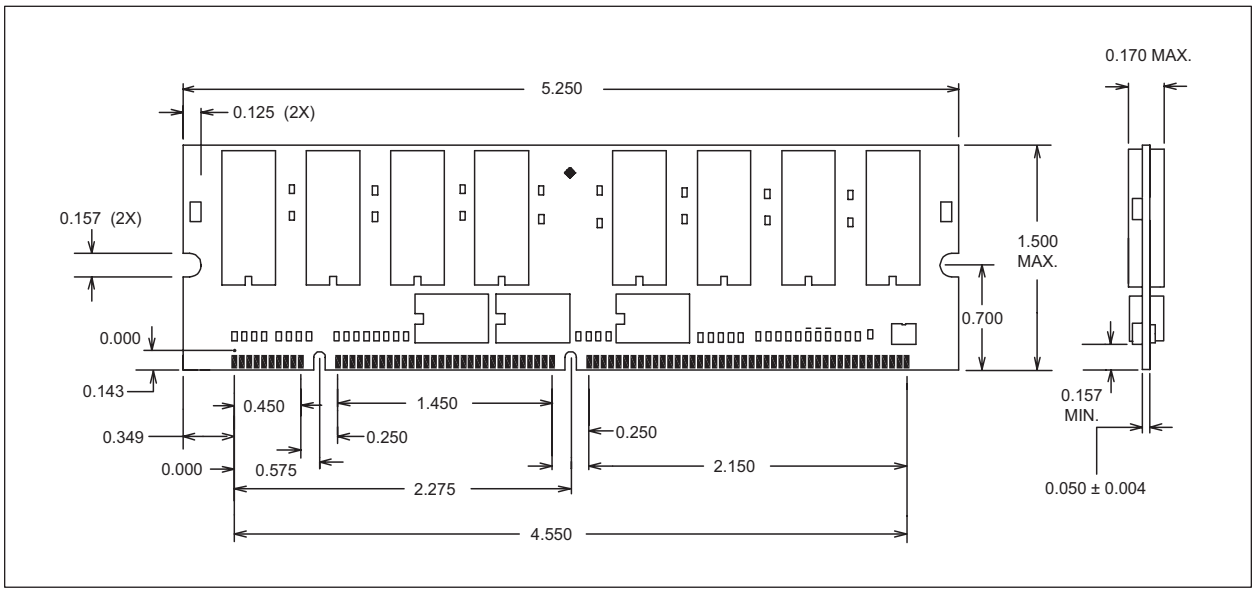
MODULE AC CHARACTERISTIC

	Symbol	**Min**	**Max**	**Units**	**Notes**
Address hold time	AH	0		ns	
Address setup time	AS	4.5		ns	
CS, RAS, CAS, WE, DQM hold time	CMH	0		ns	
CS, RAS, CAS, WE, DQM setup time	CMS	4.5		ns	

ORDERING INFORMATION

Part Number	Speed	CAS Latency
W3DG6430V10D2	100MHz	CL=2

PACKAGE DIMENSIONS



ALL DIMENSIONS ARE IN INCHES