MAX3221 3-V to 5.5-V RS-232 Line Driver and Receiver With ±15-kV ESD Protection

1 Features

- RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU V.28 Standards
- Operates With 3-V to 5.5-V V_{CC} Supply
- Operates up to 250 kbps
- One Driver and One Receiver
- Low Standby Current: 1 μA Typical
- External Capacitors: 4 × 0.1 μF
- Accepts 5-V Logic Input With 3.3-V Supply
- Alternative High-Speed Pin-Compatible Device (1 Mbps)
  – SNx5C3221
- Automatic Power-Down Feature Automatically Disables Drivers for Power Savings

2 Applications

- Battery-Powered, Hand-Held, and Portable Equipment
- Notebooks, Subnotebooks, and Laptops
- Digital Cameras
- Mobile Phones and Wireless Devices

3 Description

The MAX3221 device consists of one line driver, one line receiver with dedicated enable pin, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. These devices operate at data signaling rates up to 250 kbps and a maximum of 30-V/μs driver output slew rate.

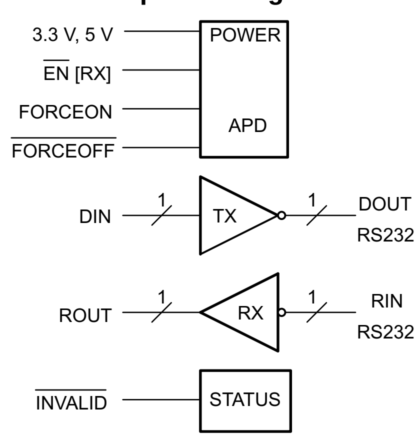
Flexible control options for power management are available when the serial port is inactive. The automatic power-down feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid
RS-232 signal on the receiver input, the driver output is disabled and the supply current is reduced to 1 μA. The $\overline{\text{INVALID}}$ output notifies the user if an RS-232 signal is present at the receiver input.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MAX3221xDB	SSOP (32)	6.20 mm × 5.30 mm
MAX3221xPW	TSSOP (32)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (January 2014) to Revision O — **Page**

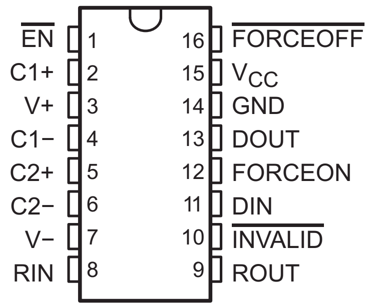
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision M (March 2004) to Revision N — **Page**

- Updated document to new TI data sheet format - no specification changes. 1
- Deleted *Ordering Information* table. 1

5 Pin Configuration and Functions

DB or PW Package
16-Pin SSOP or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	2	—	Positive terminals of the voltage-doubler charge-pump capacitors
C2+	5		
C1–	4	—	Negative terminals of the voltage-doubler charge-pump capacitors
C2–	6		
DIN	11	I	Driver input
DOUT	13	O	RS-232 driver output
$\overline{EN}$	1	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
$\overline{FORCEOFF}$	16	I	Automatic power-down control input
FORCEON	12	I	Automatic power-down control input
GND	14	—	Ground
$\overline{INVALID}$	10	O	Invalid output pin. Output low when all RIN inputs are unpowered.
RIN	8	I	RS-232 receiver input
ROUT	9	O	Receiver output
V_{CC}	15	—	3-V to 5.5-V supply voltage
V+	3	O	5.5-V supply generated by the charge pump
V–	7	O	–5.5-V supply generated by the charge pump

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
	V_{CC} to GND		–0.3	6	V
	V+ to GND		–0.3	7	
	V– to GND		0.3	–7	
	V+ + |V–|[2]			13	
V_I	Input voltage	DIN, $\overline{\text{EN}}$, $\overline{\text{FORCEOFF}}$, and FORCEON to GND	–0.3	6	V
		RIN to GND		±25	
V_O	Output voltage	DOUT to GND		±13.2	V
		ROUT to GND	–0.3	V_{CC} + 0.3	
T_J	Junction temperature[3]			150	°C
T_{stg}	Storage temperature range		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V+ and V– can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.
(3) Maximum power dissipation is a function of T_J(max), $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) – T_A) / $R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	All pins except 8, 13	±3000	V
			Pins 8, 13	±15,000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]		±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(see Figure 8)[1]

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$				0.8	V
V_I	Driver input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$		0		5.5	V
	Receiver input voltage			–25		25	
T_A	Operating free-air temperature		MAX3221C	0		70	°C
			MAX3221I	–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.4 Thermal Information

THERMAL METRIC[1]		MAX3221 DB (SSOP) 16 PINS	MAX3221 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98.0	106.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.3	41.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.7	51.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.1	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.1	50.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics – Power

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER			TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
I_I	Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$				±0.01	±1	µA
I_{CC}	Supply current	Automatic power-down disabled	No load, V_{CC} = 3.3 V to 5 V	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC}		0.3	1	mA
		Powered off		No load, $\overline{\text{FORCEOFF}}$ at GND		1	10	µA
		Automatic power-down enabled		No load, $\overline{\text{FORCEOFF}}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.6 Electrical Characteristics – Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	D_{OUT} at R_L = 3 kΩ to GND,	D_{IN} = GND	5	5.4		V
V_{OL}	Low-level output voltage	D_{OUT} at R_L = 3 kΩ to GND,	D_{IN} = V_{CC}	–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}			±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = 3.6 V	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V	V_O = 0 V		±35	±60	
r_O	Output resistance	V_{CC}, V+, and V– = 0 V	V_O = ±2 V	300	10M		Ω
I_{off}	Output leakage current	$\overline{\text{FORCEOFF}}$ = GND	V_O = ±12 V, V_{CC} = 3 V to 3.6 V			±25	µA
			V_O = ±12 V, V_{CC} = 4.5 V to 5.5 V			±25	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

6.7 Electrical Characteristics – Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.5	2.4	V
		V_{CC} = 5 V		1.8	2.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.8	1.4		
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})			0.5		V
I_{off}	Output leakage current	$\overline{\text{FORCEOFF}}$ = 0 V		±0.05	±10	µA
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.8 Electrical Characteristics – Status

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	$\overline{\text{FORCEON}}$ = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}			2.7	V
$V_{T-(valid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	$\overline{\text{FORCEON}}$ = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	–2.7			V
$V_{T(invalid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage	$\overline{\text{FORCEON}}$ = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	–0.3		0.3	V
V_{OH}	$\overline{\text{INVALID}}$ high-level output voltage	I_{OH} = –1 mA, $\overline{\text{FORCEON}}$ = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	V_{CC} – 0.6			V
V_{OL}	$\overline{\text{INVALID}}$ low-level output voltage	I_{OH} = –1 mA, $\overline{\text{FORCEON}}$ = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}			0.4	V

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.9 Switching Characteristics – Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
	Maximum data rate	C_L = 1000 pF, R_L = 3 kΩ, see Figure 3		150	250		kbps
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 to 2500 pF, R_L = 3 kΩ to 7 kΩ, see Figure 4			100		ns
SR(tr)	Slew rate, transition region (see Figure 3)	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ	C_L = 150 to 1000 pF	6		30	V/µs
			C_L = 150 to 2500 pF	4		30	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

6.10 Switching Characteristics – Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, see Figure 5		150		ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF, see Figure 5		150		ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, see Figure 6		200		ns
t_{dis}	Output disable time	C_L = 150 pF, R_L = 3 kΩ, see Figure 6		200		ns
$t_{sk(p)}$	Pulse skew(3)	See Figure 5		50		ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

6.11 Switching Characteristics – Status

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		MIN	TYP(2)	MAX	UNIT
t_{valid}	Propagation delay time, low- to high-level output		1		µs
$t_{invalid}$	Propagation delay time, high- to low-level output		30		µs
t_{en}	Supply enable time		100		µs

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.12 Typical Characteristics

V_{CC} = 3.3 V

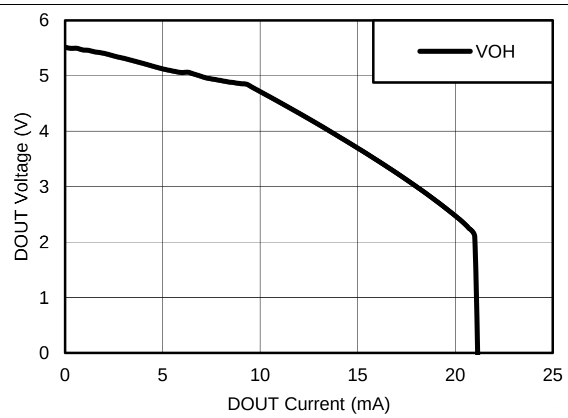


Figure 1. DOUT V_{OH} vs Load Current

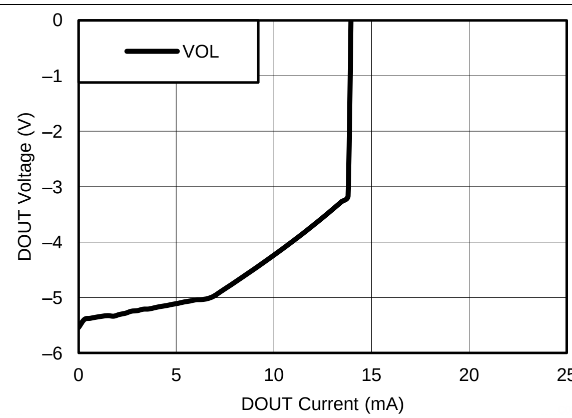
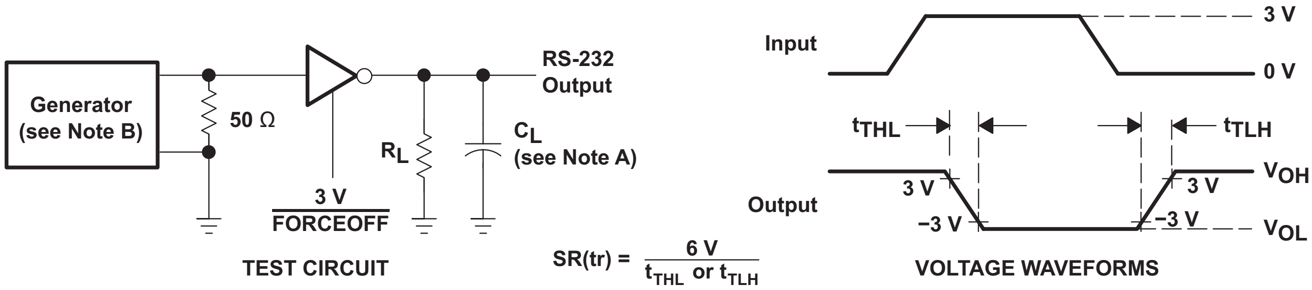


Figure 2. DOUT V_{OL} vs Load Current

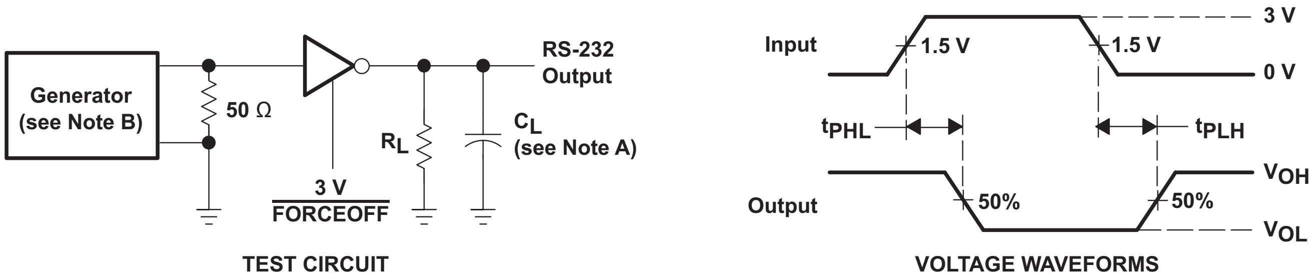
7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbps, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

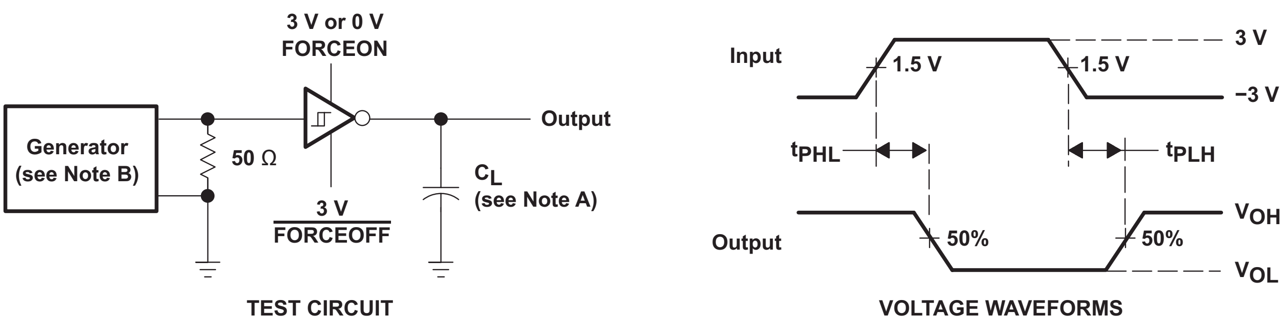
Figure 3. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbps, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 4. Driver Pulse Skew

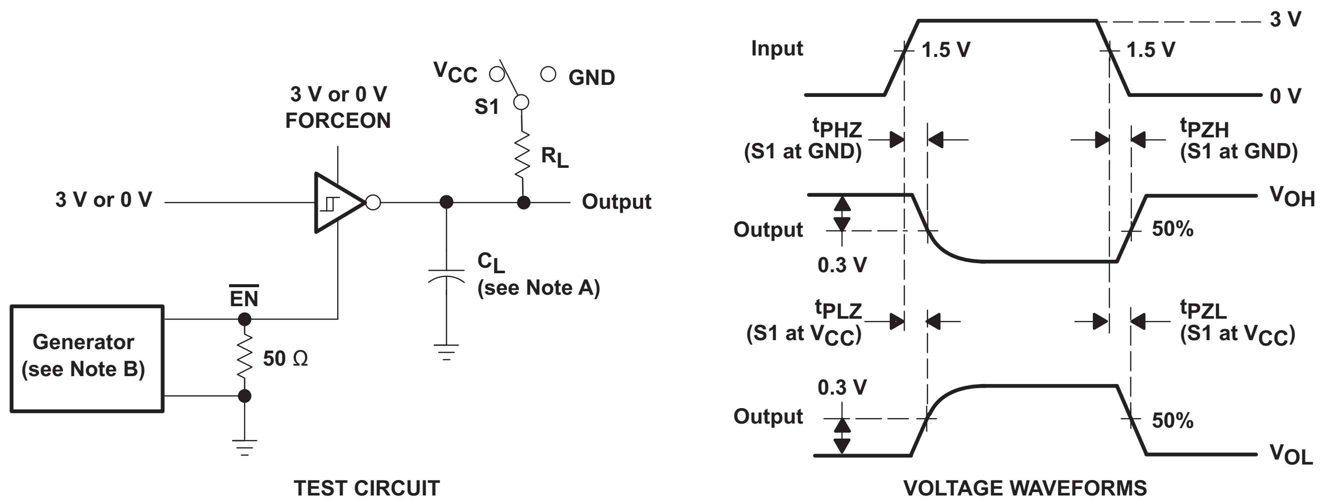


A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 5. Receiver Propagation Delay Times

Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

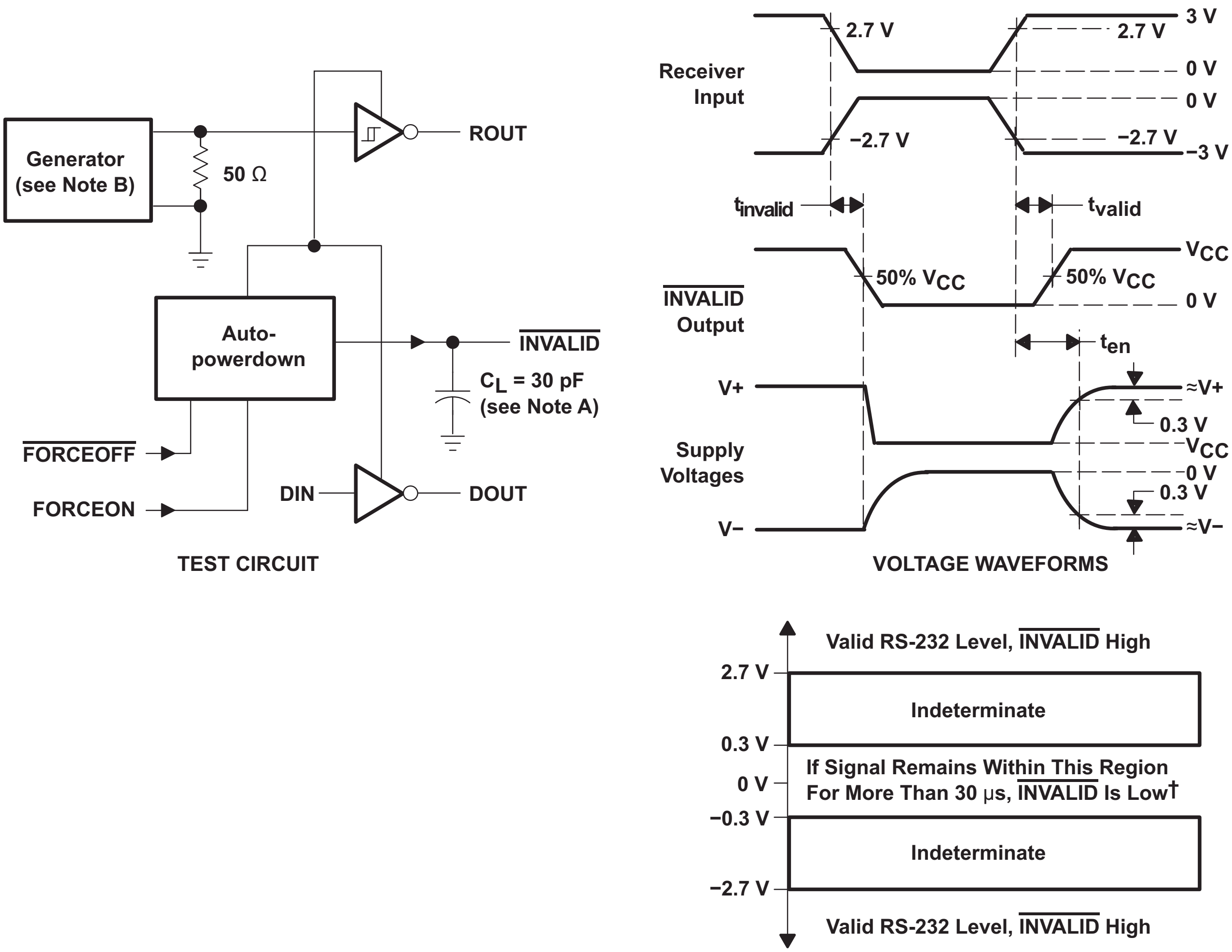
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

D. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6. Receiver Enable and Disable Times

Parameter Measurement Information (continued)



† Auto-powerdown disables drivers and reduces supply current to 1 μA.

Figure 7. INVALID Propagation Delay Times and Driver Enabling Time

8 Detailed Description

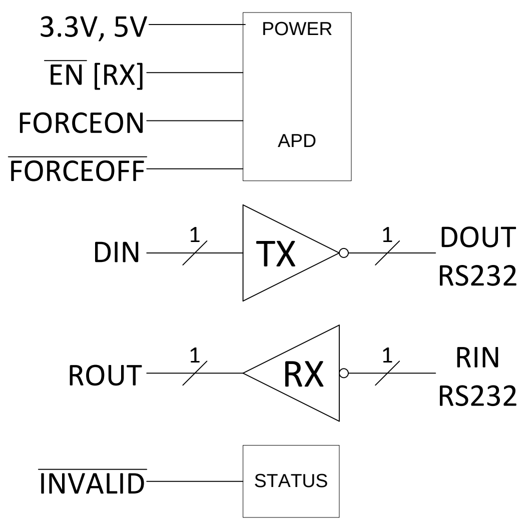
8.1 Overview

The MAX3221 device is a one-driver and one-receiver RS-232 interface device. All RS-232 inputs and outputs are protected to ±15 kV using the Human Body Model. The charge pump requires only four small 0.1-μF capacitors for operation from a 3.3-V supply. The MAX3221 is capable of running at data rates up to 250 kbps, while maintaining RS-232-compliant output levels.

Automatic power-down can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With automatic power-down plus enabled, the device activates automatically when a valid signal is applied to any receiver input. The device can automatically power down the driver to save power when the RIN input is unpowered.

$\overline{\text{INVALID}}$ is high (valid data) if receiver input voltage is greater than 2.7 V or less than –2.7 V, or has been between –0.3 V and 0.3 V for less than 30 μs. $\overline{\text{INVALID}}$ is low (invalid data) if receiver input voltages are between –0.3 V and 0.3 V for more than 30 μs. Refer to Figure 7 for receiver input levels.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V- pins using a charge pump that requires four external capacitors. Auto-power-down feature for driver is controlled by FORCEON and $\overline{\text{FORCEOFF}}$ inputs. Receiver is controlled by $\overline{\text{EN}}$ input. See Table 1 and Table 2

When MAX3221 is unpowered, it can be safely connected to an active remote RS232 device.

8.3.2 RS232 Driver

One driver interfaces standard logic level to RS232 levels. DIN input must be valid high or low.

8.3.3 RS232 Receiver

One receiver interfaces RS232 levels to standard logic levels. An open input will result in a high output on ROUT. RIN input includes an internal standard RS232 load. A logic high input on the $\overline{\text{EN}}$ pin will shutdown the receiver output.

8.3.4 RS232 Status

The $\overline{\text{INVALID}}$ output goes low when RIN input is unpowered for more than 30 μs. The $\overline{\text{INVALID}}$ output goes high when receiver has a valid input. The $\overline{\text{INVALID}}$ output is active when V_{cc} is powered irregardless of FORCEON and $\overline{\text{FORCEOFF}}$ inputs (see Table 3).

8.4 Device Functional Modes

Table 1, Table 2, and Table 3 show the behavior of the driver, receiver, and INVALID(activelow) features under all possible relevant combinations of inputs.

Table 1. Driver(1)

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with automatic power down disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with automatic power down enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by automatic power down feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance, Yes = |RIN| > 2.7 V, No = |RIN| <0.3 V

Table 2. Receiver(1)

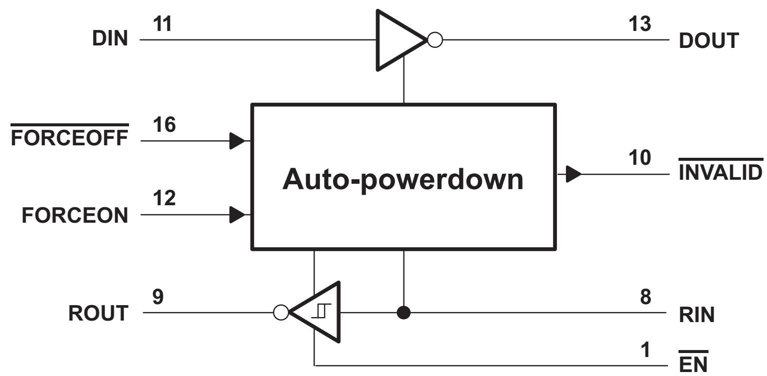
INPUTS			OUTPUT	RECEIVER STATUS
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	ROUT	
X	H	X	Z	Output off
L	L	X	H	Normal operation
H	L	X	L	
Open	L	No	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

Table 3. $\overline{\text{INVALID}}$(1)

INPUTS				OUTPUT
RIN	FORCEON	$\overline{\text{FORCEOFF}}$	$\overline{\text{EN}}$	$\overline{\text{INVALID}}$
L	X	X	X	H
H	X	X	X	H
Open	X	X	X	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off



Logic Diagram

9 Application and Implementation

NOTE

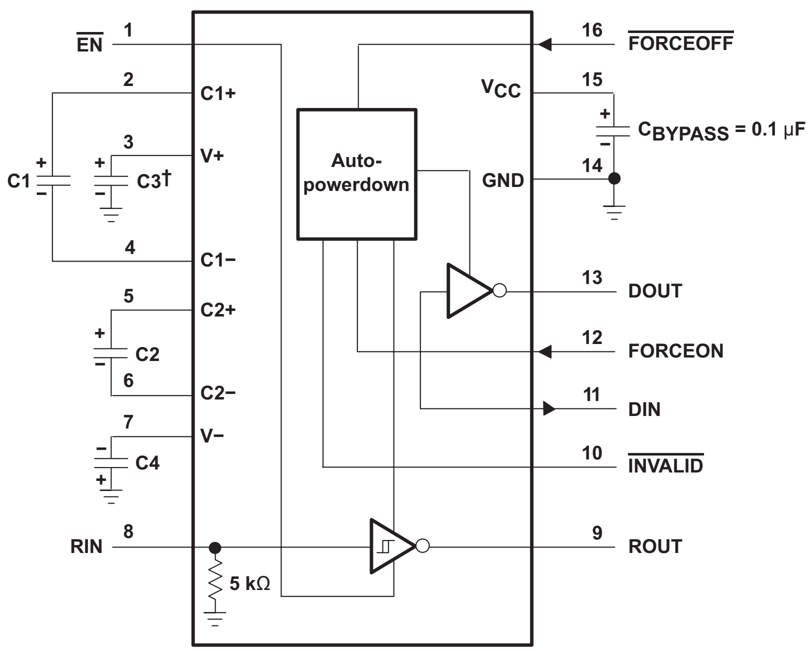
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The MAX3221 line driver and receiver is a specialized device for 3-V to 5.5-V RS-232 communication applications. This application is a generic implementation of this device with all required external components. For proper operation, add capacitors as shown in Figure 8.

9.2 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{\text{FORCEOFF}}$ may be connected general purpose logic lines or tied to ground or V_{CC}. $\overline{\text{INVALID}}$ may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS232 connector or cable. DIN, FORCEON, and $\overline{\text{FORCEOFF}}$ inputs must not be left unconnected.



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 8. Typical Operating Circuit and Capacitor Values

Typical Application (continued)

9.2.1 Design Requirements

- Recommended V_{CC} is 3.3 V or 5 V.
  - 3 V to 5.5 V is also possible
- Maximum recommended bit rate is 250 kbps.
- Use capacitors as shown in Figure 8.

9.2.2 Detailed Design Procedure

- DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels.
- Select capacitor values based on VCC level for best performance.

9.2.3 Application Curve

Curves for V_{CC} of 3.3 V and 250 kbps alternative bit data stream.

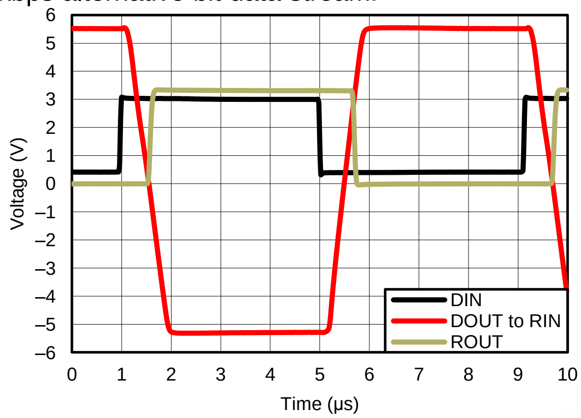


Figure 9. 250-kbps Driver to Receiver Loopback Timing Waveform, V_{CC}= 3.3 V

10 Power Supply Recommendations

TI recommends a 0.1-μF capacitor to filter noise on the power supply pin. For additional filter capability, a 0.01-μF capacitor may be added in parallel as well. Power supply input voltage is recommended to be any valid level in *Recommended Operating Conditions*.

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

11.2 Layout Example

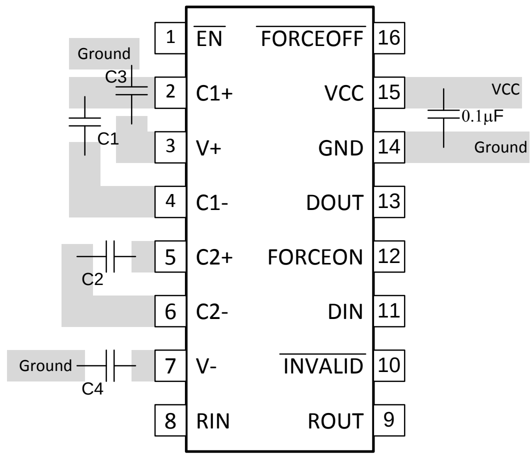


Figure 10. Layout Diagram

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3221CDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	Samples
MAX3221CDBE4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	Samples
MAX3221CDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	Samples
MAX3221CDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	Samples
MAX3221CDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	Samples
MAX3221CPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	Samples
MAX3221CPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	Samples
MAX3221CPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	Samples
MAX3221CPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	Samples
MAX3221CPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	Samples
MAX3221CPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3221C	Samples
MAX3221IDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	Samples
MAX3221IDBE4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	Samples
MAX3221IDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	Samples
MAX3221IDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	Samples
MAX3221IDBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	Samples
MAX3221IDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3221IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	Samples
MAX3221IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	Samples
MAX3221IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	MB3221I	Samples
MAX3221IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3221I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MAX3221 :

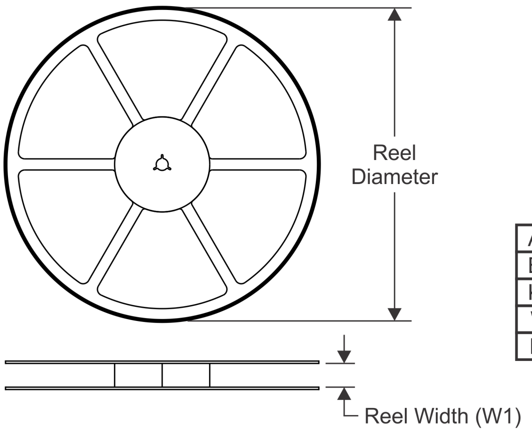
- Enhanced Product: MAX3221-EP

NOTE: Qualified Version Definitions:

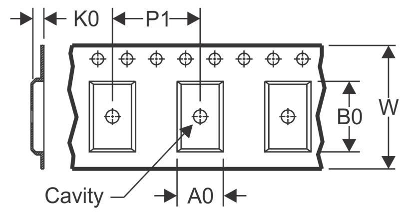
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

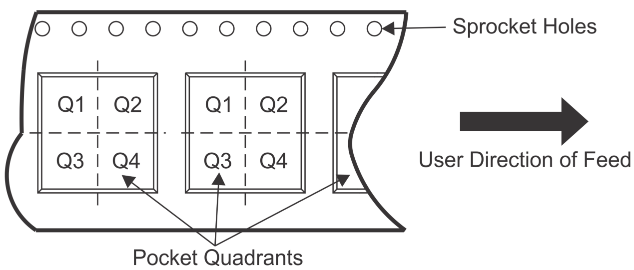


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

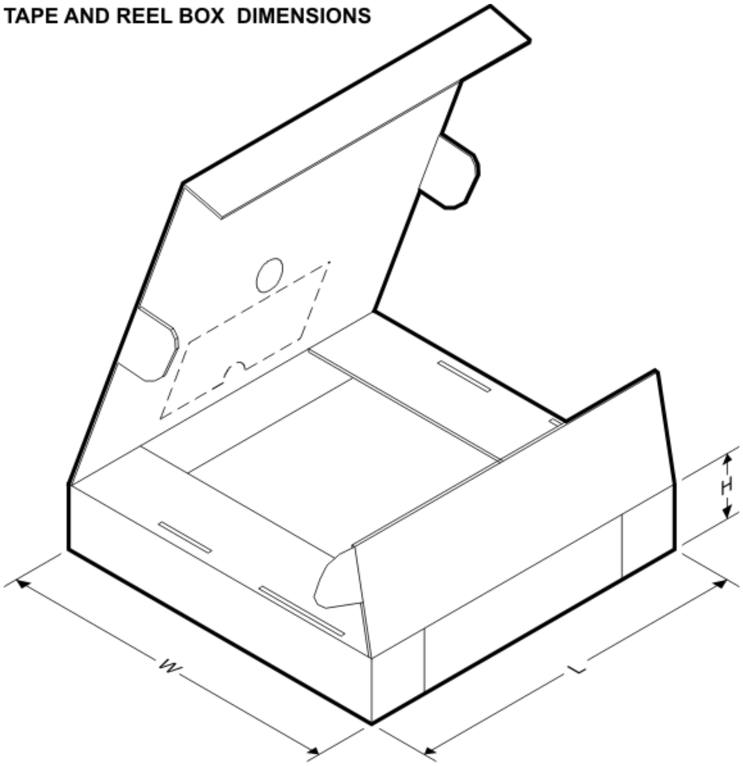
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3221CDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
MAX3221CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221IDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
MAX3221IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221IPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

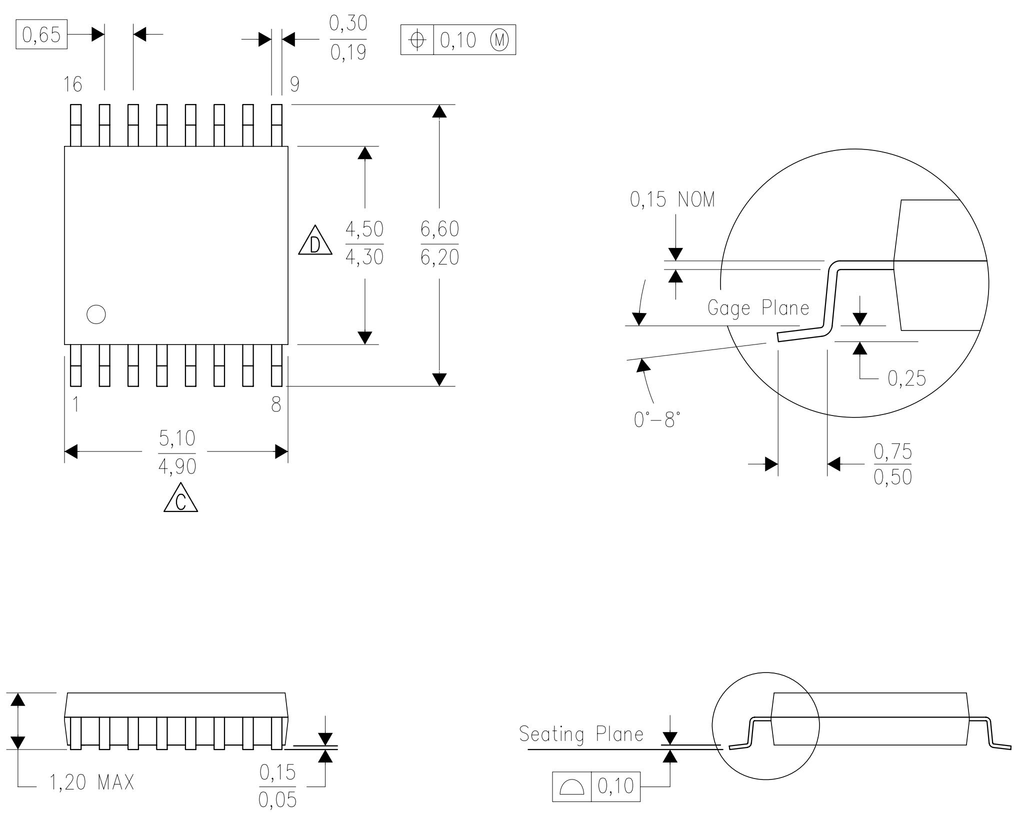
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3221CDBR	SSOP	DB	16	2000	367.0	367.0	38.0
MAX3221CPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
MAX3221IDBR	SSOP	DB	16	2000	367.0	367.0	38.0
MAX3221IPWR	TSSOP	PW	16	2000	364.0	364.0	27.0
MAX3221IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
MAX3221IPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0

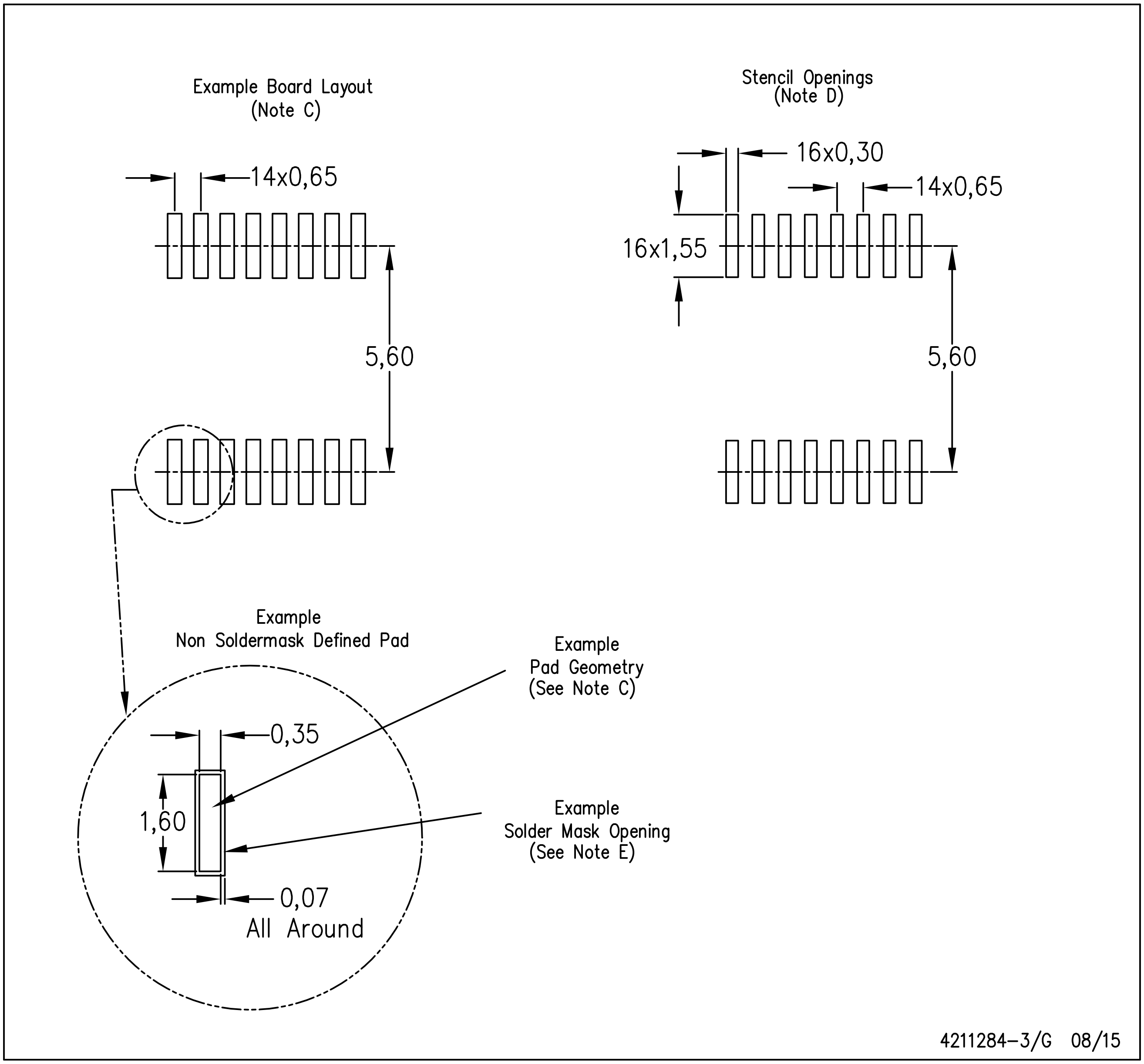
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064-4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

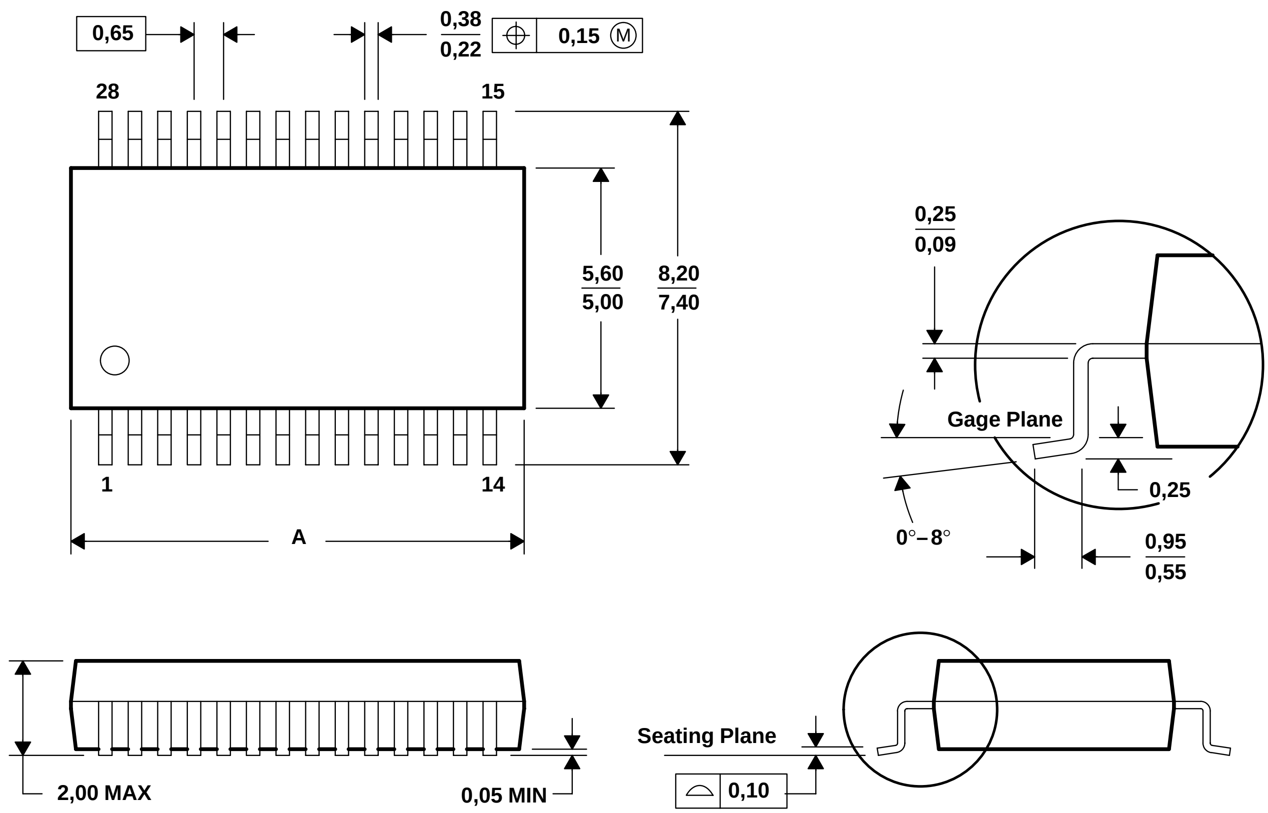
PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150