Product Specification

PE4231

SPDT High Power UltraCMOS™
DC – 1.3 GHz RF Switch

Features

- Optimized for 75 Ω systems
- Single +3-volt power supply
- Low insertion loss: 0.80 dB at 1.0 GHz
- High isolation: 42 dB at 1.0 GHz
- Typical input 1 dB compression point of +32 dBm
- Single-pin CMOS or TTL logic control
- Low cost

Product Description

The PE4231 SPDT High Power UltraCMOS™ RF Switch is designed to cover a broad range of applications from DC to 1.3 GHz. This single-supply reflective switch integrates on-board CMOS control logic driven by a simple, single-pin CMOS or TTL compatible control input. Using a nominal +3-volt power supply, a typical input 1 dB compression point of +32 dBm can be achieved. The PE4231 also exhibits input-output isolation of better than 42 dB at 1.0 GHz and is offered in a small 8-lead MSOP package.

The PE4231 SPDT High Power UltraCMOS™ RF Switch is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

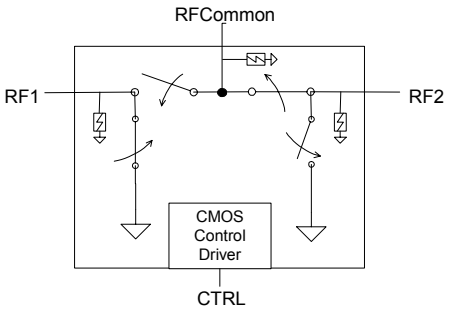


Figure 2. Package Type

8-lead MSOP



Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3 V (Z_S = Z_L = 75 Ω)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Operation Frequency[1]		DC		1300	MHz
Insertion Loss	50 MHz 1000 MHz		0.50 0.80	0.60 0.90	dB
Isolation – RFCommon to RF1/RF2	50 MHz 1000 MHz	73 40	75 42		dB
Isolation – RF1 to RF2	50 MHz 1000 MHz	58 33	60 35		dB
Return Loss	1000 MHz	16	17		dB
'ON' Switching Time	CTRL to 0.1 dB final value, 2 GHz		2000		ns
'OFF' Switching Time	CTRL to 25 dB isolation, 2 GHz		900		ns
Video Feedthrough[2]			15		mV_{pp}
Input 1 dB Compression[3]	1000 MHz	30	32		dBm
Input IP3[3]	1000 MHz, 17 dBm	50			dBm

Notes: 1. Device linearity will begin to degrade below 1 MHz.
2. Measured with a 1 ns risetime, 0/3 V pulse and 500 MHz bandwidth.
3. Measured in a 50 Ω system.

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Figure 3. Pin Configuration (Top View)

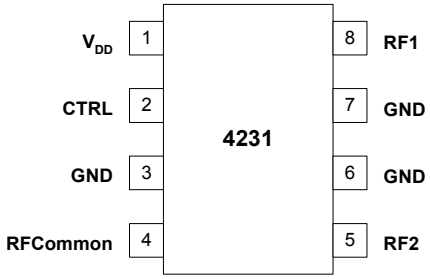


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	V_{DD}	Nominal +3 V supply connection.
2	CTRL	CMOS or TTL logic level: High = RFCommon to RF1 signal path Low = RFCommon to RF2 signal path
3	GND	Ground connection. Traces should be physically short and connected to ground
4	RF Common	Common RF port for switch.[1]
5	RF2	RF2 port.[1]
6	GND	Ground Connection. Traces should be physically short and connected to ground
7	GND	Ground Connection. Traces should be physically short and connected to ground
8	RF1	RF1 port.[1]

Note 1: All RF pins must be DC blocked with an external series capacitor or held at 0 V_{DC}.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/ Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input except for the CTRL input	-0.3	V_{DD}+ 0.3	V
V_{CTRL}	Voltage on CTRL input		5.0	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
P_{IN}	Input power (50Ω)		33	dBm
V_{ESD}	ESD voltage (Human Body Model)		200	V

Table 4. DC Electrical Specifications

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
I_{DD} Power Supply Current (V_{DD} = 3V, V_{CNTL} = 3V)		29	35	µA
Control Voltage High	0.7xV_{DD}			V
Control Voltage Low			0.3xV_{DD}	V

Table 5. Truth Table

Control Voltage	Signal Path
CTRL = CMOS or TTL High	RFCommon to RF1
CTRL = CMOS or TTL Low	RFCommon to RF2

The control logic input pin (CTRL) is typically driven by a 3-volt CMOS logic level signal, and has a threshold of 50% of V_{DD}. For flexibility to support systems that have 5-volt control logic drivers, the control logic input has been designed to handle a 5-volt logic HIGH signal. (A minimal current will be sourced out of the V_{DD} pin when the control logic input voltage level exceeds V_{DD}.)

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

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Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)

Figure 4. Insertion Loss – RFC to RF1

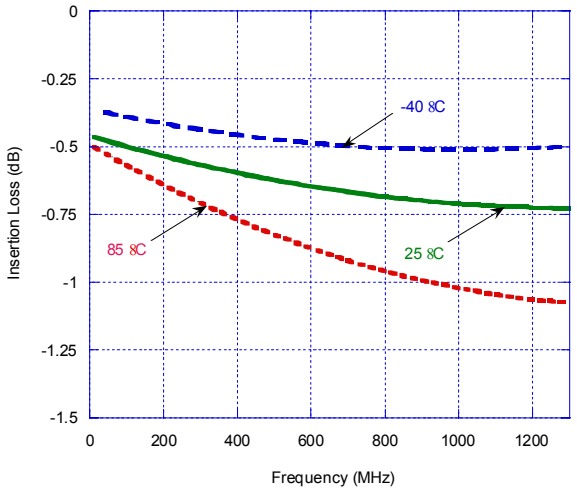


Figure 5. Input 1dB Compression Point

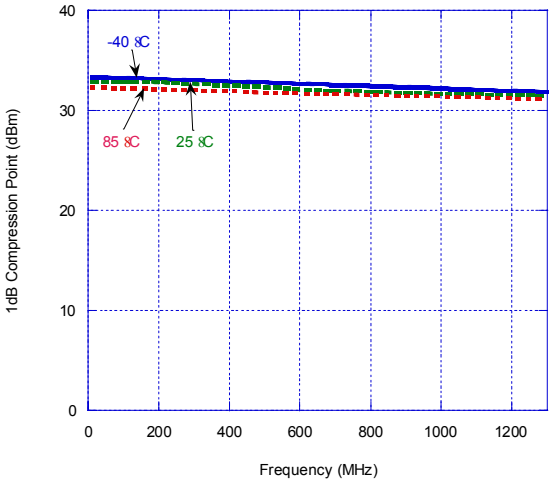


Figure 6. Insertion Loss – RFC to RF2

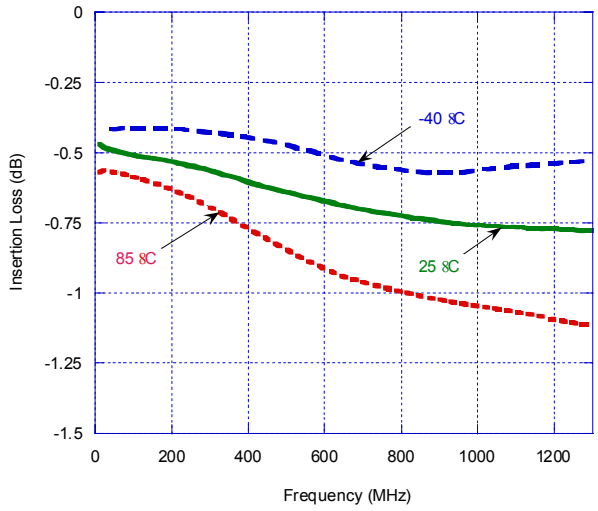
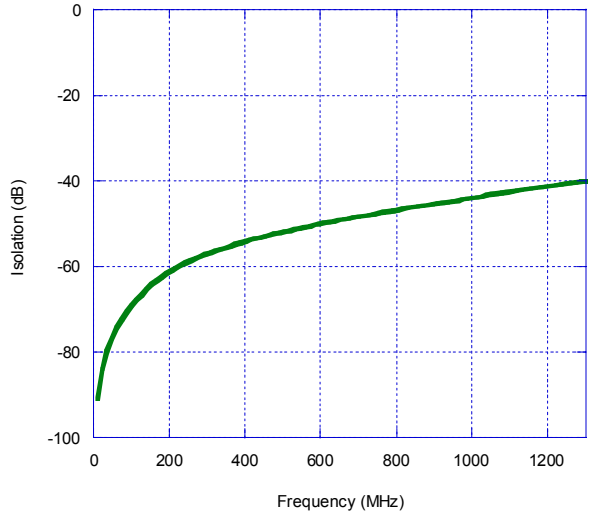


Figure 7. Isolation – RFC to RF1



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Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)

Figure 8. Isolation – RFC to RF2

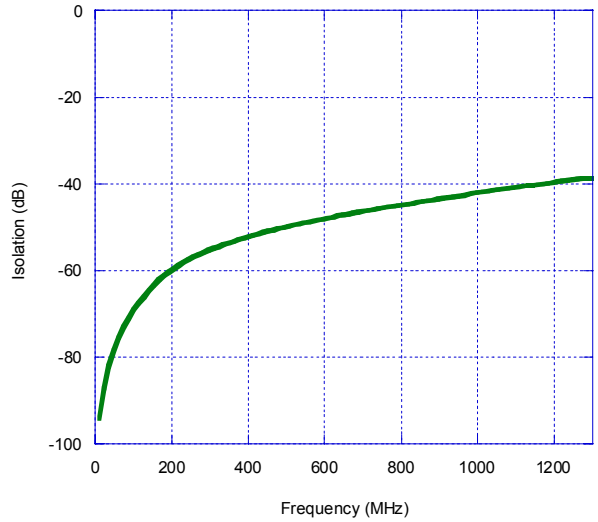


Figure 9. Isolation – RF1 to RF2, RF2 to RF1

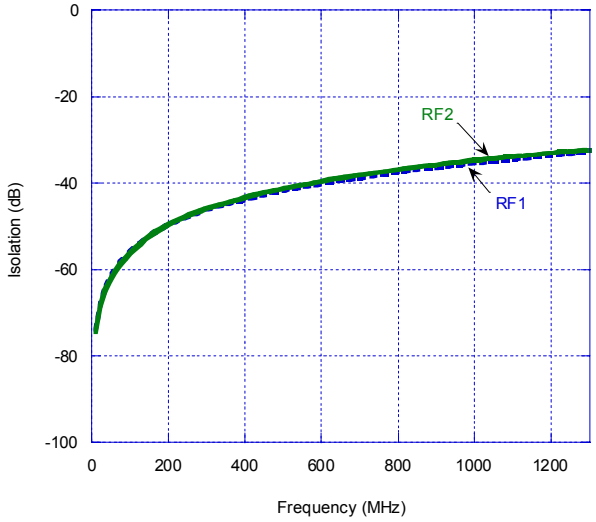


Figure 10. Return Loss – RFC

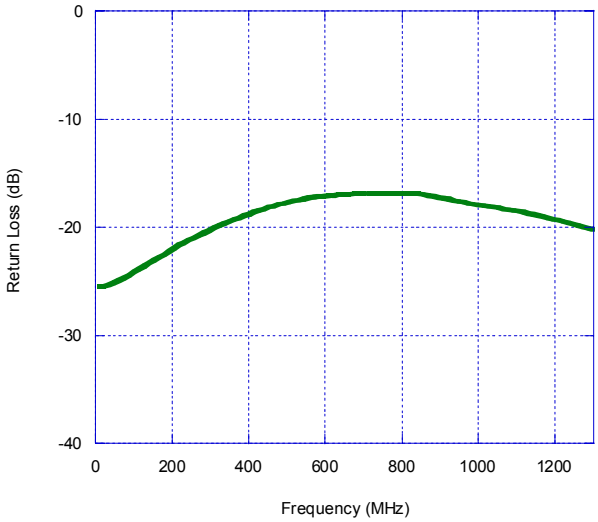
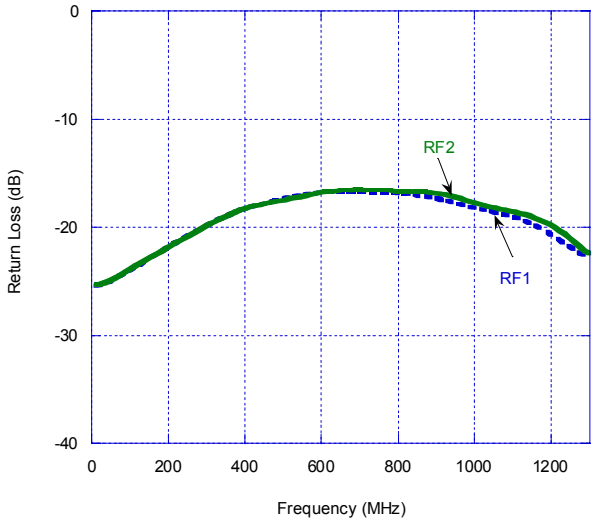


Figure 11. Return Loss – RF1, RF2



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Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4231 SPDT switch. The RF common port is connected through a 75 Ω transmission line to the top left BNC connector, J1. Port 1 and Port 2 are connected through 75 Ω transmission lines to the top two BNC connectors on the right side of the board, J2 and J3. A through transmission line connects BNC connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.021", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0014" and ε_r of 4.4.

J6 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J6-3) is connected to the device CNTL input. The fourth pin to the right (J6-7) is connected to the device VDD input. A decoupling capacitor (100 pF) is provided on both CNTL and VDD traces. It is the responsibility of the customer to determine proper supply decoupling for their design application. Removing these components from the evaluation board has not been shown to degrade RF performance.

Figure 8. Evaluation Board Layouts

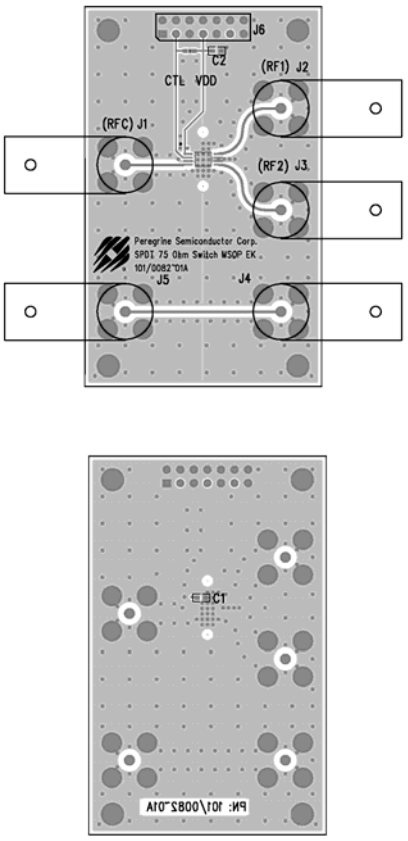
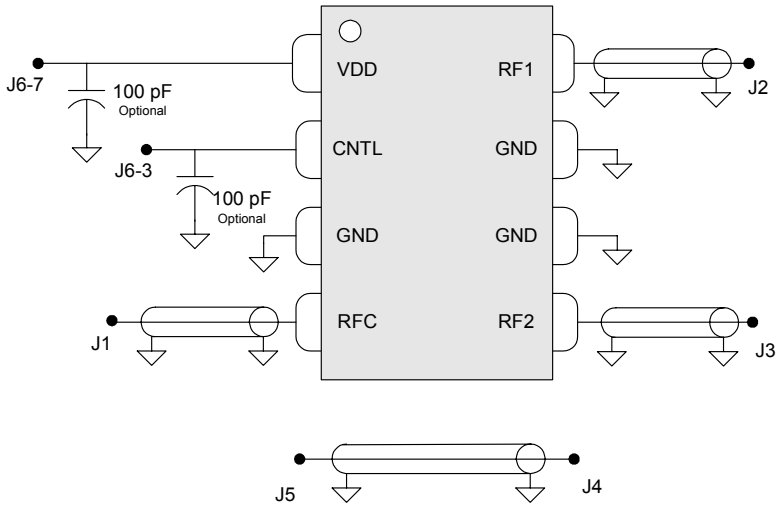


Figure 9. Evaluation Board Schematic



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Figure 14. Package Drawing

8-lead MSOP

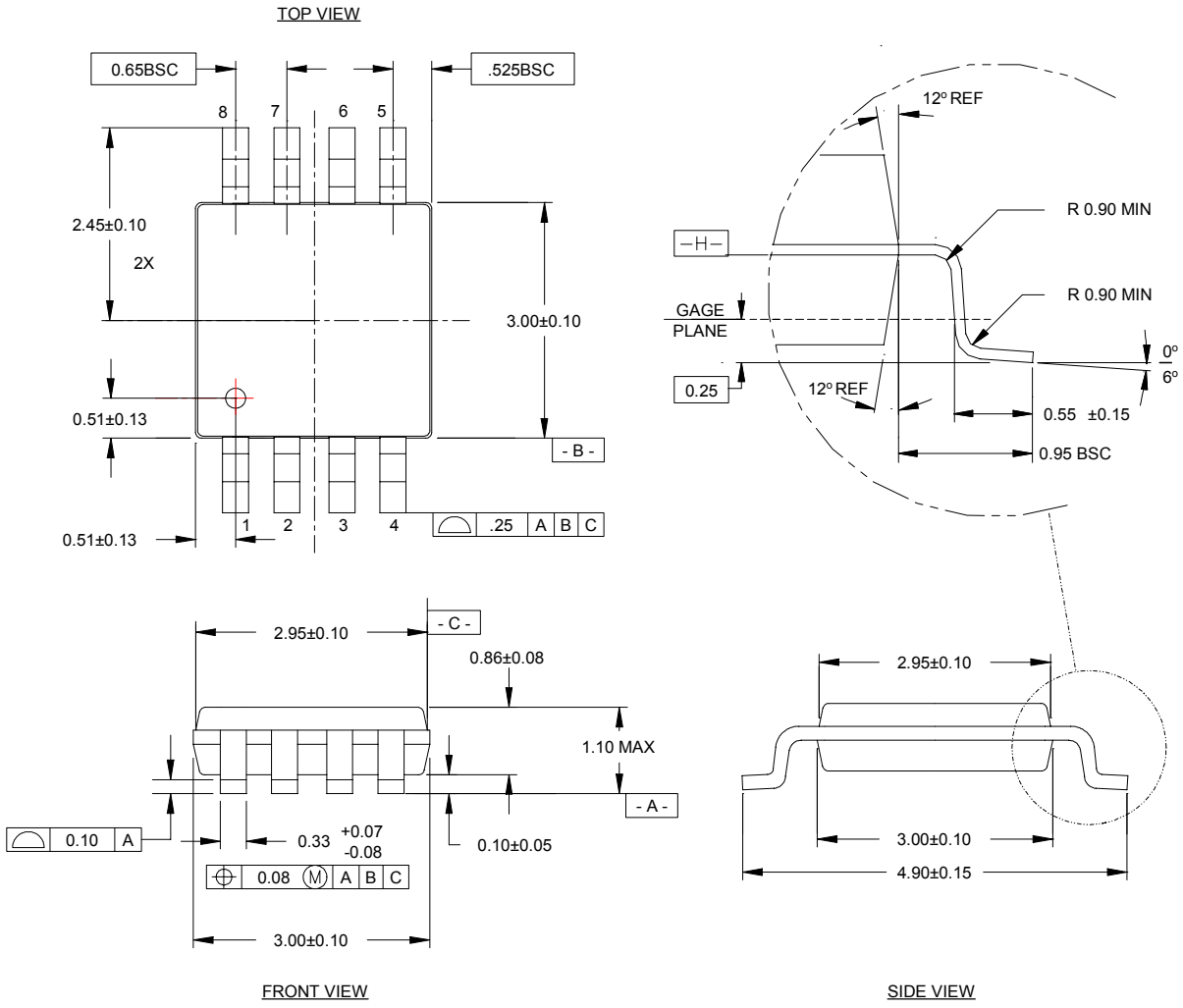


Table 6. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4231-01	4231	PE4231-08MSOP-50A	8-lead MSOP	50 units / Tube
4231-02	4231	PE4231-08MSOP-2000C	8-lead MSOP	2000 units / T&R
4231-00	PE4231-EK	PE4231-08MSOP-EK	Evaluation Kit	1 / Box
4231-51	4231	PE4231G-08MSOP-50A	Green 8-lead MSOP	50 units / Tube
4231-52	4231	PE4231G-08MSOP-2000C	Green 8-lead MSOP	2000 units / T&R

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Data Sheet Identification

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